國立臺灣師範大學電機工程學系

碩士論文

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應用於輸出級驅動電路之靜電放電防護設計

On-Chip ESD Protection Design for Output Driver Applications

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應用於輸出級驅動電路之靜電放電防護設計

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Abstract (Chinese)

隨著製程演進，晶片微縮，靜電放電(ESD)容易造成晶片內部的電子元件遭受到不可逆之破壞，而所有的微電子產品必須符合此可靠度的規範。因此，靜電放電防護的可靠度議題必須被探討。

在積體電路的應用上，本論文設計了幾種新型的靜電放電防護元件，此元件在 0.18um 1.8V/3.3V CMOS 製程下實現。透過實驗分析的結果，防護元件可以承受較大的訊號擺幅和能夠耐受 2kV 的人體放電模式之靜電放電測試。

為了驗證靜電放電防護元件在實際電路上的效能，本論文使用堆疊元件的輸出級驅動器並搭配嵌入式矽控整流器（Embedded SCR）。一種新型的靜電放電防護設計被提出來，為了改善其靜電放電的防護能力。此電路在 0.18um 1.8V/3.3V CMOS 製程下實現。本論文所提出的防護設計經實際驗證，在不影響電路正常操作的情況下，有效改善其靜電放電的防護能力，證明所提出的設計可以改善靜電放電防護的能力。

關鍵字：靜電放電，輸出驅動器，矽控整流器

On-Chip ESD Protection Design for Output Driver Applications

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Abstract (English)

With the continuous evolution of semiconductor integrated circuits (ICs) process, electrostatic discharge (ESD) events are likely to cause internal electronic components of the wafer suffered irreversible damage. All microelectronic products must meet the reliability specifications. Therefore, ESD must be taken into consideration.

In the application of integrated circuit, several novel ESD protection devices are designed in this work. By designing the structure, this work has been fabricated in 0.18-μm 1.8V/3.3V CMOS process. In the experimental results, this design can achieve large swing tolerance and endure 2kV human-body-model (HBM) test.

In order to verify the protection ability of ESD protection device on the circuits, a novel design of stacked-device output driver with embedded silicon-controlled rectifier (SCR) is proposed to improve the ESD robustness. This work has been fabricated in 0.18-um 1.8V/3.3V CMOS process. Besides, the transient behaviors of the proposed design during normal operation are not degraded. Therefore, the proposed design can be used to improve the ESD robustness of stacked-device output driver.

Keywords: electrostatic discharge (ESD), output driver, silicon-controlled rectifier (SCR).

Acknowledgment

首先，要感謝我的指導教授林群祐老師三年來耐心的教導，使我能順利完成碩士學位，在老師不厭其煩地給予更正和指導下，讓學生在靜電放電防護設計的領域上奠定了成功的基礎，特別是老師在做研究上的認真和嚴謹的態度，以及在論文寫作上的技巧都讓學生非常的欽佩。也很感謝老師給予了「晶焱科技」實習的機會，讓學生能夠直接接觸到靜電放電防護相關的工作，並且有幸認識了此產業的諸位先進，對我來說實在是受益良多阿!

在研究過程中，我要感謝「國家晶片系統設計中心」讓我有機會下線對我的電路進行驗證，此外還要感謝「國立交通大學電子工程學系」，提供量測機台協助晶片的量測與分析；同時也要感謝 「晶焱科技」的陳東暘協理以及「國立交通大學電子工程學系」的陳柏宏教授，在碩士口試時，提出了相當多寶貴的建議和想法，使學生的論文能更加精進。

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您們，因為能遇見您們我的碩班生涯才會如此精彩。

最後，我要特別至上我最深的感謝給我的父親邱進東先生、母親李琇琴女士、弟弟邱彥勳先生，沒有你們的支持、照顧與鼓勵，就沒有我今日的成就。這幾年家裡發生相當多重大的變故，都是家人在幫忙處理，很多事情我無法幫忙分攤說來實在慚愧，家人讓我沒有後顧之憂的完成碩士學位，在此衷心的地感謝您們；同時也要向二十二歲的自己說一聲謝謝你，當初有繼續堅持下去沒有輕言放棄，才能有現在的成果。另外，要祝福所有在這些年與我相處過的朋友們，有緣與您們相識是我的榮幸，願大家心想事成，身體健康。

論文雖然力求完善，但錯誤之處在所難免，請各位讀者不吝惜給予寶貴的意見，使本論文能更加完整。

邱彥璉 謹誌於師大

中華民國一零五年七月

Contents

Table Captions

Figure Captions

Chapter 1

Introduction

1.1 Background of ESD

The phenomenon of electrostatic discharge (ESD) occurs when an electrostatic voltage slowly develops between an object and its surrounding environment, commonly referred to as ground, then spontaneously discharges as an electrical current impulse [1].

1.2 Models of ESD

A typical specification for a commercial IC on ESD robustness is 2kV for the human-body-model (HBM) and 200V for the machine-model (MM) [2]-[4]. The equivalent circuits of HBM and MM ESD tests are shown in Fig. 1.1 and Fig. 1.2, respectively. In the equivalent circuits of HBM ESD test, a 100 pF capacitor represents the charged human body and the 1.5kΩ resistor is used to model the discharging resistance of human body. In the MM ESD test, the circuit component is a 200 pF capacitor with no resistive component. HBM is the most prevalent ESD event model and widely used as a basic ESD protection standard for the semiconductor products at industry.

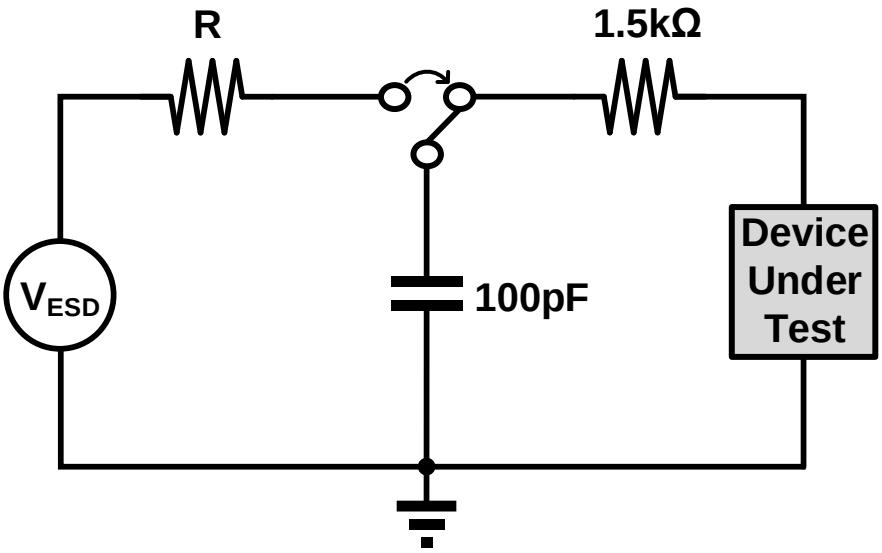


Fig. 1.1. Equivalent circuits of HBM ESD test.

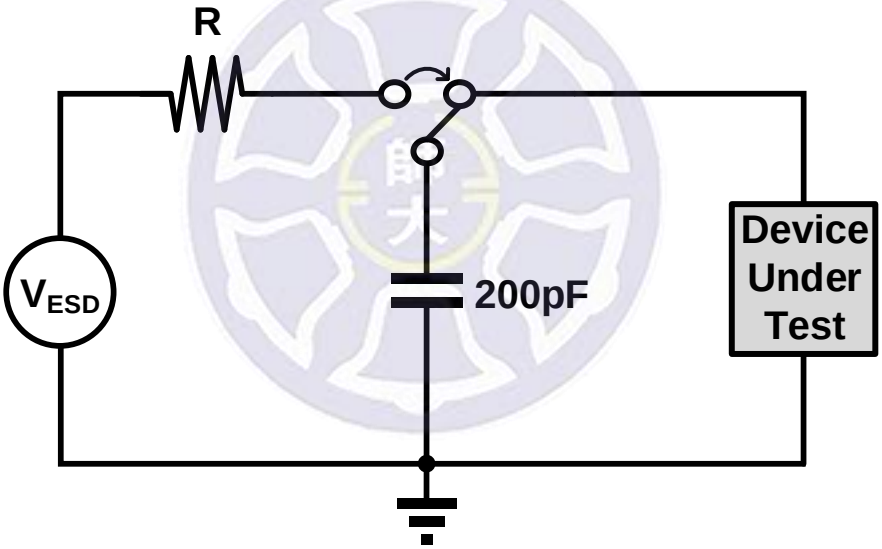


Fig. 1.2. Equivalent circuits of MM ESD test.

1.3 Typical Design of On-Chip ESD Protection Circuits

ESD failure is the major electronics reliability problems at system level and component. Industrial standards require satisfactory on-chip ESD protection for all ICs and systems, which becomes a constantly increasing IC design challenge for complex ICs using advanced IC technologies [5].

With the design of considering the possible ESD damage sites, the ESD discharging current paths need to be created and constructed. The Typical Design of On-Chip ESD Protection Circuits is shown in Fig. 1.3.

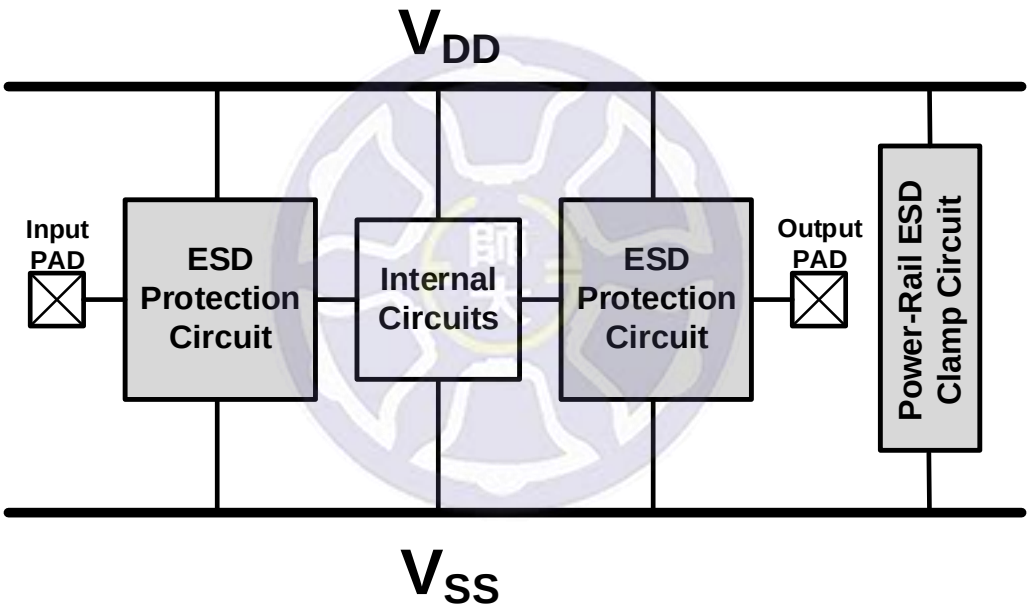


Fig. 1.3. Typical design of on-chip ESD protection circuits.

The ESD-testing modes at input-output (I/O) pads with respect to V_{DD} or V_{SS} pins, pin-to-pin and the V_{DD}-to-V_{SS} ESD stresses have been specified to judge the whole-chip ESD robustness. Under the ESD-stress condition, the V_{DD}-to-V_{SS} ESD clamp circuit can provide a low impendence path to discharge the ESD current between the V_{DD} and V_{SS} power lines.

1.3.1 ESD Protection Design with Diodes

Diode is widely used as ESD protection. Both its reverse and forward operational mode can be used to conduct ESD current. For reverse biased diode, it has smaller current conduction ability and need to deplete large area to reach the prospective protection specification. For forward biased diode, it is always assisted with power-rail ESD clamp circuits together to realize a rail based protection. Fig. 1.4 show the ESD stress modes on I/O pads. When positive electrostatic discharge form I/O PAD to V_{SS} (positive-to-V_{SS}, PS), electrostatic current will flowing through the D_P and then discharge by the power-rail ESD clamp circuit. When negative electrostatic discharge form I/O PAD to V_{SS} (negative-to-V_{SS}, NS), electrostatic current will discharge by the forward bias D_N. When positive electrostatic discharge form I/O PAD to V_{DD} (positive-to-V_{DD}, PD), electrostatic current will discharge by forward bias D_P. When negative electrostatic discharge form I/O PAD to V_{DD} (negative-to-V_{DD}, ND), electrostatic current will flowing through the power-rail ESD clamp circuit and discharge by the forward bias D_N.

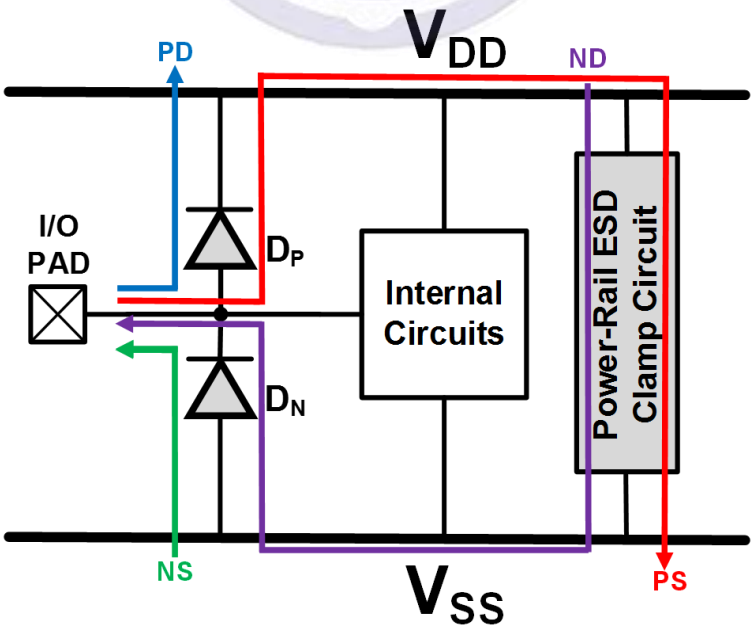


Fig. 1.4. ESD protection design with diodes.

1.3.2 ESD Protection Design with GGNMOS

A gate-grounded NMOS (GGNMOS) is widely used in ESD protection. GGNMOS, structure is made from the standard NMOS structure by grounding the gate terminal [6].

Fig. 1.5 also marked the electrostatic discharge path when this circuits is affected by ESD stress. In all different ESD protection devices, GGNMOS is often used in the industry. There are still several issues existed for the GGNMOS structures. Large layout area is required due to its destitute protection reliability needs to be improved to implement a high ESD protection.

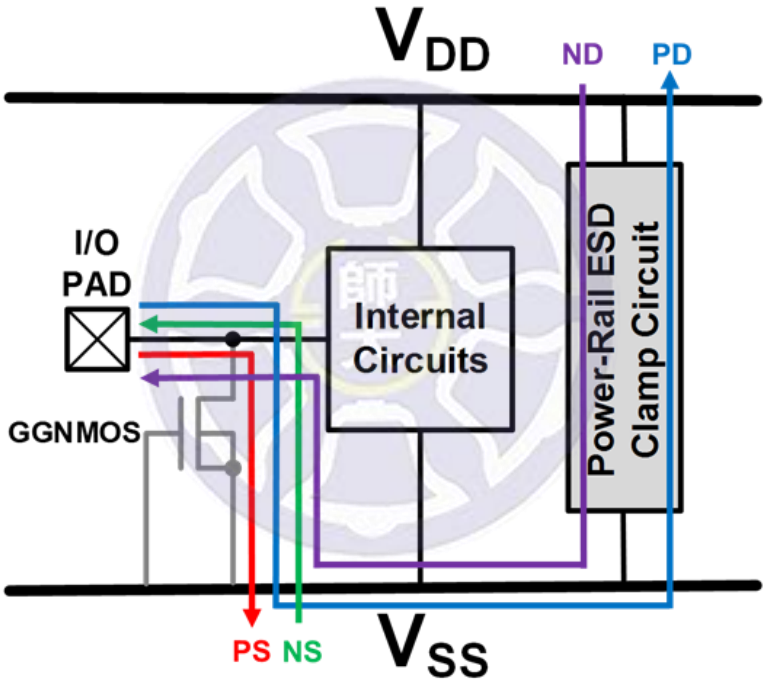


Fig. 1.5. ESD protection design with GGNMOS.

1.3.3 ESD Protection Design with SCR

Silicon-controlled rectifier (SCR) device consists of a vertical PNP and a lateral NPN bipolar transistors to form a 4-layer PNPN (P+/N-well/P-well/N+) structure, which is instinctive in the CMOS processes. Due to have the low holding voltage (V_h, about ~1.5V in general CMOS processes) of SCR device [7], the power dissipation (power ≅ $I_{ESD} \times V_h$) located on the SCR device during ESD stress is meaningful less than that located on other ESD protection devices, such as the BJT, diode, and field-oxide device. The SCR device can sustain a much higher ESD level within a smaller layout area in CMOS ICs. Fig. 1.6 also marked the electrostatic discharge path when this circuit is affected by ESD stress.

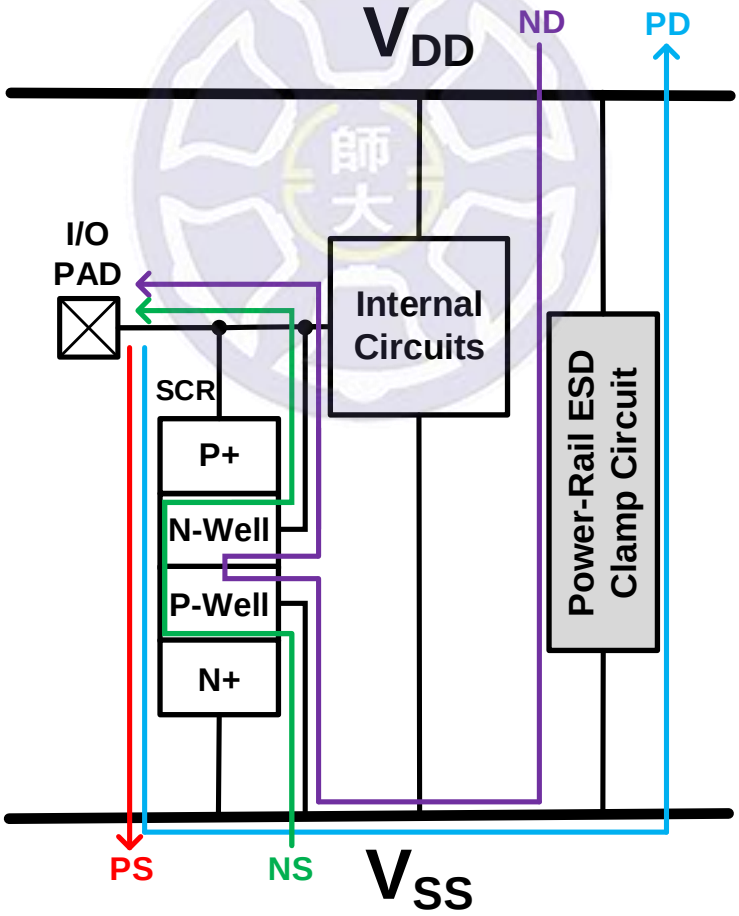


Fig. 1.6. ESD protection design with SCR.

There are some ESD design issue. The first one is ESD design optimization and prediction, which necessitate comprehensive mixed-mode ESD simulation to address the complex coupling effects among process, device, circuit and layout. Second, ESD protection device will introduce parasitic effects, such as resistance (R_{ESD}), capacitance (C_{ESD}), and leakage current (I_{leak}), etc., which will unfavorably affect IC chip performance [8].

To promise the effectiveness of an ESD protection design, it has been approved that the I-V characteristics of ESD protection devices should locate within the ESD protection window. As shown in Fig. 1.7, the ESD protection window is defined that trigger voltage (V_{t1}) should be smaller than breakdown voltage of internal circuits (V_{BD}, Internal) to ensure successful protection, and holding voltage (V_{hold}) should be higher than the operational voltage (V_{DD}) to avoid the a possible latch-up issue [9].

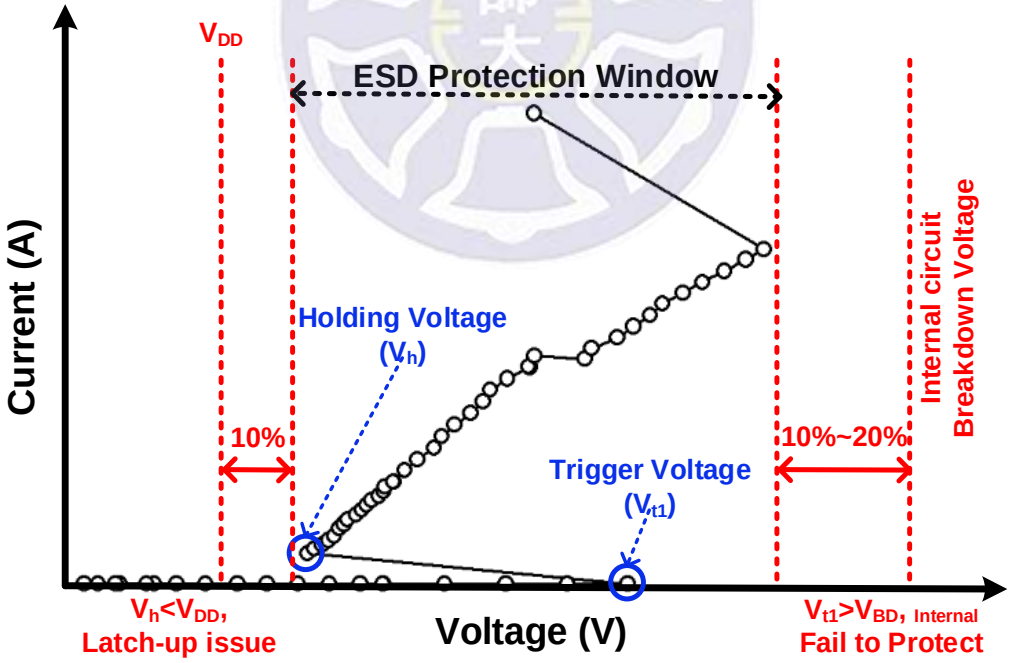


Fig. 1.7. ESD protection window of ESD protection device.

1.4 Applications for Output Driver

1.4.1 Architecture of Electrical Stimulator

As medical science and electronics engineering evolving, bioelectronics combined the microelectronics technology with medicine knowledge results in a new generation of therapy and healthcare. Nowadays, the stimulator that transmits artificial electrical signals into nervous system to repair some physical functions of a human has been investigated and verified [10]. Therapeutic electrical stimulation (TES) and functional electrical stimulation (FES) systems have been developed for restoring function in different applications such as cardiac pacing, vision restoration, muscle exercising and suppression of epileptic seizure [11]-[13]. Comparing with the traditional treatments by using surgery or medicine, the electrical stimulation is more harmless, flexible, and recoverable [14], [15].

The output driver methodology about electrode configuration is classified into two types: two leads per site (bipolar stimulation) and one lead per site (monopolar stimulation). To realize the output driver, the usually used configurations of monopolar and bipolar stimulators are shown in Figs. 1.8 and 1.9 [16], [17]. In Fig. 1.8, the monopolar stimulator utilizes the dual supply voltages (V_{HH} and V_{LL}) with anodic and cathodic output drivers to deliver anodic and cathodic stimulus currents. In Fig. 1.9, the bipolar stimulator utilizes the single supply voltage (V_{HH}) with single output driver from V_{HH}.

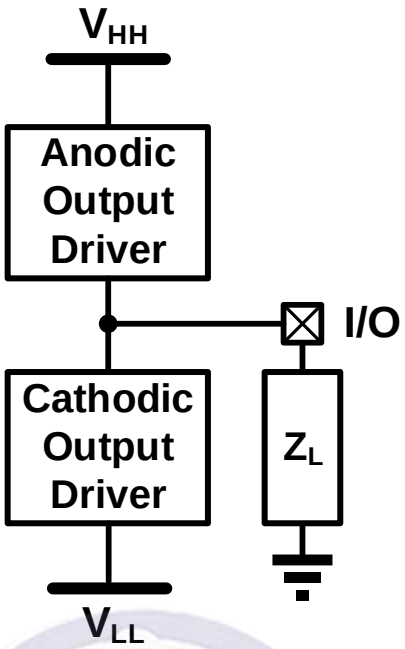


Fig. 1.8. Output driver with monopolar configuration.

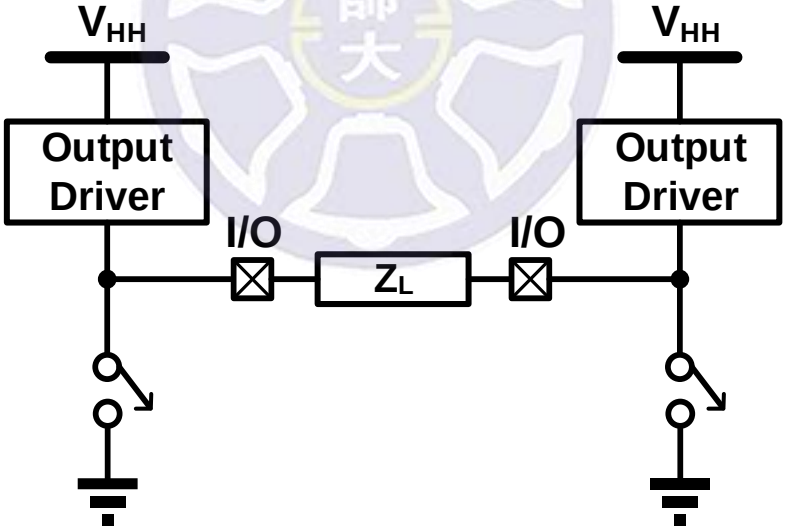


Fig. 1.9. Output driver with bipolar configuration.

The anodic and cathodic stimulus currents of the bipolar stimulator are generated by reversing the current paths using switches. The monopolar stimulation is preferred over a bipolar counterpart if the current is intended to spread over a wider area, and the monopolar stimulation is usually more efficient than the bipolar stimulation [18]. For multi-channel application, the number of interconnect leads between the stimulator and tissue by monopolar type is a half of the number by bipolar type, reducing chip area of contact pads . On the other hand, in the simultaneous stimulation using electrode arrays, the bipolar stimulation is preferred to monopolar stimulation, as the former can reduce crosstalk among neighboring sites [19].

1.4.2 ESD Protection Challenges

Biomedical electronics is becoming indispensible to health care solutions. Obviously, reliability may be the most important affect for biomedical electronics because of its life threatening nature, especially for portable and implantable devices.

For some biomedical electronics applications, the signal swing at input/output (I/O) pads may be higher than the supply voltage (V_{DD}) or lower than 0V (GND) [20]. To prevent from the reliability issues such as electrical overstress, the stacked MOS configuration is used to design the biomedical integrated circuits in these applications. Of course, the ESD protection devices at I/O pads also need to tolerate the signal swing which is higher than V_{DD} or lower than 0V, as illustrated in Fig. 1.10.

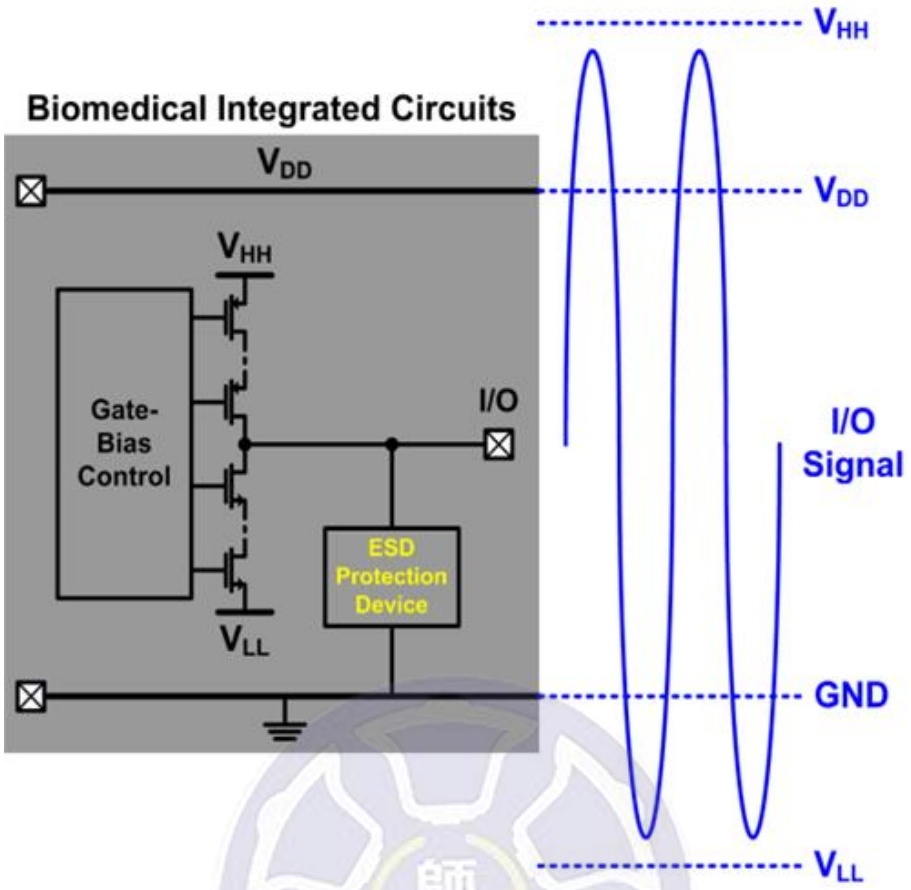


Fig. 1.10. Integrated circuits with large signal swing.

Because of its essence, biomedical electronics obviously requires robust ESD protection. Various distinct ESD design challenges must be affected for biomedical ICs. [21] - [23]. ESD has been considered as a major reliability in semiconductor industry for. As CMOS technology scales down, design of ESD protection circuits becomes more challenging. This is due to smaller channel lengths and thinner gate oxides in advanced technologies that make them more sensitive to ESD damages. As a result, design window for the ESD protection circuit becomes narrower. In the design of an ESD protection circuit, in addition to ESD robustness, the interaction between the main circuit and the protection circuit should be well understood.

The ESD specifications of commercial IC products are generally required to be higher than 2 kV in HBM ESD stress. In order to design a robust ESD protection circuit, a deeper insight of the device behavior under high current and high voltage stress conditions is required.

1.5 Thesis Organization

In Chapter 1, introduces the basic background knowledge of ESD protection design and the thesis organization.

In Chapter 2, novel dual-directional silicon-controlled rectifier (DDSCR) ESD protection devices will be introduced in detail. In this study, all testing devices are fabricated in 0.18um CMOS process.

In Chapter 3, novel high-voltage output driver is successfully verified in 0.18um CMOS process in the chapter, some simulation of the high-voltage output driver will be introduced. Next, the novel high-voltage output driver will also be equipped with the novel ESD protection devices to measure the ESD robustness of the circuits.

The last chapter, chapter 4, recapitulates the major consideration of this thesis and concludes with suggestions for future investigation.

Chapter 2

Novel Dual-Directional SCR in Output Stage with Monopolar Configuration

2.1 Introduction

CMOS technologies are attractive to implement the integrated circuits for biomedical electronics applications [24]-[26]. However, the transistors currently used in CMOS technologies are vulnerable to electrostatic discharge (ESD) events, which is the major reliability concern. In order to sustain the required ESD robustness, the on-chip ESD protection devices must be added in the IC products. A typical specification for a commercial IC on human-body-model (HBM) ESD robustness is 2 kV. If consider the reliability of biomedical integrated circuits used on the human, the required ESD robustness may be even higher.

The conventional ESD protection devices have the drawback of leakage current. Fig. 2.1 shows the conventional ESD protection devices used in the CMOS technologies, including diode, gate-grounded NMOS (GGNMOS), silicon-controlled rectifier (SCR), and dual-directional SCR (DDSCR) [27]-[30]. A parasitic pn junction exists in the conventional ESD protection devices with the common grounded P-substrate, as shown in Fig. 2.1.

In this chapter, a novel ESD protection design for output stage is investigated in a 0.18-um 1.8V/3.3V CMOS process.

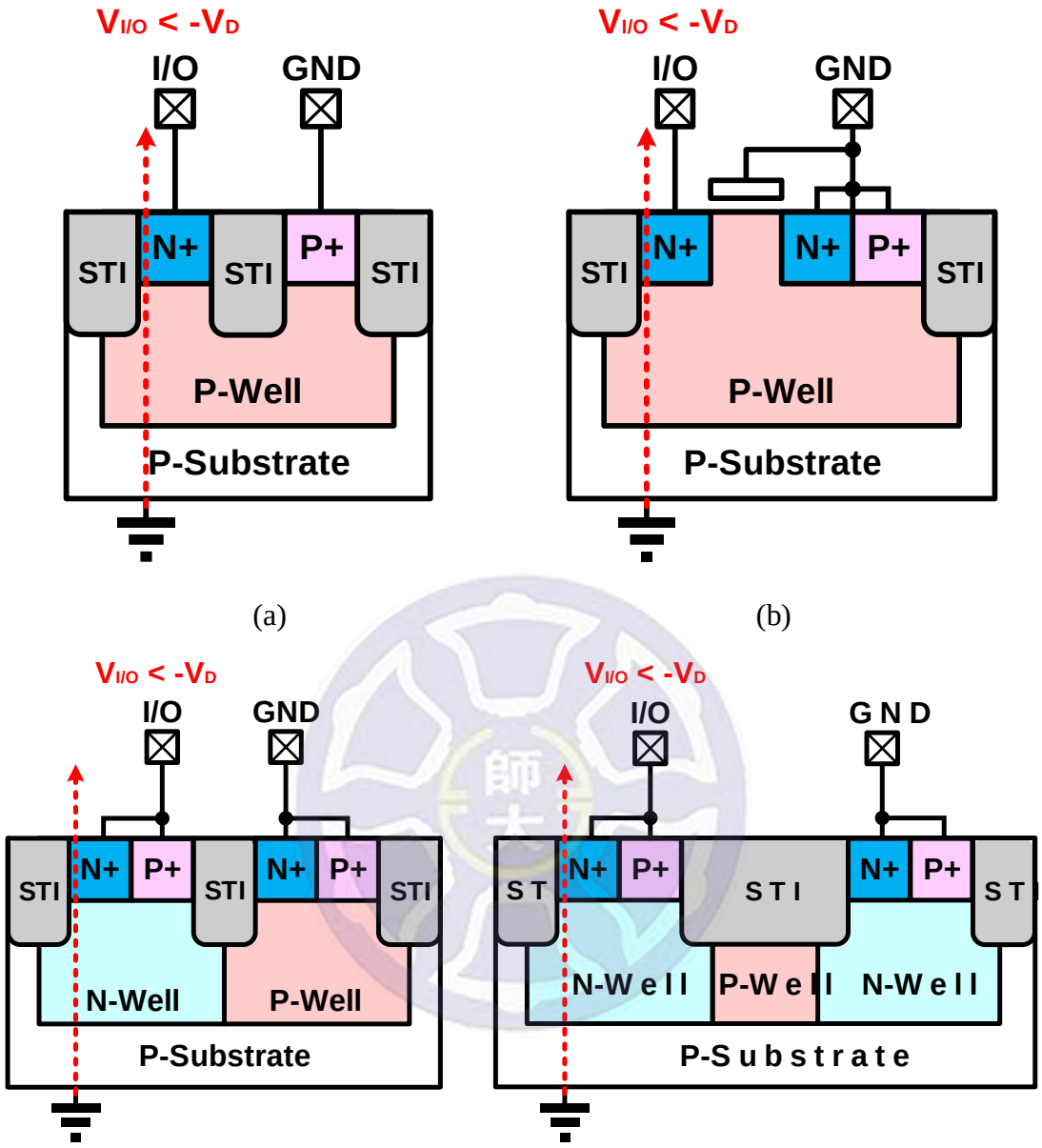
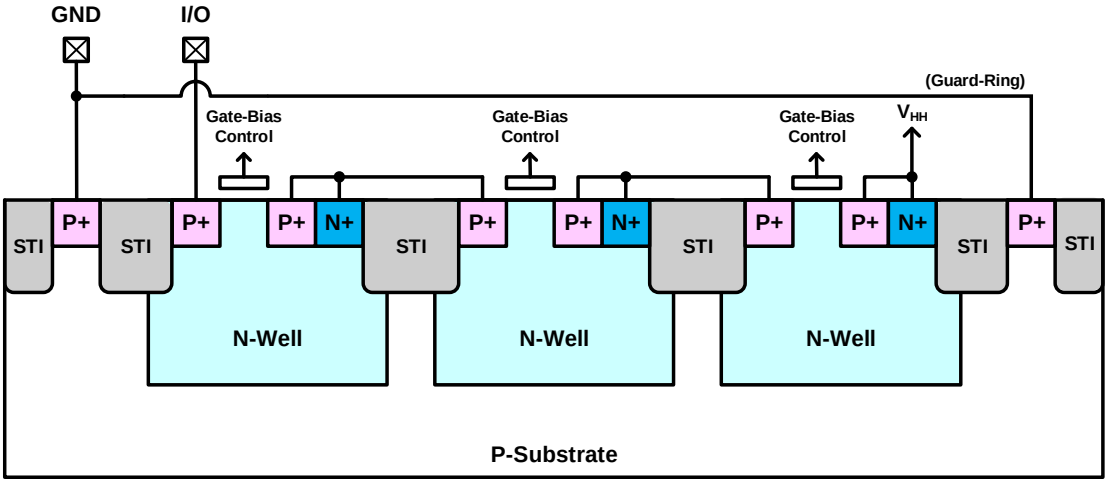


Fig. 2.1. Cross-sectional view of conventional ESD protection devices: (a) diode, (b) GGNMOS, (c) SCR, and (d) DDSCR.

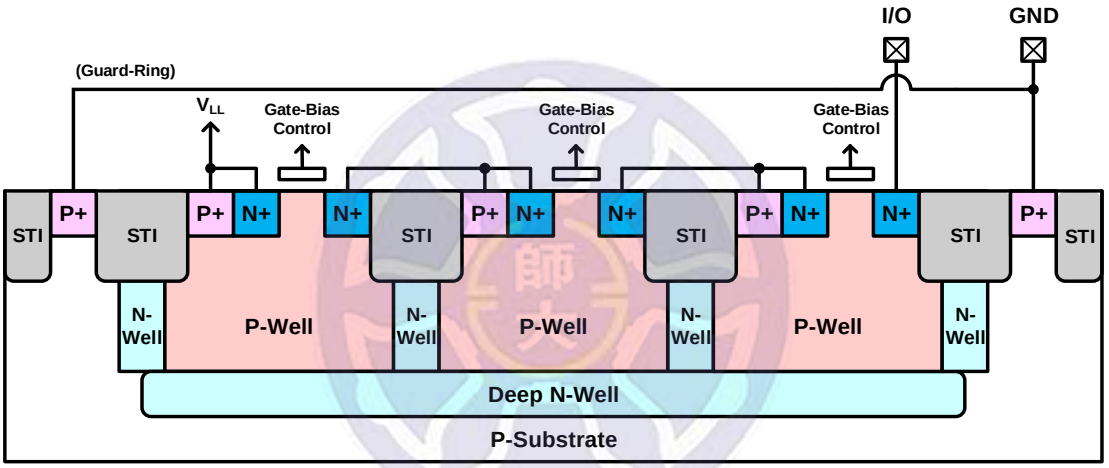
2.2 ESD Robustness of Stand-Alone Output Stage with monopolar configuration

The stacked PMOS and NMOS of the output stage of electrical stimulator are shown in Figs. 2.2(a) and 2.2(b), respectively. To investigate the I-V characteristics of the stand-alone output stage of electrical stimulator under ESD-like conditions, the transmission line pulsing (TLP) system with a 10-ns rise time and a 100-ns pulse width is used. The TLP-measured I-V curves of the test devices are shown in Fig. 2.3.

According to the test results, the stacked PMOS and NMOS under ESD-like conditions can sustain up to 27V and 25V, respectively, without damage (increasing leakage current). In other word, the additional ESD protection device must clamp the overshoot voltage lower than 25V to prevent the electrical stimulator from ESD damages.

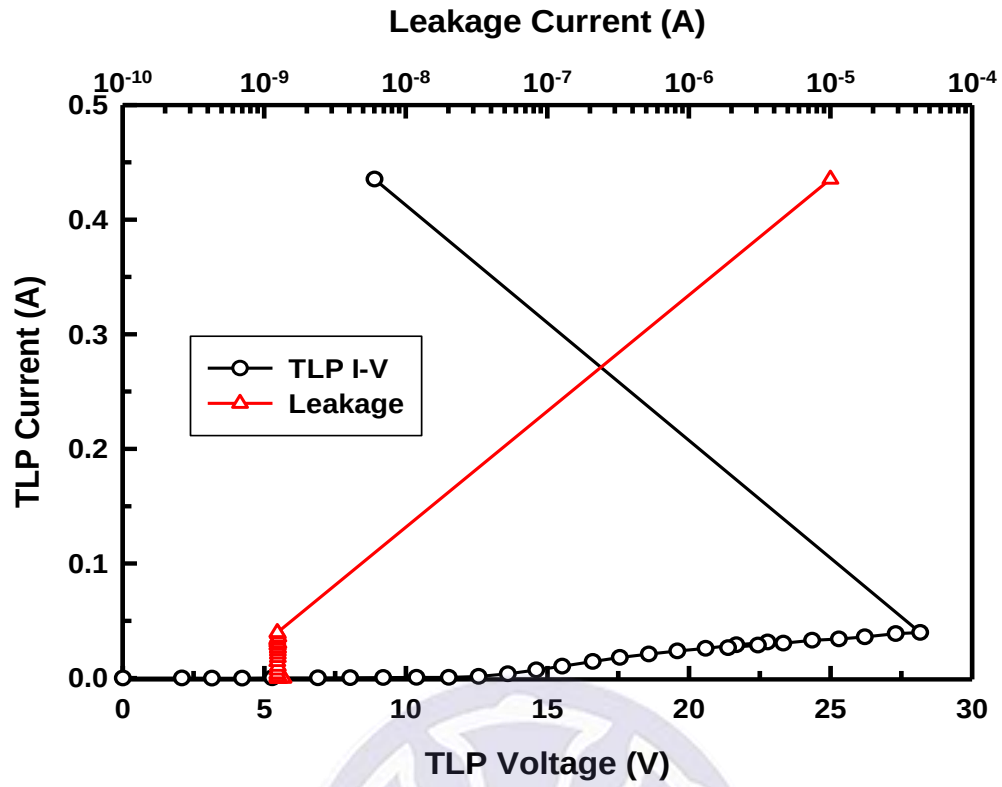


(a)

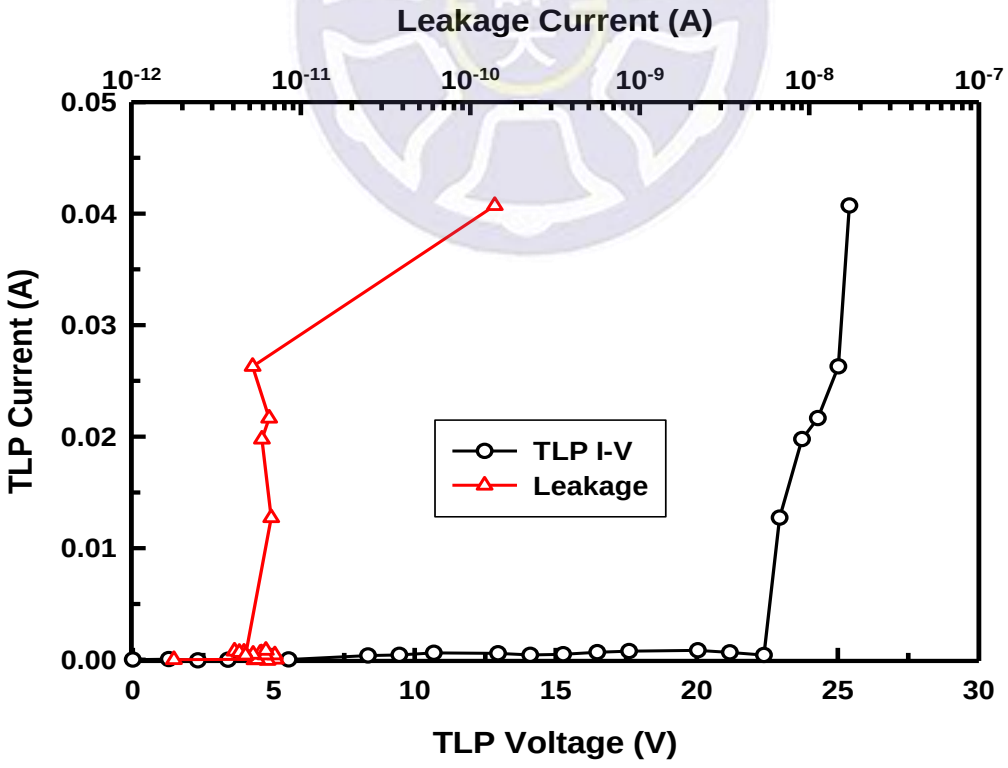


(b)

Fig. 2.2. Cross-sectional view of output stage of electrical stimulator: (a) stacked PMOS and (b) stacked NMOS.



(a)



(b)

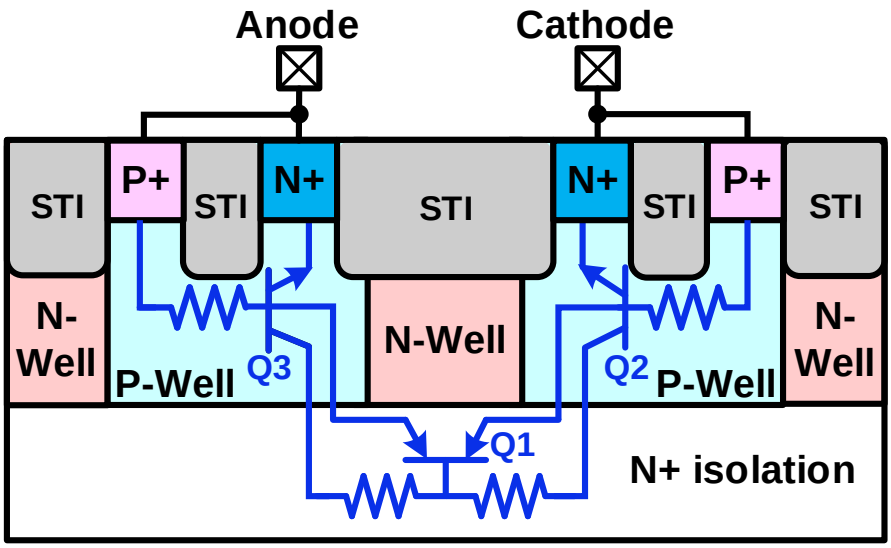
Fig. 2.3. Measured TLP I-V curves of (a) stacked PMOS and (b) stacked NMOS.

2.3 ESD Protection Design for Output Stage

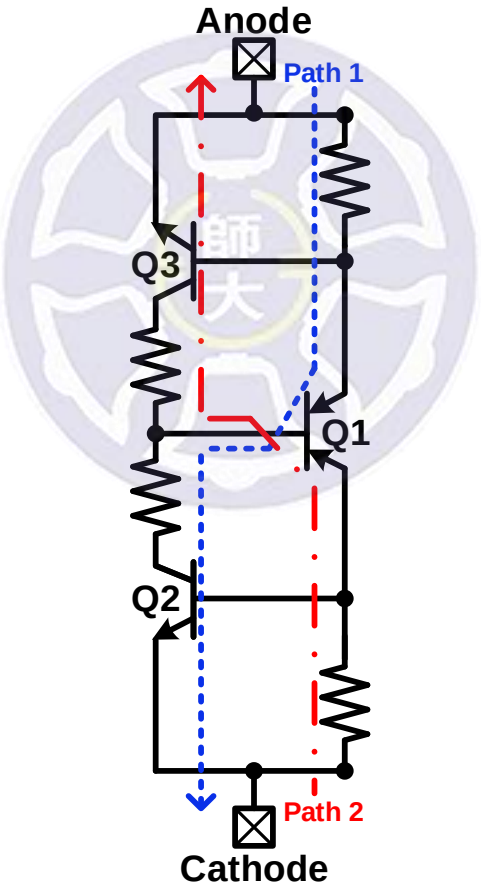
2.3.1 DDSCR-Based Devices for CMOS On-Chip ESD Protection

A typical SCR device provides only one direction ESD protection path. The dual-direction SCR (DDSCR) device can protect each I/O pad against ESD stress in the PS-mode (positive-to-V_{SS}), NS-mode (negative-to-V_{DD}), PD-mode (positive-to-V_{DD}), and ND-mode (negative-to-V_{SS}) [31]. The device structure of a DDSCR device illustrated in Fig. 2.4(a) is a symmetrical five-layer NPNPN structure comprising two vertical NPN and one lateral PNP. Adding another layer of N+ isolation can avoid leakage current issue of conventional ESD devices.

When a positive ESD pulse is applied to the anode of DDSCR and its cathode is relatively grounded. The positive ESD current can be discharged through the current path1 is shown in Fig. 2.4(b). Similarly, when a negative ESD pulse is applied to anode of DDSCR with its cathode grounded, the negative ESD current can be discharged through the current path2 is shown in Fig. 2.4(b). The DDSCR provides low holding voltage and low impedance path to discharge the ESD current under every stress mode.



(a)



(b)

Fig. 2.4 (a) The cross-sectional view of the dual-direction SCR structure, (b) Equivalent circuit schematic of a SCR device.

2.3.2 Novel Dual-Directional SCR

In this work, a novel dual-directional SCR (DDSCR) device for ESD protection in biphasic output driver was proposed. This design can achieve low leakage, large swing tolerance, and high ESD robustness.

Two kinds of layout of the DDSCR device are shown in Fig. 2.5. In the Figs. 2.5(a) and 5(b), the SCR paths are divided into 4 and 8 segments, respectively. The SCR paths consist of P+/P-well/N-well/P-well/N+. The SCR paths along A-A' and B-B' provide the discharging path from I/O to GND and from GND to I/O, respectively, as shown in Fig. 2.6. The distance between I/O and GND of SCR is wished to be minimized, so the layout style with minimized "d" is used. The test devices have been fabricated in a 0.18-um 1.8-V CMOS process. All the dimensions of test devices are listed in Table 2.2.

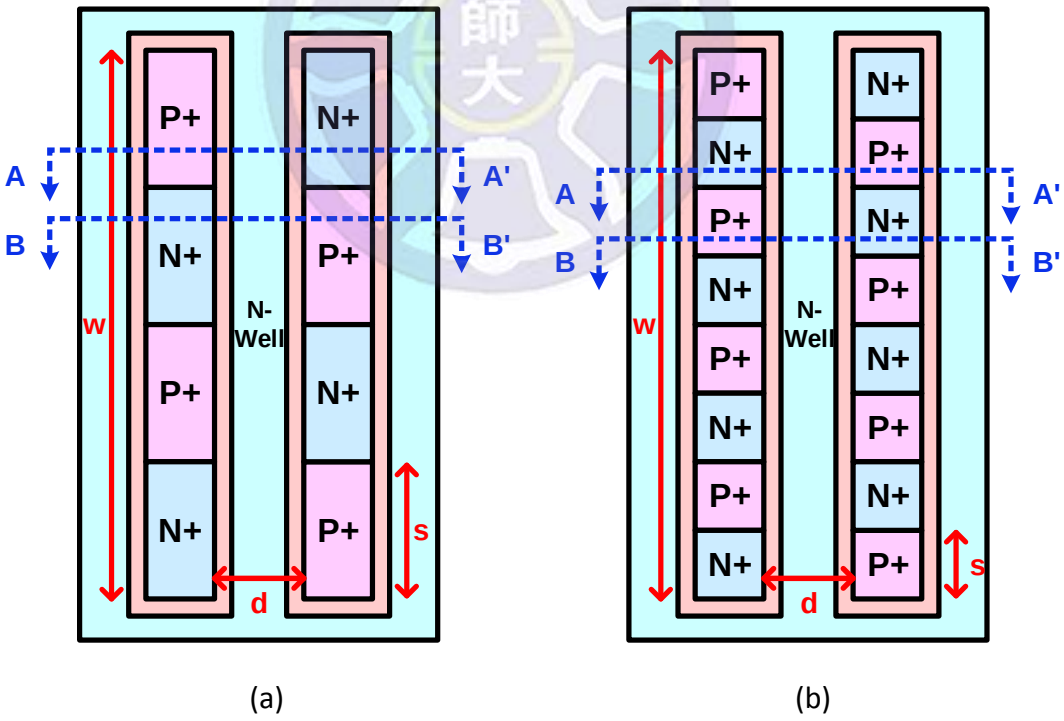


Fig. 2.5. Layout top view of DDSCR1 with (a) 4 segments and (b) 8 segments.

In order to reduce the switching voltage of DDSCR1 device to provide more effective ESD protection for the internal circuits, the DDSCR2 and DDSCR3 was invented. The devices structure of the DDSCR2 and DDSCR3 are illustrated in Fig. 2.7 and Fig. 2.8.

The DDSCR2 and DDSCR3 devices are made by adding an N+ diffusion is inserted into the N-well to lower the avalanche breakdown voltage of N-well/P-well junction. The inserted N+ diffusions are connected out as the n-trigger nodes of the DDSCR2 and DDSCR3 devices.

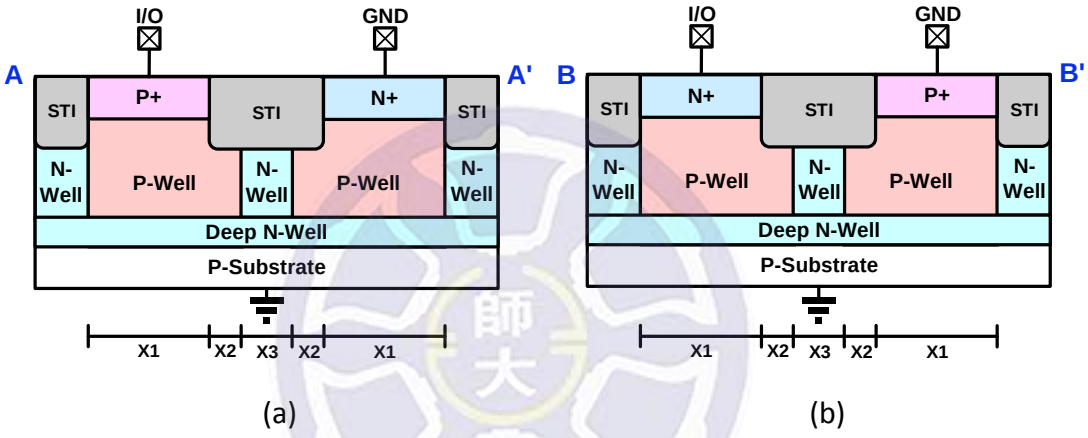


Fig. 2.6. Cross-sectional view of DDSCR1 along (a) A-A' and (b) B-B'.

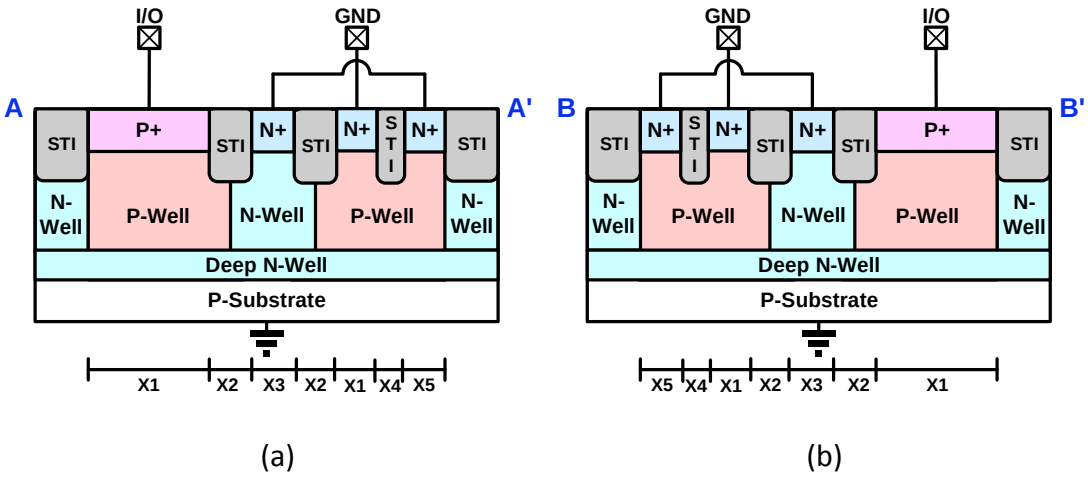


Fig. 2.7. Cross-sectional view of DDSCR2 along (a) A-A' and (b) B-B'.

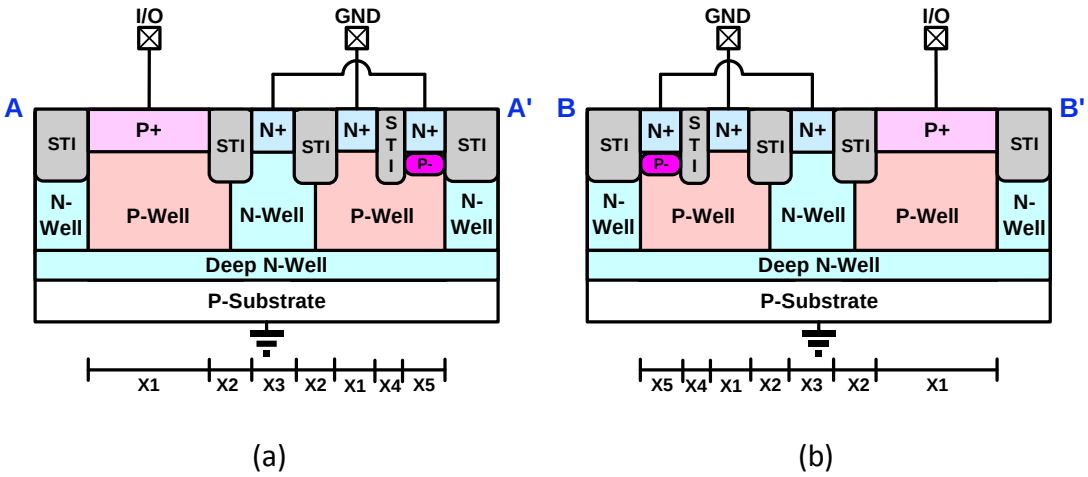
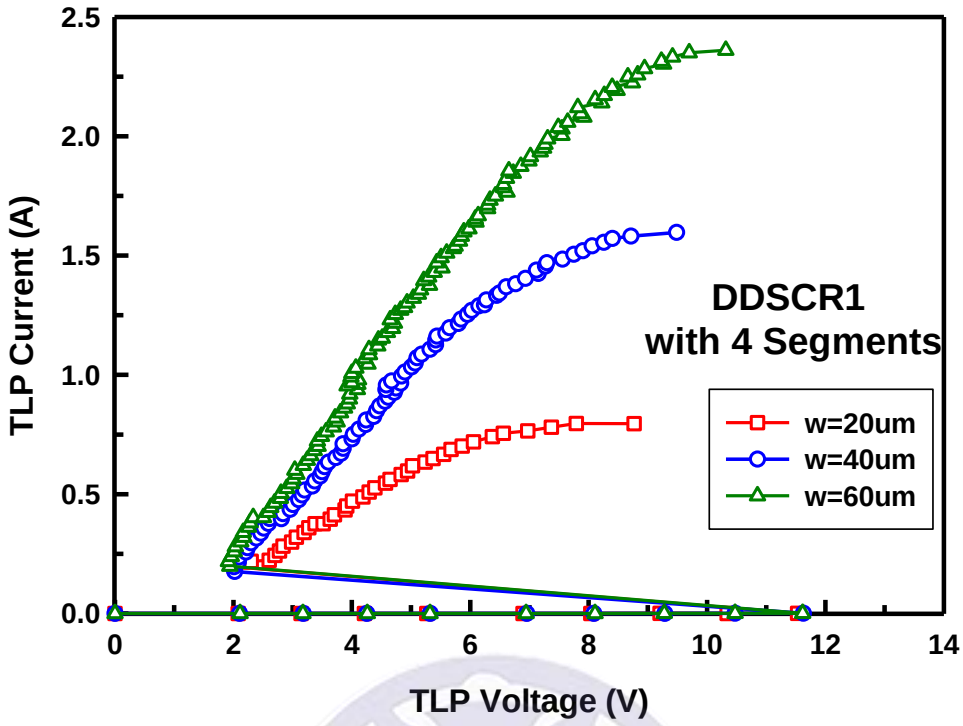


Fig. 2.8. Cross-sectional view of DDSCR3 along (a) A-A' and (b) B-B'.

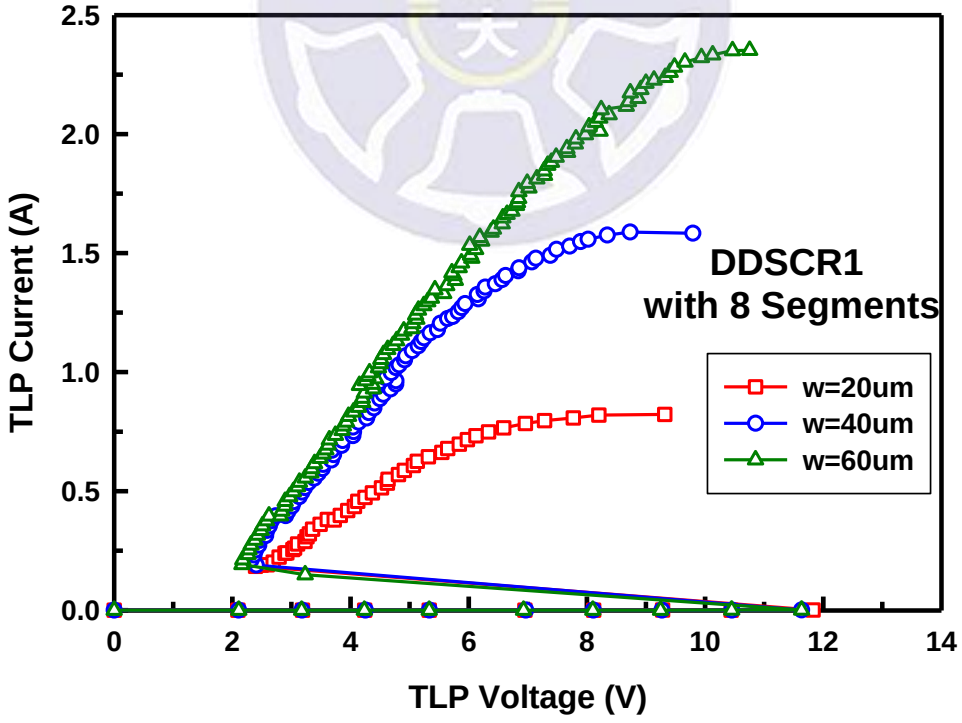
2.4 Experimental Results of novel DDSCR

2.4.1 Measured TLP I-V Characteristics

To investigate the turn-on behavior and the I-V characteristics in high-current regions of the ESD protection devices, the transmission-line-pulsing (TLP) system with 10-ns rise time and 100-ns pulse width is used. The TLP-measured I-V characteristics are shown in Figs. 2.9~2.11. The trigger voltages (V_{t1}) of the test devices are about 9~12V, which means the ESD protection devices can sustain the signal swing up to ±9V. The secondary breakdown current (I_{t2}) of ESD protection device, which indicated the current-handling ability, can also be obtained from the TLP-measured I-V curves. All these measurement results are also listed in Table 2.3.

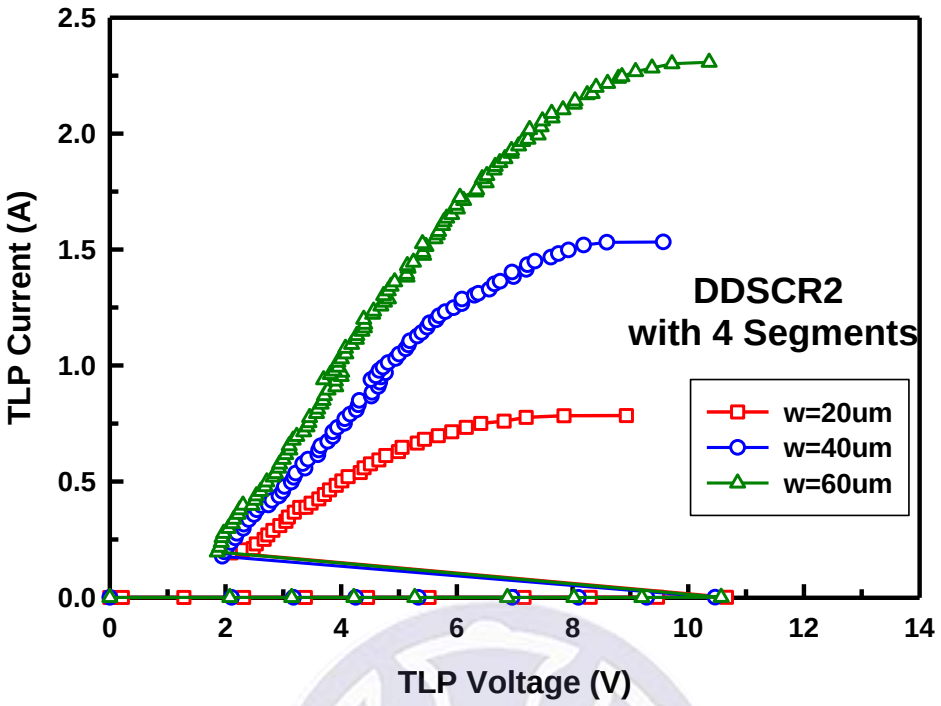


(a)

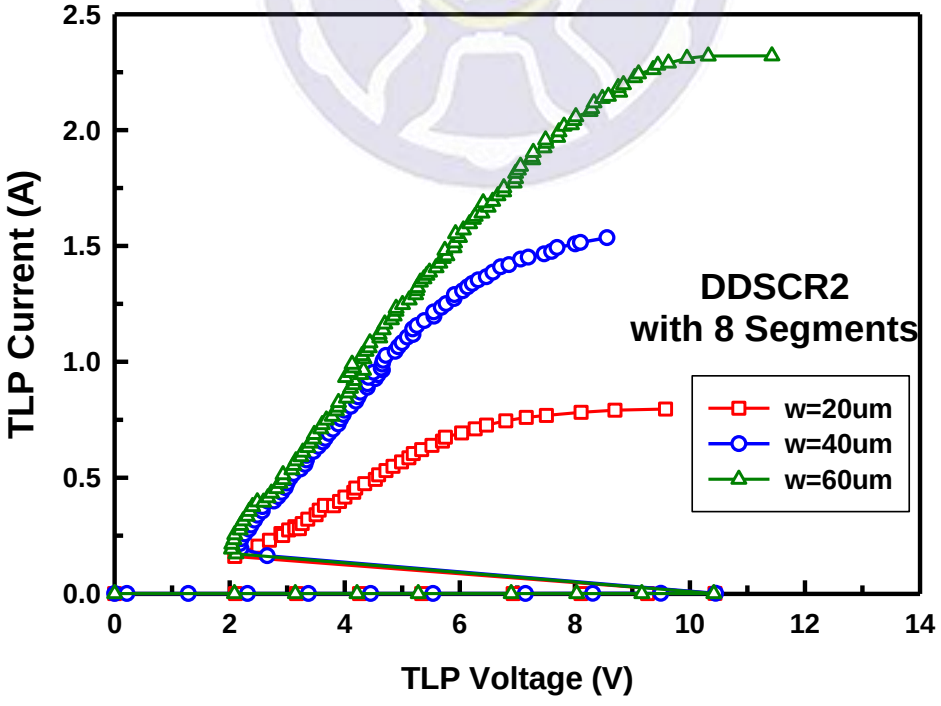


(b)

Fig. 2.9. Measured TLP I-V curves of DDSCR1 with (a) 4 segments and (b) 8 segments.

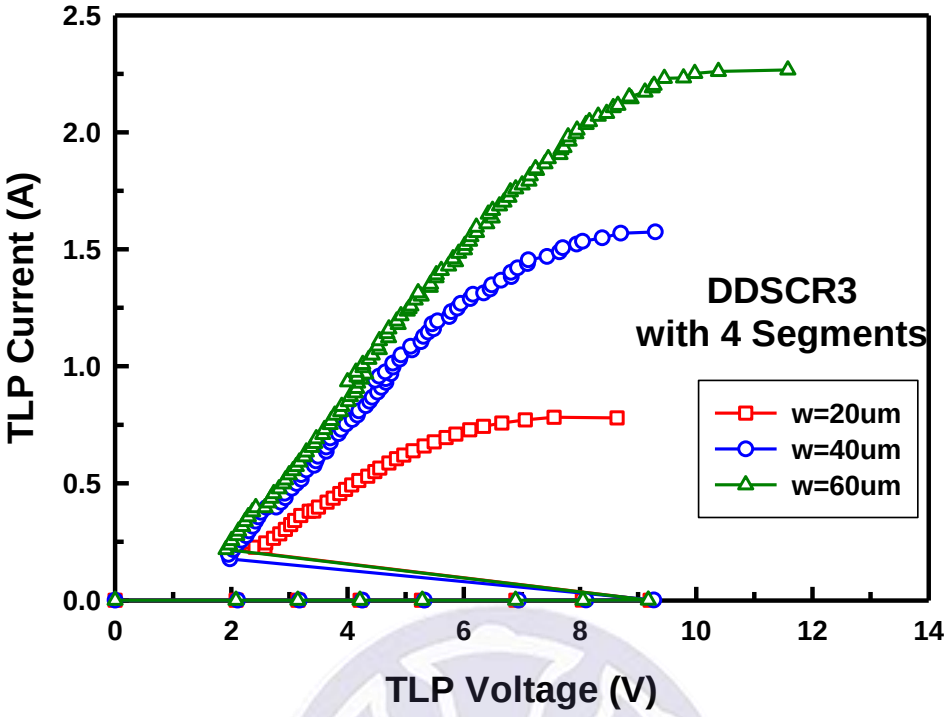


(a)

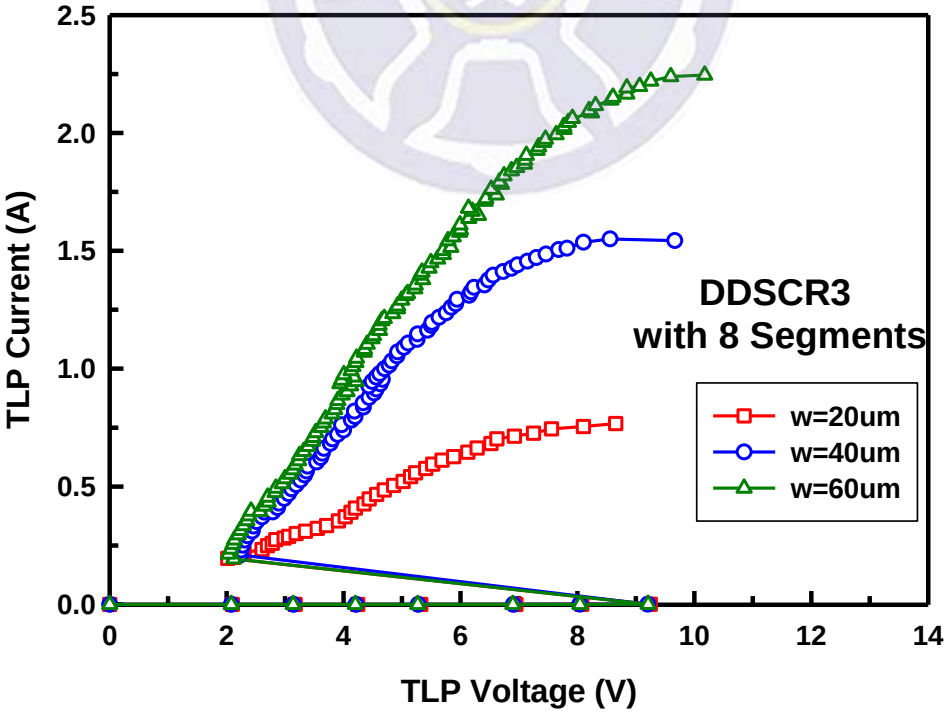


(b)

Fig. 2.10. Measured TLP I-V curves of DDSCR2 with (a) 4 segments and (b) 8 segments.



(a)



(b)

Fig. 2.11. Measured TLP I-V curves of DDSCR3 with (a) 4 segments and (b) 8 segments.

2.4.2 Measured DC I-V Characteristics

In order to further ascertain the possibility of the parasitic bipolar to reach and maintain holding state, relationship between power supply voltage and holding voltage need to be explored. In this work, the snapback holding voltage of novel DDSCR devices, have been investigated by curve tracer, the measurement was carried out with Tektronix 370A curve tracer as shown in Fig. 2.12~ 2.17. All these measurement results are listed in Table 2.1.

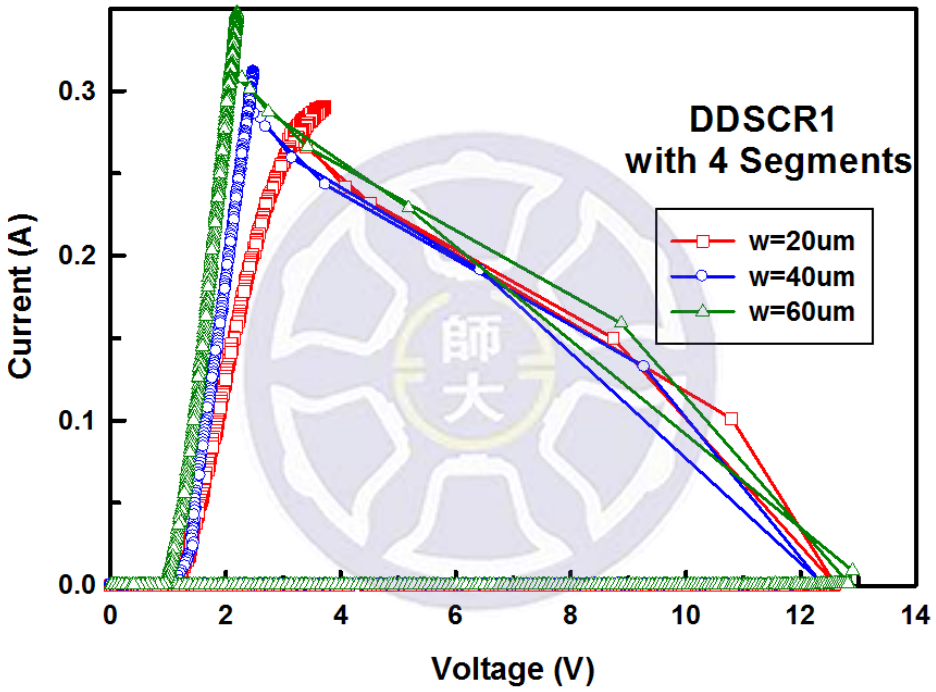


Fig. 2.12. I-V characteristics of DDSCR1 with 4 segments measured by dc curve tracer.

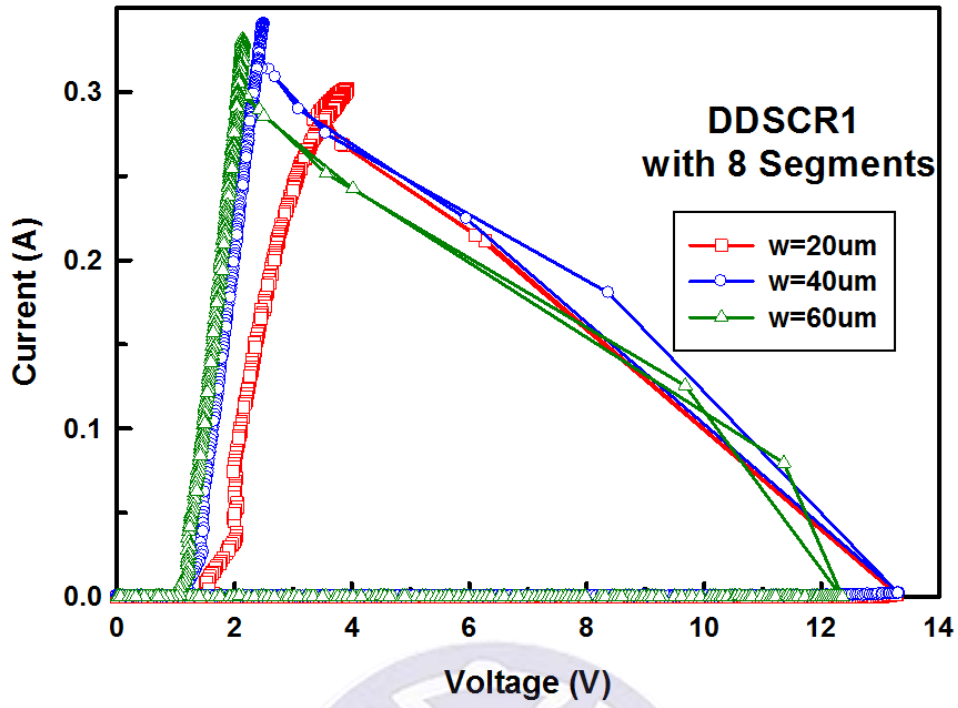


Fig. 2.13. I-V characteristics of DDSCR1 with 8 segments measured by dc curve tracer.

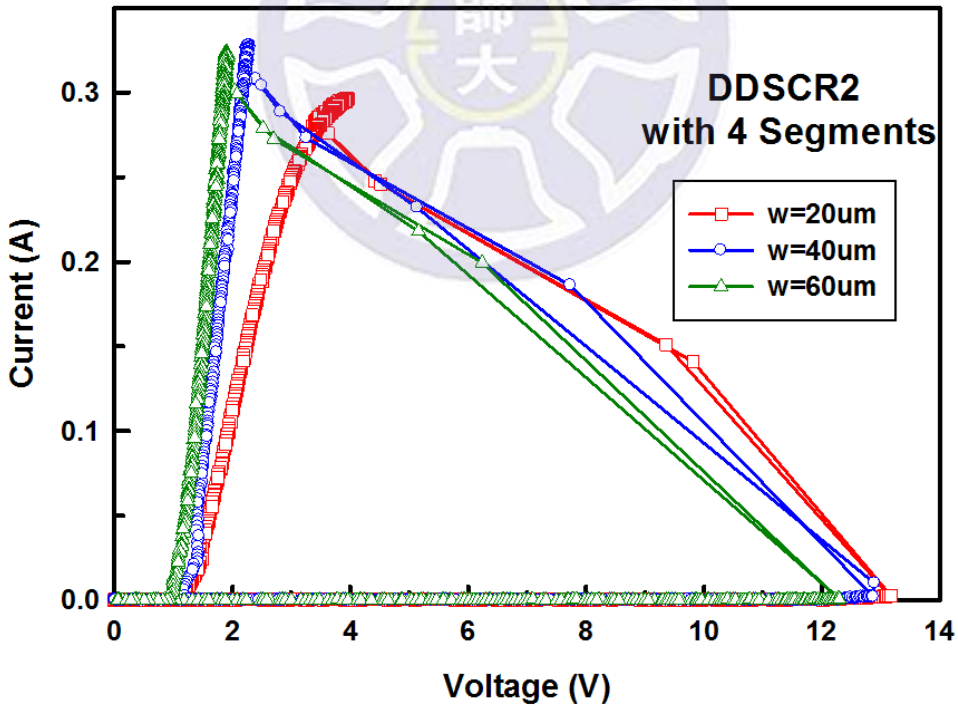


Fig. 2.14. I-V characteristics of DDSCR2 with 4 segments measured by dc curve tracer.

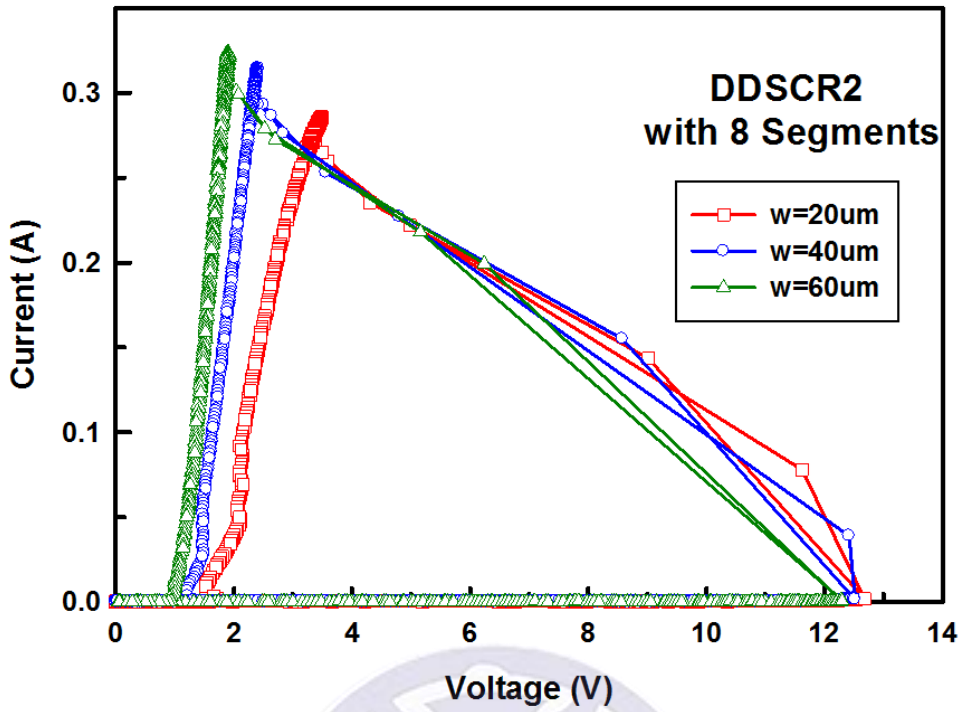


Fig. 2.15. I-V characteristics of DDSCR2 with 8 segments measured by dc curve tracer.

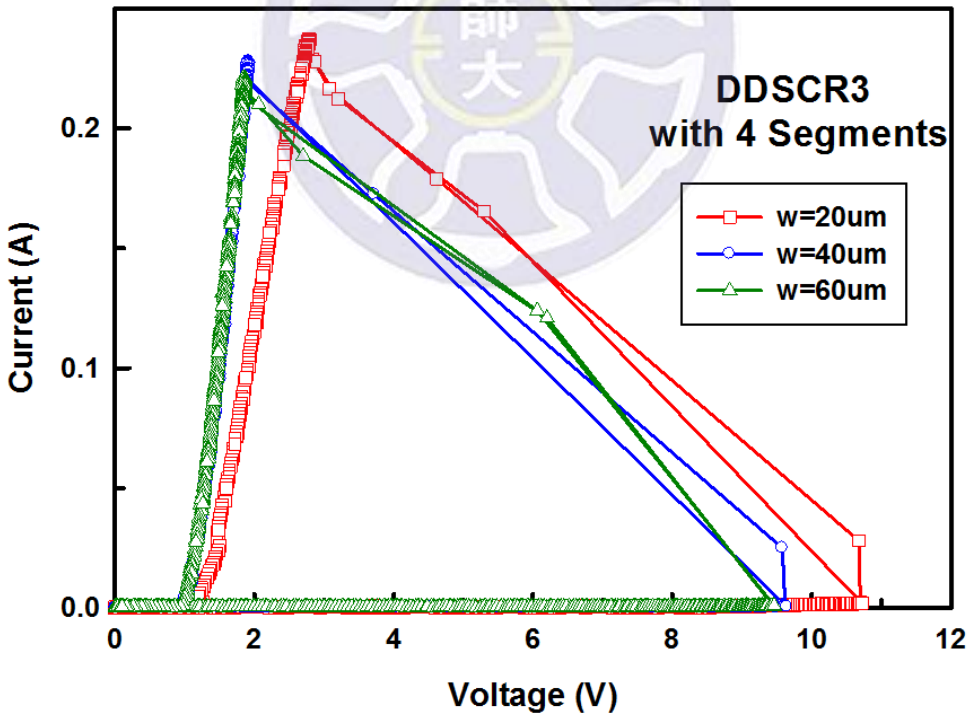


Fig. 2.16. I-V characteristics of DDSCR3 with 4 segments measured by dc curve tracer.

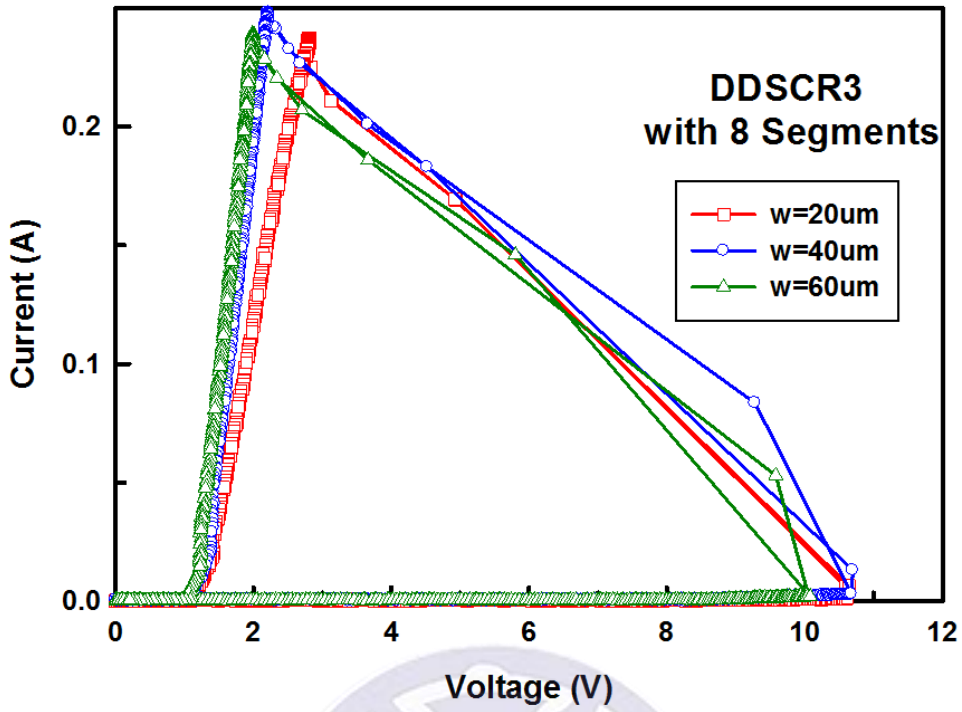


Fig. 2.17. I-V characteristics of DDSCR3 with 8 segments measured by dc curve tracer.

Table 2.1

The I-V characteristics of the DDSCR measured results by DC curve tracer.

Test Device	w (um)	Vt1 (V)	Test Device	w (um)	Vt1 (V)
DDSCR1 with 4 Segments	20	1.49	DDSCR1 with 8 Segments	20	1.14
	40	1.20		40	1.18
	60	1.06		60	1.02
DDSCR2 with 4 Segments	20	1.22	DDSCR2 with 8 Segments	20	1.51
	40	1.14		40	1.20
	60	0.99		60	0.98
DDSCR3 with 4 Segments	20	1.20	DDSCR3 with 8 Segments	20	1.16
	40	1.00		40	1.16
	60	0.96		60	1.06

2.4.3 Measured ESD Robustness

The ESD robustness of test devices are evaluated by the HBM tester. The failure criterion is defined as the I-V characteristics shifting over 30 % from its original curve after ESD stressed at every ESD test level. All these measurement results are listed in Table 2.3.

2.4.4 Measured Parasitic Capacitance

With the on-wafer measurement, the two-port S-parameters of the test devices were measured by using the vector network analyzer. The parasitic effects of the pads have been removed by using the de-embedding technique [32]. The parasitic capacitance of each test device can be extracted from the S-parameters. Fig. 2.12 shows the extracted parasitic capacitance of the test devices.

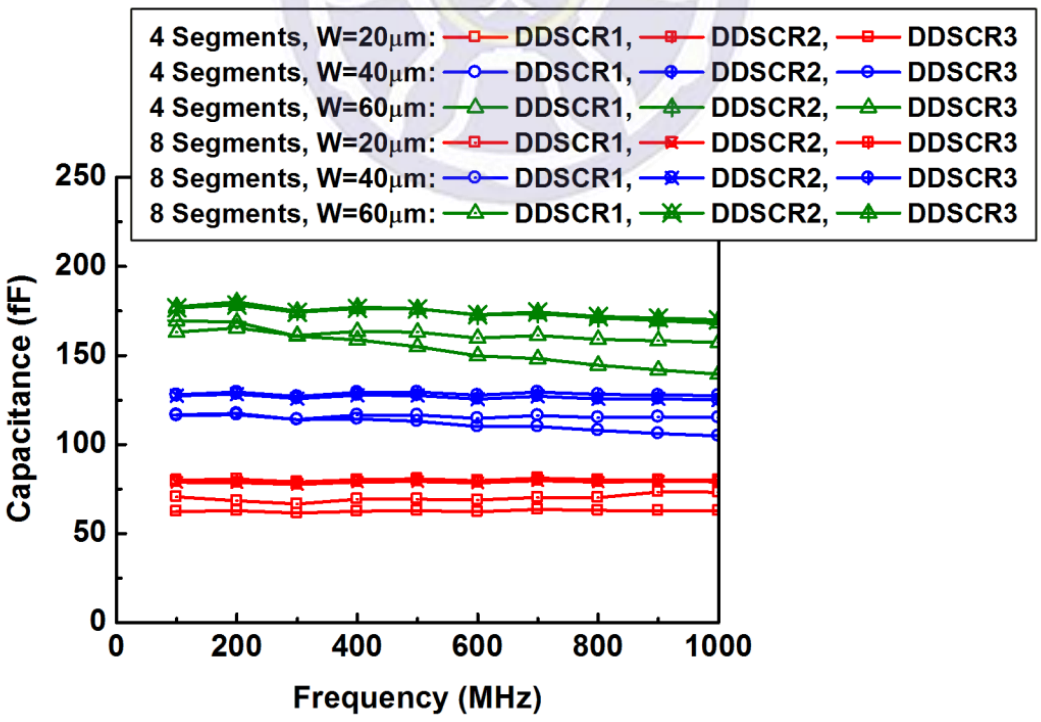


Fig. 2.18. Measured parasitic capacitances.

Table 2.2

Design parameters of test devices

Test Device	w (um)	d (um)	s (um)	X1 (um)	X2 (um)	X3 (um)	X4 (um)	X5 (um)
DDSCR1 with 4 Segments	20	2.26	5	1.29	0.43	1.4	N/A	N/A
	40	2.26	10	1.29	0.43	1.4	N/A	N/A
	60	2.26	15	1.29	0.43	1.4	N/A	N/A
DDSCR1 with 8 Segments	20	2.26	2.5	1.29	0.43	1.4	N/A	N/A
	40	2.26	5	1.29	0.43	1.4	N/A	N/A
	60	2.26	7.5	1.29	0.43	1.4	N/A	N/A
DDSCR2 with 4 Segments	20	2.26	5	1.29	0.92	0.42	0.8	1.5
	40	2.26	10	1.29	0.92	0.42	0.8	1.5
	60	2.26	15	1.29	0.92	0.42	0.8	1.5
DDSCR2 with 8 Segments	20	2.26	2.5	1.29	0.92	0.42	0.8	1.5
	40	2.26	5	1.29	0.92	0.42	0.8	1.5
	60	2.26	7.5	1.29	0.92	0.42	0.8	1.5
DDSCR3 with 4 Segments	20	2.26	5	1.29	0.92	0.42	0.8	1.5
	40	2.26	10	1.29	0.92	0.42	0.8	1.5
	60	2.26	15	1.29	0.92	0.42	0.8	1.5
DDSCR3 with 8 Segments	20	2.26	2.5	1.29	0.92	0.42	0.8	1.5
	40	2.26	5	1.29	0.92	0.42	0.8	1.5
	60	2.26	7.5	1.29	0.92	0.42	0.8	1.5

Table 2.3

Measurement results of test devices

Test Device	HBM Level (kV)	V_{t1} (V)	V_h (V)	I_{t2} (A)	C (fF)	R_{ON} (ohm)
DDSCR1 with 4 Segments	2.0	11.5	2.0	0.8	67.1	6.55
	4.0	11.5	2.0	1.6	110.5	3.39
	5.0	11.6	1.9	2.3	154.9	2.85
DDSCR1 with 8 Segments	2.0	11.8	2.3	0.8	70.6	6.82
	3.5	11.6	2.3	1.6	116.4	3.43
	5.0	11.8	2.2	2.4	163.1	2.92
DDSCR2 with 4 Segments	2.0	10.4	2.0	0.8	74.9	6.48
	3.5	10.5	1.9	1.5	121.0	3.32
	5.0	10.4	1.9	2.3	167.8	2.89
DDSCR2 with 8 Segments	2.0	10.4	2.0	0.8	78.9	6.73
	3.5	10.4	2.0	1.5	127.4	3.47
	4.5	10.4	2.0	2.2	176.7	2.91
DDSCR3 with 4 Segments	2.0	9.2	2.0	0.7	62.5	6.57
	3.5	9.2	1.9	1.5	116.7	3.35
	5.0	9.2	2.0	2.2	169.5	2.81
DDSCR3 with 8 Segments	2.0	9.2	2.0	0.8	80.1	6.63
	3.5	9.2	2.0	1.5	128.0	3.43
	4.5	9.2	2.0	2.2	177.3	2.88

2.4.5 Document Comparison of DDSCR

The comparison among various DDSCR-based devices for CMOS on-chip ESD protection has been summarized in Table 2.4. The trigger voltage (V_{t1}) and the holding voltage (V_h) of DDSCR-based devices must be finely designed to fully and effectively protect the output stage.

Table 2.4

Comparison among the DDSCR-based devices for on-chip ESD protection

Test Device	Technology	W (um)	HBM Level (kV)	V_{t1} (V)	V_h (V)	I_{t2} (A)	C (fF)	R_{ON} (ohm)
References [44]	0.18um CMOS	30	3.0	16.9	4.5	2.9	N/A	3.33
References [47]	N/A	N/A	N/A	10.2	4.6	2.2	N/A	N/A
DDSCR1 with 4 Segments	0.18um CMOS	20	2.0	11.5	2.0	0.8	67.1	6.55
		40	4.0	11.5	2.0	1.6	110.5	3.39
		60	5.0	11.6	1.9	2.3	154.9	2.85
DDSCR2 with 4 Segments	0.18um CMOS	20	2.0	10.4	2.0	0.8	74.9	6.48
		40	3.5	10.5	1.9	1.5	121.0	3.42
		60	5.0	10.4	1.9	2.3	167.8	2.89
DDSCR3 with 4 Segments	0.18um CMOS	20	2.0	9.2	2.0	0.7	62.5	6.57
		40	3.5	9.2	1.9	1.5	116.7	3.35
		60	5.0	9.2	2.0	2.2	169.5	2.81

2.5 Summary

The dual-directional SCR (DDSCR) device has been developed for on-chip ESD protection in output driver. Verified in 0.18-um CMOS process, this design can achieve low leakage, large swing tolerance, and high ESD robustness.

Chapter 3

Novel Embedded SCR Device in Output Stage with Bipolar Configuration

3.1 Introduction

In nanoscale CMOS technologies, the feature size has been scaled down to improve circuit performances with the decreased power supply voltage for low-power applications. However, the higher output voltage levels are still needed for the external I/O to communicate with other circuits in the microelectronic systems or subsystems, such as 3.3V or 5V for some signaling standards. Even higher output voltage levels are needed for some applications, such as >10V for display driver and biomedical stimulator. Therefore, the high-voltage output driver must be designed with the consideration of high-voltage tolerance [33], [34]. To avoid the overstress issue without using additional high-voltage device, stacking low-voltage devices is usually used for the high-voltage output driver [35]-[37]. Once the voltage drop divided equally across the stacked devices, this configuration allows for higher voltage, and no single device is overstressed. A conventional $3xV_{DD}$-tolerant stacked-device output driver is shown in Fig. 3.1, which consists of a control circuit and a pair of triply-stacked MOS in the output stage [38], [39].

Electrostatic discharge (ESD), which is the significant reliability issue, may cause the damage in IC products. The transistors currently used in CMOS technologies are vulnerable to ESD events. To provide the required ESD robustness, on-chip ESD protection design must be added in the integrated circuits, including the output driver [40]. For example, a typical specification for a commercial IC on HBM ESD robustness is 2kV. With the help of high-voltage-tolerant ESD clamp circuit [41]-[43] and the parasitic body-to-drain diodes, the on-chip ESD protection for stacked-device output driver is shown in Fig. 3.2. The ESD currents can be discharged from V_{OUT} to $3xV_{DD}$ (path ①), from GND to V_{OUT} (path ②), from V_{OUT} to GND (path ①+③), and from $3\times V_{DD}$ to V_{OUT} (path ④ + ②). This ESD protection design can provide the corresponding ESD current paths during all kinds of ESD events at V_{OUT} pad. However, in the output stage, the sizes of PMOS devices are usually larger than those of NMOS devices to have symmetrical driving ability, which makes the asymmetrical ESD current paths. With the smaller NMOS devices, the ESD robustness of path ② is usually lower than that of path ①. Of course, the designer can use some dummy NMOS devices or additional ESD diodes to improve the ESD robustness. In this work, a more efficient design by using embedded silicon-controlled rectifier (SCR) to improve ESD robustness is proposed. With the assistance of embedded SCR, the ESD robustness of NMOS part of stacked-device output driver can be improved without using any additional ESD protection device and layout area.

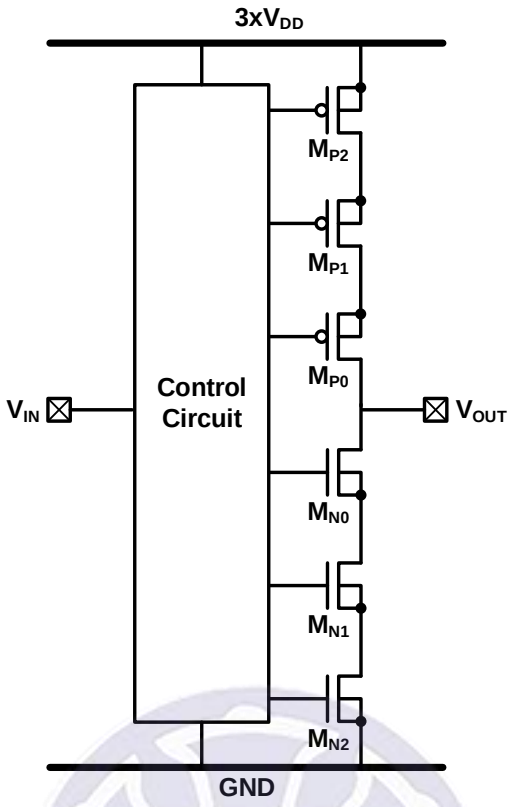


Fig. 3.1. Block diagram of $3xV_{DD}$-tolerant stacked-device output driver.

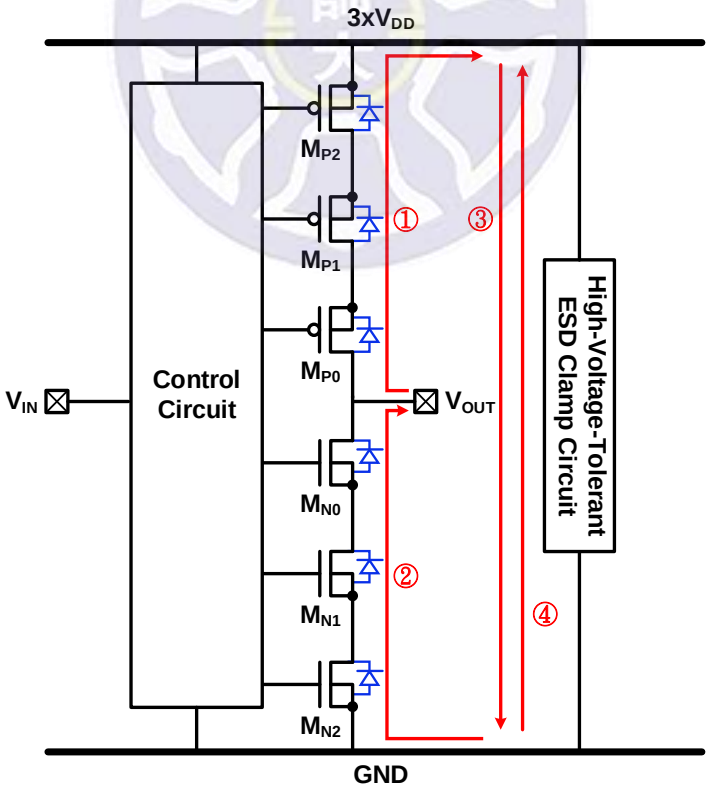


Fig. 3.2. ESD current paths in $3xV_{DD}$-tolerant stacked-device output driver with high-voltage-tolerant ESD clamp circuit.

3.2 Design of Novel High Voltage Output Driver

Fig. 3.3 shows the design of high voltage output driver, which consists of bias circuit, control circuit, and output stage. The 3.3V transistors in a standard 0.18μm CMOS process are used. Once the voltage differences across each transistor are lower than 3.63V (3.3V + 10%) [48], the foundry promises their reliability. The output driver is controlled by the input signal (V_{IN}) with voltage swing between 0V and 3.3V. The aims of this design are that the output signal (V_{OUT}) can swing between 0 and ~10V ($3xV_{DD}$), and the voltage differences across each transistor are lower than 3.63V to prevent from reliability issues, whether the output driver is turned on or off. In order to sustain the high voltage (~10V) without gate-oxide overstress, the stacked MOS configuration between $3xV_{DD}$ and ground is used. The bias circuit, which consists of three PMOS-diodes (M_{R1}~M_{R3}), is used to provide the biases of $2xV_{DD}$ (V_{DD2}) and $1xV_{DD}$ (V_{DD1}) from the $3xV_{DD}$. To reduce the bias current to the range of < mA, three PMOS with small width/length ratio are used. The control circuit includes two level shifters, and three buffers. The level shifters 1 and 2 transfer the signals with low-voltage level ($1xV_{DD}$) to the high-voltage levels ($2xV_{DD}$ and $3xV_{DD}$). The level shifter 1 with differential structure can transfer the V_{IN} and V_{i1a} (voltage swing: 0V ~ $1xV_{DD}$) to V_{i2} and V_{i2b} (voltage swing: $1xV_{DD}$ ~ $2xV_{DD}$). Similarly, the level shifter 2 can further transfer the V_{i2} and V_{i2b} to V_{i3} (voltage swing: $2xV_{DD}$ ~ $3xV_{DD}$). The buffers control the output stage to turn on or off.

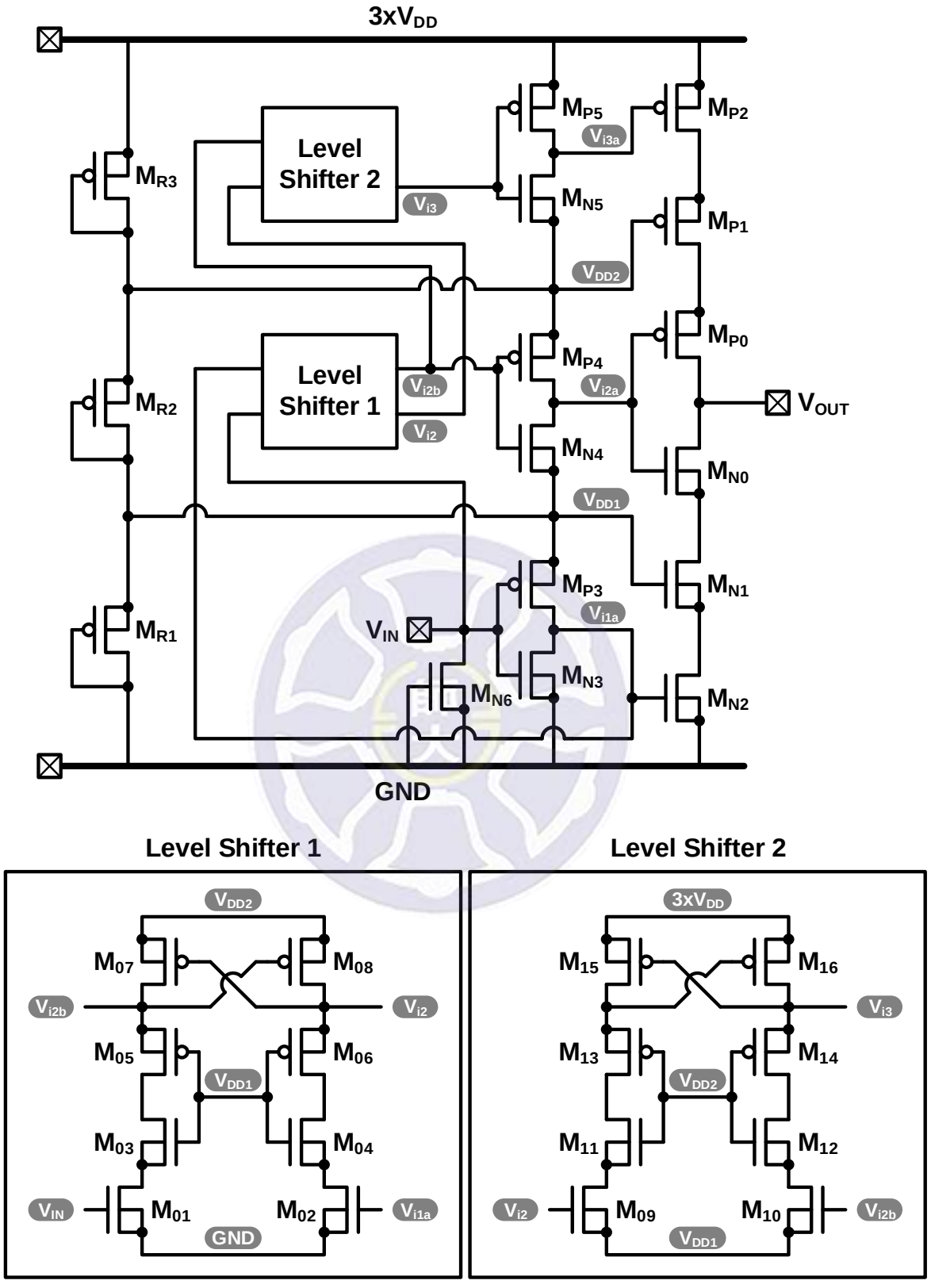


Fig. 3.3. Structure of high voltage output driver fabricated in 0.18-um 3.3-V CMOS process.

As V_{IN} is 0V, the gate potentials of M_{P0}, M_{P1}, and M_{P2} are designed to be $1xV_{DD}$, $2xV_{DD}$, and $3xV_{DD}$, respectively, so the stacked PMOS are kept off. In the meantime, the gate potentials of M_{N0}, M_{N1}, and M_{N2} are all $1xV_{DD}$, so the stacked NMOS conduct the V_{OUT} to 0V. As V_{IN} is 3.3V, the gate potentials of M_{N0}, M_{N1}, and M_{N2} are $2xV_{DD}$, $1xV_{DD}$, and 0V, respectively, so the stacked NMOS are kept off. In the meantime, the gate potentials of M_{P0}, M_{P1}, and M_{P2} are all $2xV_{DD}$, so the stacked PMOS conduct the V_{OUT} to $3xV_{DD}$. Shown in Fig. 3.4 is the schematic of a triply-stacked output driver that enables voltage drive up to 3x the transistor rating. Both scenarios are better depicted by the schematics in Fig. 3.4(b) and 3.4(c). Simple device stacking as explained poses certain reliability risks during switching transitions.

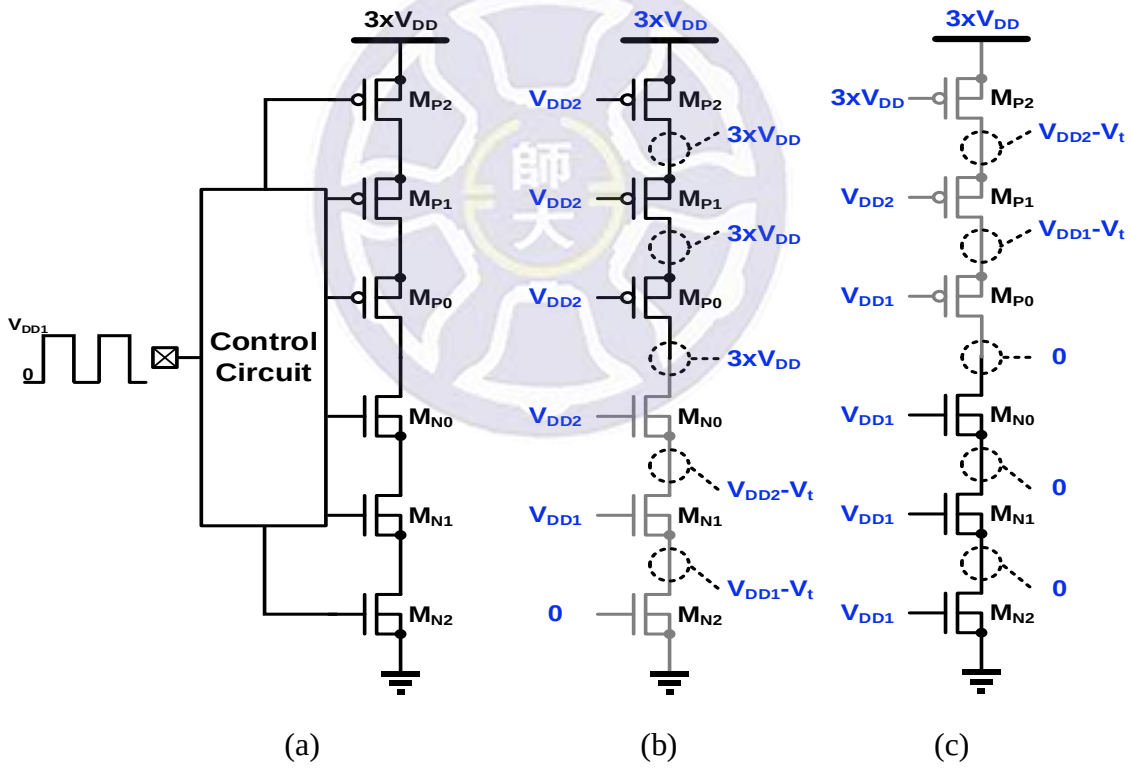


Fig. 3.4. (a) A triply-stacked output driver (b) high-level drive (c) low-level drive.

The stacked-device output driver has been simulated in HSPICE with the 0.18μm CMOS process. Fig. 3.5 ~ 3.7 shows the simulated transient waveforms of stacked-device output driver. As long as the V_{IN} is 0V or 3.3V, the V_{i1a} is inverted instantaneously. The V_{i2}, V_{i2a}, and V_{i2b} swing between 3.3V and 6.6V, the V_{i3a} swing between 6.6V and 9.9V, and the V_{OUT} finally swings between 0V and 9.9V.

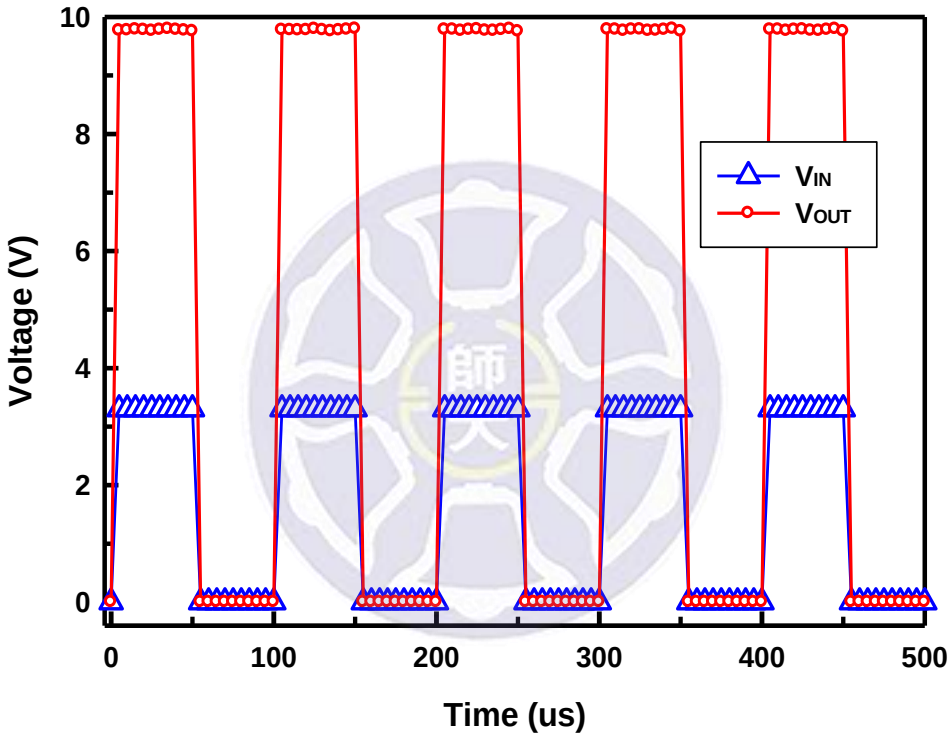


Fig. 3.5. Simulated transient waveforms of high voltage output driver with V_{IN}-V_{OUT}.

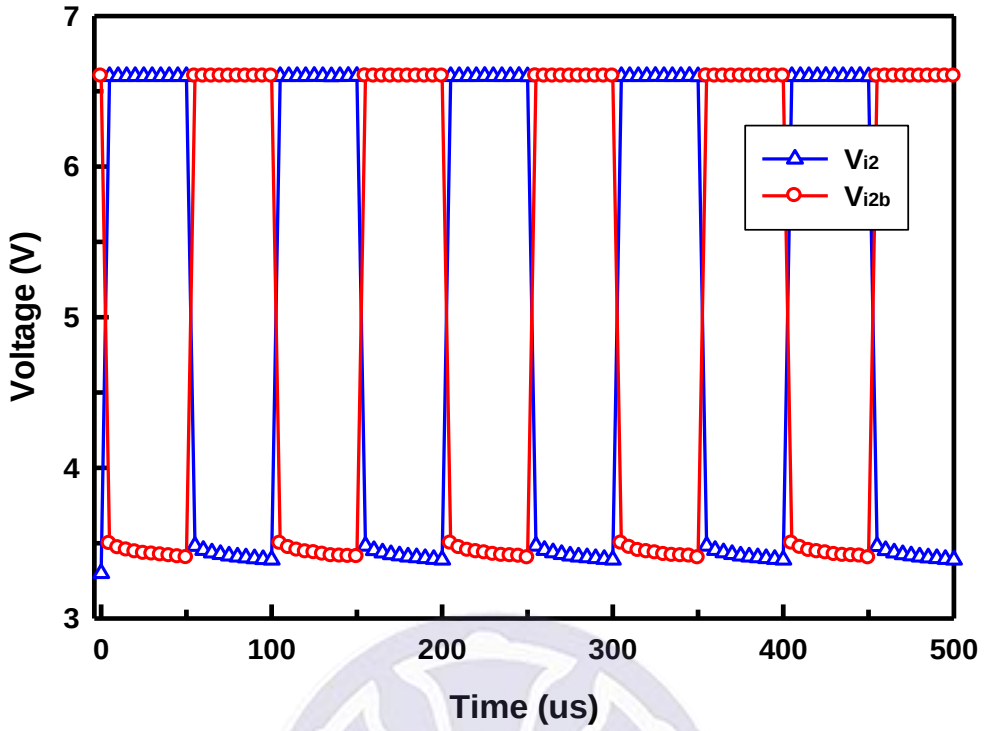


Fig. 3.6. Simulated transient waveforms of high voltage output driver with V_{i2}-V_{i2b}.

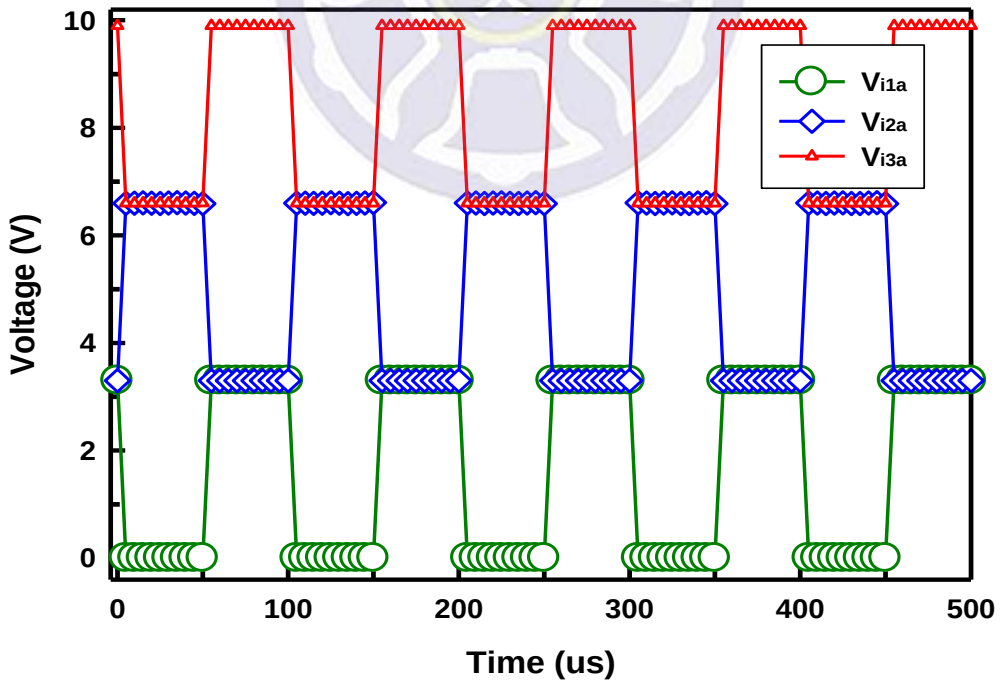


Fig. 3.7. Simulated transient waveforms of high voltage output driver with V_{i1a}-V_{i2a}-V_{i3a}.

To verify the voltage differences across each transistor are lower than 3.63V during all V_{IN} potentials, a ramp voltage from 0V to 3.3V is injected into V_{IN}, and then the voltage of each node is captured. Fig. 3.8 shows the simulated |Vgd|, |Vgs|, and |Vds|, of each transistor, as the V_{IN} is between 0V and 3.3V. For the M_{N2}, each terminal is constrained to swing between 0V and $1xV_{DD}$, as shown in Fig. 3.8(a). For the M_{N1}, its gate potential is kept at $1xV_{DD}$, its source potential is constrained to swing between 0V and $1xV_{DD}$, and its drain potential will swing between 0V and $2xV_{DD}$. Even though, the voltage differences across each terminals of M_{N1} are still lower than 3.63V, as shown in Fig. 3.8(b). For the M_{N0}, its gate potential will swing between $1xV_{DD}$ and $2xV_{DD}$, its source potential will swing between 0V and $2xV_{DD}$, and its drain potential will swing between 0V and $3xV_{DD}$. The simulation results show that the voltage differences across each terminals of M_{N0} are still lower than 3.63V, as shown in Fig. 3.8(c). The operations of M_{P0}~M_{P2} are complementary to those of M_{N0}~M_{N2}, so the similar results can be found, as shown in Figs. 3.8(d) ~ 3.8(f).

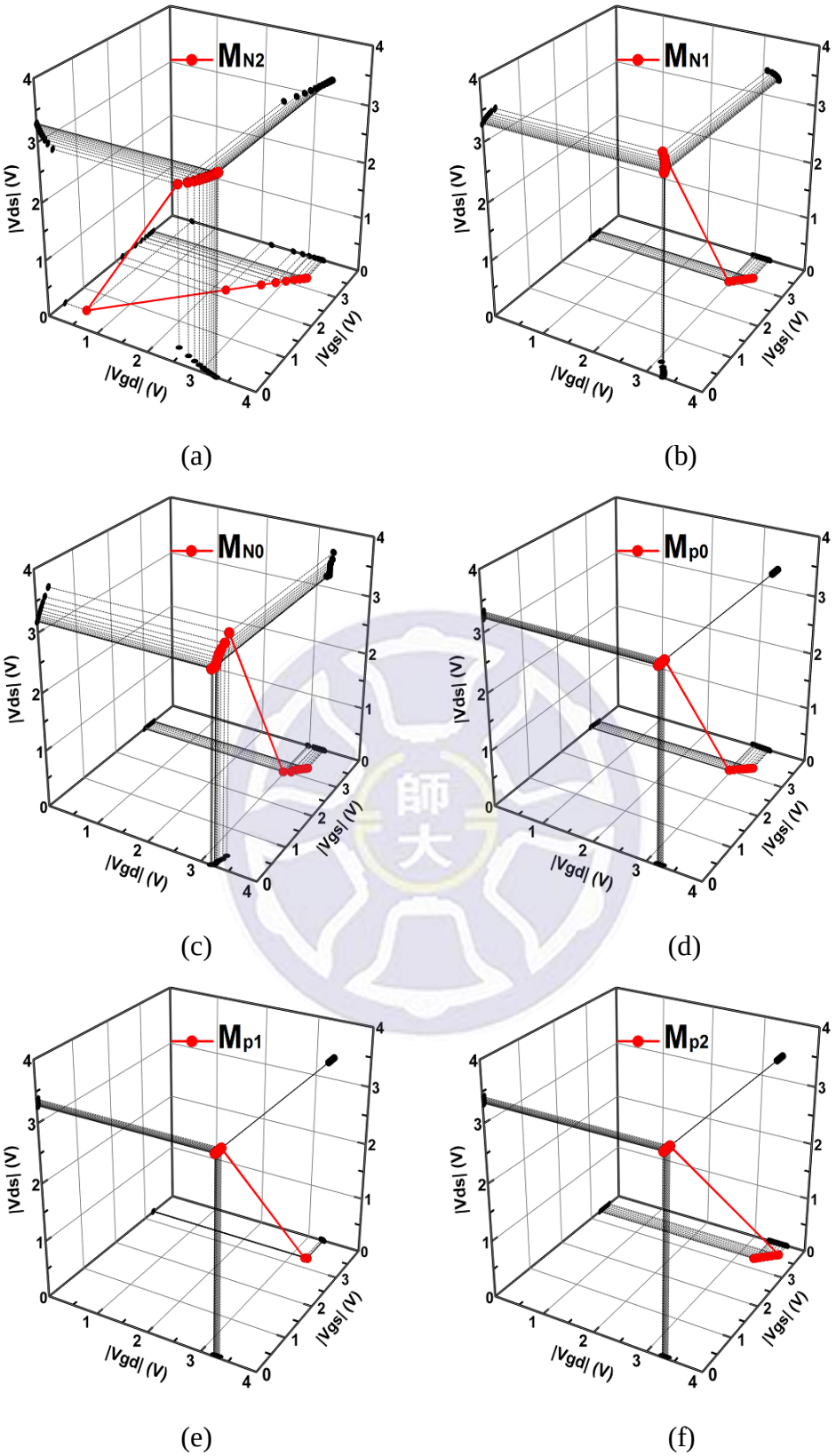


Fig. 3.8. Simulated |Vgd|, |Vgs|, and |Vds|, of transistors in output stage: (a) M_{N2}, (b) M_{N1}, (c) M_{N0}, (d) M_{P0}, (e) M_{P1}, and (f) M_{P2}.

With the proper design of control circuit, the PMOS and NMOS transistors in output stage are well controlled to turn on or off. The simulation results show that the voltage differences across each transistor are 3.63V at most, which meets the design target.

Although the stacked-device output driver with embedded SCR can't be simulated, its transient behaviors should be equal to the output driver without embedded SCR, since the additional P+ region in the proposed design will not affect the operation of drain, gate, source, and body terminals of three NMOS devices during normal operation.

3.3 Proposed ESD Protection Design for Stacked-Device Output Driver

The cross-sectional view of NMOS part in output stage of conventional $3xV_{DD}$-tolerant stacked-device output driver is shown in Fig. 3.9. The N-well and deep N-well regions are used to isolate the P-well region of each stacked NMOS from the common P-substrate. The body-to-drain (P-well/N+) diodes form the ESD current path from GND to Vo. Besides, a parasitic SCR (P-well/Deep N-well/P-well/N+) can also help to discharge the ESD current from GND to V_{OUT}, but its path is too long to effectively discharge the ESD current.

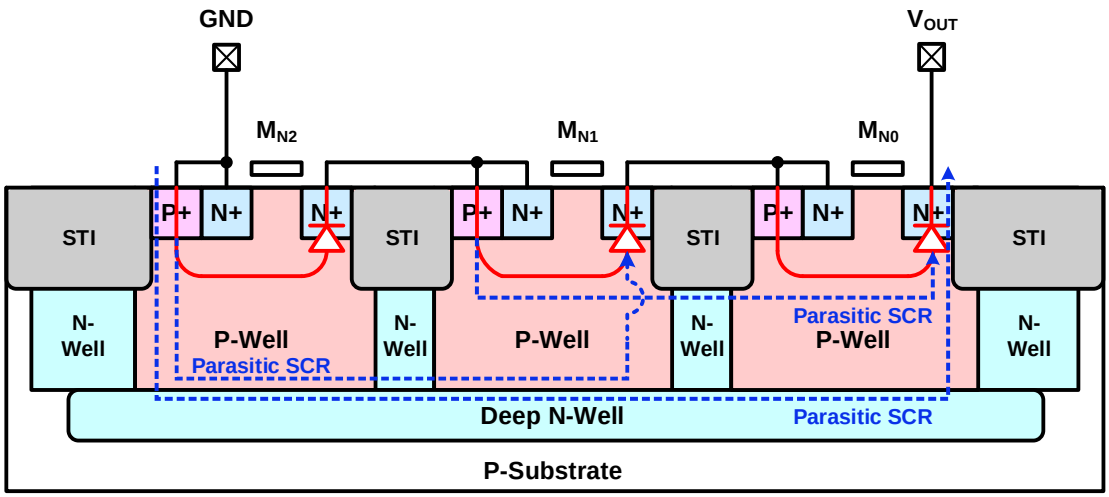


Fig. 3.9. Cross-sectional view of stacked NMOS devices in output stage of conventional 3xV_{DD}-tolerant stacked-device output driver.

To have symmetrical ESD protection ability in PMOS and NMOS parts, a stacked-device output driver with embedded SCR is proposed, as shown in Fig. 3.10. In the proposed design, additional P+ region is added into the N-well region, and then an embedded SCR device is formed from GND to V_{OUT}. Since the existing N-well region is usually large enough to contain the additional P+ region, this design will not increase the layout area. Besides, the SCR device can be safely used without latchup danger in the proposed design, since the anode (GND) potential is always lower than the cathode (V_{OUT}) potential during normal operation, and the SCR device can't keep turning on.

The SCR device has been reported to be useful for ESD protection. The equivalent circuit of the embedded SCR consists of the cross-coupled PNP (P+/N-well/P-well) and NPN (N-well/P-well/N+) BJTs. In the proposed design, the body-to-drain (P-well/N+) diodes play the role of trigger circuit of embedded SCR to enhance the turn-on speed. As ESD stresses from anode (GND) to cathode (V_{OUT}) of the SCR are applied, the diode path will turn on to discharge the initial ESD currents, and then the SCR path will take over to discharge the primary ESD currents. The positive-feedback regenerative

mechanism of PNP and NPN BJTs results in the SCR device becoming highly conductive to make the SCR very robust against ESD stresses.

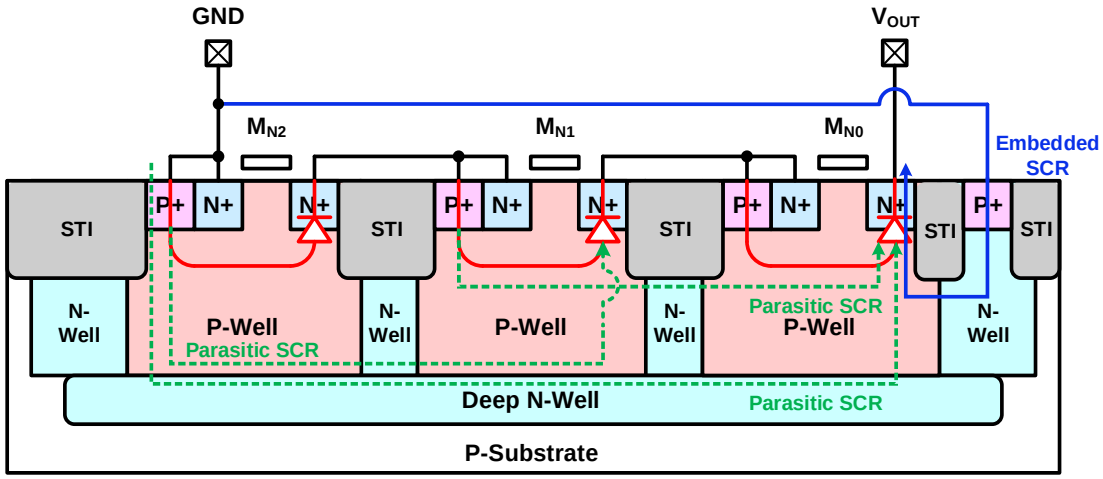


Fig. 3.10. Cross-sectional view of stacked NMOS devices with additional P+ region in output stage of proposed $3\times V_{DD}$-tolerant stacked-device output driver with embedded SCR.

This research designed 2 kinds of high-voltage output driver, contains without ESD protective element of the driver, and the driver in the output stage with embedded SCR. The driver match output stage of different sizes to explore the characteristics of electrostatic discharge protection design. Comparison of three different sizes, are used in the output stage of the driver, in output stage finger to change the number of transistors. In order to investigate the reliability of related problems, this study also designed test circuit as shown in Table 3.1.

Table 3.1.

Design parameters of the test circuits

	Test Circuits	$(W/L)_n$	$(W/L)_p$	Finger width		Total Width	
		M_{N0}~M_{N2}	M_{P0}~M_{P2}	M_{N0}~ M_{N2}	M_{P0}~ M_{P2}	M_{N0}~ M_{N2}	M_{P0}~ M_{P2}
Pure Output Driver	Output Driver_10	10/0.35 um/um	10/0.35 um/um	10 um	10 um	10 um	10 um
	Output Driver_30	30/0.35 um/um	30/0.35 um/um	10 um	10 um	30 um	30 um
	Output Driver_50	50/0.35 um/um	50/0.35 um/um	10 um	10 um	50 um	50 um
Driver with Embedded SCR	Driver + SCR_10_10	10/0.35 um/um	10/0.35 um/um	10 um	10 um	10 um	10 um
	Driver + SCR_30_10	30/0.35 um/um	30/0.35 um/um	10 um	10 um	30 um	30 um
	Driver + SCR_50_10	50/0.35 um/um	50/0.35 um/um	10 um	10 um	50 um	50 um
	Driver + SCR_30_30	30/0.35 um/um	30/0.35 um/um	30 um	30 um	30 um	30 um
	Driver + SCR_50_50	50/0.35 um/um	50/0.35 um/um	50 um	50 um	50 um	50 um

3.4 Experimental Results

To verify the stacked-device output driver in silicon chip, both circuits without and with embedded SCR (pure output driver and driver with embedded SCR) have been fabricated in 0.18μm CMOS process. Each circuit occupies a chip area is less than 250×175μm^2, including 3xV_{DD}, GND, V_{IN}, and V_{OUT} pads without high-voltage-tolerant ESD clamp circuit.

3.4.1 Transient Waveforms

A 9.9V supply voltage is used for $3xV_{DD}$, a 3.3V and 10kHz square wave is applied to V_{IN}, a 100kΩ resistance is loaded to V_{OUT}, and then the V_{OUT} swing is measured, as shown in Fig. 3.11 ~ 3.18. Fig. 3.11 ~ 3.13 shows the measured waveforms of general stacked-device output driver (pure output driver), and Fig. 3.14~ 3.18 shows those of proposed stacked-device output driver with SCR (driver with embedded SCR). As long as the V_{IN} is 0V or 3.3V, the V_{OUT} of both circuits can swing between 0V and ~9.7V.

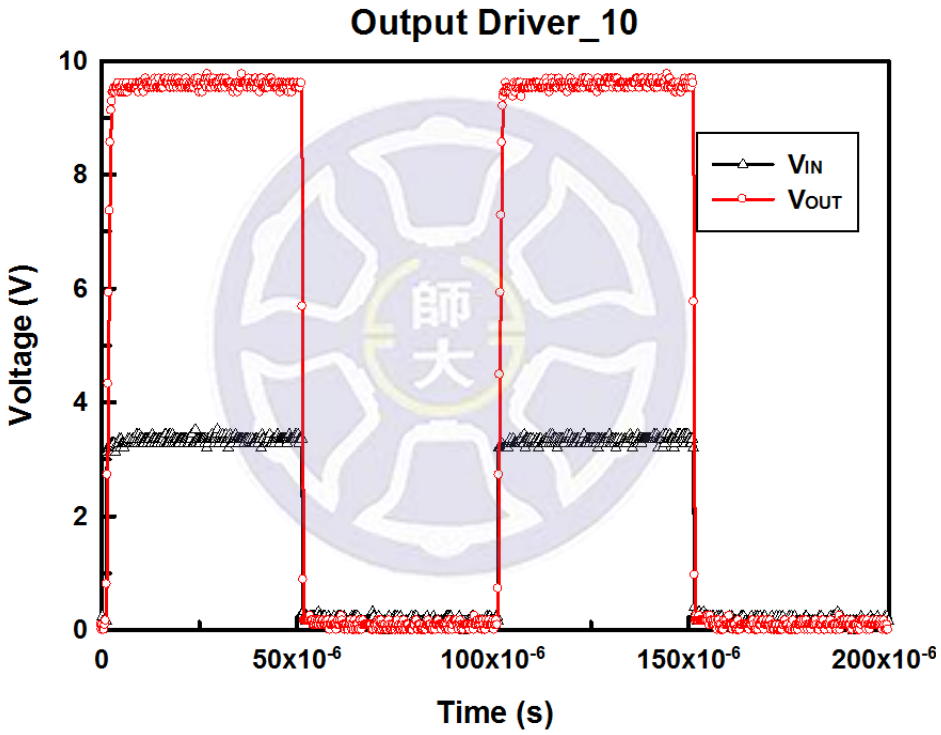


Fig. 3.11. Measured transient waveforms of general $3xV_{DD}$-tolerant stacked-device output driver in Output Driver_10.

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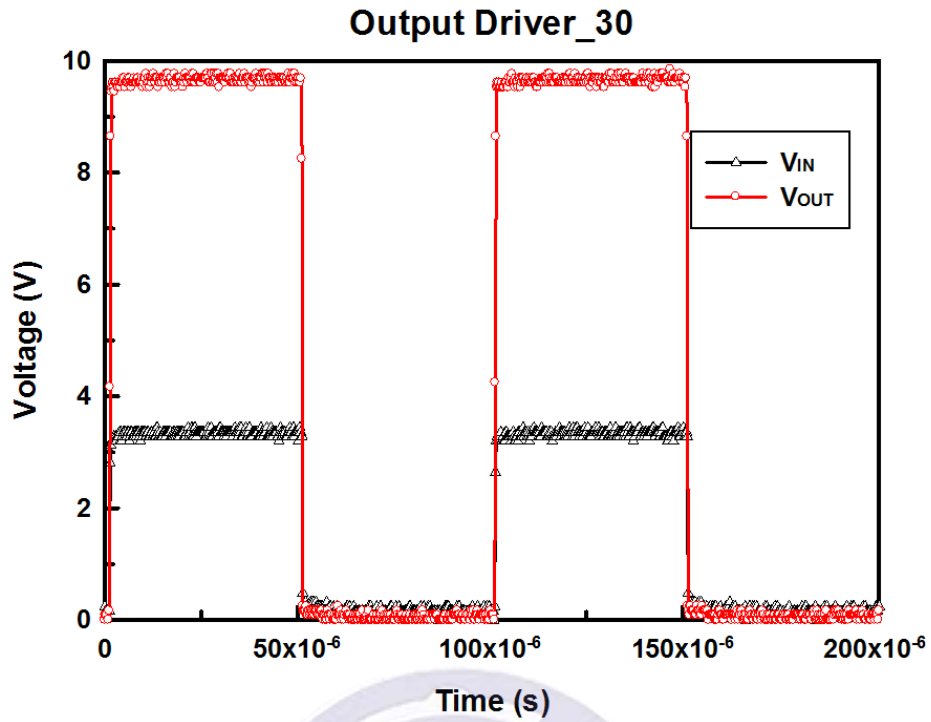

Fig. 3.12. Measured transient waveforms of general 3xV_{DD}-tolerant stacked-device output driver in Output Driver_30.

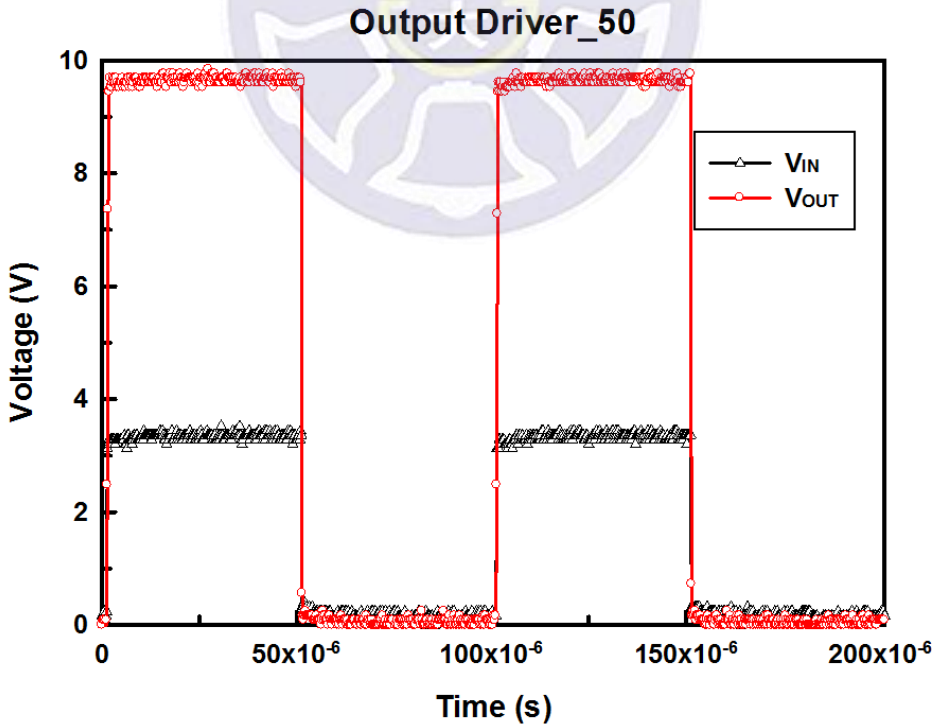

Fig. 3.13. Measured transient waveforms of general 3xV_{DD}-tolerant stacked-device output driver in Output Driver_50.

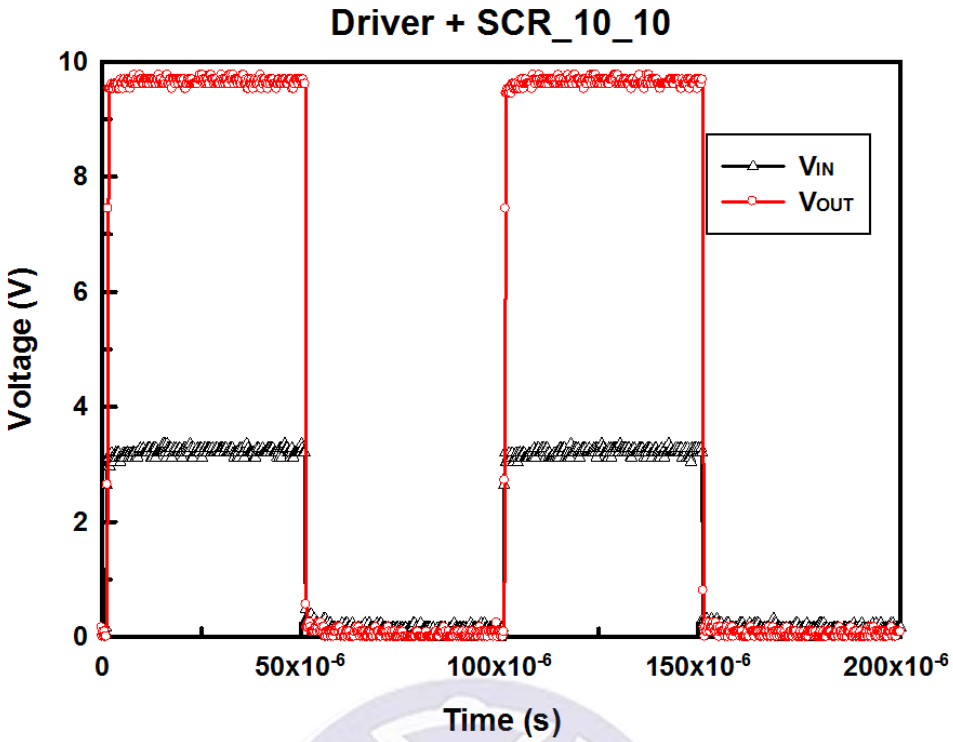

Fig. 3.14. Measured transient waveforms of proposed $3xV_{DD}$-tolerant stacked-device output driver with embedded SCR in Driver + SCR_10_10.

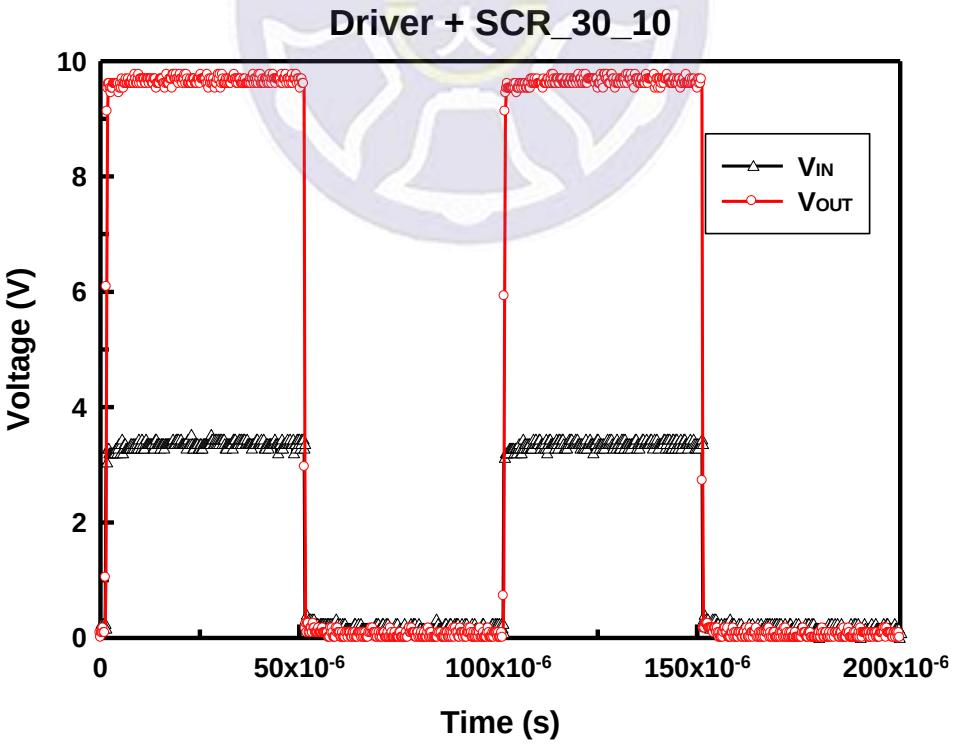

Fig. 3.15. Measured transient waveforms of proposed $3xV_{DD}$-tolerant stacked-device output driver with embedded SCR in Driver + SCR_30_10.

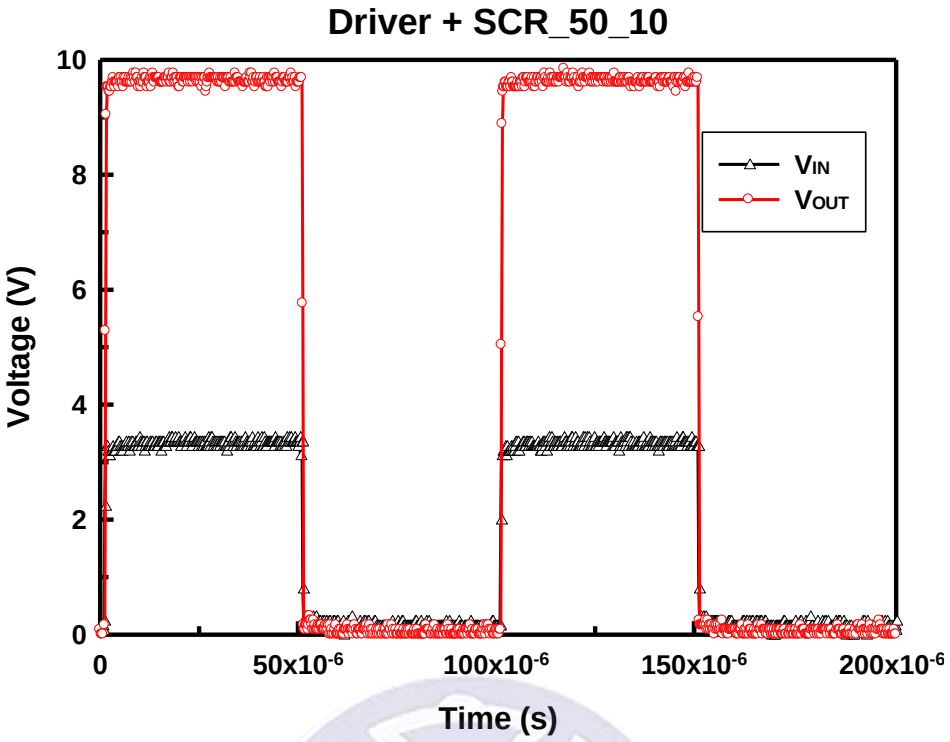

Fig. 3.16. Measured transient waveforms of proposed 3xV_{DD}-tolerant stacked-device output driver with embedded SCR in Driver + SCR_50_10.

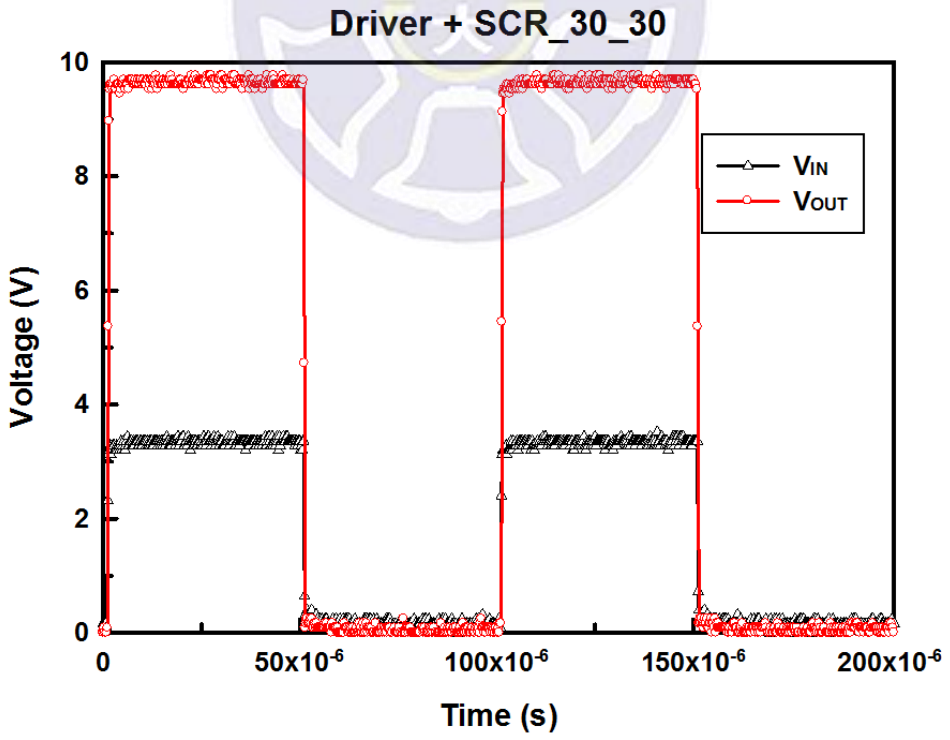

Fig. 3.17. Measured transient waveforms of proposed 3xV_{DD}-tolerant stacked-device output driver with embedded SCR in Driver + SCR_30_30.

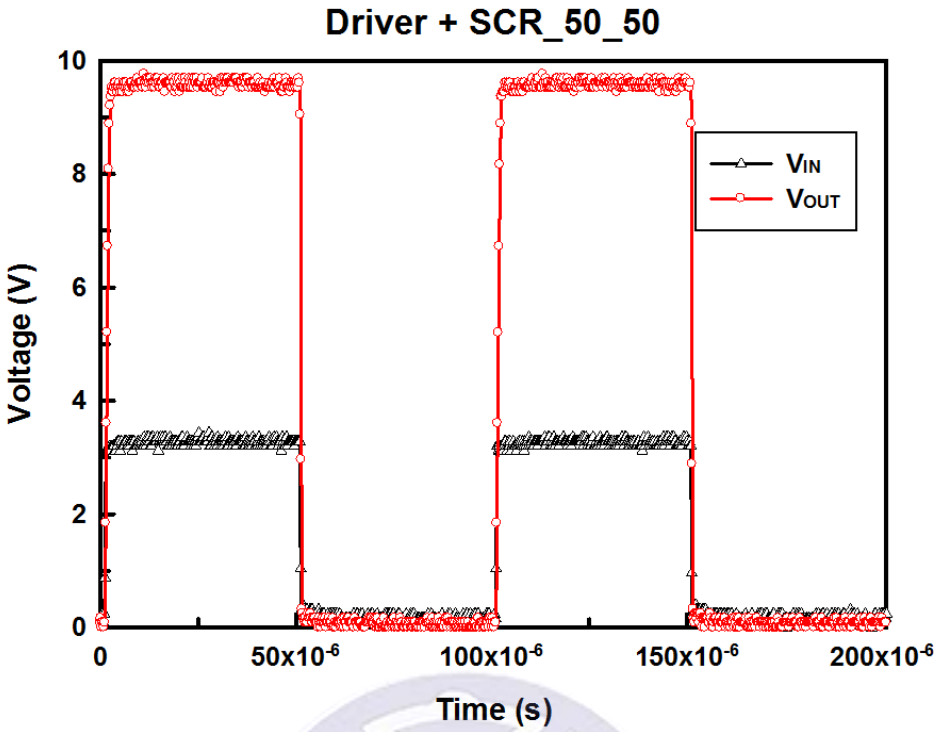

Fig. 3.18. Measured transient waveforms of proposed 3xV_{DD}-tolerant stacked-device output driver with embedded SCR in Driver + SCR_50_50.

3.4.2 ESD Robustness and TLP I-V Characteristics

The HBM ESD robustness of each circuit is evaluated by the HBM tester. The failure criterion is defined as the I-V characteristics shifting over 30 % from its original curve after ESD stressed at every ESD test level. According to the measurement results, the V_{OUT}-to-3xV_{DD} ESD robustness of both circuits are more than 1.25kV. The GND-to-V_{OUT} ESD robustness of general stacked-device output driver (Output Driver_10 and Output Driver_30) are 0.75kV, while that of proposed stacked-device output driver with embedded SCR (Driver + SCR_10_10 and Driver + SCR_30_10) are improved to 1.75kV and 2.25kV, respectively, the GND-to-V_{OUT} ESD robustness of general stacked-device output driver (Output Driver_50) is 1.25kV, while that of proposed stacked-device output driver with embedded SCR is improved to 2.50kV. All these HBM measurement results are listed in Table 3.2.

Table 3.2

HBM ESD robustness of test circuits

	Test Circuits	HBM Level	
		GND-to-V_{OUT}	V_{OUT}–to-3xV_{DD}
Pure Output Driver	Output Driver_10	750V	1250V
	Output Driver_30	750V	1250V
	Output Driver_50	1250V	1500V
Driver with Embedded SCR	Driver + SCR_10_10	1750V	1250V
	Driver + SCR_30_10	2250V	1250V
	Driver + SCR_50_10	2500V	1750V
	Driver + SCR_30_30	4000V	3500V
	Driver + SCR_50_50	4500V	4000V

To investigate the turn-on behavior and the I-V characteristics of the circuits in the domain of HBM ESD event, the transmission-line-pulsing (TLP) system with a 10ns rise time and a 100ns pulse width is used. The current-handling ability, i.e. the secondary breakdown current (I_{t2}), of test circuit can be obtained from the TLP-measured I-V curves. The TLP-measured I-V curves of test circuits are shown in Fig. 3.19 ~ 3.28. As measuring from V_{OUT} to 3xV_{DD}, the test circuits of Output Driver_10 and Driver + SCR_10_10 have almost the same TLP I-V characteristics, and the TLP-measured It2 are ~0.85A, the test circuits of Output Driver_30 and Driver + SCR_30_10 have almost the same TLP I-V characteristics, and the TLP-measured I_{t2} are ~1.03A, the test circuits of Output Driver_50 and Driver + SCR_50_10 have almost the same TLP I-V characteristics, and the TLP-measured I_{t2} are ~1.20A, the test circuits

of Driver + SCR_30_30 and Driver + SCR_50_50 can achieve the TLP-measured (I_{t2}) of 2.16A and 3.29A, respectively. As measuring from GND to V_{OUT}, the embedded SCR in the proposed design can be triggered lower than ~2.5V, and then be latched to ~1.5V. The GND-to-V_{OUT} I_{t2} of general stacked-device output driver (Output Driver_10, Output Driver_30, and Output Driver_50) are 0.47A, 0.77A, and 1.02A, respectively, while that of proposed stacked-device output driver with embedded SCR (Driver + SCR_10_10, Driver + SCR_30_10, and Driver + SCR_50_10) are improved to 0.81A, 0.97A, and 1.26A, respectively, the test circuits of Driver + SCR_30_30, and Driver + SCR_50_50 can achieve the TLP-measured (I_{t2}) of 2.29A and 3.51A, respectively.

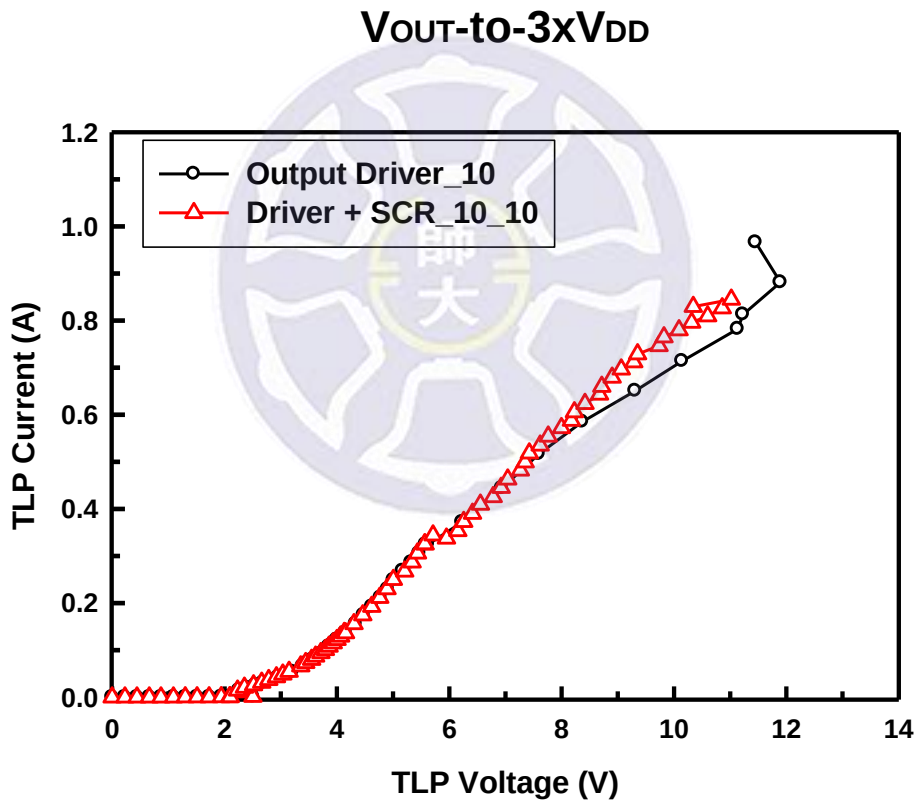

Fig. 3.19. Measured TLP I-V curves of Output Driver_10 and Driver + SCR_10_10, as zapping from V_{OUT} to $3xV_{DD}$.

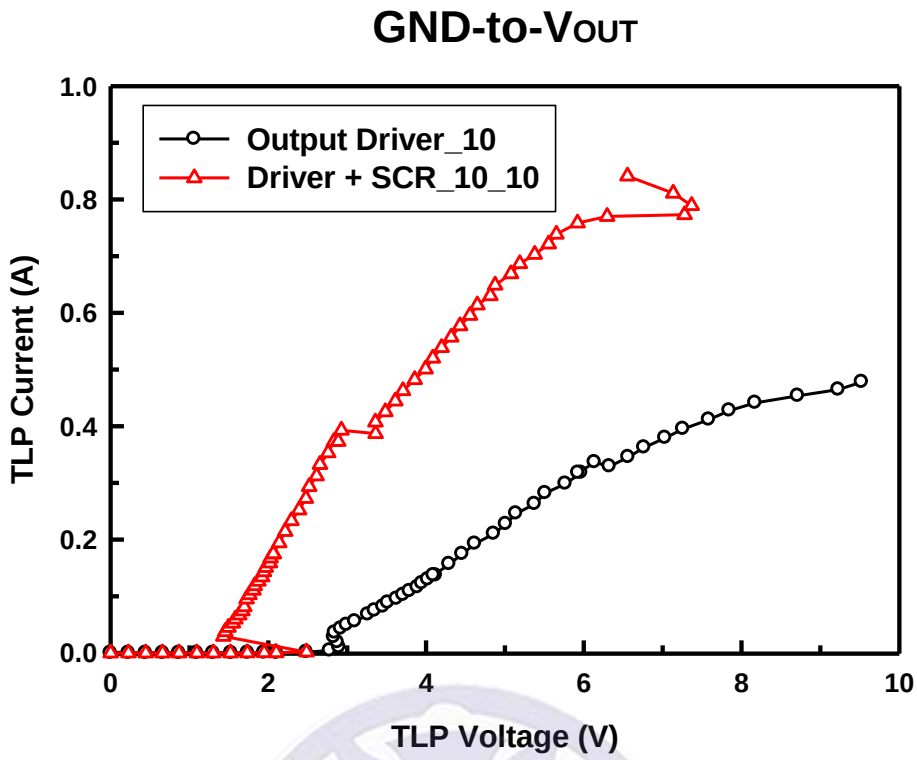

Fig. 3.20. Measured TLP I-V curves of Output Driver_10 and Driver + SCR_10_10, as zapping from GND to V_{OUT}.

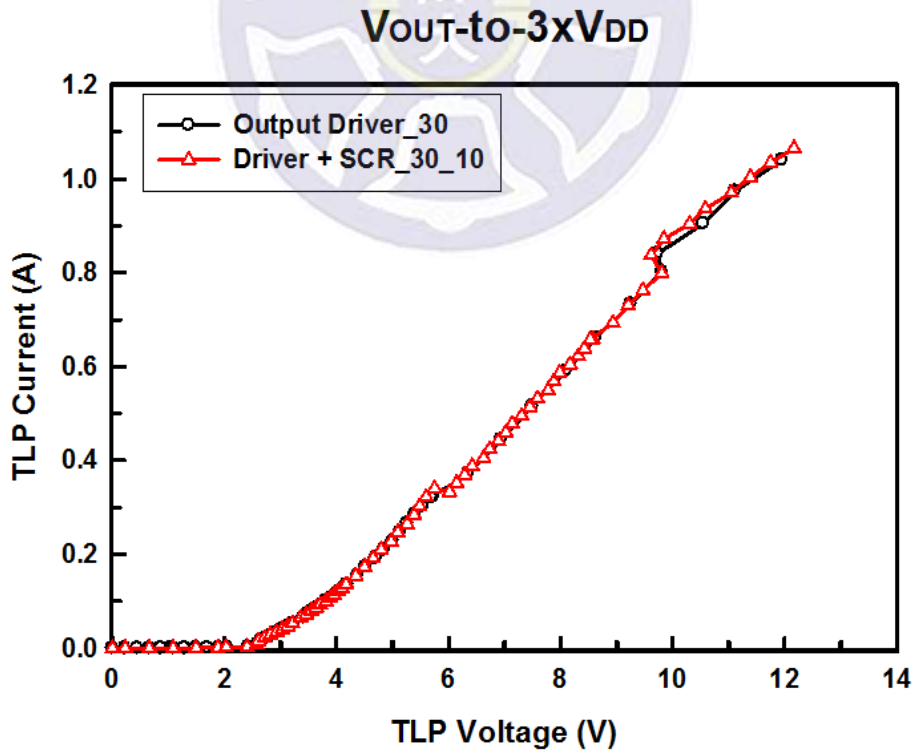

Fig. 3.21. Measured TLP I-V curves of Output Driver_30 and Driver + SCR_30_10, as zapping from V_{OUT} to $3xV_{DD}$.

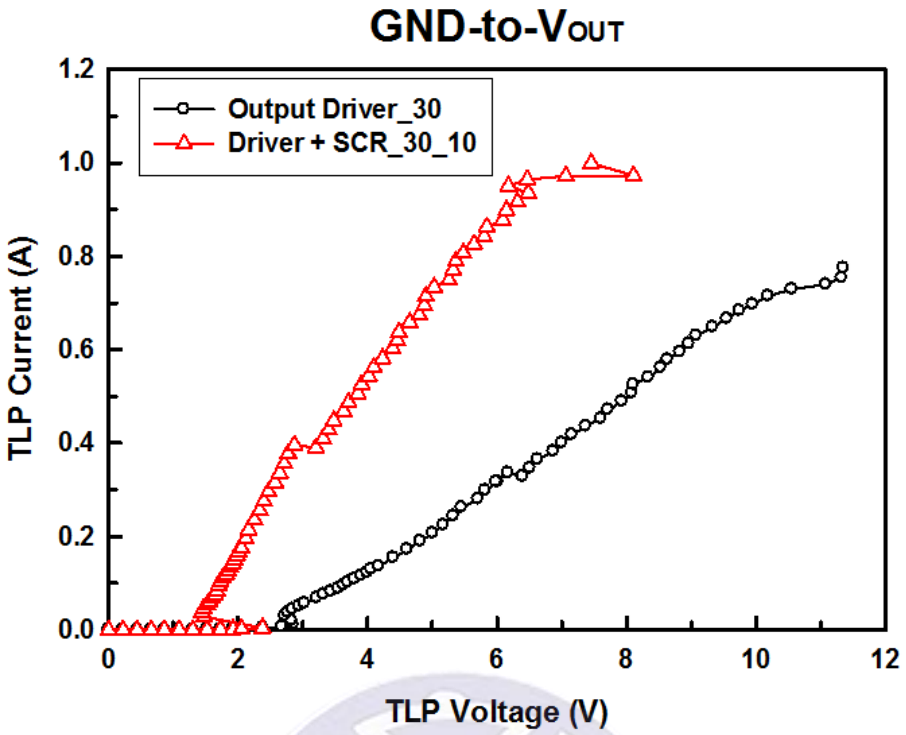

Fig. 3.22. Measured TLP I-V curves of Output Driver_30 and Driver + SCR_30_10, as zapping from GND to V_{OUT}.

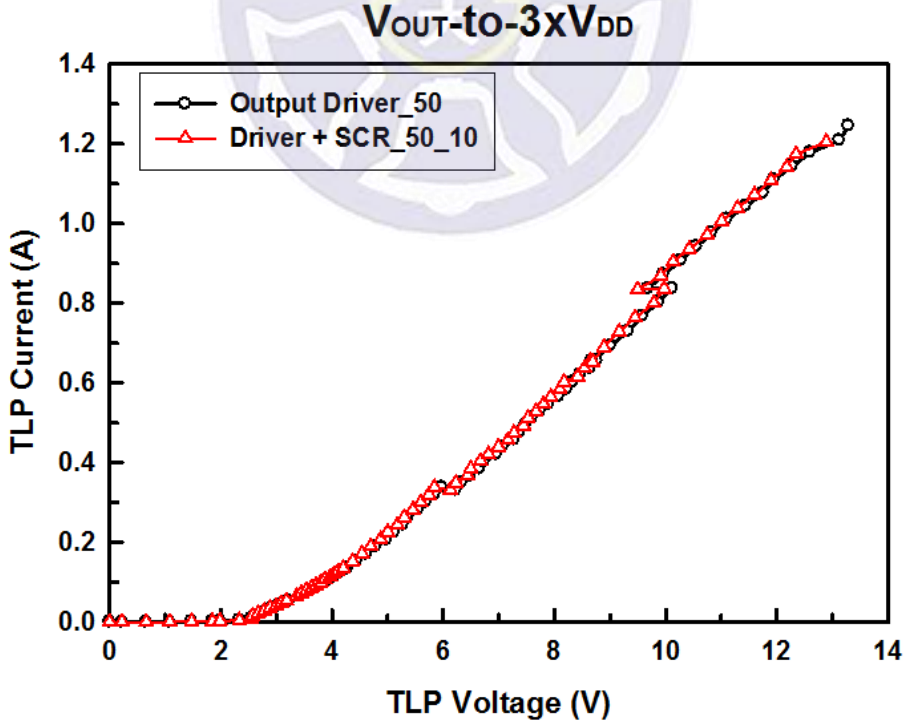

Fig. 3.23. Measured TLP I-V curves of Output Driver_50 and Driver + SCR_50_10, as zapping from V_{OUT} to $3xV_{DD}$.

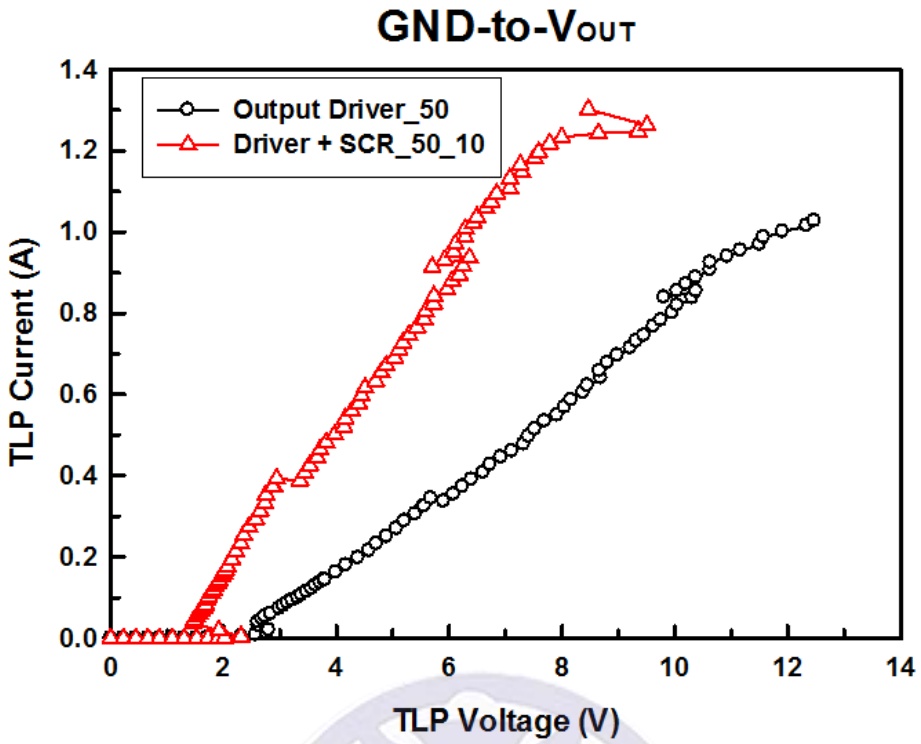

Fig. 3.24. Measured TLP I-V curves of Output Driver_50 and Driver + SCR_50_10, as zapping from GND to V_{OUT}.

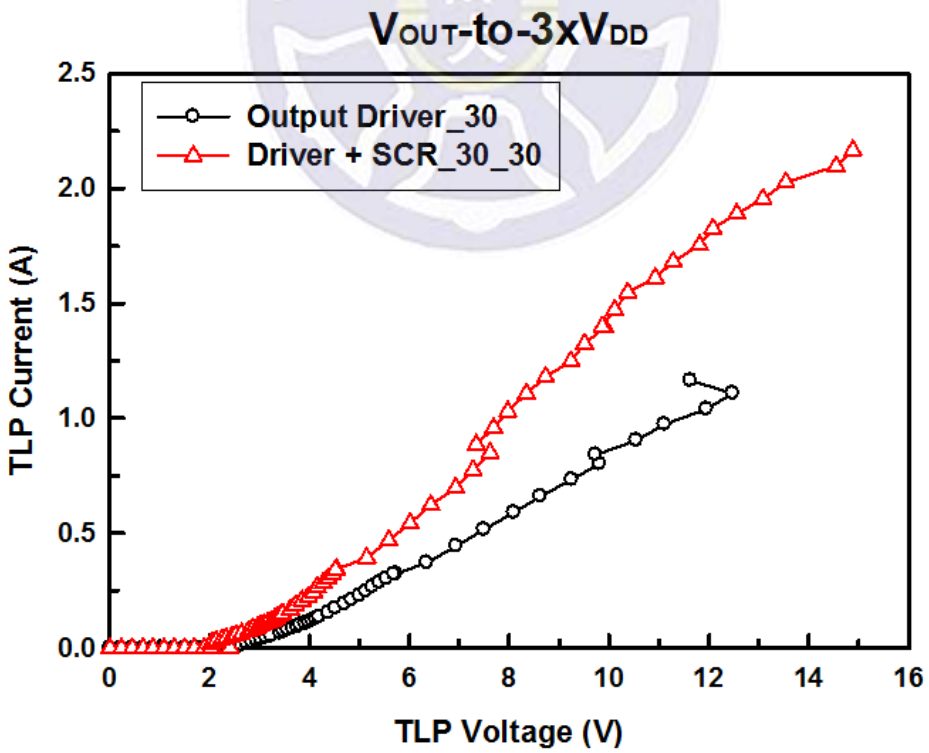

Fig. 3.25. Measured TLP I-V curves of Output Driver_30 and Driver + SCR_30_30, as zapping from V_{OUT} to $3xV_{DD}$.

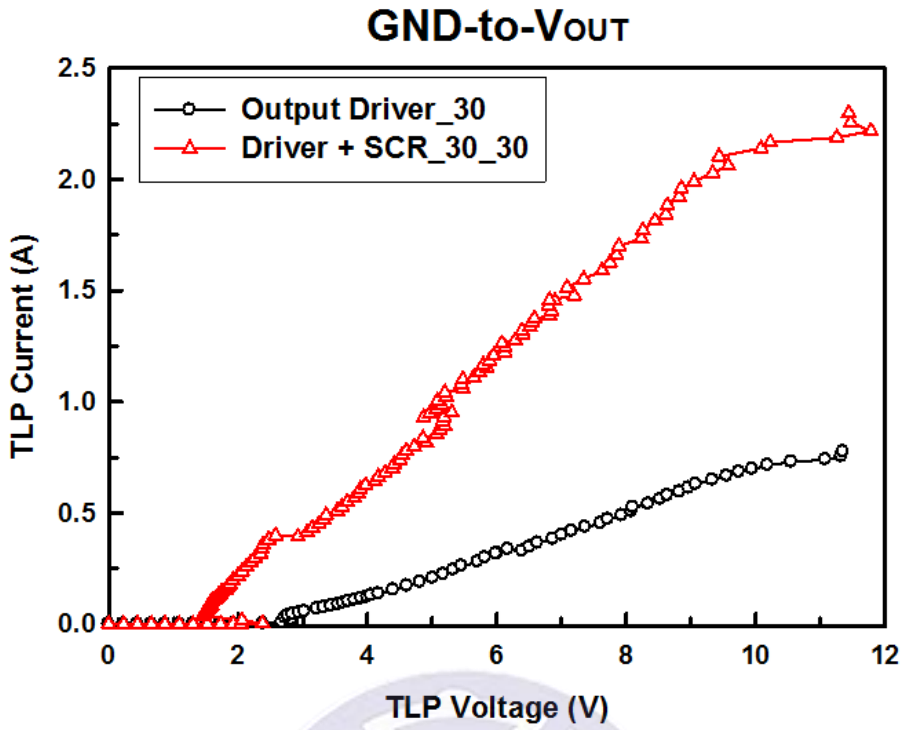

Fig. 3.26. Measured TLP I-V curves of Output Driver_30 and Driver + SCR_30_30, as zapping from GND to V_{OUT}.

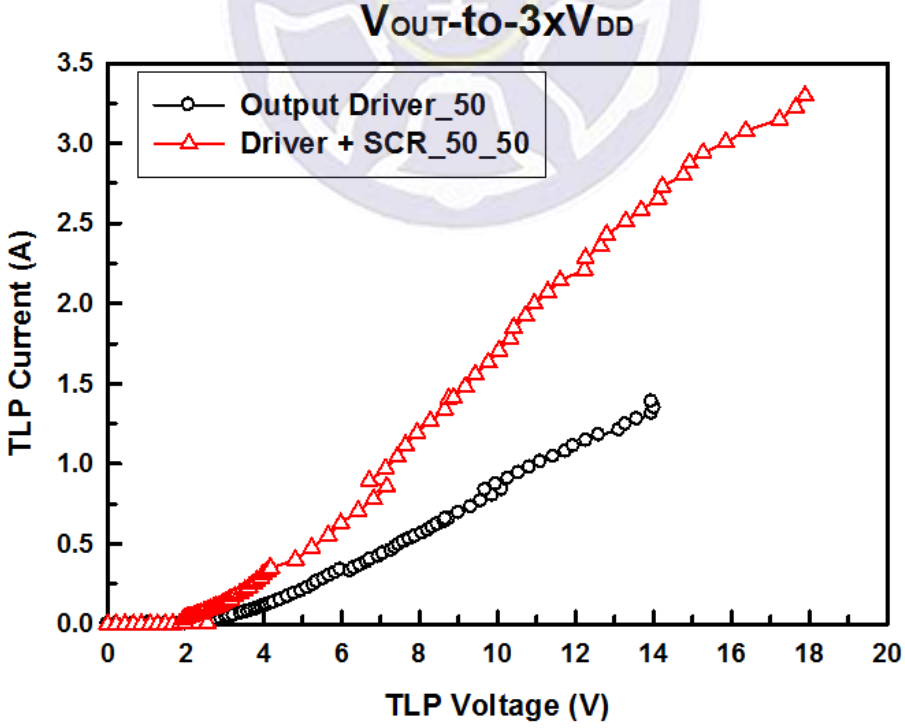

Fig. 3.27. Measured TLP I-V curves of Output Driver_50 and Driver + SCR_50_50, as zapping from V_{OUT} to $3xV_{DD}$.

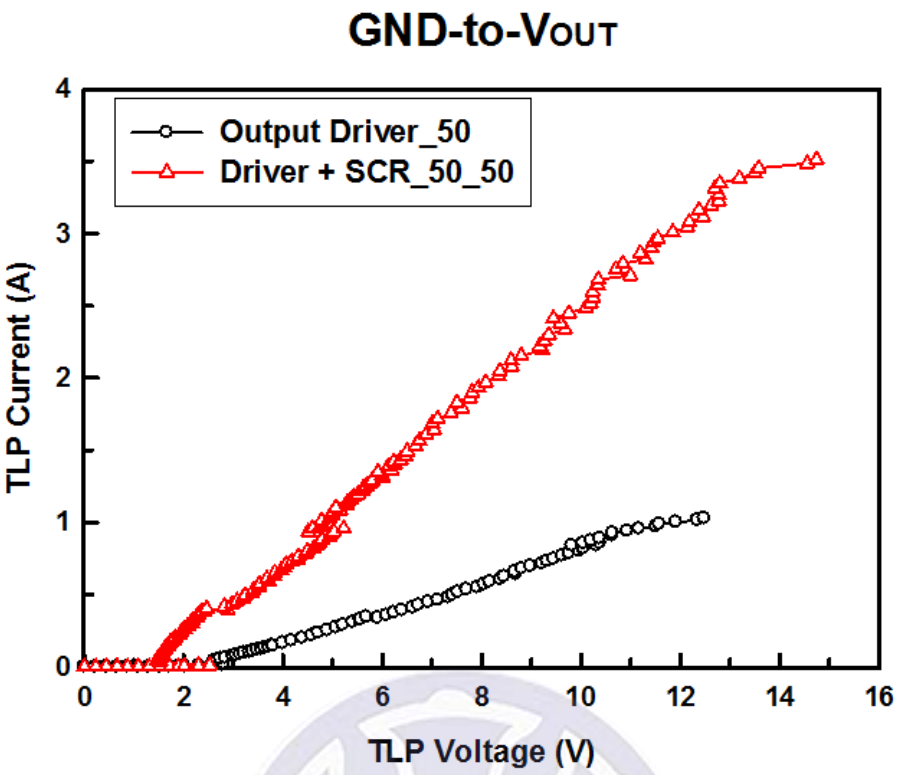

Fig. 3.28. Measured TLP I-V curves of Output Driver_50 and Driver + SCR_50_50, as zapping from GND to V_{OUT}.

In order to investigate the reliability of driver and ESD protection device, using 3 different dimensions in the output stage to collocation the different size with embedded SCR. TLP measurement results as shown in Fig. 3.29.

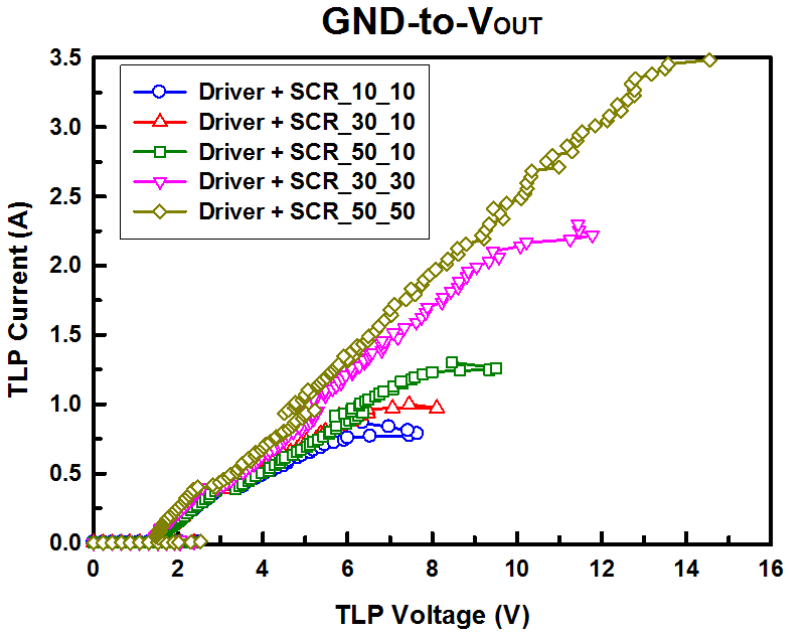

Fig. 3.29. Measured TLP I-V curves, as zapping from GND to V_{OUT} of driver with embedded SCR.

As measuring from V_{OUT} to GND, the test circuits of Output Driver_10, Output Driver_30, and Output Driver_50 can achieve the TLP-measured I_{t2} of 0.32A, 0.28A, and 0.33A, respectively as shown in Fig.3.30.

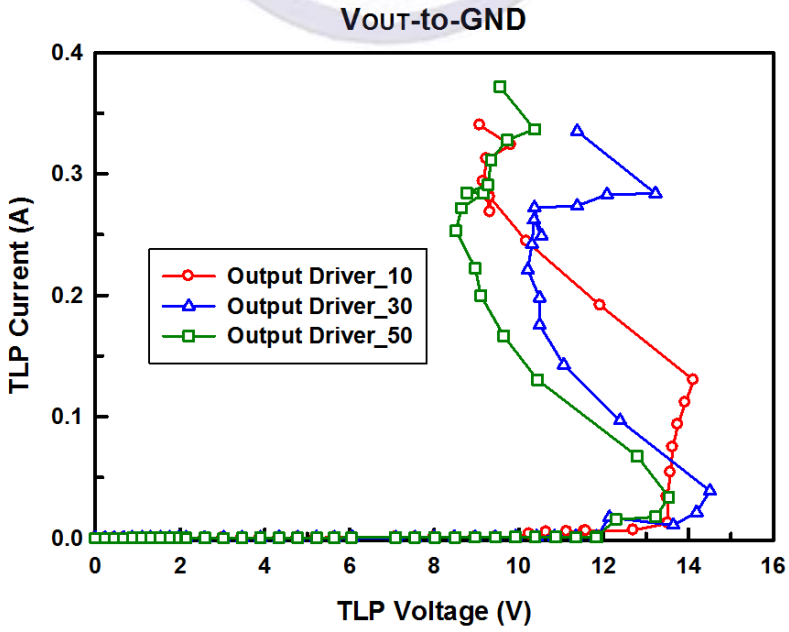

Fig. 3.30. Measured TLP I-V curves, as zapping from V_{OUT} to GND.

As measuring from 3xVDD to VOUT, the test circuits of Output Driver_10, Output Driver_30, and Output Driver_50 can achieve the TLP-measured I_{t2} of 0.34A, 0.39A, and 0.39A, respectively as shown in Fig.3.31.

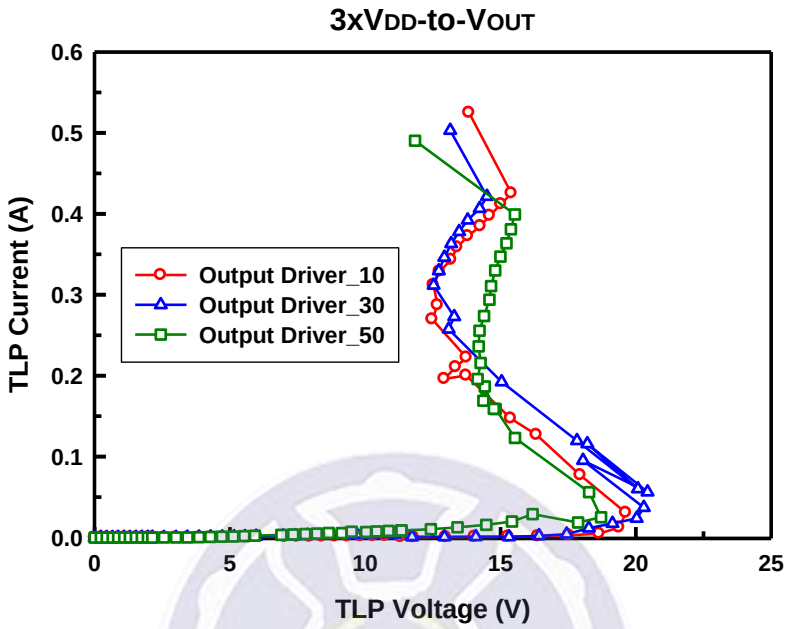

Fig. 3.31. Measured TLP I-V curves, as zapping from 3xVDD to VOUT.

From GND to VOUT, embedded SCR varies with the size of the driver, this design consideration can be more effectively utilized in the layout area. All these TLP measurement results are also listed in Table 3.3 and Table 3.4.

Table 3.3

TLP measurement results, as zapping from GND-to-V_{OUT} and V_{OUT}-to-3xV_{DD}

	Test Circuits	TLP					
		GND-to-V_{OUT}			V_{OUT}–to-3xV_{DD}		
		V_{t1} (V)	V_h (V)	I_{t2} (A)	V_{t1} (V)	V_h (V)	I_{t2} (A)
Pure Output Driver	Output Driver_10	2.89	2.83	0.47	2.50	2.25	0.85
	Output Driver_30	2.85	2.72	0.77	2.64	2.64	1.03
	Output Driver_50	2.77	2.61	1.02	2.61	2.61	1.20
Driver with Embedded SCR	Driver + SCR_10_10	2.48	1.42	0.81	2.50	2.23	0.84
	Driver + SCR_30_10	2.37	1.47	0.97	2.60	2.60	1.06
	Driver + SCR_50_10	2.31	1.46	1.26	2.57	2.57	1.24
	Driver + SCR_30_30	2.37	1.46	2.29	2.40	2.02	2.16
	Driver + SCR_50_50	2.52	1.53	3.51	2.55	1.94	3.29

Table 3.4

TLP measurement results, as zapping from V_{OUT}-to-GND and 3xV_{DD}-to-V_{OUT}

	Test Circuits	TLP					
		V_{OUT}-to-GND			3xV_{DD}–to-V_{OUT}		
		V_{t1} (V)	V_h (V)	I_{t2} (A)	V_{t1} (V)	V_h (V)	I_{t2} (A)
Pure Output Driver	Output Driver_10	13.51	13.51	0.32	19.38	19.38	0.34
	Output Driver_30	13.64	13.64	0.28	18.26	18.26	0.42
	Output Driver_50	13.53	13.53	0.33	18.71	18.71	0.42

3.4.3 Reliability of Novel High Voltage Output Driver

Measure swing voltage of novel high voltage output driver (Output Driver_10 and Driver + SCR_10_10) for one month, as shown in Fig. 3.32. The swing voltage of novel high voltage output driver on the 30th day still can maintain about ~9.6V.

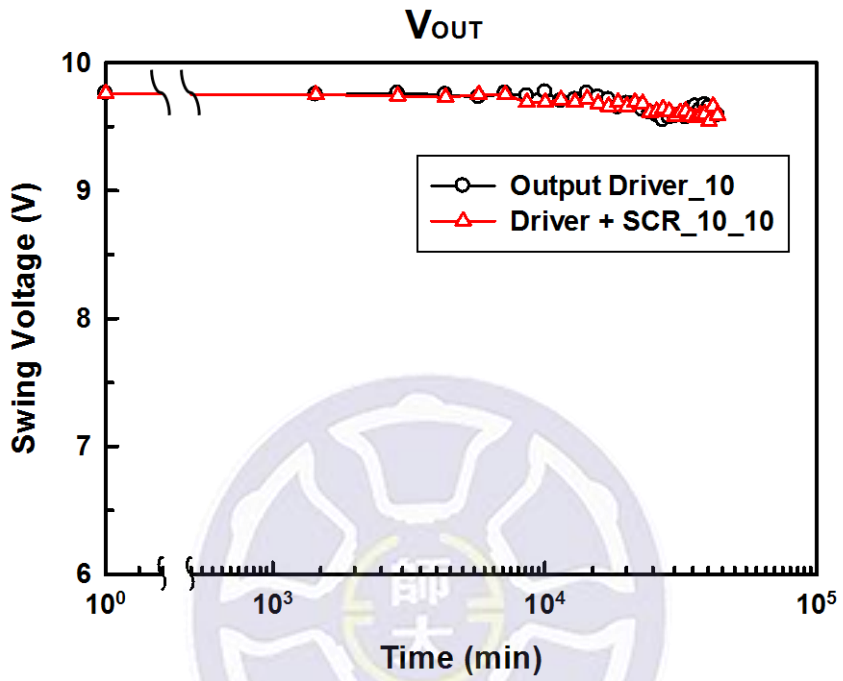

Fig. 3.32. Long-term test of high voltage output driver.

3.4.4 Comparison of High Voltage Output Drivers

Table 3.5 show the document comparison of high voltage output driver, also using stacked MOS to achieve the purpose of the output swing voltage by n x V_{DD}, and without the use of any additional wafer production technology. The proposed novel high voltage output driver can be a good solution for ESD protection.

Table 3.5

Comparison of high voltage output drivers

Parameter / Spec.	Technology	Operated Supply Voltage	Output Swing	HBM ESD Robustness	
				GND-to-V_{OUT}	V_{OUT}-to-3xV_{DD}
References [42]	0.25um CMOS	2.5V	6.4V	N/A	N/A
References [45]	0.35um CMOS	5V	10V	N/A	N/A
References [46]	65nm CMOS	2.5V	*7.5V	N/A	N/A
Driver + SCR_10_10	0.18um CMOS	3.3V	9.7V	1750V	1250V
Driver + SCR_30_10	0.18um CMOS	3.3V	9.7V	2250V	1250V
Driver + SCR_50_10	0.18um CMOS	3.3V	9.7V	2500V	1750V
Driver + SCR_30_30	0.18um CMOS	3.3V	9.7V	4000V	3500V
Driver + SCR_50_50	0.18um CMOS	3.3V	9.7V	4500V	4000V

*** Simulation results**

3.5 Summary

The proposed stacked-device output driver with embedded SCR has been developed for on-chip ESD protection in high-voltage-tolerant output stage where the signal swing may be as high as n x V_{DD}. The 3xV_{DD}-tolerant stacked-device output driver with embedded SCR has been verified in silicon chip. Without using any additional ESD protection device and layout area, the proposed design has the symmetrical ESD protection ability in GND-to-V_{OUT} and V_{OUT}-to-3xV_{DD} paths. Besides, the transient behaviors of the proposed design during normal operation are not degraded. Therefore, the proposed design can be used to improve the ESD robustness of stacked-device output driver.

Chapter 4

Conclusions and Future Works

4.1 Conclusions

This Chapter summarizes the main results and contributions of this study. Future works of the embedded silicon-controlled rectifier for ESD protection design in CMOS process are also provided in the chapter. In this study, a kind of novel ESD protection device has been developed in nanoscale CMOS technology for output stage ESD protection design. Each of the test devices and high voltage output driver has been successfully verified in the test chip.

In Chapter 2, to protect the biomedical integrated circuits in CMOS technologies from ESD damage, a DDSCR device was presented in this work. Verified in silicon chip, experimental results show that the DDSCR has the advantages of high ESD robustness and low parasitic capacitance. The DDSCR was suitable for ESD protection in biomedical integrated circuits.

In Chapter 3, a novel design of stacked-device output driver with embedded SCR is proposed to improve the ESD robustness. A $3xV_{DD}$-tolerant stacked-device output driver with embedded SCR is demonstrated in a 0.18um 3.3V CMOS process. Verified in silicon chip, the proposed design can deliver the $3xV_{DD}$ output voltage. Besides, the ESD robustness can be improved without using any additional ESD protection device and layout area. The proposed design can be further used for n x V_{DD}-tolerant stacked-device output driver to improve its ESD robustness.

4.2 Future Works

Although there have been significant improvements in on-chip ESD protection circuit robustness, there are still several unresolved issues that should be investigated. According to the results of measurement, the proposed design has the symmetrical ESD protection ability in GND-to-V_{OUT} and V_{OUT}-to-3xV_{DD} paths, but 3xV_{DD}-to-GND and GND-to-3xV_{DD} paths is relatively poor. In order to provide a complete ESD protection ability, additional high-voltage-tolerant ESD clamp can provide ESD discharge path, the ESD currents can be discharged from 3xV_{DD} to GND and GND to 3xV_{DD}.

Finally ESD protection design can provide the corresponding ESD current paths during all kinds of ESD events at V_{OUT} pad, as shown in Fig. 4.1.

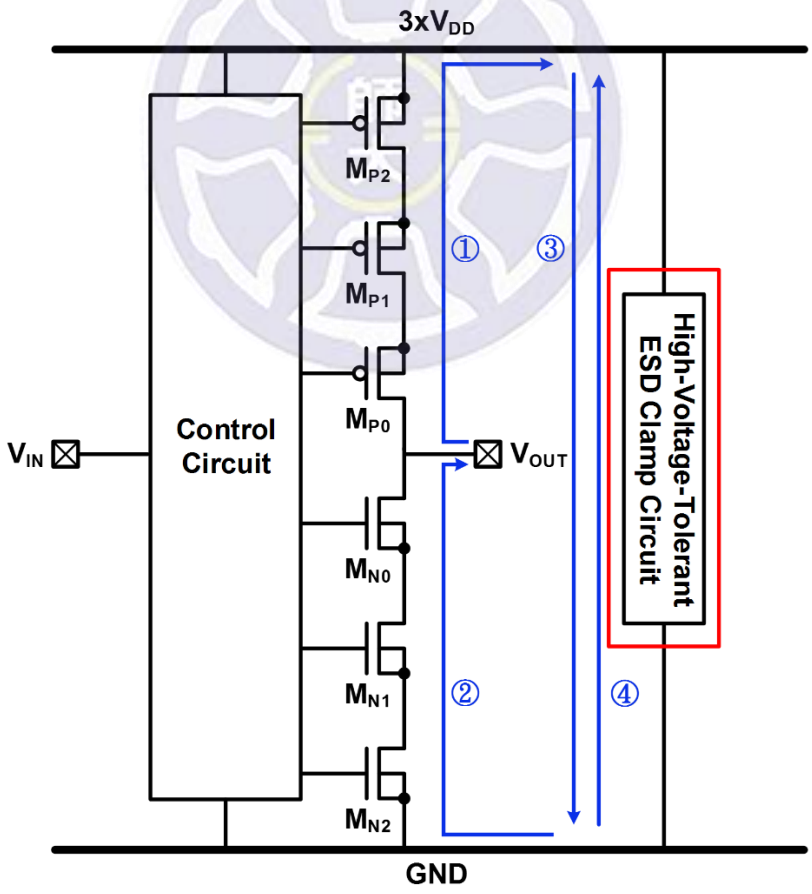

Fig. 4.1. 3xV_{DD}-tolerant stacked-device output driver with high-voltage-tolerant ESD clamp circuit.

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Publication List

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