國立臺灣師範大學電機工程學系

碩士論文

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應用於 K/Ka 頻段積體電路之靜電放電防護設計

On-Chip ESD Protection Design for K/Ka-Band Applications

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摘　　要

本論文設計之電感嵌入矽控整流器的靜電放電防護元件可在共振的頻率之下使電路的小訊號增益損耗降低，只要選擇正確的電感感值便可以達成目標。此外，矽控整流器能在最小的面積下提供最高的靜電放電耐受度，達成較佳的電路靜電放電防護能力。

為了驗證靜電放電防護元件在實際電路上的效能，本論文同時設計了一個低雜訊放大器電路，並且裝備本論文所提出之電感嵌入矽控整流器的靜電放電防護元件，在實驗結果比較中，本論文所提出的設計並不會降低電路的小訊號增益。

本論文中的所有電路皆使用 0.18um CMOS 製程實現。透過實驗分析比較結果，本論文所提出的設計確實能夠達成良好的靜電放電防護能力，使電路能夠承受 4kV 的人體放電模式之靜電放電測試，證明電路能夠有效地被該元件保護。

關鍵字：靜電放電耐受度、電感、矽控整流器

On-Chip ESD Protection Design for K/Ka-Band Applications

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All ABSTRACT

An inductor-assisted silicon-controlled rectifier (LASCR) electrostatic discharge (ESD) protection device was designed in this study. The signal loss under the resonant frequency can be reduced by selecting the appropriate inductor in the LASCR. Furthermore, silicon-controlled rectifier has good ESD robustness and small layout area, and let circuit achieve good ESD protection ability.

In order to verify the protection ability of ESD protection device on the radio frequency (RF) circuit, a low-noise amplifier (LNA) circuit has been fabricated in this study, which equipped with LASCR ESD protection device. In the experimental results, the proposed design did not degrade the small-signal gain of the LNA circuit.

All devices and circuits in this study are fabricated in 0.18um CMOS process. Through analysis and comparison of the experimental results, the proposed design can achieve a good ESD protection ability. In the experimental

results, the proposed design can bear 4kV HBM test without degrade the small-signal gain of the circuit. This proves that the circuit can be effectively protected by the LASCR.

Keywords : electrostatic discharge, inductor, silicon-controlled rectifier.

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榮塋 謹誌於

中華民國一零四年七月

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Chapter 1

Introduction

1.1 Motivation

In recent decade, developments of the wireless technologies are rapid and continued. People already have more than one wireless communication device such as smart phones or tablet PC. Therefore, high quality and low cost processes is necessary. That's why RF ICs have been widely fabricated in CMOS processes.

All CMOS ICs must meet the reliability specifications during mass production. Electrostatic discharge (ESD), which was one of the most important reliability issues and must been taken into consideration. All integrated circuits must be equipped with ESD protection device. As IC technology continuously scales down, thinner gate oxide cause ESD problem getting worse and must be carefully considered. Basic ESD protection circuit consists of a pair of diodes which beside I/O pads and a power-rail ESD clamp circuit. It can provide whole-chip ESD protection. However, this design also has some drawback such as parasitic capacitance and would degrade the RF performance of the circuit.

ESD protection devices are generally equipped with the circuits which might be stressed by ESD. Typically, low-noise amplifier (LNA) is the input interface of the RF ICs. Therefore, it might easily stressed by the ESD. Thus, the LNA is necessary to equipped ESD protection device.

The matching network is very important for LNA. Although the general ESD protection devices such as diodes can provide good protection ability, but the large parasitic capacitances would cause the circuit degrade. Therefore, to

meet a good ESD protection ability without degrade the performance of the circuit is a great challenge.

Silicon-controlled rectifier (SCR) is a useful ESD protection device due to some advantages such as high ESD robustness and small layout area. This makes SCR become a highly regarded device in the recent years, but it also has some drawback such as high turn-on voltage. Therefore, to reducing the turn-on voltage is the main study of SCR. Diode strings is a good device which can reduce the turn-on voltage, but it also has the large parasitic capacitance for the RF circuit. In this study, an inductor-assisted silicon-controlled rectifier (LASCR) has been successfully fabricated in 0.18um CMOS process. LASCR can effectively reduce the SCR trigger voltage without degrade the high-frequency performances of the LNA.

In 0.18um CMOS process technology, LASCR devices have been successfully verified in silicon chip to achieve 4-7.5kV human-body-model (HBM) ESD robustness with 1-3dB loss in K/Ka-band (18-40GHz). According to the measurement results, the proposed ESD protection device also provides desired ESD robustness without degrading RF performance of LNA.

1.2 Organization of This Dissertation

In Chapter 2, some ESD protection devices such as diode will be introduced. Four discharge path including positive-to-V_{SS}(PS) mode, negative-to-V_{SS} (NS) mode, positive-to-V_{DD} (PD) mode, and negative-to-V_{DD} (ND) mode of each circuit will be introduced in this chapter.

In Chapter 3, inductor-assisted silicon-controlled rectifier (LASCR) ESD

protection devices will be introduced in detail. In this study, all testing devices are fabricated in 0.18um CMOS process. This chapter also includes simulation and measurement results of LASCR.

In Chapter 4, K/Ka-band low-noise amplifier (LNA) has been fabricated in 0.18um CMOS process. In this chapter, some parameters of the LNA such as S-parameter and stability will be introduced. Next, the design procedure of LNA will be described, including the selection of transistor and design of the matching network. The LNA will also be equipped with the ESD protection device to measure the ESD robustness of the circuit.

In Chapter 5, the conclusions and some suggestions for future investigation have been indicated.

Chapter 2

ESD Protection Device for RF Applications

2.1 Introduction

Nanoscale CMOS technologies have been used to implement the high-frequency integrated circuits with the advantages of scaling-down feature size, low power consumption, high integration capability, improving high-frequency characteristics, and low cost for mass production [1]. However, the MOS transistors are very sensitive to the electrostatic discharges (ESD) events [2], [3]. In order to sustain the required ESD robustness, such as 2kV in human-body model (HBM) [4], [5], the on-chip ESD protection circuit must be equipped for the pads that may be stressed by ESD, including the input/output (I/O) pads [6], as shown in Fig. 2.1. Conventional ESD protection devices with large dimensions have large parasitic capacitances. The parasitic capacitance will cause signal loss from the pad to ground. Therefore, the ESD protection device couldn't introduce too large parasitic capacitance to degrade the circuit performance [7].

The conventional on-chip ESD protection scheme is shown in Fig. 2.2, where dual diodes at I/O pad are assisted with the power-rail ESD clamp circuit to prevent internal circuits from ESD damage [6]-[8]. The diode is typically used as effective on-chip ESD protection device due to the small parasitic loading effect and high ESD robustness [9], [10]. However, as the operating frequency of circuits increase, the parasitic capacitance is more strictly limited. To overcome this challenge, several prior designs have been reported. The ESD

protection designs with T-coil [11] and T-diode [12] have been presented for teen GHz applications. The stacked diodes [13] and inductor-to-ground [14] have been presented for 24GHz applications. Some ESD protection designs for 60GHz applications have been presented, including inductor-to-ground [15], [16], distributed ESD protection [17], modified LC tank [18], inductor-trigger SCR [19], diodes hidden behind an inductor [20], T-coil with distributed ESD diodes [21], and pi-type ESD block [22].

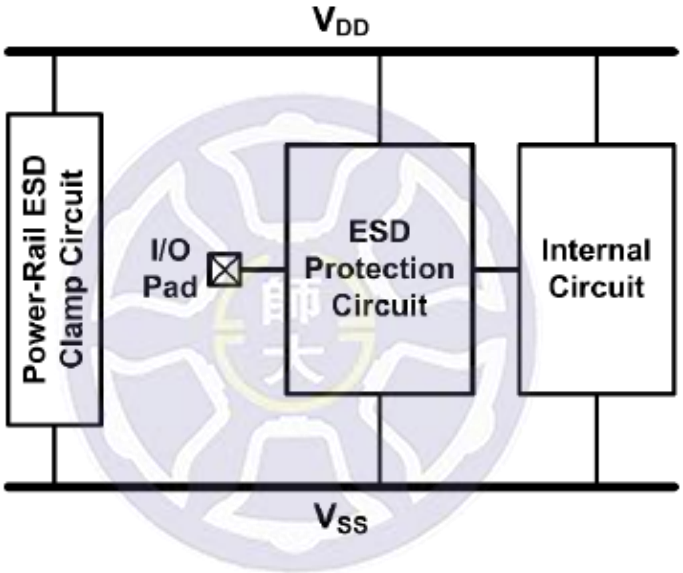


Fig. 2.1. Whole-chip ESD protection for internal circuit.

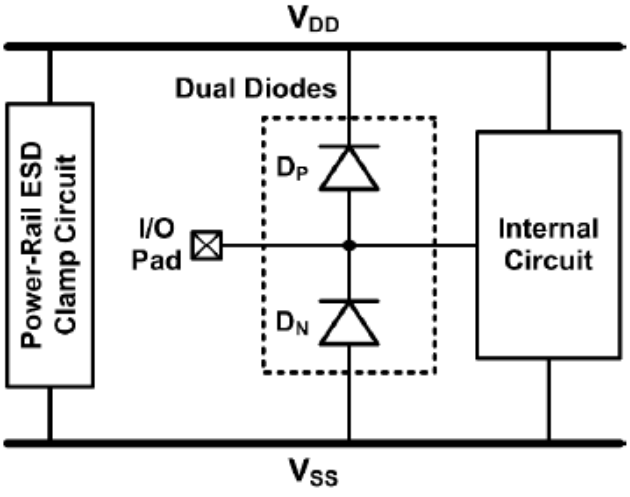
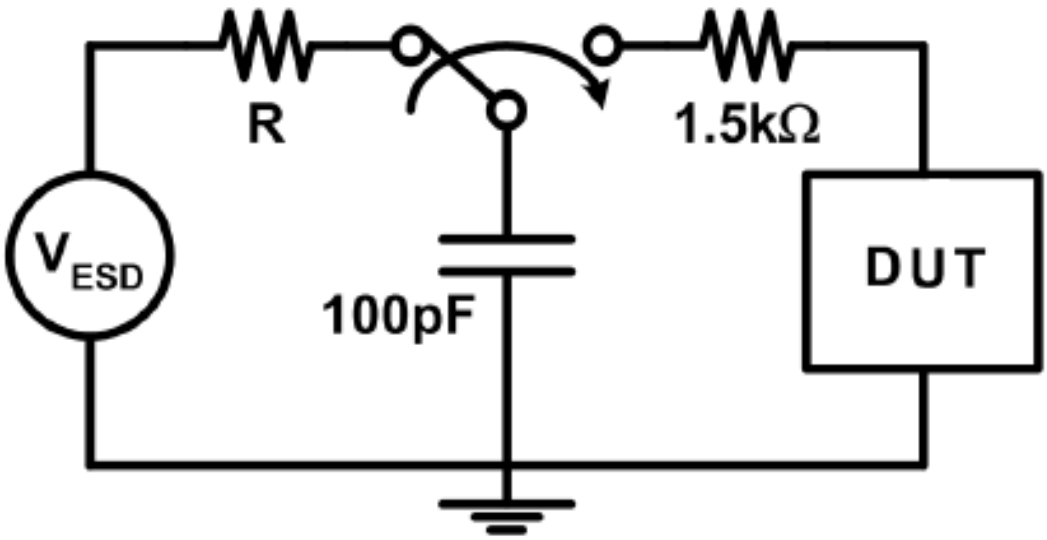


Fig. 2.2. Conventional ESD protection with dual diodes.

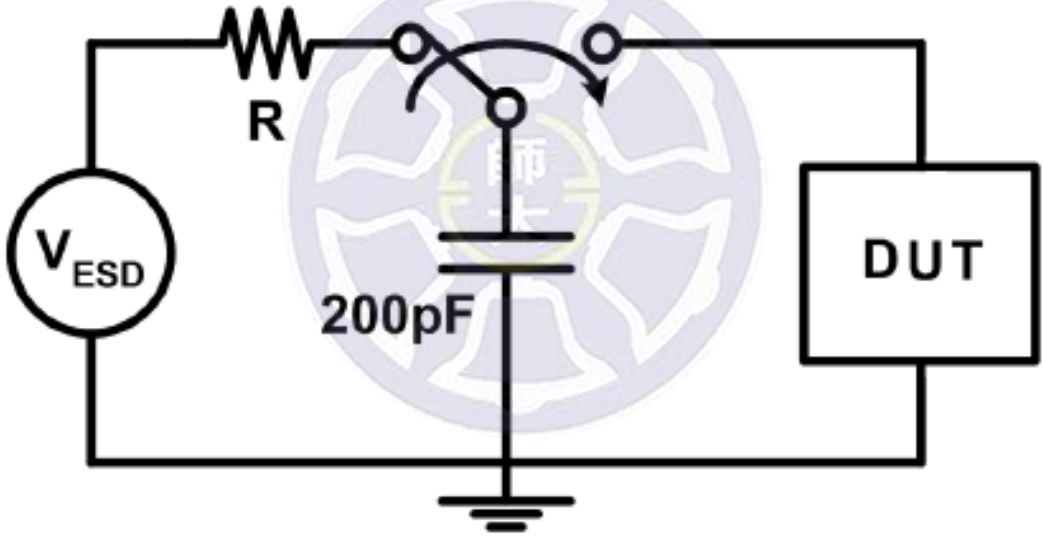
2.2 Whole-Chip ESD Protection Design

Electrostatic discharge (ESD) becomes an important issue on the reliability of integrated circuit (IC). The advanced processes obviously degrade the ESD robustness of IC's in the CMOS technologies. Generally, a typical specification for an RF circuit on human-body-model (HBM) ESD robustness and machine-model (MM) ESD robustness are 2 kV and 200 V, respectively [23], [24]. Both of them are used to evaluate the robustness of the ESD when the IC has been charged through touching by human body or machine. The equivalent circuits of HBM and MM ESD tests are show in Fig. 2.3(a) and (b), respectively. In the HBM ESD test, the charges stored in the capacitor would be discharged through the 1.5kΩ resistor into the device under test (DUT). On the other hand, the charges stored in the capacitor would be discharged directly into the DUT in the MM ESD test.

Therefore, it is necessary to adding the ESD protection circuit beside I/O pads, which provide electrostatic discharge path and keep the circuit without damage from ESD stress. There's also equipped power-rail ESD clamp circuit between V_{DD} and V_{SS} to realize whole-chip ESD protection design.



(a)



(b)

Fig. 2.3. Equivalent circuits of (a) HBM and (b) MM ESD tests.

2.3 CMOS ESD Protection Device for RF Circuit

2.3.1 ESD Protection Design with Diodes.

Forward bias diode is an ESD protection device with good ESD robustness and has been widely used in the design of RF electrostatic discharge protection circuit. Fig. 2.4 show the four ESD-stress modes on I/O pads. When positive electrostatic discharge from I/O pads to V_{DD} (positive-to-V_{DD}, PD), electrostatic current will release by forward bias D_P. When positive electrostatic discharge from I/O pads to V_{SS} (positive-to-V_{SS}, PS), electrostatic current will flowing through D_P and then release by the power-rail ESD clamp circuit. When negative electrostatic discharge form I/O pads to V_{SS} (negative-to-V_{SS}, NS), electrostatic current will release by forward bias D_N. When negative electrostatic discharge from I/O pads to V_{DD} (negative-to- V_{DD}, ND), electrostatic current will flowing through the power-rail ESD clamp circuit and release by forward bias D_N. However, the parasitic capacitance of ESD protection diodes would degrade the performance of circuit when circuit operating frequency gradually increase.

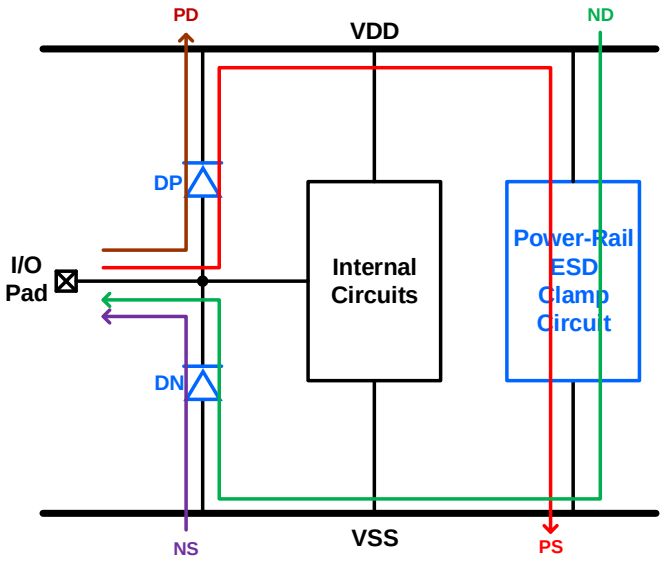


Fig. 2.4. ESD protection design with diodes.

2.3.2 ESD Protection Design with SCR

Silicon-controlled rectifier (SCR) device consists of a lateral NPN and a vertical PNP bipolar transistor to form a 4-layer PNPN structure is shown in Fig. 2.5. This four-layer structure has the same performance with the structure which will occur the latch up problem. SCR has excellent ability to provide the good ESD robustness with minimal layout area. Fig. 2.5 also marked the electrostatic discharge path when this circuit is affected by ESD stress. Compared with the diode, silicon controlled rectifier has smaller parasitic capacitance. Furthermore, advanced process operating voltage gradually decline lets the risk of the latch up gradually reduced. Therefore, SCR becomes a very potentially ESD protection device. In the practical application, Silicon-controlled rectifier must design with the trigger circuit to enhance the turn on speed. The trigger circuit may consist of transistors, diodes, resistors, capacitors and other active and passive components.

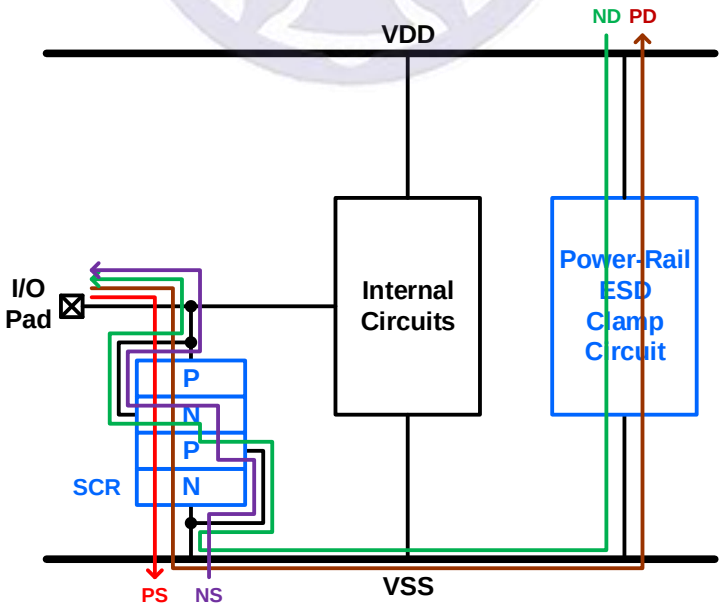


Fig. 2.5. ESD protection design with SCR.

2.3.3 ESD Protection Design with Inductor-Triggered SCR.

When the operating frequency of the circuit is gradually increased to more than ten GHz, the parasitic capacitance of silicon controlled rectifier may still too large to the high-frequency circuits. Thus, Fig. 2.6 is a concept based on silicon-controlled rectifiers parallel with an inductor [25]. This design can lets the signal loss be zero because the equivalent impedance at the resonant frequency is infinite. However, this design requires a MOS switch. This switch is operating at high frequencies and it should turn on when the circuit stressed by ESD. Furthermore, the control signals of this MOS switch required by the power clamp ESD protection circuit. Therefore, this design might be more complex to achieve.

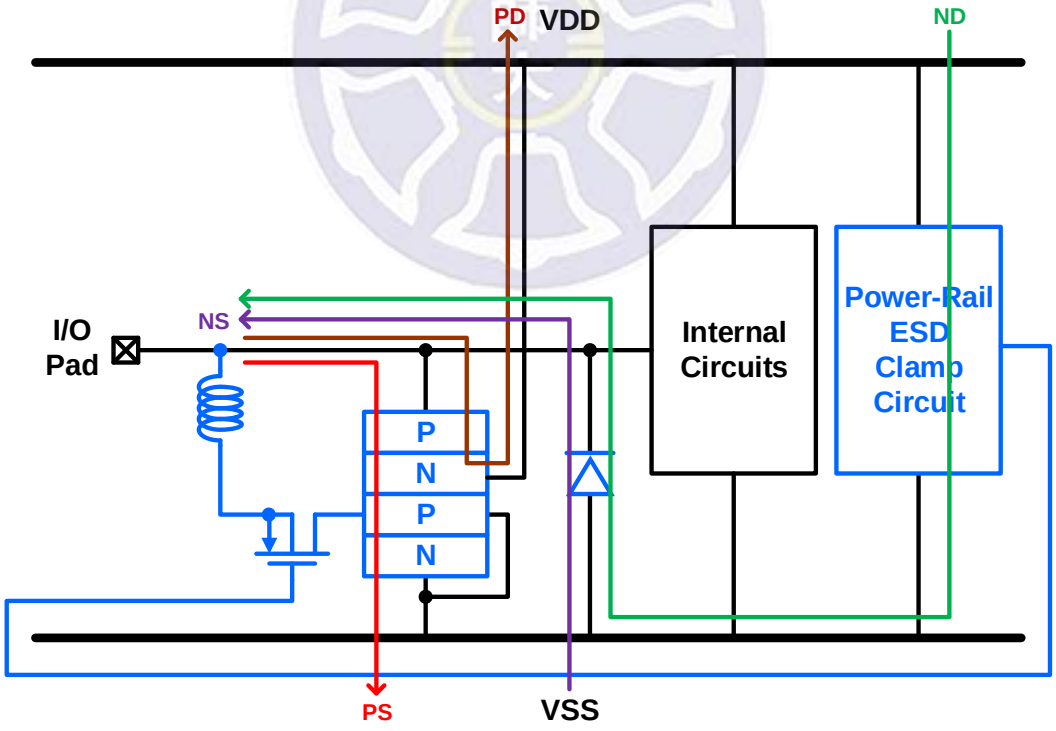


Fig. 2.6. ESD protection design with LTSCR.

Chapter 3

Design of Inductor-Assisted Silicon-Controlled Rectifier

3.1 Introduction

The integrated circuits operated in K-band (18-27GHz) and Ka-band (26.5-40GHz) have been developed for short-range communication [26]-[30]. For example, 24GHz for wireless network solutions [26], 22-29GHz for short-range automotive radars [27], and 22-46GHz for local multipoint distribution service [28], [29]. The ESD protection design for the integrated circuits operated in K/Ka band is needed. In this work, a novel inductor-assisted silicon-controlled rectifier (LASCR) device is proposed for effective on-chip ESD protection in K/Ka-band.

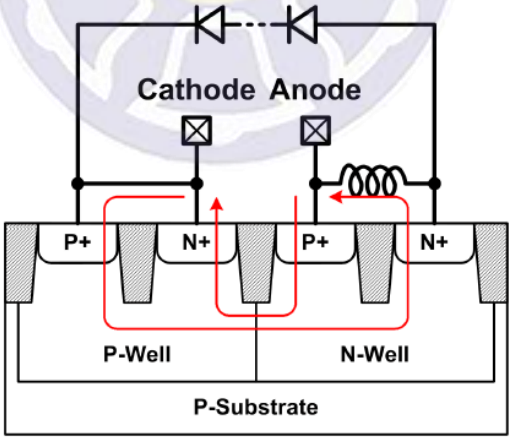
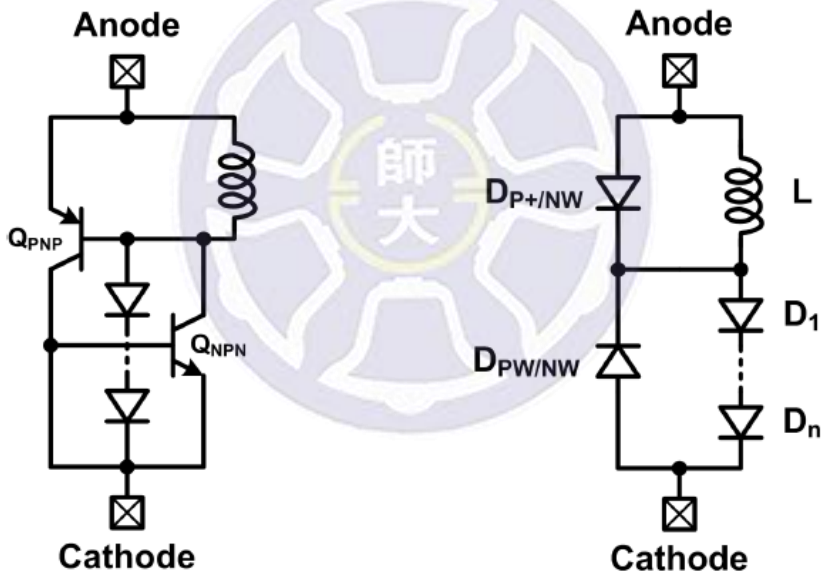


Fig. 3.1. SCR cross-sectional view and ESD current paths.

The proposed LASCR is shown in Fig. 3.1, which consists of an SCR [31], an inductor, and a diode string. The ESD current path from anode to cathode

consists of P+/N-well/P-well/N+ SCR. The diode string is used to enhance the turn-on efficiency of SCR [32], [33]. The ESD current path from cathode to anode consists of P-well/N-well diode and inductor. The equivalent circuit of the LASCR is shown in Fig. 3.2(a), where Q_{PNP} is formed by the P+, N-well, and P-well, and the Q_{NPN} is formed by the N-well, P-well, and N+. As ESD zapping from anode to cathode, the positive-feedback regenerative mechanism of Q_{PNP} and Q_{NPN} results in the SCR device highly conductive to make SCR very robust against ESD stresses. Under normal circuit operating condition, the inductor can resonate with the parasitic capacitance.



(a) (b)

Fig. 3.2. Equivalent circuit of LASCR, where SCR expressed by (a) BJT and (b) diodes.

To simulate this device by using foundry provided model, the equivalent circuit of the LASCR can be further expressed by P+/N-well diode ($D_{P+/NW}$), P-

well/N-well diode ($D_{PW/NW}$), inductor (L), and diode string (D_1, ..., D_n), as shown in Fig. 3.2(b). The dimension of SCR depends on the required ESD robustness, and the diode numbers and dimension of diode string depend on the trigger ability. Once the dimension of SCR has been chosen, the inductor can be designed to minimize the high-frequency performance degradation by using

$$L = \frac{1}{C_{P+/N-well} \times (2\pi f_0)^2} \tag{3.1}$$

where f_0 is the operating frequency and $C_{P+/NW}$ is the parasitic capacitance of $D_{P+/NW}$ and is show in Fig. 3.3. Of course, the high-frequency performances are also affected by the parasitic resistances of diodes and inductor, and they can be simulated by using the real diode and inductor models.

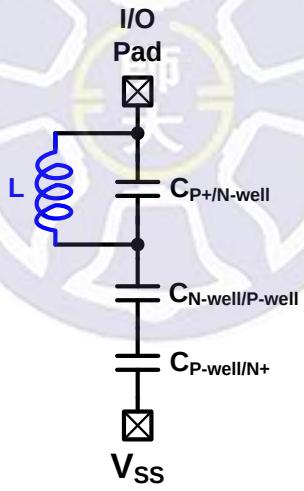


Fig. 3.3. Equivalent circuit of LASCR.

Fig. 2.8 shows that electrostatic discharge path of inductor-assisted silicon-controlled rectifier when the circuit is stressed by ESD. When positive electrostatic discharge from I/O pads to V_{SS} (positive-to-V_{SS}, PS), electrostatic current will release by silicon-controlled rectifier. When positive electrostatic

discharge from I/O pads to V_{DD} (positive-to-V_{DD}, PD), electrostatic current will flows through silicon-controlled rectifier to V_{SS} and then release by power-rail ESD clamp circuit. When negative electrostatic discharge form I/O pads to V_{SS} (negative-to-V_{SS}, NS), electrostatic current will release by inductor and PN junction ($N-well/P-well$) which is in the silicon-controlled rectifier. When negative electrostatic discharge from I/O pads to V_{DD} (negative-to-V_{DD}, ND), electrostatic current will flowing through the power-rail ESD clamp circuit and release by PN junction ($N-well/P-well$) and inductor. Besides, LASCR provide the bidirectional ESD current paths between I/O pads and V_{SS}, so it can achieve the whole chip ESD protection by using only an LASCR and a power-rail ESD clamp circuit.

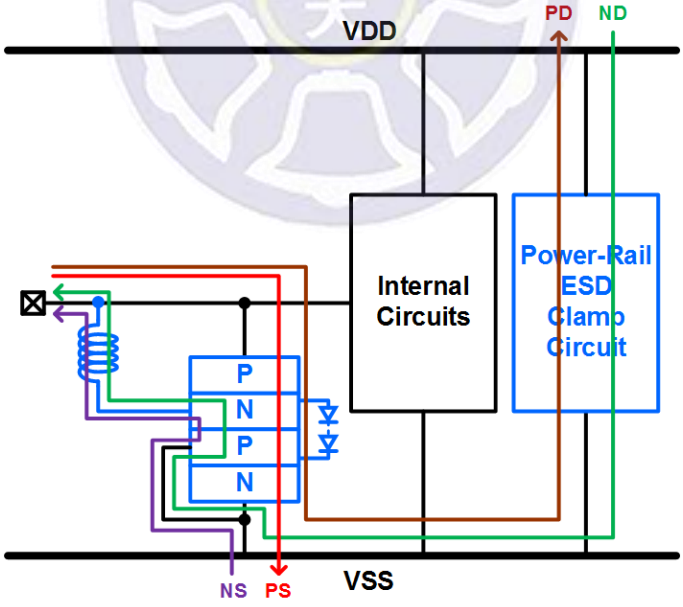


Fig. 3.4. Co-design of SCR and inductor's ESD protection circuit.

3.2 Design of LASCR

In this work, all LASCR devices are fabricated in 0.18 CMOS process and shown in Table 3.1. The sizes of SCR are selected as 30um and 60um. Since the circuit which fabricated in 0.18 CMOS process typically operated at 1.8V, the diode number in the diode string should more then 3, so as not to trigger the ESD protection device when the circuit is under the normal operation mode. As the result, the diode numbers in the diode string are selected as 3 and 5, and the size of each diode is 15um or 30um. The $C_{P+/NW}$ of 30um and 60um SCR around 30GHz are ~60fF and ~120fF, respectively. Therefore, the values of required L for K/Ka-band applications are 460pH and 230pH, respectively. The simulation of inductor is completed by using HFSS, as shown in Fig. 3.3.

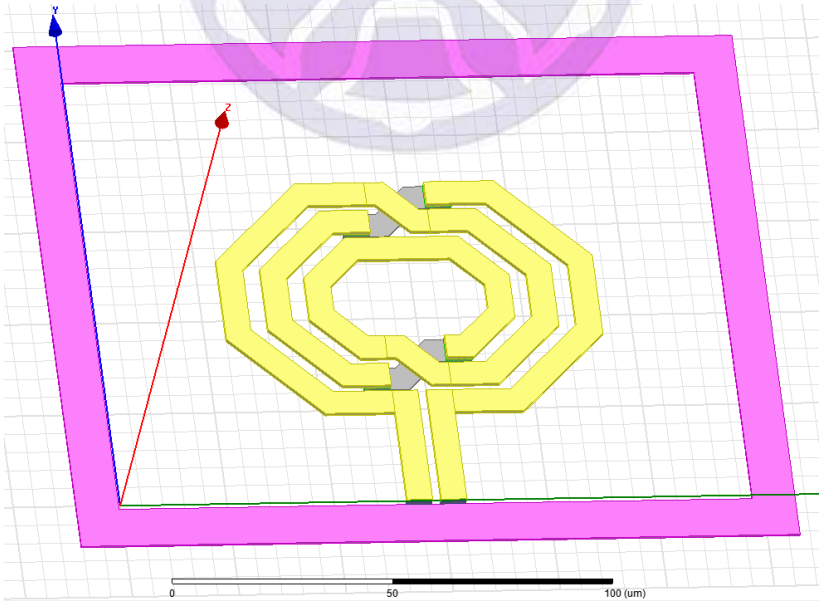


Fig. 3.5. 3D EM simulation of inductor.

Table 3.1

Design specification of the proposed LASCR

Cell Name	SCR Width (um)	SCR Length (um)	Diode Width (um)	Diode Quantity	Operating Frequency (GHz)	Power-Rail ESD Clamp Circuit
LASCR_W30_3D	30	7	15	3	30	No
LASCR_W30_5D				5		
LASCR_W60_3D	60		30	3		
LASCR_W60_5D				5		

3.3 Comparing Device

In order to compare the difference between the proposed design and previous designs, this study also fabricated few kinds of diode-triggered SCR (DTSCR) and diode devises. Table 3.2 show that size of SCR are selected to be 30um and 60um, while the diode numbers in the diode string are 3 and 5, the dimension of each diode is 15um or 30um, four devices are not equipped with the power-rail ESD clamp circuit. Fig. 3.6 is the equivalent circuit of DTSCR and can be seen that inductance is the only difference between DTSCR and LASCR. The size of diode device is show in Table 3.3.

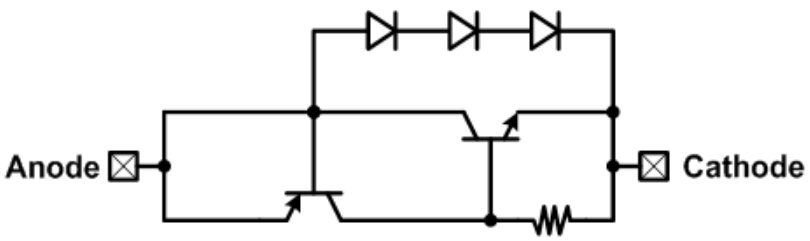


Fig. 3.6. Equivalent circuit of DTSCR.

Table 3.2

Design specification of the proposed DTSCR

Cell Name	SCR Width (um)	Diode Width (um)	Diode Quantity	Power-Rail ESD Clamp Circuit
DTSCR_W30_3D	30	15	3	No
DTSCR_W30_5D			5	
DTSCR_W60_3D	60	30	3	
DTSCR_W60_5D			5	

Table 3.3

Design specification of the proposed diode

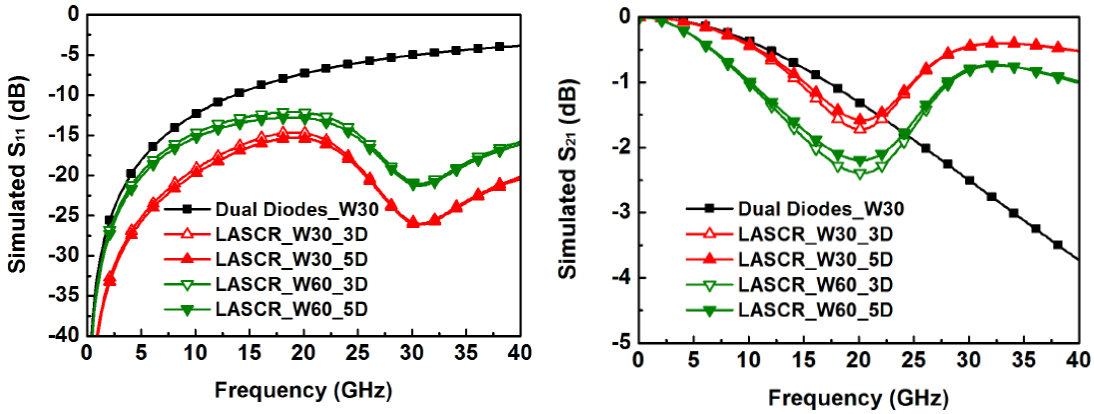
Cell Name	Diode Type	Diode Width (um)	Power Clamp Circuit
Dual Diodes_W30	N＋/PW	30	Yes
	P＋/NW		

3.4 Simulation Results

The high-frequency characteristics are simulated by using the microwave circuit simulator ADS with the selected device dimensions. In the two-port simulation, a signal source with 50Ω impedance drives the port 1 and a 50Ω load is connected to the port 2. The port 1, port 2, and the anode of LASCR are connected together, and the cathode of LASCR is connected to ground. The simulated S11 and S21 of test devices are compared in Fig. 3.5. At 30GHz, the

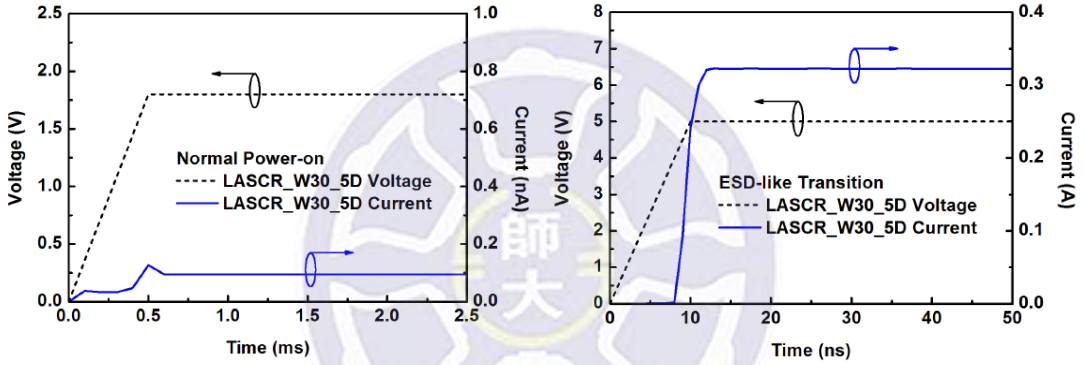
30um dual diodes (Dual Diodes_W30) have 2.5dB loss, while the 30um LASCR with three diodes (LASCR_W30_3D), the 30um LASCR with five diodes (LASCR_W30_5D), the 60um LASCR with three diodes (LASCR_W60_3D), and the 60um LASCR with five diodes (LASCR_W60_5D) only have 0.5dB, 0.4dB, 0.8dB, and 0.8dB loss, respectively. Among the K/Ka-band, the loss of each LASCR is lower than 3dB, which is more suitable for ESD protection.

The proposed devices under normal power-on conditions and ESD transient events are simulated by using HSPICE. Fig. 3.6(a) shows the HSPICE-simulated voltage/current waveforms of one test device, LASCR_W30_5D, under the normal power-on condition. Under the normal power-on condition, the dc bias of anode is raised from 0V to 1.8V with 0.5ms rise time. The test device is kept off with very low leakage current. Fig. 3.6(b) shows the simulated voltage/current waveforms of LASCR_W30_5D under the ESD transition, where a 0V-to-5V voltage pulse with 10ns rise time is applied to the test device to simulate the fast transient voltage of HBM ESD event. When a positive fast-transient ESD voltage is applied to anode with cathode grounded, the LASCR_W30_5D can be turned on to discharge ESD current from anode to cathode. With the limited voltage height of 5 V in the voltage pulse, the simulation result can check the clamping ability of LASCR before the internal circuit breakdown.



(a) (b)

Fig. 3.7. Simulated S_{11} and S_{21} of test devices.



(a) (b)

Fig. 3.8. Simulated voltage/current waveforms of LASCR_W30_5D under (a) normal power-on condition and (b) ESD-like transition.

3.5 Experimental Results of Test Devices

Five test devices have been fabricated in a nanoscale CMOS process. All test devices are implemented with ground-signal-ground (G-S-G) pads to facilitate on-wafer two-port S-parameters measurement. Fig. 3.7 shows the chip micrograph of one test device, LASCR_W30_3D. The other LASCR devices

have almost the same layout arrangement. The cell area of LASCR_W30_3D, LASCR_W30_5D, LASCR_W60_3D, and LASCR_W60_5D are 100x95um^2, 100x105um^2, 90x90um^2, and 90x100um^2, respectively.

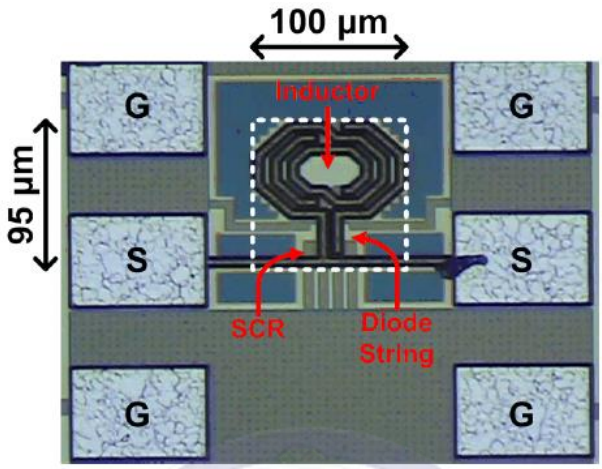
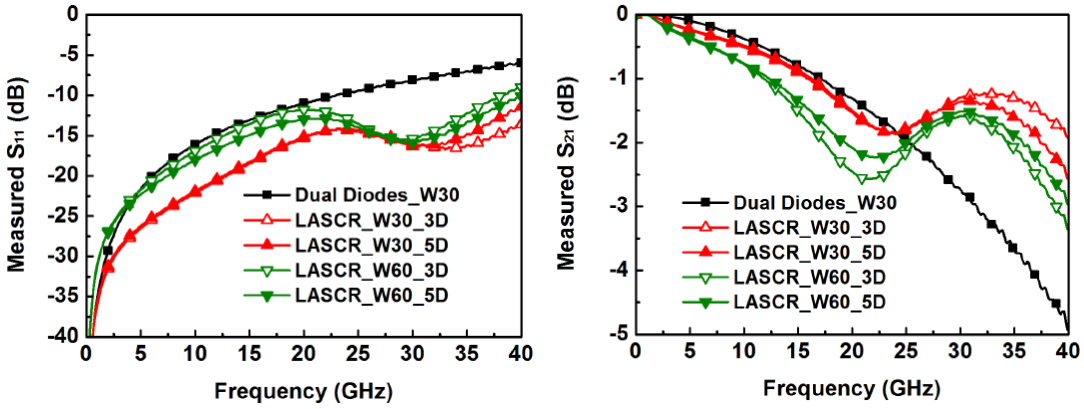


Fig. 3.9. Chip micrograph of LASCR_W30_3D.

3.5.1 High-Frequency Performances

In order to extract the intrinsic characteristics of the test devices in high frequencies, the parasitic effects of the G-S-G pads have been removed by using the de-embedding technique [34]. With the on-wafer two-port measurement, the S-parameters of these test devices have been extracted. The source and load resistances to the test circuits are kept at 50 Ω. The measured S11 and S21 versus frequencies among the test devices are shown in Fig. 3.8. As shown in Fig. 3.8(a), the LASCR devices exhibit good input matching (S11 < -15dB) around 30 GHz, while Dual Diodes_W30 only has S11 = -8.1dB. At 30GHz, LASCR_W30_3D, LASCR_W30_5D, LASCR_W60_3D, and LASCR_W60_5D have 1.3dB, 1.4dB, 1.6dB, and 1.5dB loss, respectively, while Dual Diodes_W30 has 2.7dB loss.



(a) (b)

Fig. 3.10. Measured S_{11} and S_{21} of test devices.

3.5.2 ESD Robustness

The HBM ESD robustness of each device is tested. The failure criterion is defined as the I-V curve seen between test pads shifting over 30% from its original curve after ESD stressed at every ESD test level. According to the measurement results, LASCR_W30_3D, LASCR_W30_5D, LASCR_W60_3D, and LASCR_W60_5D can pass +4.5kV, +4kV, +7.5kV, and +7.5kV HBM ESD tests, respectively. Besides, these LASCR devices can also pass -4kV, -4kV, -7.5kV, and -7.5kV HBM ESD tests, respectively. The Dual Diodes_W30 can only pass +3kV and -3.5kV HBM ESD tests.

To investigate the turn-on behavior and the I-V characteristics in high-current regions of the test devices, the transmission line pulsing (TLP) system with a 10ns rise time and a 100ns pulse width is used. The trigger voltage (V_{t1}), holding voltage (V_h), and secondary breakdown current (I_{t2}) of test devices in the time domain of HBM ESD event can be extracted from the TLP-measured I-V curves. The TLP-measured I-V curves of test devices are shown in Fig. 3.9. Once the pulses stressed to the test devices, LASCR_W30_3D and

LASCR_W60_3D (LASCR_W30_5D and LASCR_W60_5D) can be triggered on at ~5V (~7.6V). The V_h of all LASCR devices exceed V_{DD} (1.8V in the given CMOS process), which is safe from latchup event. For the current-handling ability of ESD protection devices, LASCR_W30_3D, LASCR_W30_5D, LASCR_W60_3D, and LASCR_W60_5D can achieve the TLP-measured I_{t2} of 2.4A,2.1A, 4.2A, and 4.0A, respectively, while Dual Diodes_W30 has only 1.8A. The turn-on behavior can ensure the effective ESD protection capability of the proposed LASCR.

The standby leakage current of the test devices can also be measured by using the TLP system. At 1.8V bias, all LASCR devices have the leakage current of <1nA. All measurement results of the test devices are summarized in Table 3.4.

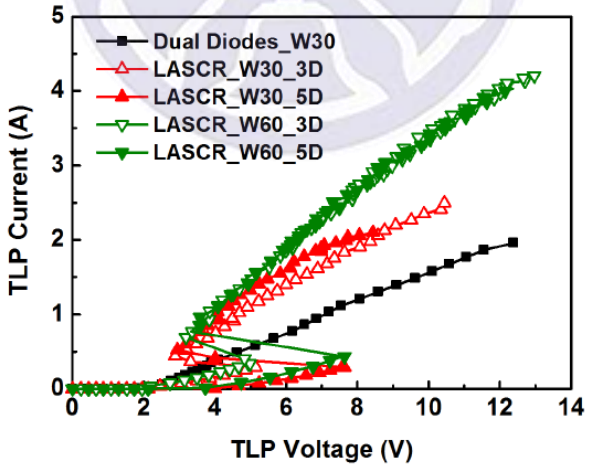


Fig. 3.11. TLP I-V curves of test devices.

Table 3.4

Design Parameters and Measurement Results of Test Devices

		LASCR_W30_3D	LASCR_W30_5D	LASCR_W60_3D	LASCR_W60_5D	Dual Diode_W30
Design Parameters	SCR	30μm	30μm	60μm	60μm	$D_P = 30\mu m$ $D_N = 30\mu m$
	Diode String	15μm×3	15μm×5	30μm×3	30μm×5	
	Inductor (L)	460pH	460pH	230pH	230pH	
	Area	$100\times95\mu m^2$	$100\times105\mu m^2$	$90\times90\mu m^2$	$90\times 100\mu m^2$	$20\times35\mu m^2$
Measurement Results	S_{11} at 30GHz	-16.0dB	-16.3dB	-15.4dB	-15.9dB	-8.1dB
	S_{21} at 30GHz	-1.3dB	-1.4dB	-1.6dB	-1.5dB	-2.7dB
	HBM ESD Level	+4.5kV/-4kV	+4kV/-4kV	+7.5kV/-7.5kV	+7.5kV/-7.5kV	+3kV/-3.5kV
	TLP V_{t1}	5.1V	7.6V	5.0V	7.6V	N/A
	TLP V_h	2.9V	2.9V	3.2V	3.3V	N/A
	TLP I_{t2}	2.4A	2.1A	4.2A	4.0A	1.8A
	Leakage at 1.8V (25°C)	0.5nA	0.2nA	0.9nA	0.5nA	<0.1nA
	Leakage at 1.8V (100°C)	4.5nA	4.0nA	7.9nA	8.6nA	-

3.5.3 Failure Analysis

The failure analysis (FA) has been done to seek the failure location. The FA picture of the LASCR_W30_3D after 5kV HBM ESD stress, LASCR_W30_5D after 4.5kV HBM ESD stress, LASCR_W60_3D after 8kV HBM ESD stress, and LASCR_W60_5D after 8kV HBM ESD stress are shown in Figs. 3.12-3.15. After HBM ESD stress, the damaged regions are all located on the SCR device.

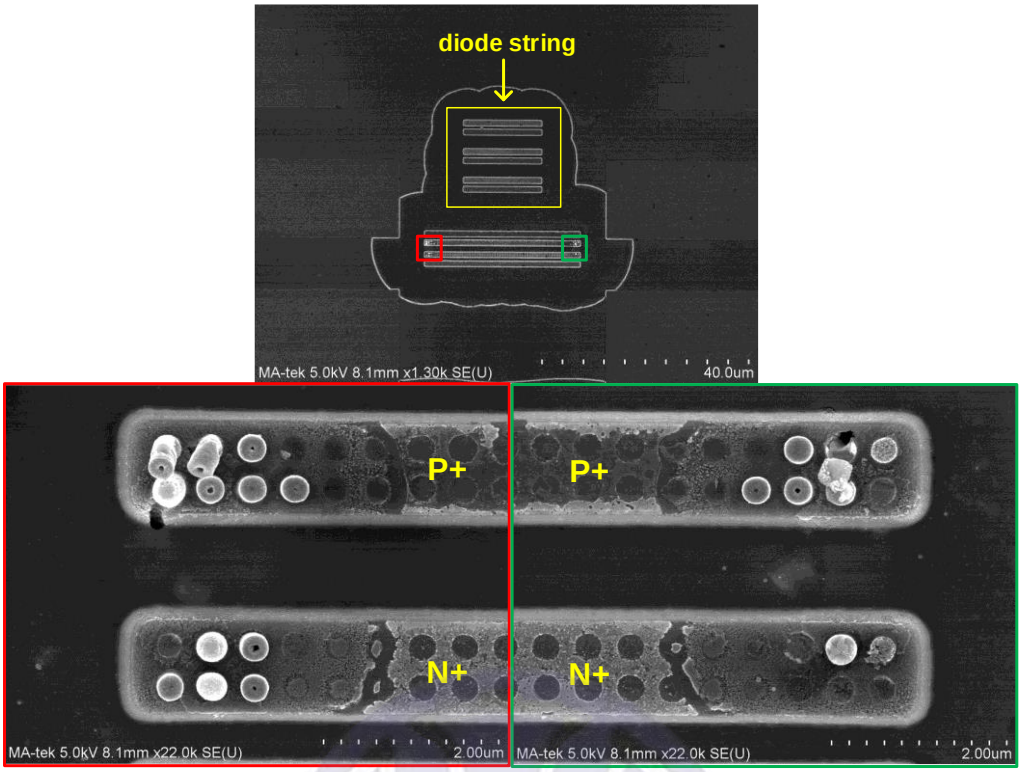


Fig. 3.12. The SEM pictures of the LASCR_W30_3D after +5kV HBM stresses.

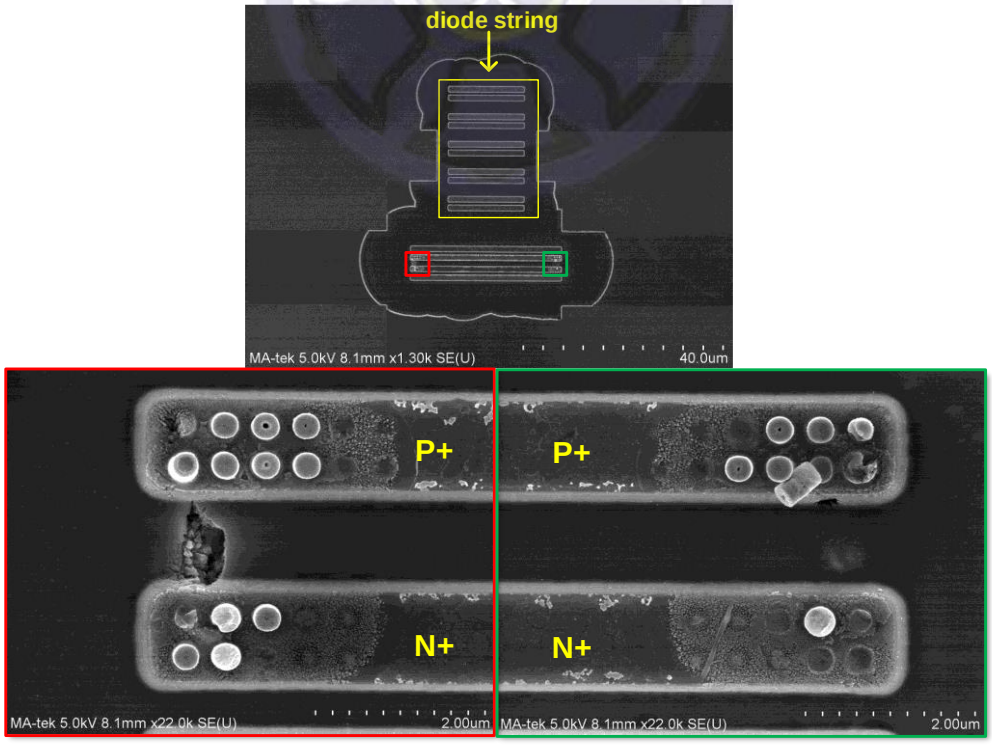


Fig. 3.13. The SEM pictures of the LASCR_W30_5D after +4.5kV HBM stresses.

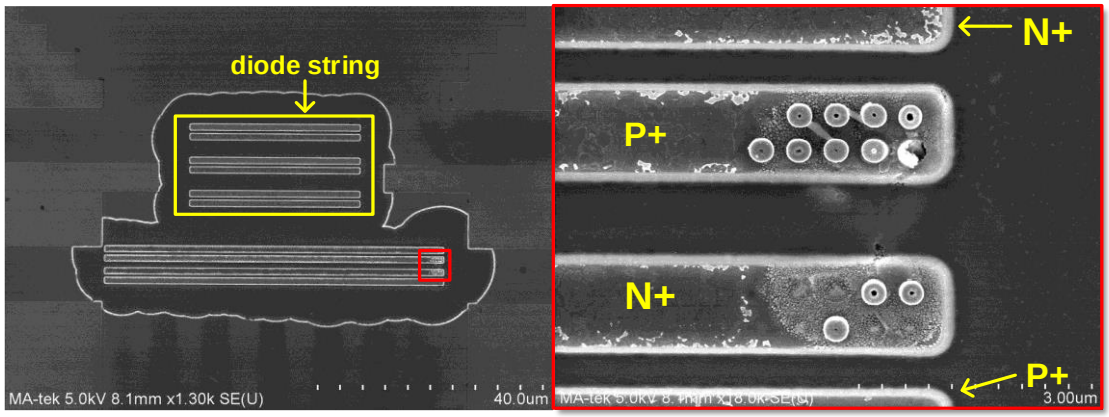


Fig. 3.14. The SEM pictures of the LASCR_W60_3D after +8kV HBM stresses.

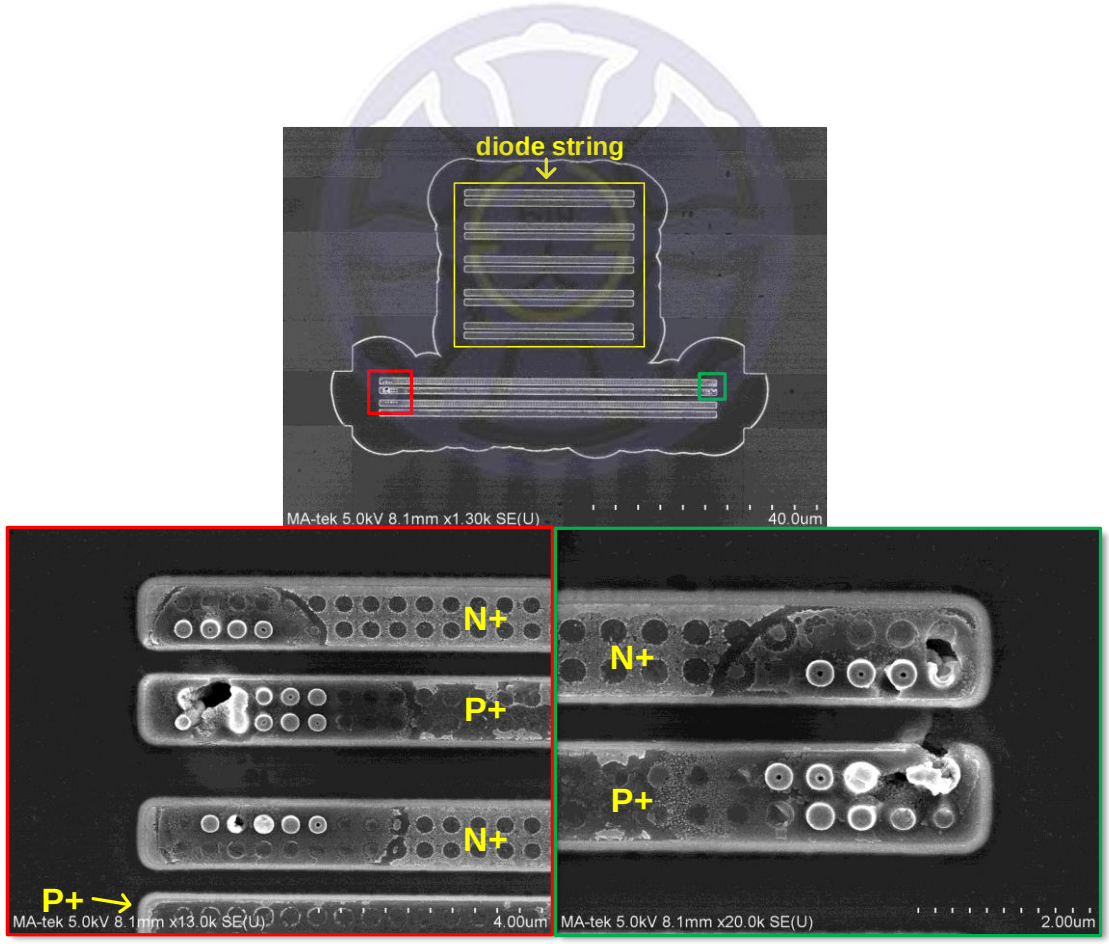


Fig. 3.15. The SEM pictures of the LASCR_W60_5D after +8kV HBM stresses.

3.5.4 Leakage

In order to investigate the influence of temperature on the device, the leakage of LASCR devices at 25°C and 100°C are measured. Table 3.4 also shows that leakage of LASCR devices at different temperatures. At 25°C, leakage of LASCR_W30_3D is 0.5 nA, LASCR_W30_5D is 0.2 nA, LASCR_W60_3D is 0.9 nA, and LASCR_W60_5D is 0.5 nA, respectively. At 100°C, leakage of LASCR_W30_3D is 4.5 nA, LASCR_W30_5D is 4.0 nA, LASCR_W60_3D is 7.9 nA, and LASCR_W60_5D is 8.6 nA, respectively. It can be seen that leakage of the LASCR devices are still small under high temperature.

3.6 Conclusion

The proposed ESD protection device of LASCR has been developed in nanoscale CMOS process for K/Ka-band applications. Verified in silicon chip, LASCR devices with 30um (LASCR_W30_3D and LASCR_W30_5D) and 60um (LASCR_W60_3D and LASCR_W60_5D) width can pass 4kV and 7.5kV HBM ESD tests, respectively, and they have the loss lower than 3dB in K/Ka-band. In fact, LASCR devices exhibit good high-frequency performances between 0~40 GHz, so they can also be used for wideband or high-speed applications. Measurement results verify the high-frequency performances and confirm the ESD protection ability of LASCR. Therefore, the proposed LASCR can be a good solution for ESD protection.

Chapter 4

K/Ka-Band Low Nosie Amplifier

4.1 Introduction

As technology progresses, more important applications are use in the K/Ka band, such as wireless network, short-range automotive radars, and local multipoint distribution service. Considering the sensitivity of the system in RF applications, the low noise receiver is necessary. In the receiver system, low noise amplifier (LNA) is a very important and critical circuit as shown in Fig. 4.1.

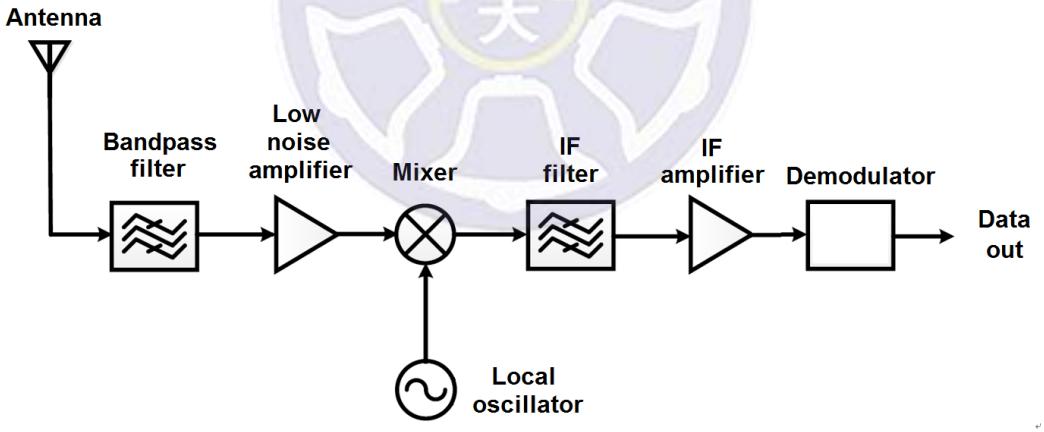


Fig. 4.1. Receiver system architecture.

The function of low noise amplifier is to provide enough gain to amplify the weak RF signal received by antenna and suppress the influence of noise generated by subsequent stage at the same time. It can also improve signal to

noise ratio (SNR) and let signal without distortion. Thereby allowing received signals can be correctly demodulation out by the subsequent circuit.

Therefore, the needed of accurate transistor small signal model and noise model when design the low noise amplifier is necessary. Because the noise from transistor is the main noise of the overall circuit and may interfere RF signal, then signal will distortion and couldn't be demodulated by the subsequent stage circuit. Therefore, an accurate transistor small signal model and noise model is very important.

4.2 Source of Transistor Noise

Transistor noise generated by interpreting the results as Brownian motion caused. However, transistors is susceptible noise in the small signal operating conditions. Generally, transistor noise can be divided into thermal noise, distributed gate resistance noise, and flicker noise.

4.2.1 Channel thermal noise

Channel thermal noise is due to the electron perturbations within the transistor channel. Channel electrons excited by the heat and random motion, so that transistor produces random changes in voltage and current. These voltage and current changes produce thermal noise, and then define the effective noise power with equation (4.1)

$$P_{av} = kT\Delta f \tag{4.1}$$

where k is Boltzmann constant, which is 1.38×10^{-23}(J/K). T is the absolute temperature, Δf is the noise bandwidth with units of Hz. By equation (4.1) knows that, when the conductor temperature increase, effective noise power will

increase.

Analysis the influence of thermal noise in the circuit would equivalent the thermal noise to a parallel noise current source, and must assume the transistor as ideal state without any noise. Schematic diagram is show in Fig. 4.2. The noise power equation is (4.2)

$$\overline{I_n^{\,2}}(\mathrm{f}) = 4\mathrm{kT}\gamma g_m \tag{4.2}$$

where k is Boltzmann constant, which is 1.38×10^{-23}(J/K). T is the absolute temperature. g_m is the drain transduction value when bias is zero. Value of γ would greater than 1 in the short channel, and would be $2/3$ in the long channel.

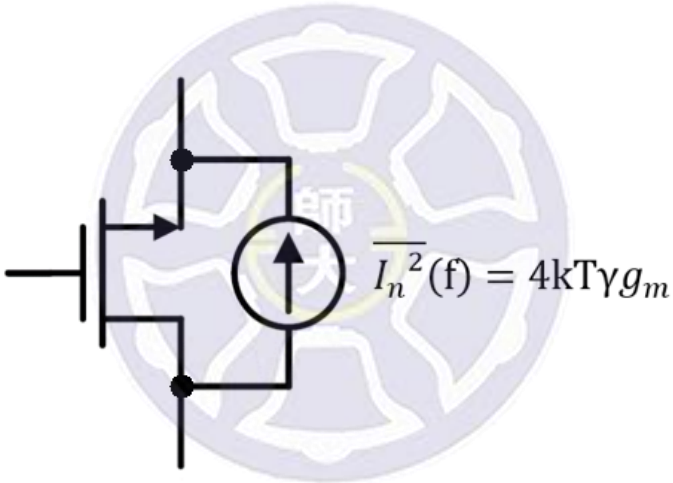


Fig. 4.2. Transistor channel thermal noise model.

4.2.2 Distributed Gate Resistance Noise

During the CMOS process, the poly layer is used on the gate. Therefore, the gate will produce polysilicon resistors. Equation and model is show in equation (4.3) and Fig. 4.3, respectively.

$$R_g = R_h \frac{W}{3n^2 L} \tag{4.3}$$

In equation (4.3), R_h is the polysilicon resistors, n is the number of transistors

finger, W and L are the transistors width and length, respectively. The equation of output noise provided by the distributed gate resistance is

$$\overline{V_{n,out}}^2 = 4kT\frac{R_g}{3}(g_m r_o)^2 \tag{4.4}$$

From equation (4.3) and (4.4), if want to achieve low noise circuit design, use larger number of fingers and lower channel width in the same transistor size can make gate resistance smaller. Thereby reducing the noise generated by the resistor.

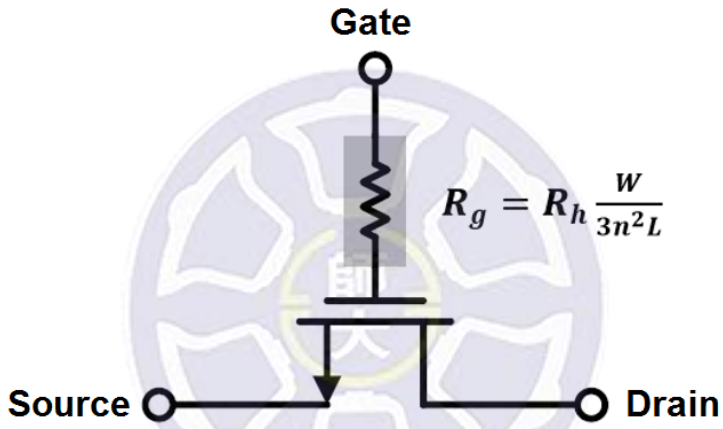


Fig. 4.3. CMOS transistors gate resistance model.

4.2.3 Flicker Noise

Flicker noise is the major noise when CMOS transistors operating at low frequencies. The flicker noise mostly occurs between the gate oxide layer and the silicon substrate surface. Due to silicon crystal and the surface at this interface will produce a discontinuous bond, when the current passes will randomly be captured and released, causing transistor drain current unstable and produce flicker noise, but when the frequency greater than a specific frequency,

flicker noise will be smaller than the thermal noise. This situation can be explained by equation (4.5).

$$\overline{V_n^{\,2}} = \frac{K}{C_{ox}WL} \times \frac{1}{f} \tag{4.5}$$

Where K is the process parameters.

4.3 Parameters of Low-Noise Amplifier

4.3.1 Noise Figure

To know the amplifier noise figure (NF), we must first understand the noise factor (F). The definition of noise factor is the input signal-noise ratio dividing the output signal-noise ratio, and can calculated by equation (4.6).

$$\mathrm{F} = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{S_{in}/N_{in}}{GS_{in}/(GN_{in}+N_a)} = 1 + \frac{N_a}{GN_{in}} \tag{4.6}$$

S_{in} is input signal power, S_{out} is output signal power, N_{in} is input noise power, N_{out} is output signal power, G is the amplifier gain, and N_a is the noise power interior of amplifier.

For example, in a two-stage amplifier, equation (4.7) show that two-stage amplifiers noise factor.

$$\mathrm{F} = \frac{N_2}{N_{in}G_1G_2} = 1 + \frac{N_{a1}}{N_{in}G_1} + \frac{N_{a2}}{N_{in}G_1G_2} = F_1 + \frac{F_2-1}{G_1} \tag{4.7}$$

In equation (4.7), $F_1 = 1 + \frac{N_{a1}}{N_{in}G_1}$ is the first-stage amplifiers noise factor, $F_2 = 1 + \frac{N_{a2}}{N_{in}G_2}$ is the second-stage amplifiers noise factor. So we can use the results of the two-stage amplifier to infer the n-stage amplifier noise factor should be the following equation (4.8).

$$\mathrm{F} = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2} + \cdots + \frac{F_n-1}{G_1G_2\ldots G_{n-1}} \tag{4.8}$$

By observation of equation (4.8), knows that multiple cascading amplifier noise

factor is mainly determined by the first-stage amplifier. Therefore, the first-stage amplifier matching network and architecture are the most important things during the design of low-noise amplifier. Other stage of amplifier is primarily responsible for increasing the gain. Finally, we can define the noise figure of the following equation (4.9). F in this equation is noise factor.

$$\mathrm{NF} = 10 \log F \tag{4.9}$$

4.3.2 Gain

In the low-noise amplifier design, gain is an important parameter to consider. If the gain of low-noise amplifier not enough, it could be unable to suppress the noise of subsequent circuit. It also cause the large noise figure and let signal distortion. When design the RF amplifier, there have three kinds of power gain equation (4.10)-(4.12). They are transducer power gain (G_T), operation power gain (G_P), and available power gain (G_A), respectively. Definition of G_T is the value of power delivered to the load divided the value of power available from the source. Definition of G_P is the value of power delivered to the load divided the value of power input to the network. Definition of G_A is the value of power available from the network divided the value of power available from the source. They also are displayed in Fig. 4.4.

$$G_T = \frac{P_L}{P_{AVS}} = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2} \times |S_{21}|^2 \times \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{4.10}$$

$$G_P = \frac{P_L}{P_{in}} = \frac{1}{|1-\Gamma_{in}|^2} \times |S_{21}|^2 \times \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{4.11}$$

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} \times |S_{21}|^2 \times \frac{1}{|1-\Gamma_{OUT}|^2} \tag{4.12}$$

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \tag{4.13}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{11}\Gamma_L} \tag{4.14}$$

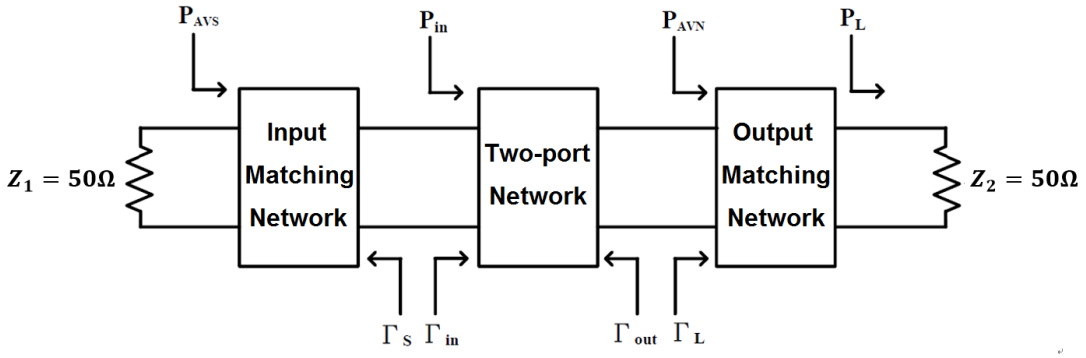


Fig. 4.4. Two-port network actual power diagram.

4.3.3 Stability

In the design of the amplifier, stability is a very important parameter need to take into consideration. If the amplifier is in an unstable state, characteristic of the circuit will be substantially reduced. Equation (4.15) and (4.16) are the amplifier circuit unconditionally stable definition, if the circuit is fit to these two equation, the amplifier is unconditionally stable.

$$\mathrm{k} = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{4.15}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{4.16}$$

4.4 Design of K/Ka Band Low-Noise Amplifier

Traditionally, low-noise amplifier architecture most commonly used as a common-source configuration or cascode configuration. Compare the performance of these two configuration can found some features between them.

DC supply for cascode configuration is twice times of common-source configuration, so cascode configuration maximum available gain will much higher than the common-source configuration, but the power consumption of the cascode configuration will double, and the minimum noise figure will be more than common-source configuration, too.

Due to hoping to reach the application of low-voltage and low noise figure in this design, so choose the common-source configuration for low-noise amplifier design. On the other hand, to provide the low-noise amplifier has enough gain at K/Ka band to suppress the noise from the subsequent stage. We choice the two-stage cascade common-source amplifier for this study.

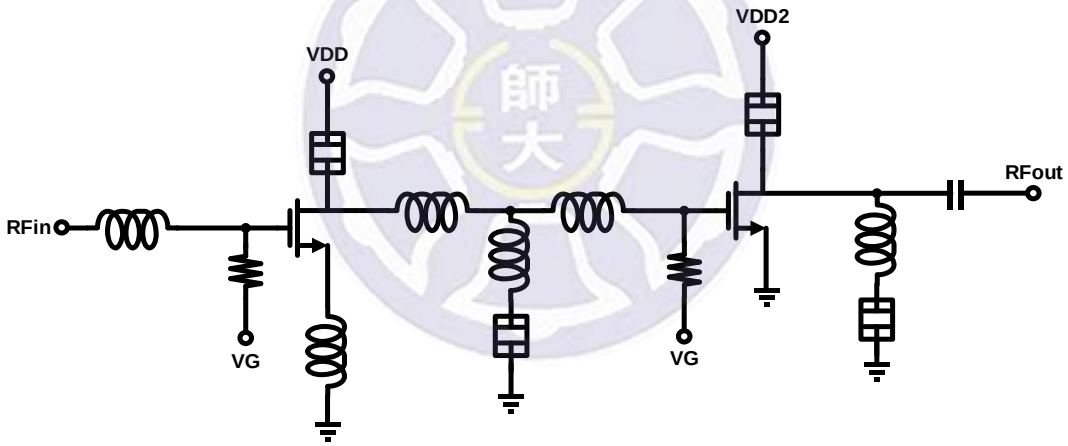


Fig. 4.5. K/Ka-band low noise amplifier architecture.

Fig. 4.5 is the low-noise amplifier architecture of this study. First input stage using a series inductor and a source degeneration inductor to achieve the input noise match and still have a good gain to suppress the noise figure from subsequent stage. Between the first stage and second stage, T-model is use to complete the stage-to-stage conjugate match. The second output stage using

series capacitance and inductor to complete output conjugate match.

4.4.1 Common-source transistor bias and size analysis

Select the bias of transistor is the first step of amplifier design. In CMOS 0.18μm process, the maximum of common-source configuration V_{DD} is 1.8V, and the gate bias (V_G) is one of the main selection during design. V_G choice will affect the value of transduction (g_m), the drain current (I_d), and the noise figure (NF). So the greater V_G will cause the greater current and the greater power consumption. According to system requirements, we need to make trade-offs between these three parameters.

Fig. 4.6 is the transistor DC-IV curve. Through the figure we can observe the ID become lower when V_{GS} increase. Then Fig. 4.7 show that the transistor will enter the saturation region when V_{GS} is more than 0.8V, and I_d will rapidly increase when V_{GS} is more than 0.4V. In order to prevent excessive power consumption, the smaller I_d will be choose in this study. Fig. 4.8 show that there is a minimum of noise figure when V_{GS} is near 0.7V. Based on the above considerations, the final choice of the LNA transistor V_{GS} is 0.7V.

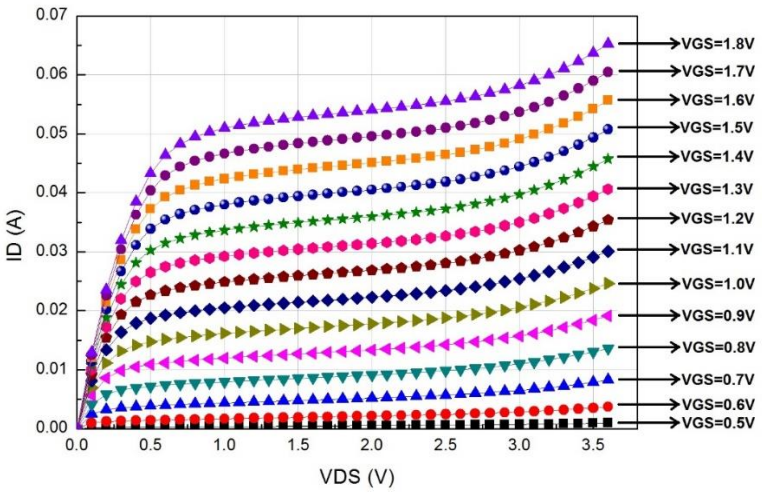


Fig. 4.6. Transistor dc I-V curve.

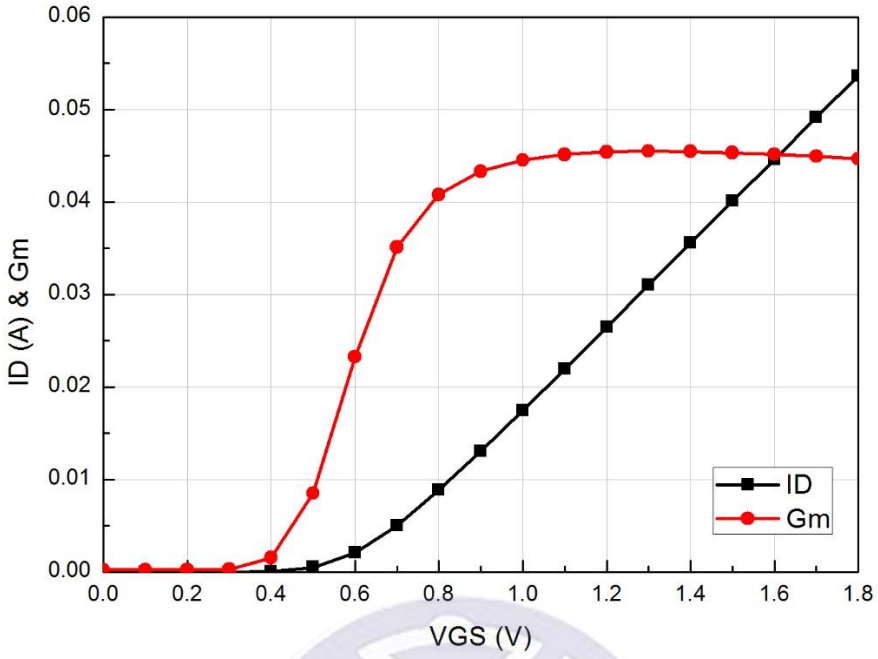


Fig. 4.7. Transistor g_m and I_d curve.

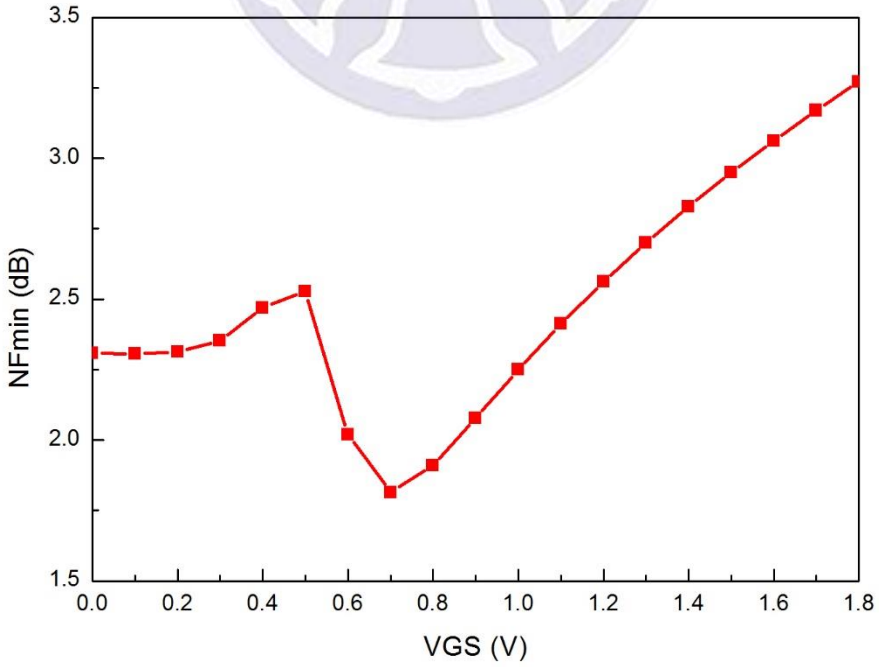


Fig. 4.8. Transistor minimum noise figure curve.

The second step is selected transistor size. Transistor has three optional parameters, they are channel length, channel width, and number of finger, respectively. However, the channel length of transistors are usually choice of the smallest value, which can reach a maximum value of transistors transduction. In TSMC 0.18μm CMOS process, the minimum value of channel length is 0.18μm, so the channel length is choose as 0.18μm.

The Maximum of gain (MAG) and minimum of noise figure (NF_{min}) under different channel length is show in Fig. 4.9 and Fig. 4.10, respectively. Fig. 4.9 show that the available maximum gain (MAG) increase with the transistor width, but when the channel width is greater than 5μm, the increase rate of gain become smaller. Therefore, the channel length will design near 5μm. Fig. 4.10 show that when number of finger become larger, the minimum noise figure and power consumption will increases. After consideration of the above conditions, select the channel width of 5μm, the number of finger with 10 as common-source transistor size.

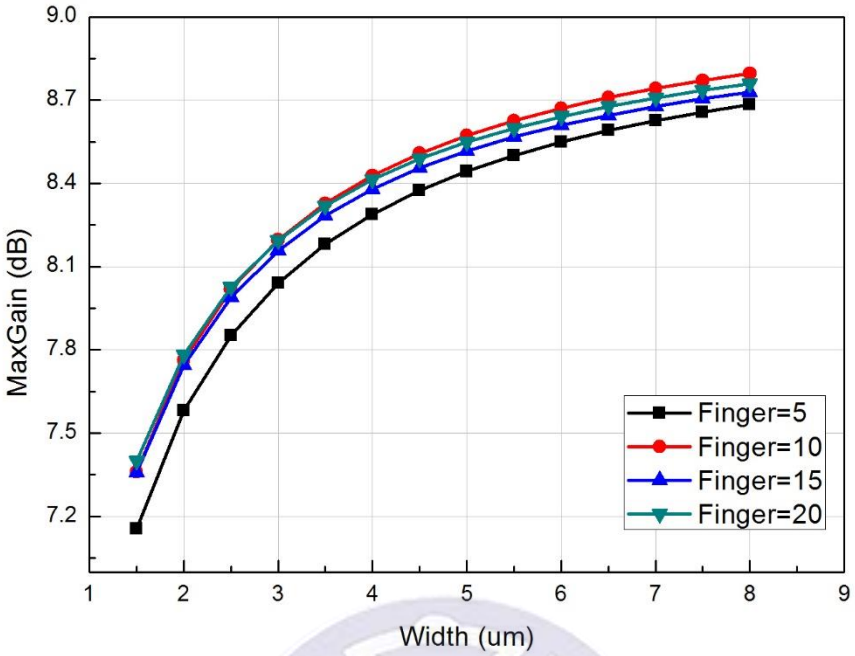


Fig. 4.9. MAG in different channel width and number of finger.

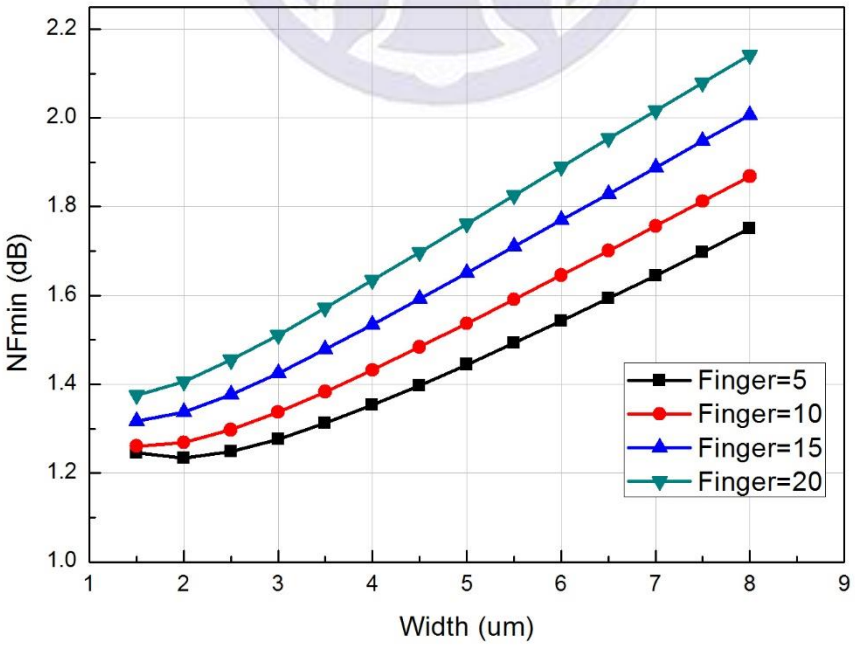


Fig. 4.10. NF_{min} in different channel width and number of finger.

4.4.2 Matching network design

After deciding the amplifier overall structure, followed by low noise amplifier matching network design. Matching network using inductors and capacitors to achieve.

Fig. 4.11 is the two-stage cascade low-noise amplifier matching network. Input matching is use the noise match, that noise figure can be minimized. Both of output matching and stage-to-stage matching are use the conjugate match, which can provide the greatest gain. In the low-noise amplifier matching network design, input noise matching network is the most important part of design. If design is not well, it would let the signals which transfer to the post-stage circuit have excessive noise and make signal distortion. Therefore, we prefer to design the input matching network, then design stage-to-stage matching and output matching, finally tuning the circuit.

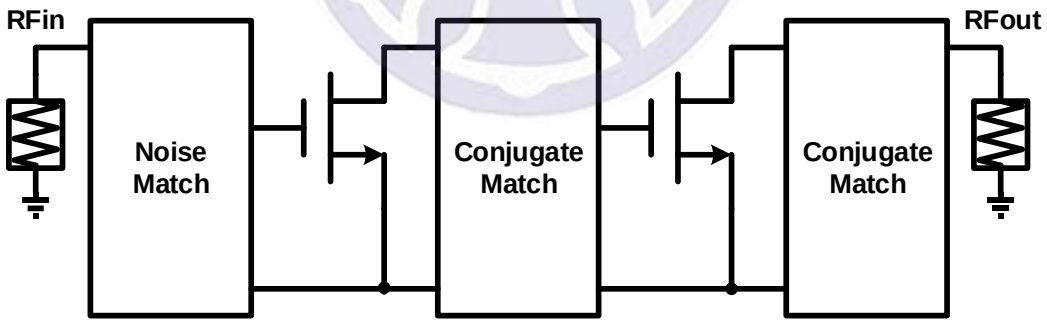


Fig. 4.11. Two-stage cascade low-noise amplifier matching network design.

1. Input noise matching

To achieve noise matching, the first step is to find the noise circle and

NF_{min} can be found in the noise circle. Then design the input matching network let the input impedance of 50Ω matched to NF_{min} point. First stage noise matching design circuit is show in Fig. 4.12. It is using source degeneration inductance and series a gate inductance to achieve input noise match.

Fig. 4.13 is the simulation of input noise circle. The lowest noise can available at NF_{min} impedance point. The step size of noise circle is 0.25dB every lap. In order to let the amplifier get the lowest noise, input port of 50Ω need to reach NF_{min} impedance point through the matching network design. The matching network locus plot can be seen from Fig. 4.13. First, source degeneration inductor would let input impedance increase, make the input impedance conjugate point closer to the NF_{min} point, then series a gate inductor. Therefore, that could be able to reach a conjugate match and noise match at the same time, then send the signal to the next stage with low-noise and high-gain.

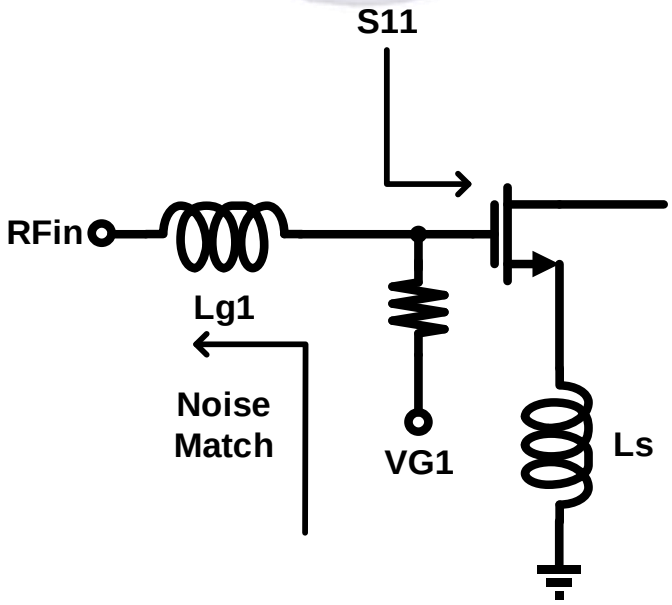


Fig. 4.12. First stage noise matching design circuit.

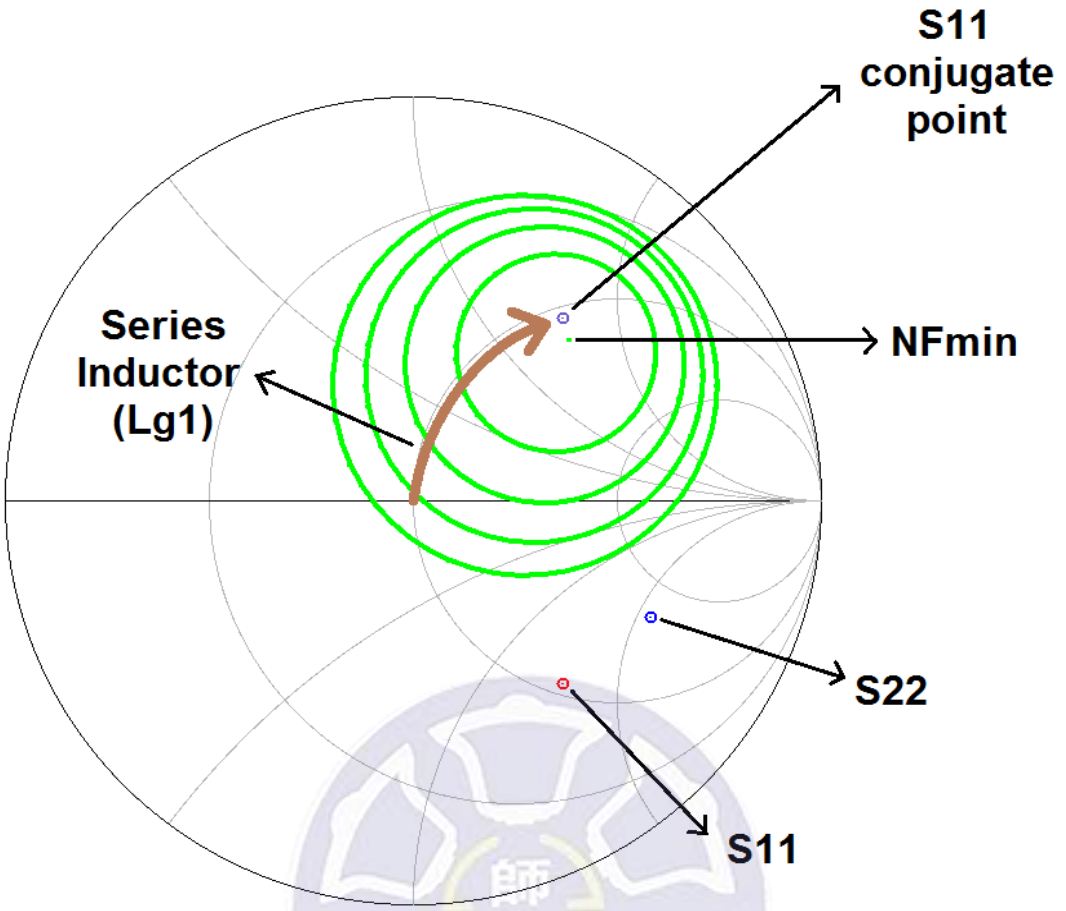


Fig. 4.13. Input noise match locus plot.

2. First stage and second stage matching

After design the input matching circuit, the first stage and second stage matching would use conjugate match. First, find the first-stage common-source amplifier output impedance point (S_{22}), and then find the second stage common-source amplifier input impedance point (S_{11}). The goal is matching the first-stage common-source amplifier output impedance point (S_{22}) to the second stage common-source amplifier input impedance conjugate point ($S_{11}*$). In this study, using a T-model design in Fig. 4.14, which contains two series inductor and a shunt inductor. Fig. 4.15 is

matching locus smith chart. Then we can complete the stage-to-stage conjugate match.

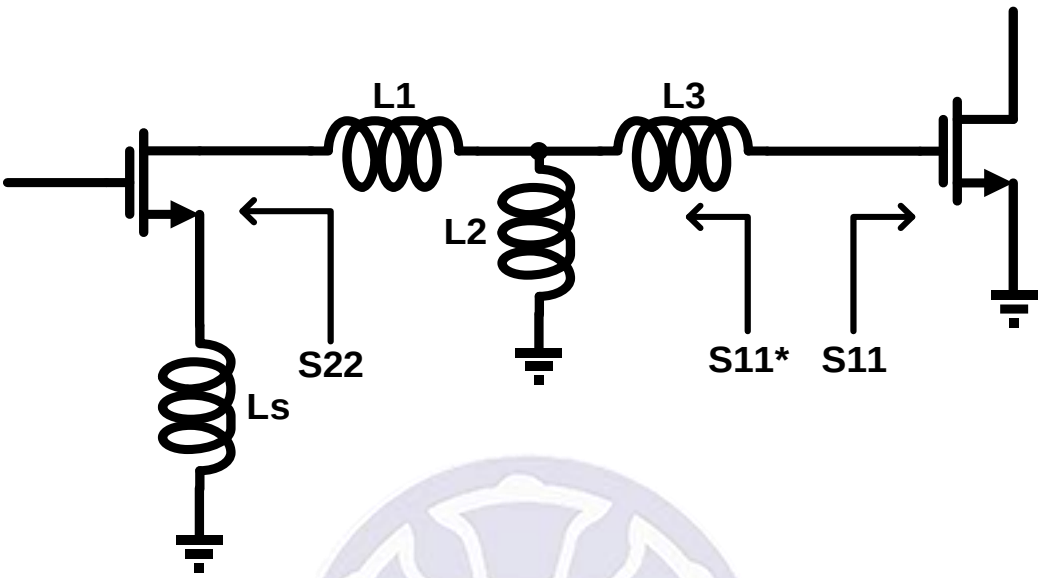


Fig. 4.14. Stage-to-stage matching circuit.

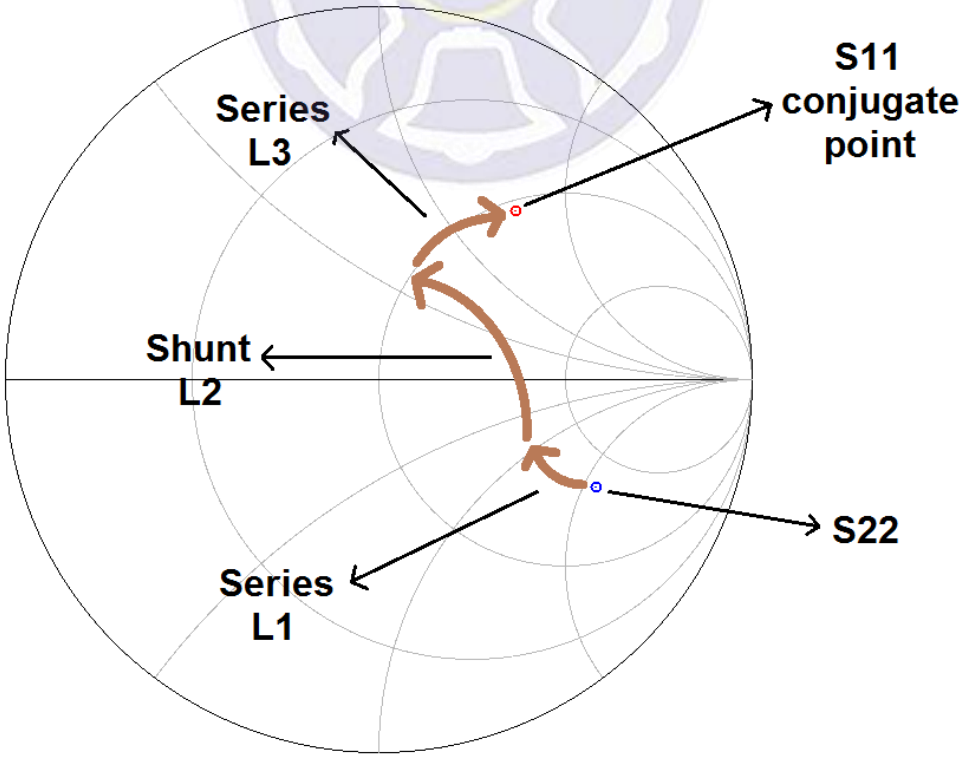


Fig. 4.15. Stage-to-stage matching locus plot.

3. Output conjugate matching

Final is the output matching design. Output stage will use conjugate match to reach the maximum gain. Fig. 4.16 show that to find the second stage output impedance point (S_{22}), and matching the 50Ω output impedance to the second stage output impedance point (S_{22}), then finished the output matching.

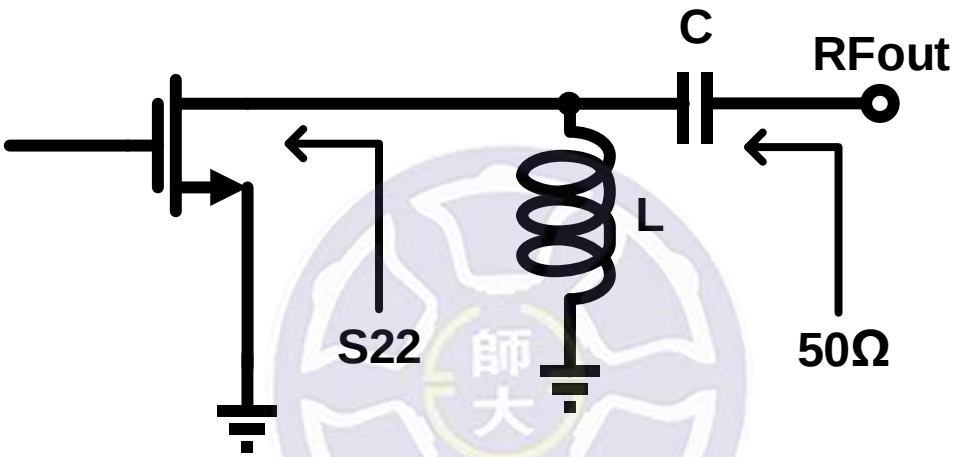


Fig. 4.16. Output matching circuit.

4.5 Simulation Result

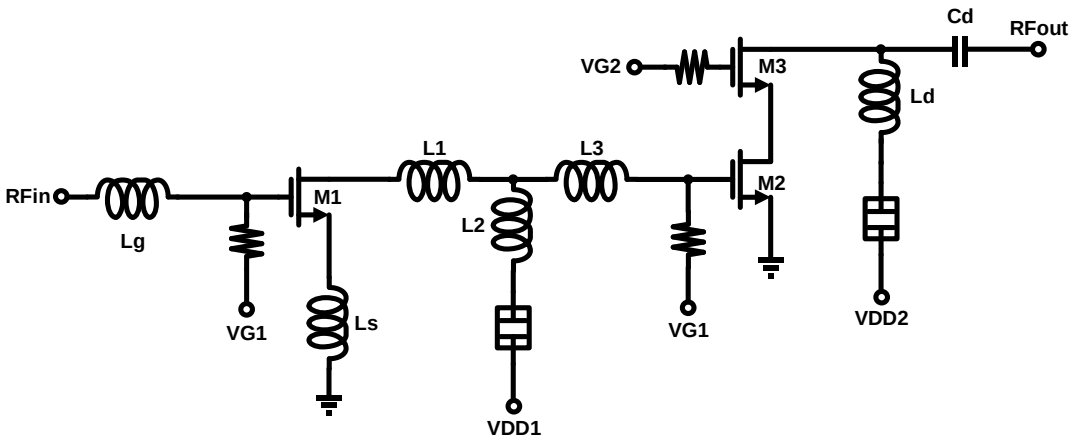


Fig. 4.17. K/Ka band low noise amplifier overall architecture figure.

The low-noise amplifier in this study is using 0.18um CMOS process, the overall circuit architecture shown in Fig. 4.17. Simulation of small-signal S-parameters and noise figure is using Agilent ADS (Advanced Design System). All passive components in the architecture such as transmission lines, inductors, and capacitors are using EM electromagnetic simulation software (HFSS) to complete full-wave electromagnetic simulation, and analysis all simulated results by ADS. The parameters of the components is show in Table 4.1.

Table 4.1

K/Ka-band low-noise amplifier components parameters

Device	Value	Device	Value
M1	**5um / 0.18um**	**Input-stage Lg**	**529.8 pH**
M2	**5um / 0.18um**	**Input-stage Ls**	**220 pH**
M3	**5um / 0.18um**	**Inter-stage L1**	**291.2 pH**
Output-stage Ld	**755.5 pH**	**Inter-stage L2**	**329.0 pH**
Output-stage Cd	**27.6 fF**	**Inter-stage L3**	**238.3 pH**

Fig. 4.18 is the S-parameter simulation result. Small-signal gain (S21) at 24GHz is about 18dB. Input return loss (S11) is greater than 15dB. Output return loss (S22) is greater than 25dB. Fig. 4.19 is the simulation of noise figure, and noise figure is about 3.5dB at 24GHz. Fig. 4.20 is the layout diagram of the chip.

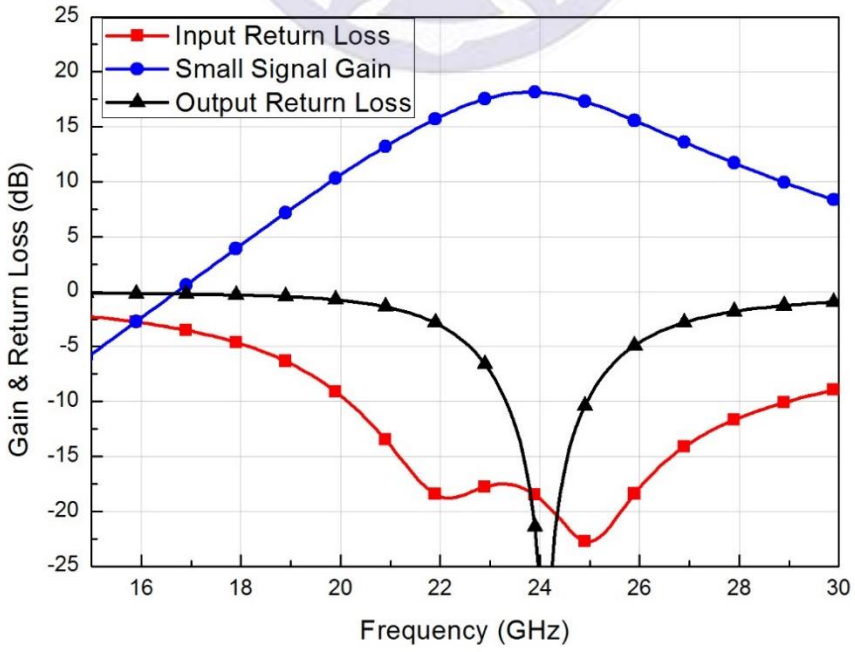


Fig. 4.18. Low-noise amplifier S-parameters simulation result.

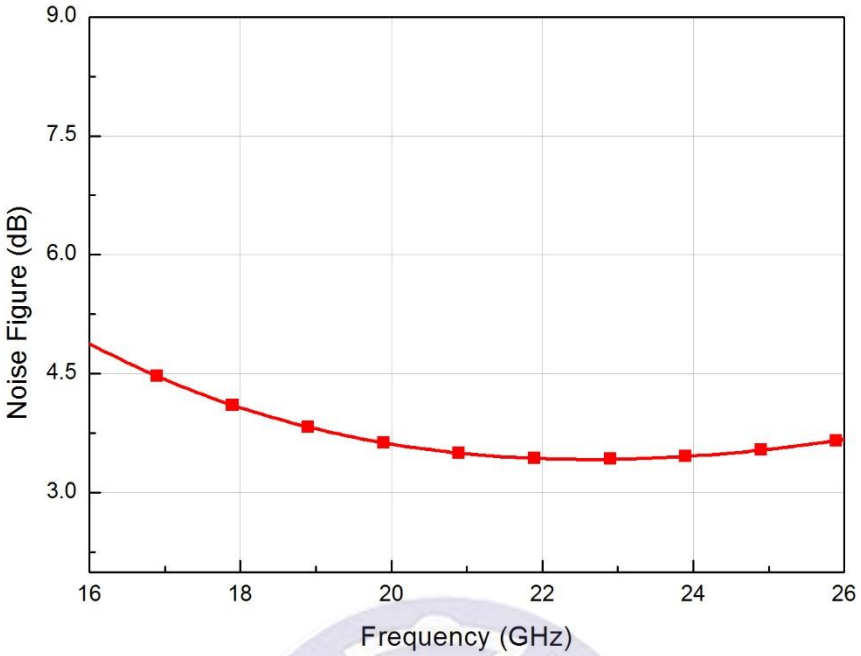


Fig. 4.19. Low-noise amplifier noise figure simulation result.

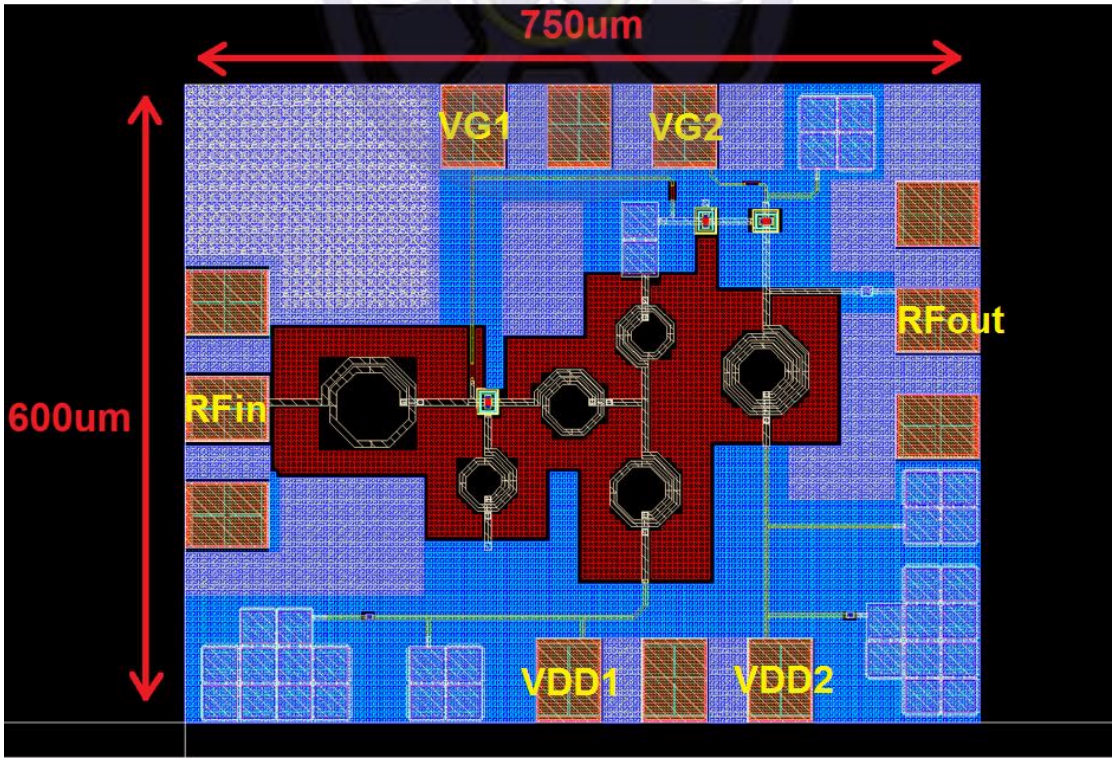


Fig. 4.20. Layout top view of low-noise amplifier.

4.6 Measurement results

Fig. 4.21 is chip micrograph of K/Ka-band low-noise amplifier. Layout area is 0.75mm × 0.60mm. Chip measurement methods using on wafer measurement mode.

The high-frequency signal input and output terminals using GSG RF probe measurements. DC supply voltage using a power supply, S-parameter using a network analyzer to measure. Noise figure using noise analyzer measurements.

Fig. 4.22 is the low-noise amplifier S-parameter measurement value, the small signal gain at 21GHz is maximum about 9.46dB. Fig. 4.23 is the low-noise amplifier noise figure, value of noise figure between 16.5-26.5 GHz is less than 10dB, and has minimum about 7dB at 21GHz.

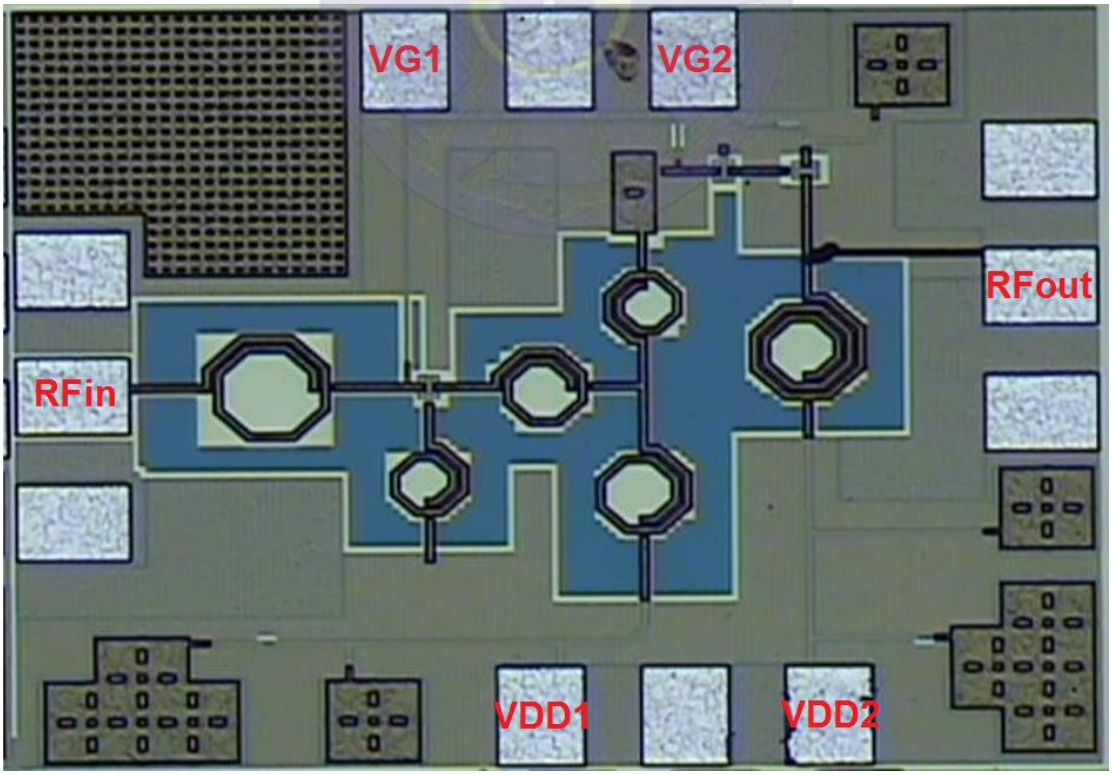


Fig. 4.21. Chip micrograph of low-noise amplifier.

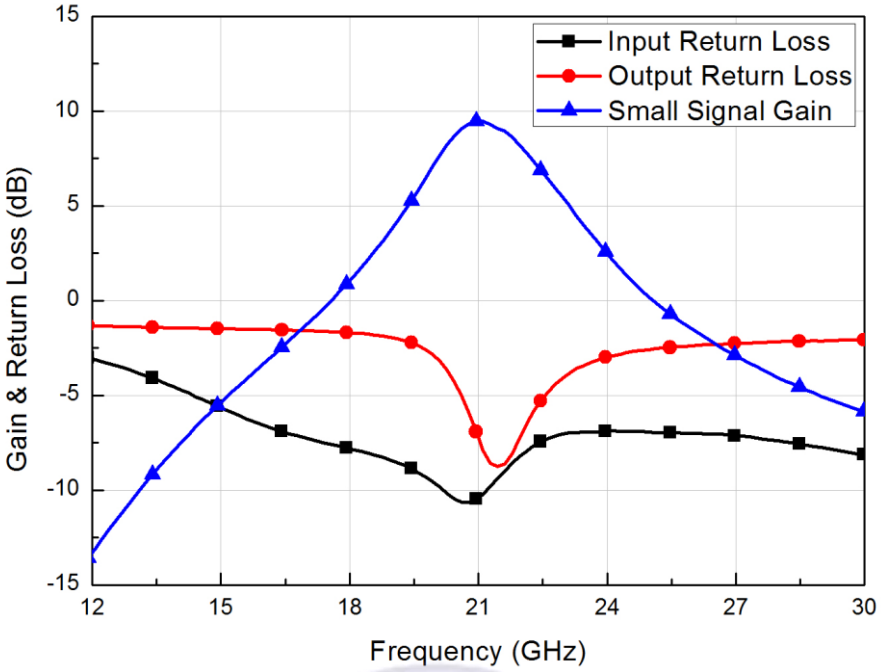


Fig. 4.22. Gain and return loss of the low-noise amplifier.

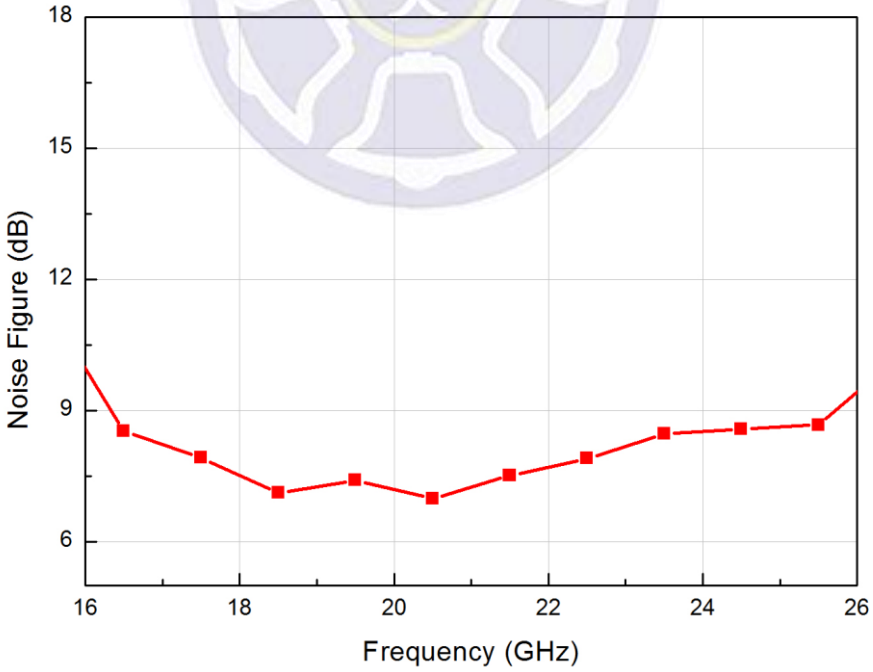


Fig. 4.23. Noise figure of low-noise amplifier.

4.7 ESD protection device equipped with LNA

To test the ESD protection ability of the ESD protection device, we also fabricated other three LNA equipped with different kinds of ESD protection device. Fig. 4.24-4.29 are LNA layout diagram and chip micrograph which equipped LASCR, dual diode, and DTSCR, respectively. Fig. 4.30 show that gain of the LNA. Through the figure can be seen LNA without equipped ESD protection device can't bear 0.5kV ESD HBM test.

At 21GHz, dual diodes_LNA has maximum gain about 11.27dB, DTSCR_LNA has maximum gain about 12.09dB, and LASCR_LNA has maximum gain about 11.61dB, respectively.

Dual diodes_LNA equipped with a N+/PW diode (DN30) and a P+/NW (DP30) diode. Both of the diode width is 30μm. Fig. 4.31-4.33 show that comparison of gain, S_{11}, S_{22} before and after HBM test, respectively. Dual diodes_LNA has gain of 11.07dB after 1.5kV HBM test and 2.90dB after 2kV HBM test at 21GHz, respectively.

DTSCR_LNA equipped with a SCR and series three diodes. Width of the SCR and diodes are 30um and 15um, respectively. Fig. 4.34-4.36 show that comparison of gain, S_{11}, S_{22} before and after HBM test, respectively. DTSCR_LNA has gain of 12.13dB after 2kV HBM test and 0.05dB after 3kV HBM test at 21GHz, respectively.

LASCR_LNA equipped with a SCR, an inductance, and series three diodes. Width of the SCR and diodes are 30um and 15um, respectively. The value of inductance is 460pH. Fig. 4.37-4.39 show that comparison of gain, S_{11}, S_{22} before and after HBM test, respectively. LASCR_LNA has gain of 11.3dB after 4kV HBM test and 9.22dB after 5kV HBM test at 21GHz, respectively.

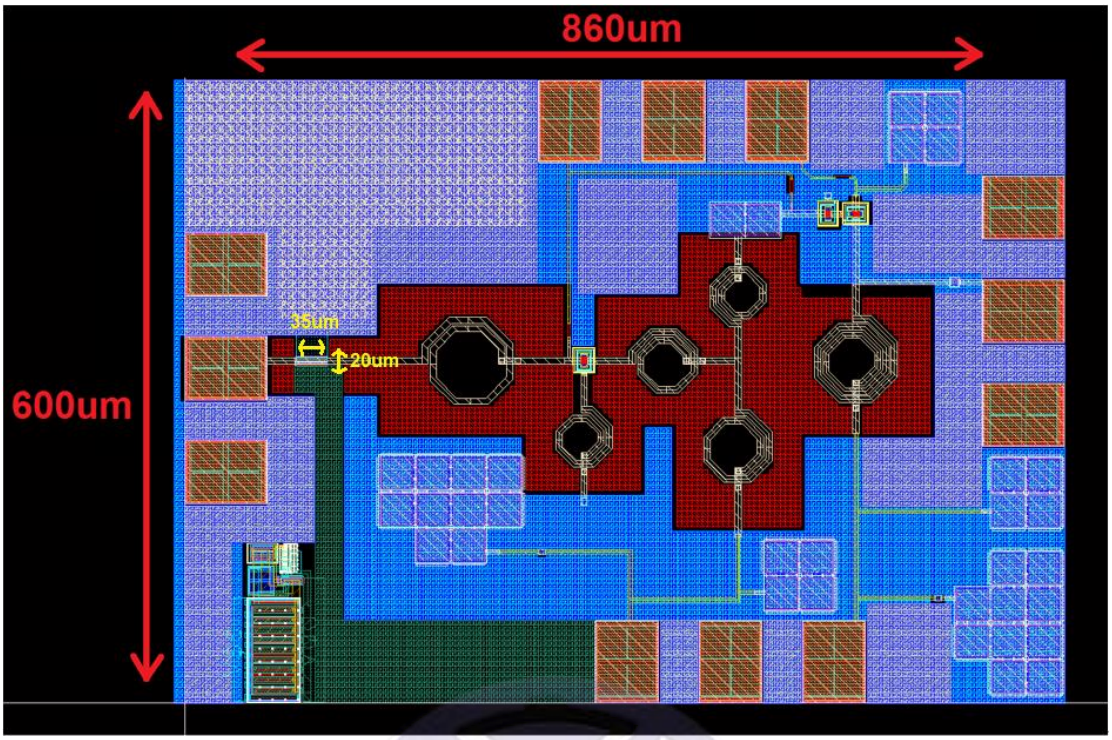


Fig. 4.24. Layout top view of LNA equipped dual diode.

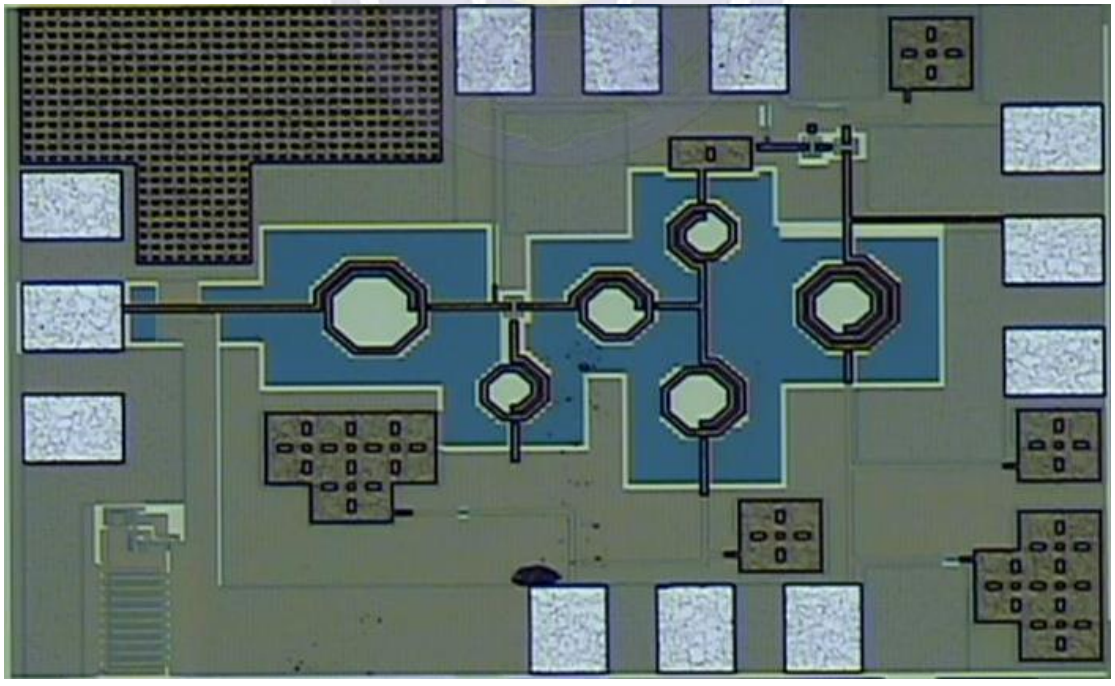


Fig. 4.25. Chip micrograph LNA with dual diode.

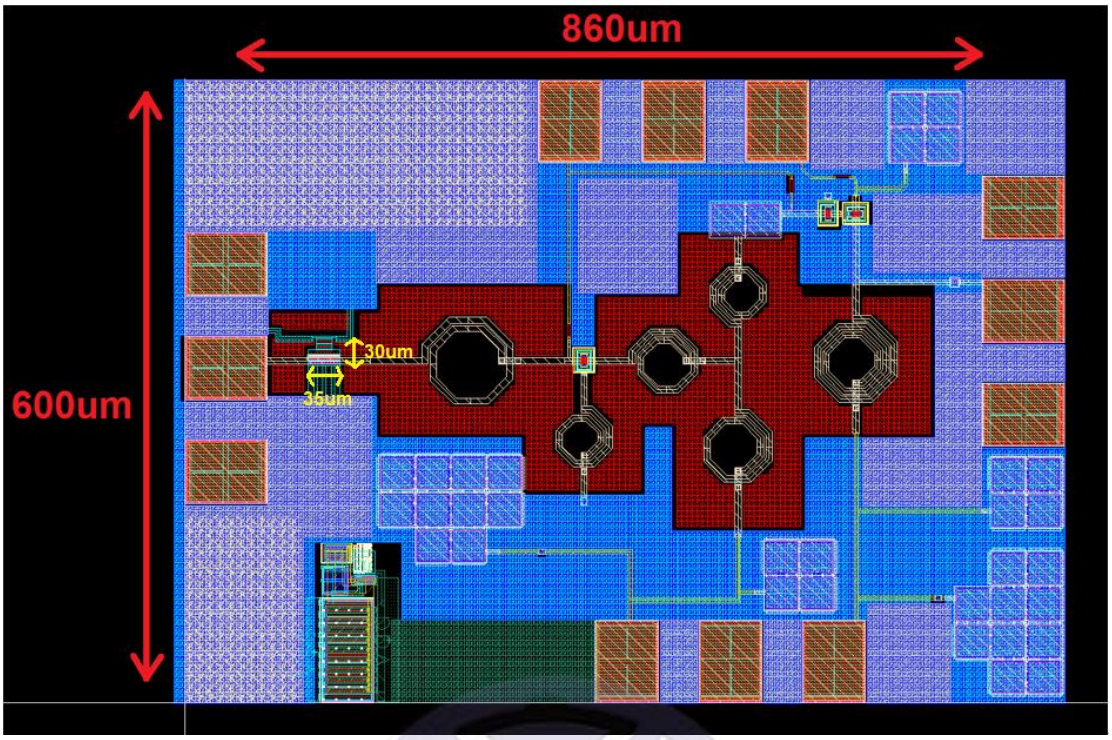


Fig. 4.26. Low-noise amplifier equipped DTSCR layout top view.

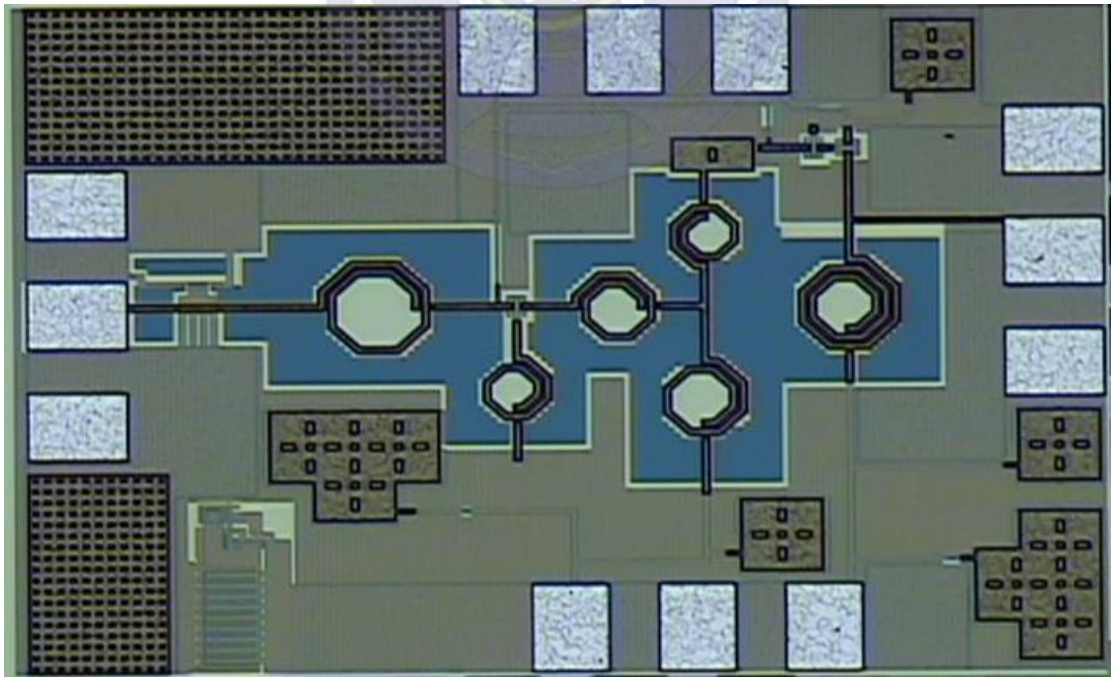


Fig. 4.27. Low-noise amplifier with DTSCR chip micrograph.

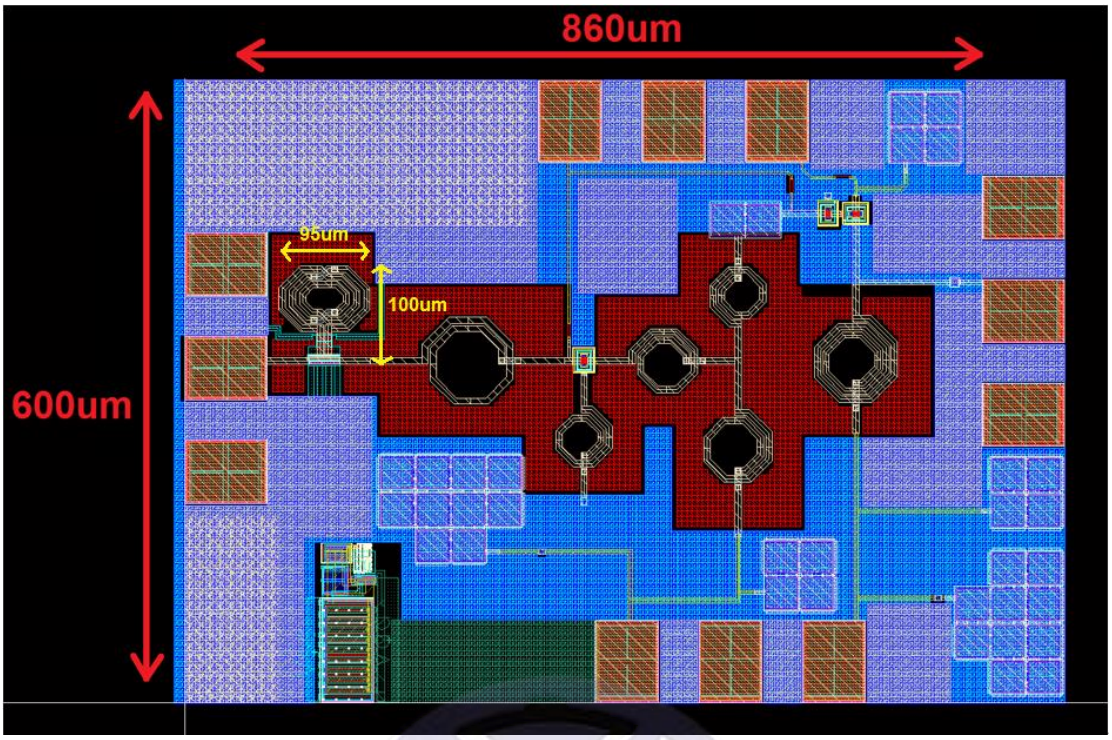


Fig. 4.28. Low-noise amplifier equipped LASCR layout top view.

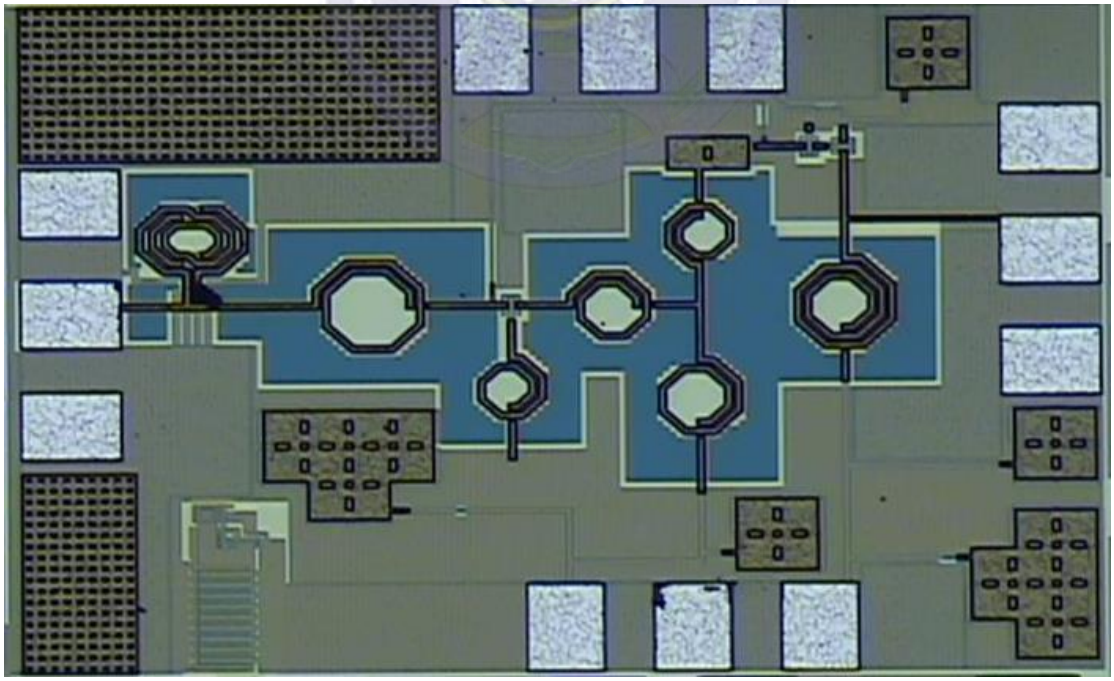


Fig. 4.29. Low-noise amplifier with LASCR chip micrograph.

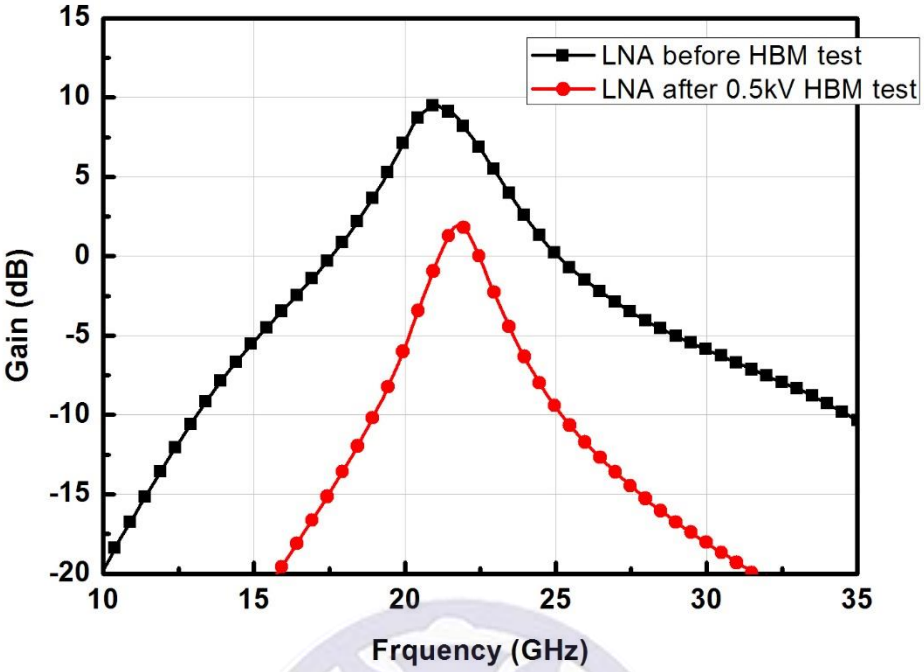


Fig. 4.30. Gain of the LNA before and after HBM ESD test.

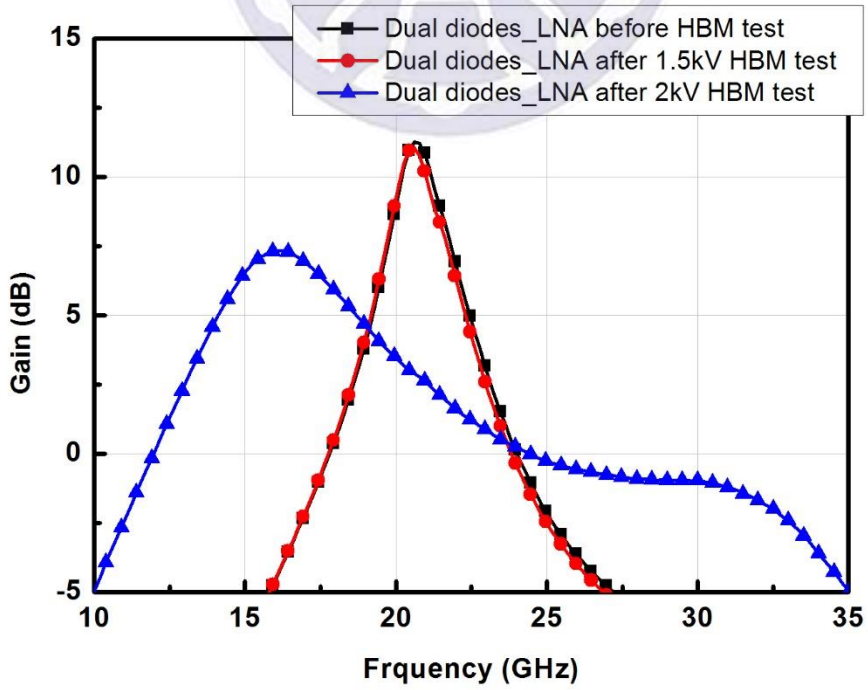


Fig. 4.31. Gain of the dual diodes_LNA before and after HBM ESD test.

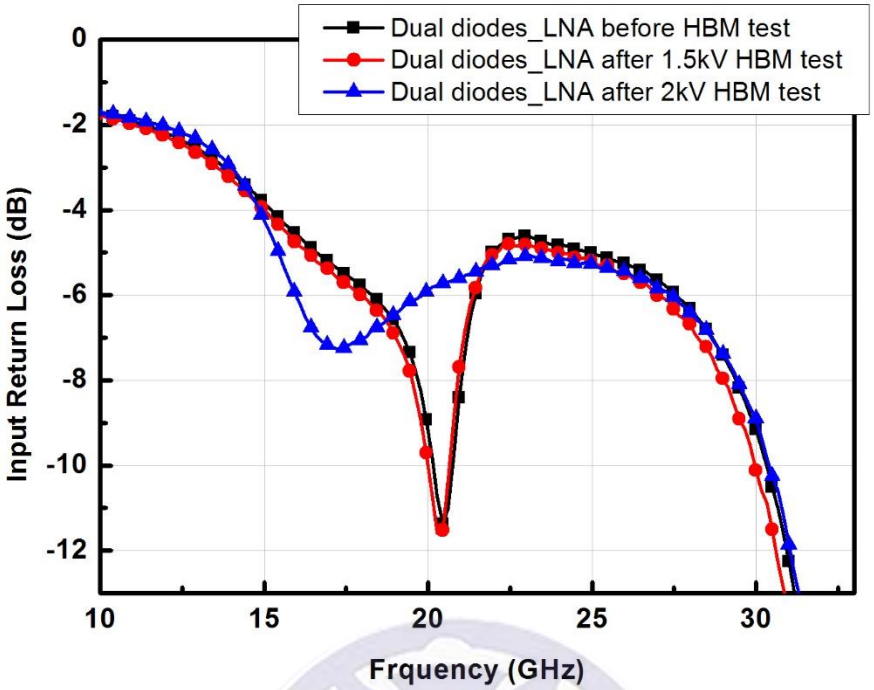


Fig. 4.32. S_{11} of the dual diodes_LNA before and after HBM ESD test.

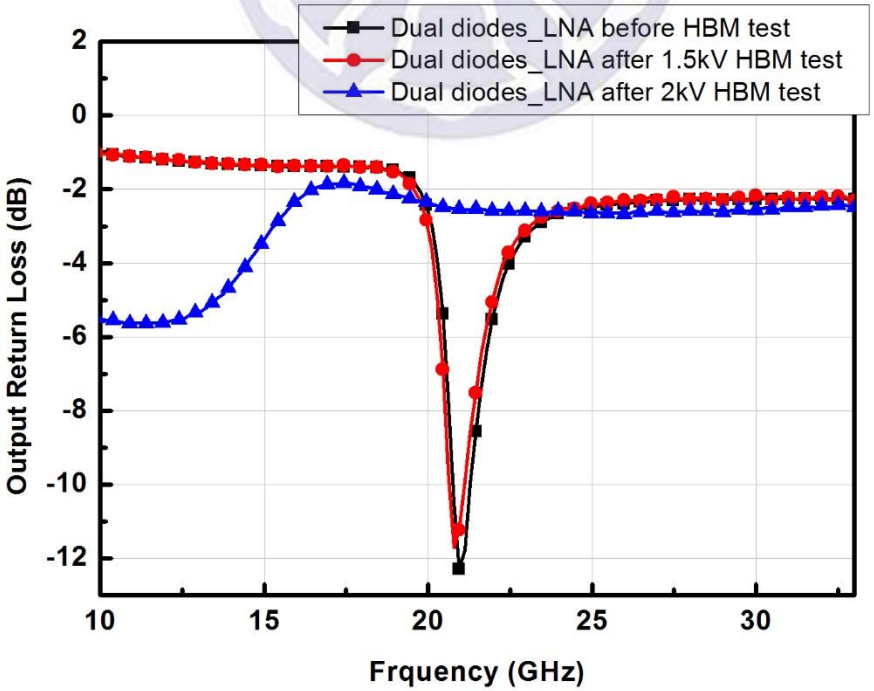


Fig. 4.33. S_{22} of the dual diodes_LNA before and after HBM ESD test.

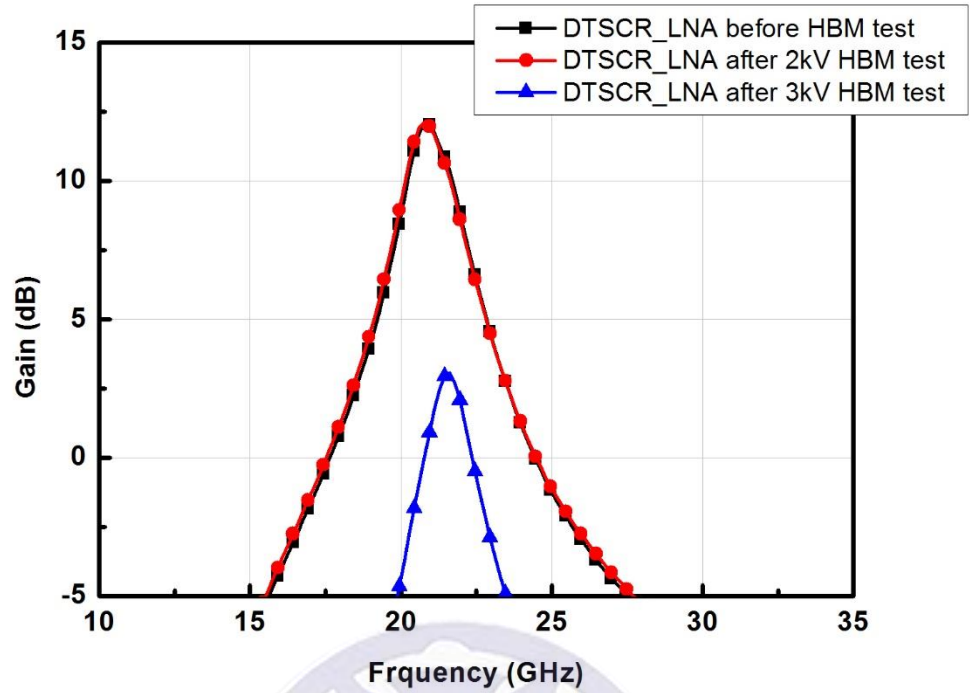


Fig. 4.34. Gain of the DTSCR_LNA before and after HBM ESD test.

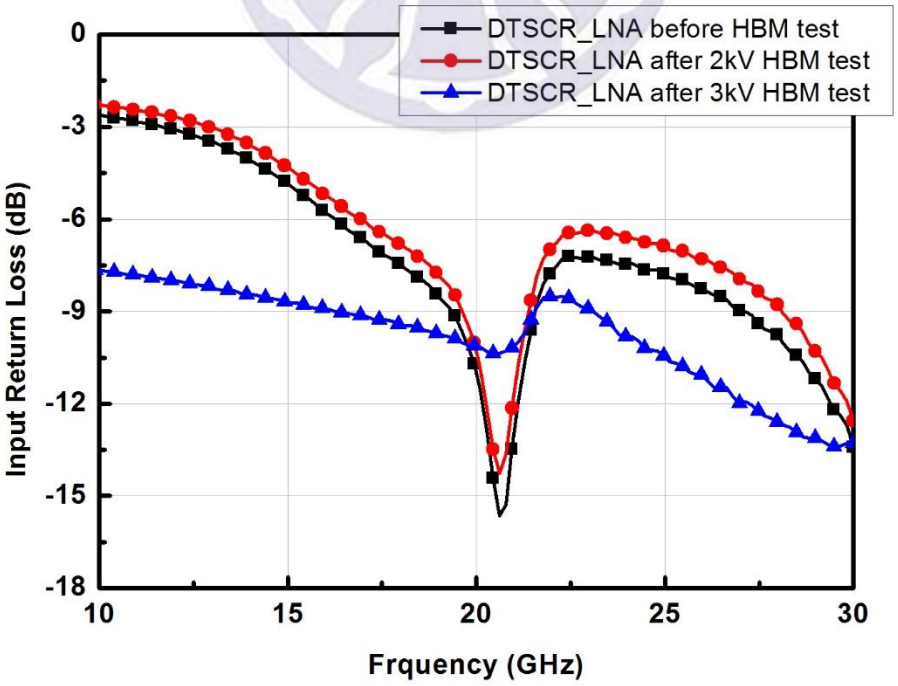


Fig. 4.35. S_{11} of the DTSCR_LNA before and after HBM ESD test.

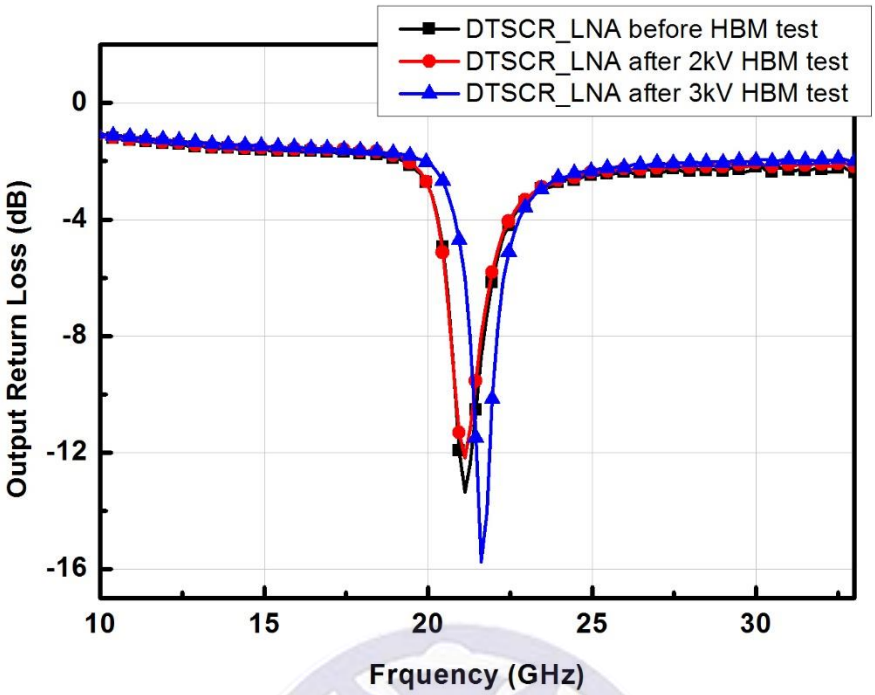


Fig. 4.36. S_{22} of the DTSCR_LNA before and after HBM ESD test.

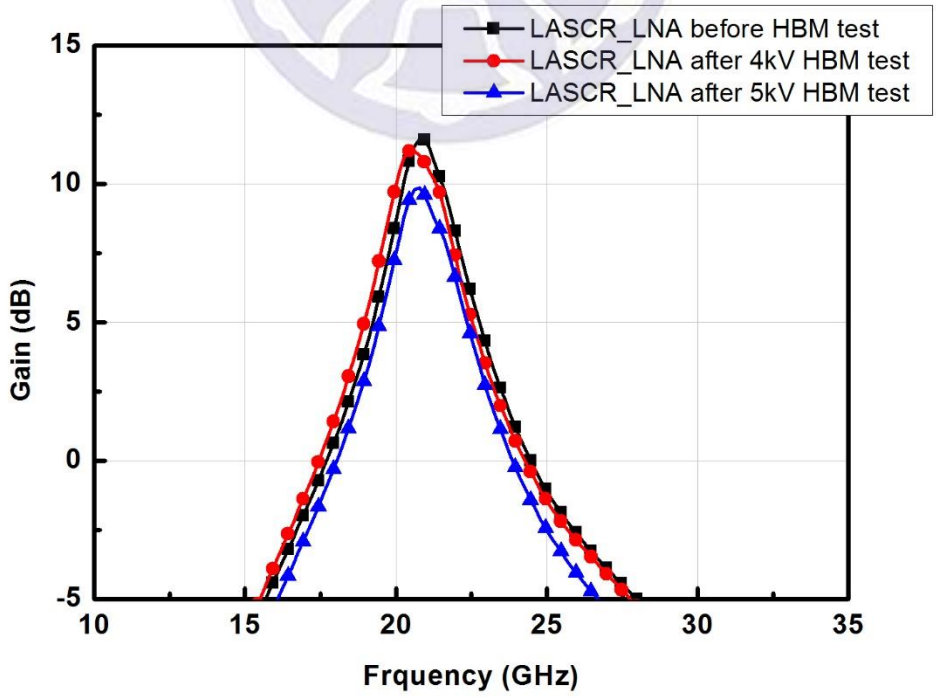


Fig. 4.37. Gain of the LASCR_LNA before and after HBM ESD test.

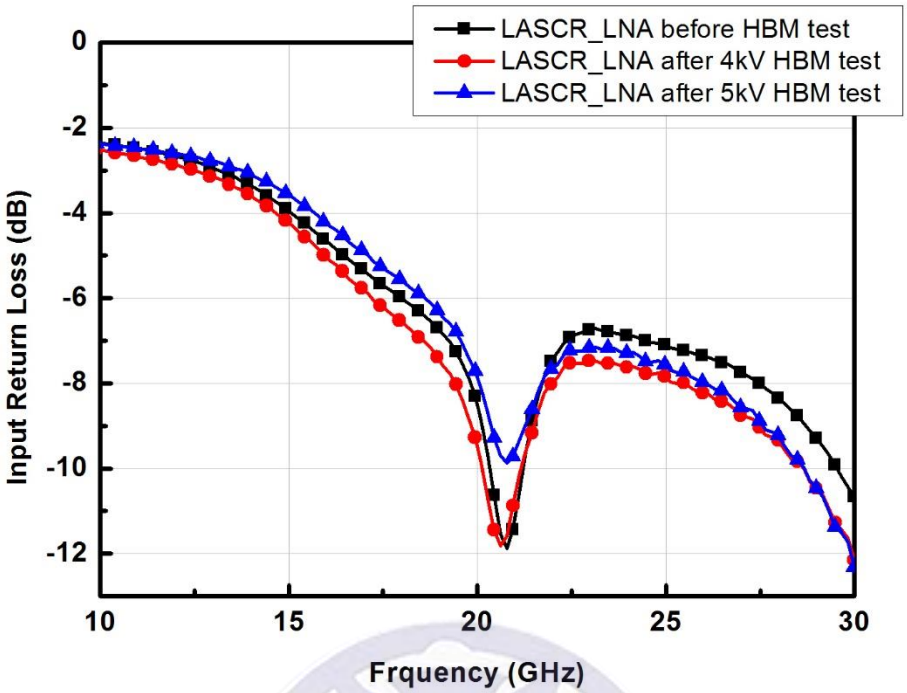


Fig. 4.38. S_{11} of the LASCR_LNA before and after HBM ESD test.

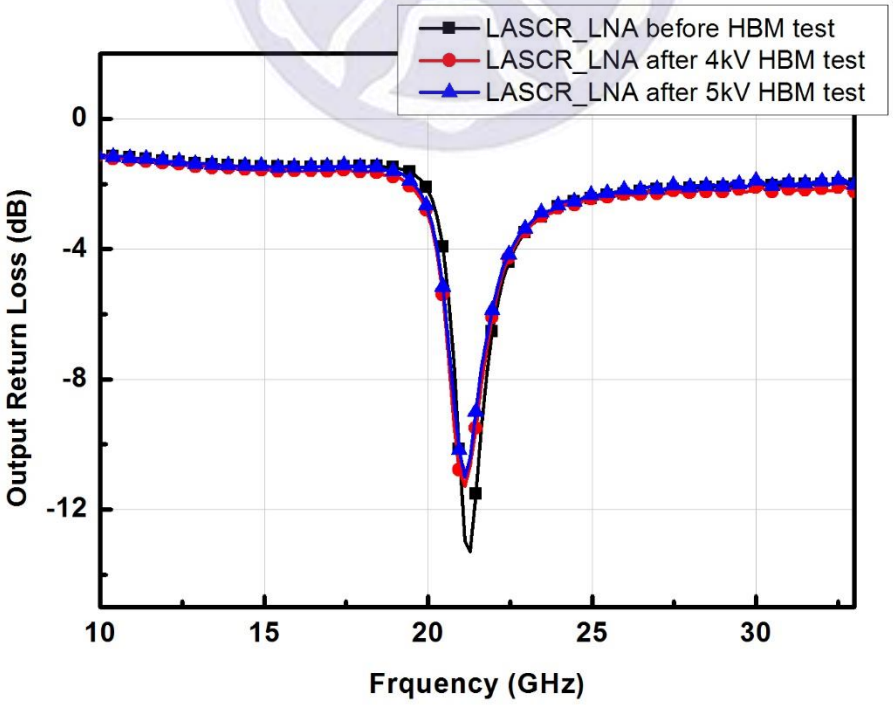


Fig. 4.39. S_{22} of the LASCR_LNA before and after HBM ESD test.

4.8 Discussion

In order to investigate the relationship between the components, frequency, and gain, we re-simulate the LNA with precise parameter to meet the measurement result. Fig. 4.40 shows the low noise amplifier architecture with parasitic capacitance and resistance. The measurement results of this study didn't fit the simulation results might be caused by components parasitic effect. To find out the parasitic component values, we do the simulation of LNA again. Simulation of S-parameters are shown in Fig. 4.41. Table 4.2 also shows the components parameters of parasitic capacitance and resistance. The main reason of the operating frequency change is caused by the output-stage parasitic capacitance (C_{Ld}). Small signal gain is mainly affected by inter-stage capacitance resistances (R2 and R3) and output-stage capacitance resistances (R4 and R5).

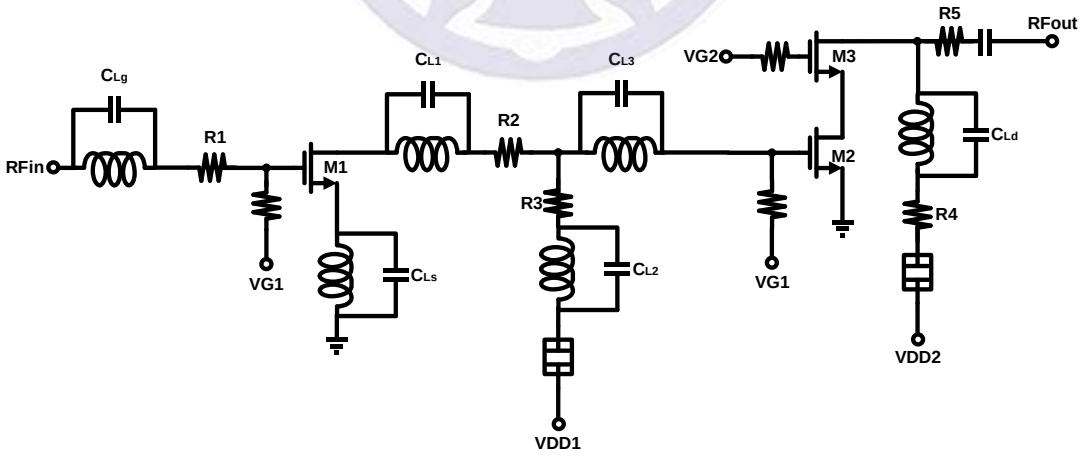


Fig. 4.40. K/Ka-band low noise amplifier architecture with parasitic capacitance and resistance.

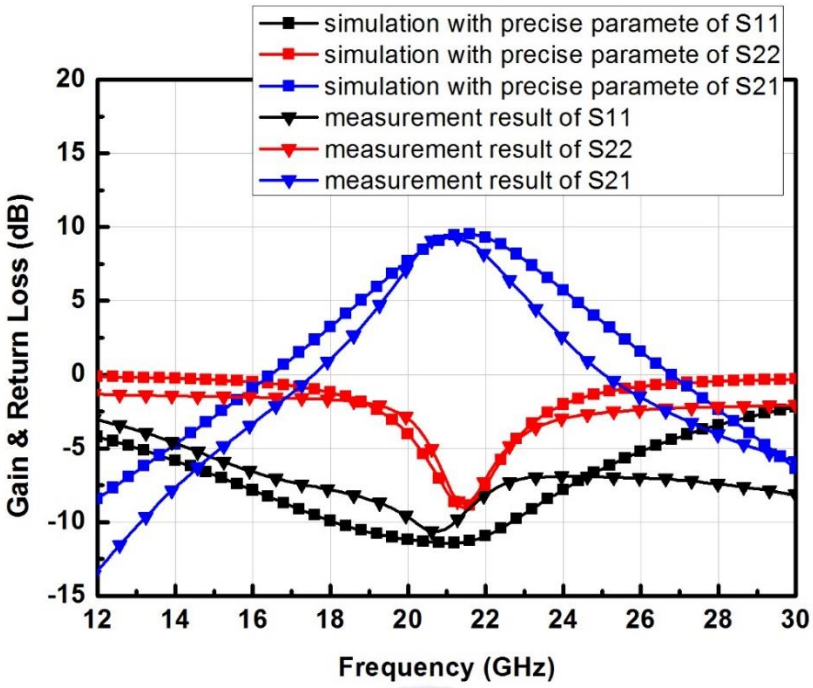


Fig. 4.41. Simulation with precise parameter and measurement result of LNA.

Table 4.2

Low-noise amplifier components parameters of parasitic capacitance and resistance

Device	Value	Device	Value
C_{Lg}	20 fF	R1	15 Ω
C_{Ls}	60 fF	R2	15 Ω
C_{L1}	15 fF	R3	100 Ω
C_{L2}	50 fF	R4	7.5 Ω
C_{L3}	20 fF	R5	0.5 Ω
C_{Ld}	17 fF		

4.9 Conclusion

This study is using 0.18μm CMOS process to complete the design of K/Ka band low-noise amplifier. Overall circuit architecture is using a two-stage common-source cascade design to achieve the low–voltage and low-noise demand. Input stage uses the source degeneration inductance and gate inductance to achieve conjugate matching and noise matching at the same time. Stage-to-stage matching using the T-model inductance to achieved conjugate matching. Output matching uses series inductors and capacitors to achieve conjugate matching. This low-noise amplifier has a maximum gain 9.46dB at 21GHz, the minimum noise figure of 7dB, layout area is 0.75mm × 0.60mm. After adding the ESD protection device of dual diode, low-noise amplifier can bear 1.5kV HBM test, and maximum gain is 11.07dB at 21GHz. DTSCR_LNA can bear 2kV HBM test, and maximum gain is 12.13dB at 21GHz. LASCR_LAN can bear 4kV HBM test, and maximum gain is 11.3dB at 21GHz. Table. 4.3 summarizes out the HBM ESD robustness of each LNA.

Table. 4.3

HBM ESD robustness of LNA

Cell Name	HBM ESD Robustness
LNA	**0kV**
Dual diode LNA	**1.5kV**
DTSCR_LNA	**2kV**
LASCR_LNA	**4kV**

Chapter 5

Conclusions and Future Works

This chapter summarizes the main results and contributions of this study. Future works of the inductor-assisted silicon-controlled rectifier for ESD protection design in CMOS process are also provided in the chapter.

5.1 Main Contributions of This Study

In this study, a kind of ESD protection device has been developed in nanoscale CMOS technology for RF ESD protection design. Each of the test devices and low-noise amplifier has been successfully verified in the test chip.

In Chapter 2, some ESD protection devices such as diode and SCR has been introduces. This chapter also show that four discharge path when circuits are stress by ESD.

In Chapter 3, LASCR's architecture and design process is described in detail. Verified in silicon chip, LASCR devices with 30um (LASCR_W30_3D and LASCR_W30_5D) and 60um (LASCR_W60_3D and LASCR_W60_5D) width can pass 4kV and 7.5kV HBM ESD tests, respectively, and they have the loss lower than 3dB in K/Ka-band. All devices in this chapter are fabricated by 0.18um CMOS process.

In Chapter 4, design of low-noise amplifier has been described in this chapter. It also contains some important parameters and design considerations of LNA. This chapter also introduced the low-noise amplifier design procedure, few kinds of ESD protection devices are co-design with the LNA. All low-noise

amplifier in this chapter is fabricated in 0.18um CMOS process, and the small-signal gain of the stand-alone LNA circuit has maximum 9.46dB at 21GHz and minimum noise figure at 21GHz for 7dB. After Inductor-Assisted Silicon-Controlled Rectifier (LASCR) has been equipped, the circuit can bear 4kV HBM test. The small-signal gain at 21GHz has maximum of 11.3dB.

The circuit ESD protection function can be achieved without degrade the low-noise amplifier performance, and also can reach 4kV HBM test.

5.2 Future Works

With the continuously scaling CMOS technology, the gate oxide becomes much thinner. ESD become one of the most important reliability issues during mass production, must be taken into consideration. Therefore, all integrated circuits used in the wireless communication products need to be equipped with ESD protection designs. However, ESD protections cause radio-frequency (RF) performance degradation with several undesired effects, such as degrade the small-signal gain of the circuit or takes up too much layout area. Inductor-Assisted Silicon-Controlled Rectifier (LASCR) of this study will be able to overcome these drawbacks. LASCR devices exhibit good high-frequency performance between 0~35GHz, so they can be used for wideband or high-speed applications without degrading the performance of circuit.

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自　　傳

研究生張榮堃，生於台中市，家中父母關係良好，一家和樂，雖然國高中階段的求學路程並非順利，所幸最後進入國立台灣師範大學應用電子科技學系就讀。然而大學期間還在摸索未來的定位，以致於成績並非理想，在大三的專題課程選擇了晶片設計的方向，意外的發現對此頗感興趣。研究所階段幸運的考取國立台灣師範大學電機工程學系，繼續選擇晶片設計這方向深造，雖然學習能力並不是頂尖，但也很願意去了解所有相關知識，也喜歡和同學們互相交換想法和意見。感謝老師的提拔，未來將會繼續深造，願能用己微薄之力為人類社會創造更好的未來。

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