國立臺灣師範大學電機工程學系

碩士論文

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射頻功率放大器之靜電放電防護設計

On-Chip ESD Protection Design for Radio-Frequency Power Amplifier

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摘要

本論文旨在利用嵌入矽控整流器之串接二極體來完成大訊號擺幅功率放大器的靜電放電防護設計，為了比較所提出的靜電放電防護電路的優劣性，也設計了串接二極體以及二極體觸發矽控整流器兩種靜電放電防護電路來提供比較。

為了驗證所提出的靜電放電防護電路在實際電路上的效能，本論文也設計了一個功率放大器電路來搭配此次所設計的三種靜電放電防護電路。實驗結果顯示，嵌入矽控整流器之串接二極體不會造成訊號的衰減及失真，且能夠有效的保護功率放大器。

在本論文中所設計的電路皆使用0.18-μm CMOS製程完成。並在實際的量測中發現，搭配串接二極體寄生矽控整流器的功率放大器電路能承受7 kV以上人體放電模式之靜電放電測試。

關鍵字：靜電放電防護、矽控整流器、串接二極體、射頻功率放大器

On-Chip ESD Protection Design for Radio-Frequency Power Amplifier

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Abstract

In this thesis, the diode string with embedded silicon-controlled rectifier (DSSCR) is designed to provide electrostatic discharge (ESD) protection of radio-frequency (RF) power amplifiers (PAs). To examine and evaluate the performance of the DSSCR, ESD protection circuits using the diode string (DS) and the diode-triggered SCR (DTSCR) are also designed and implemented for comparison with the proposed DSSCR protection circuit.

To validate the effectiveness of the designed ESD protection circuits, radio-frequency power amplifiers which equipped with the above-mentioned ESD protection circuits were designed and fabricated in this research. The measured results show that the protection circuit using DSSCR will not cause undesired signal degradation and distortion, and meanwhile can offer instant and effective protection to the RF PAs.

All of the ESD protection circuits designed in this thesis were fabricated using 0.18-um CMOS process. It is found in measurement that the RF PA equipped with the

DSSCR protection circuit can bear 7-kV human-body-model (HBM) test.

Keywords: Electrostatic discharge protection, silicon-controlled rectifier, diode string, power amplifier

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動的場所，希望你也能緊接著快點畢業；感謝柏維陪我焊接 PCB 板，也都很自告奮勇的要幫忙跑模擬，而且時常都會主動拿東西過來討論，真的很認真，希望你之後跟玉瑄除了實驗室日常的互相陷害以外，也要同心協力把研究做好並把學弟妹帶好；感謝玉瑄總是很貼心的關心每個人，還要負責幫大家看英文，做事情都很細心，而且上課筆記都抄得很詳細，學妹很認真記得要好好帶人家；感謝鈺凱在實驗室的幫忙，不管是任何人問任何問題，你都當成是自己的事，就算自己不會也會找人幫忙，也幫我解決了很多問題，真的很感動，對於實驗室的貢獻相信是大家有目共睹的，希望你能順利畢業來新竹再一起住，還有很多有趣的事要一起完成；感謝俊宇都很認真積極的幫忙實驗室的事物，你自願主動幫忙的做海報、做名牌，在每個忙碌或是找不到人幫忙的時刻，總會第一個出現，也常帶好吃的東西分享給大家，希望你未來能夠成為一個好老師；感謝日彥在實驗室對學長姊都任勞任怨，尤其是陪學長買點心和看學長們的英文，總是很有禮貌的幫助大家，希望你跟義全都可以考到理想的研究所，當然直升也是很好的選擇；感謝義全平常對學長姐也都任勞任怨，只是不要一直拿世界上最難的問題問我，因為那問題難到只要花幾秒就可以解決了，記得研究要認真但是要找正確的方向前進，才會有更好的效果，加油!祝你考上理想的研究所；除了 407 的夥伴外，也要感謝暐辰陪我聊天了三年，還住我家附近，真的很有緣份，只不過之後和你要分隔兩地了，希望你在工研院能找到你想要的，然後記得要常連絡；感謝煒崴在這三年的陪伴，希望以後在新竹大家也都可以常保聯絡；感謝方儒、啟銘和東宏，雖然研究領域不一樣，但還是合得來聊天聊得很開心，希望畢業後也還能常保聯絡；感謝峻佑和冠汎，陪我走完碩班最後的尾巴，記得以後研究上要互相扶持、互相學習，對彼此都會是好事；特別感謝望龍學長在我碩一時教了我好多東西，使我開始有了方向；感謝佳龍提供給我非常多的建議，真的獲益良多，希望以後還能保持聯絡；在學校要感謝的人實在太多了，謝謝你們大家對我的包容和關心，碩

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Introduction

1.1 Literature Survey and Research Motivation

Nowadays, nanoscale complementary metal-oxide-semiconductor (CMOS) technology has been broadly used in implementation of radio-frequency (RF) circuits due to the merits of scaling-down size, improved high-frequency characteristics, high integration capability, and potential for mass production. However, since the nanoscale CMOS technology may seriously degrade the electrostatic discharge (ESD) robustness of the CMOS ICs due to the thinner gate oxide [1]-[3], ESD protection circuits have to be implemented at all input/output (I/O) pads in RF ICs to protect them from ESD damages. On the other hand, because ESD is one of the most important reliability issues to the CMOS IC manufacturing process, ESD protection should be considered carefully in the process. Also, due to the increasing reliability demand of the circuit systems, military electronics, aerospace technology, smart wearable devices, such as smart phones and smart watches, and so forth, are facing more reliability problems in circuit design. Especially, as stated above, when the circuit size continues to scale down and the oxide layer becomes thinner, electrostatic can cause significant damage to circuits, and this challenge the design of ESD protection nowadays.

ESD events usually occur in input and output (I/O) terminals of the circuits. Therefore, it is necessary to implement the ESD protection circuits in the I/O terminals. For the RF circuits, the input and output terminals are usually connected to the low-noise amplifier (LNA) and power amplifier (PA), respectively. In general, the ESD protection circuits located at I/O terminals would degrade the RF performance.

Thus, to meet a higher ESD robustness requirement without degrading the performance of the RF circuits is a difficult challenge.

Besides, since the silicon-controlled rectifier (SCR) device has the positive-feedback mechanism, it will be more conductive to release the ESD discharging current when the ESD stress is from anode to cathode of the SCR device. Conventionally, the low holding voltage of the SCR device may cause the circuits that are to be protected the problem of latch-up. However, in recent years, the supply voltage decreases with the progress of the process. This makes the SCR a potential device in the ESD protection design.

In the past, many ESD protection designs have been proposed for RF circuits. Among those, double-diode configuration is a conventional ESD protection design [4]-[5]. It has been widely used for gigahertz RF circuits since it can fit the typical specification of the parasitic capacitance and ESD robustness. For large-swing PA's ESD protection circuits, preventing output signal swing from distortion should be considered carefully. For such a case, instead of using double-diode ESD protection, the diode string (DS) may be adopted for ESD protection design. In addition, stacked diodes can prevent signals from distortion, but excessive number of stacked diodes may cause the voltage across the ESD protection circuit too large to damage the PN junction or the oxide layer of the internal circuits. Therefore, low-turn-on-resistance ESD protection devices are preferred in order to produce less voltage across them.

In this work, the ESD protection design of large-signal-swing power amplifier will be examined and discussed in detail. A novel ESD protection design to further improve the ESD robustness is proposed for gigahertz large-swing PAs and verified in a 0.18-μm CMOS process.

1.2 Background of ESD

Electrostatic discharge (ESD) is the transformation between positive and negative electrostatic charges. A familiar example of ESD can be experienced as the shock when walking across a carpet floor and then touch a metal doorknob. However, ESD is a serious problem for semiconductor industry among product reliability and yields, profit, and manufacturing cost. A great deal of effort has been placed on ESD protection during the past decades. So if we can give full consideration of the ESD protection design for the whole manufacturing process, the cost can be reduced significantly.

Nowadays, the rapid development of advanced process leads to the decreasing robustness of the circuit itself with size gradually reduced. However, since the amount of charge in environment is fixed, the damage of ESD to the chip is increased.

1.3 Test Standards of ESD

According to the ways of charge accumulating and discharging path, the ESD phenomena are classified into three models, namely, the human-body model (HBM, which simulates the ESD discharge from a human-body delivered to the device), the machine model (MM, which simulates a charged manufacturing machine, discharging through the device to ground), and the charged-device model (CDM, which simulates an charged integrated circuit discharging to a grounded metal surface). As integrated circuits become more and more complex and involve very sensitive structures, it is difficult to design an efficient ESD protection network that meets ESD target levels that is commonly requested by customers [6]. The required levels are typically 2 kV for the HBM and 250 V for the CDM in most of the advanced CMOS technologies.

The equivalent circuits of the HBM, MM, and CDM ESD tests are shown in Figs. 1.1-1.3, respectively [7]-[8]. The equivalent circuit of the HBM ESD test is composed

of a 100-pF capacitor and a 1.5-kΩ resistor that represents the charge and parasitic resistance of the human body, respectively. The equivalent circuit of the MM ESD test comprises a 200-pF capacitor and no resistor. In the CDM ESD test, the equivalent circuit also consists of a capacitor and no resistor. Because most machines are made of metal, the parasitic resistance of the MM ESD test is nearly 0 Ω. But the electrostatic charge that a machine accumulates is more than that on the human body. The capacitance of the CDM ESD test is mainly due to the charge that comes from the substrate of the circuit board. The amount of charge is accumulated on the circuit board itself with size increase. The response waveform of the HBM, MM, and CDM ESD tests are plotted in Figs. 1.4. The classification for the HBM, MM, and CDM ESD levels are listed in Tables 1.1 and 1.2. The 250 V of HBM ESD stress seems to be larger than the 100 V of MM ESD stress or 125 V of CDM ESD stress. But the discharging current of the former is smaller than the latter two. So the danger caused by the latter two is more than that of the former. HBM is the most common ESD stress model and widely adopted as the basic ESD protection standard for the semiconductor industry.

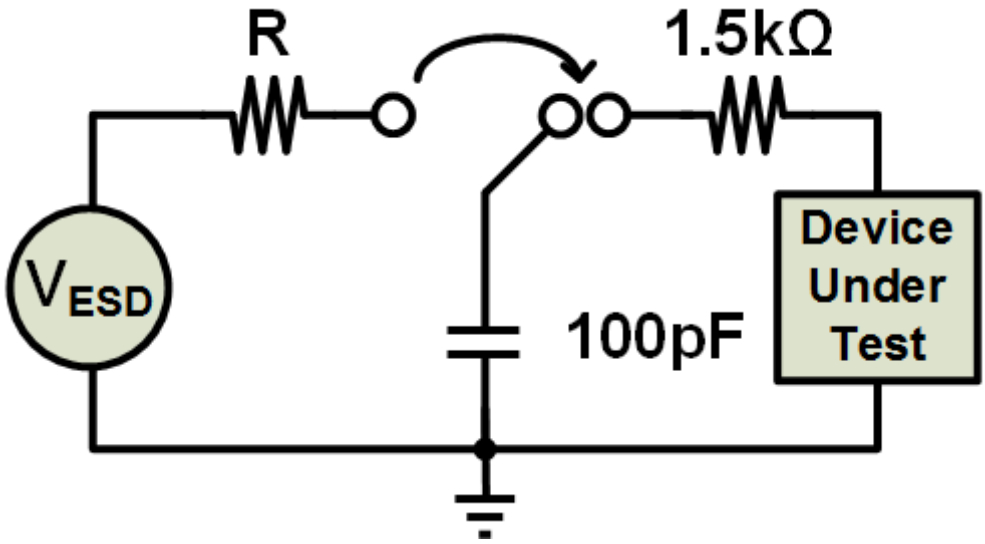


Fig. 1.1 Equivalent circuit of the HBM ESD test.

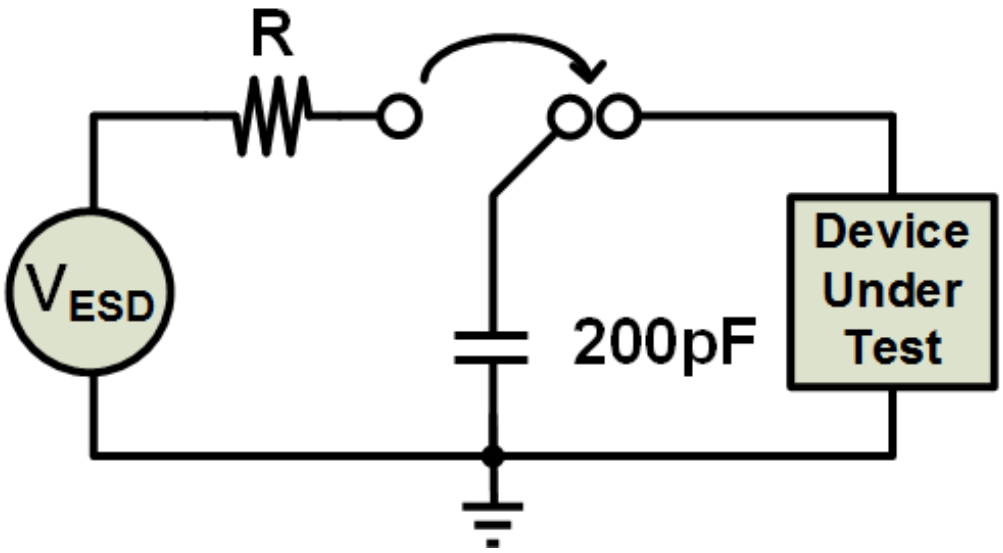


Fig. 1.2 Equivalent circuit of the MM ESD test.

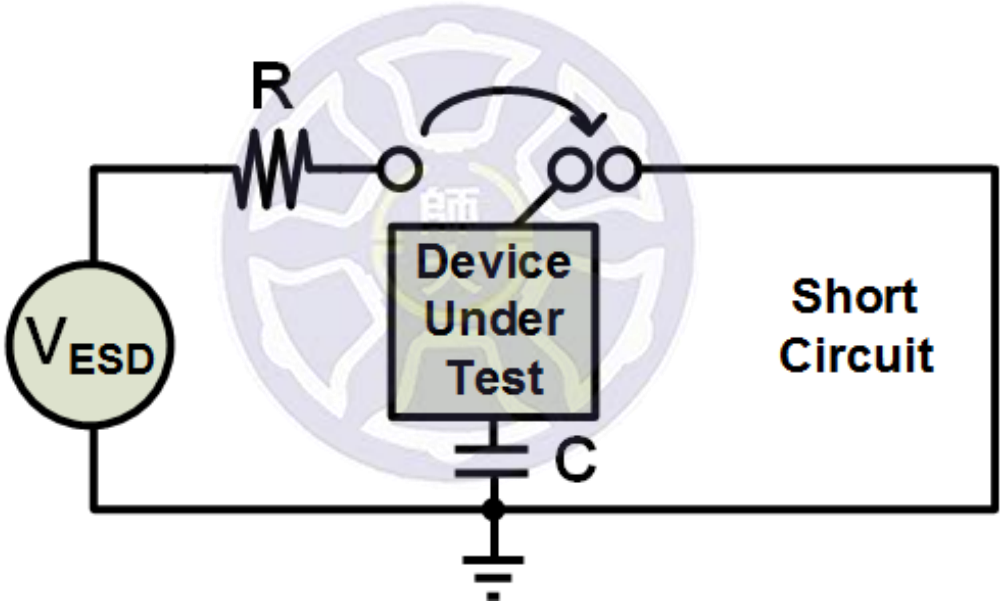


Fig. 1.3 Equivalent circuit of the CDM ESD test.

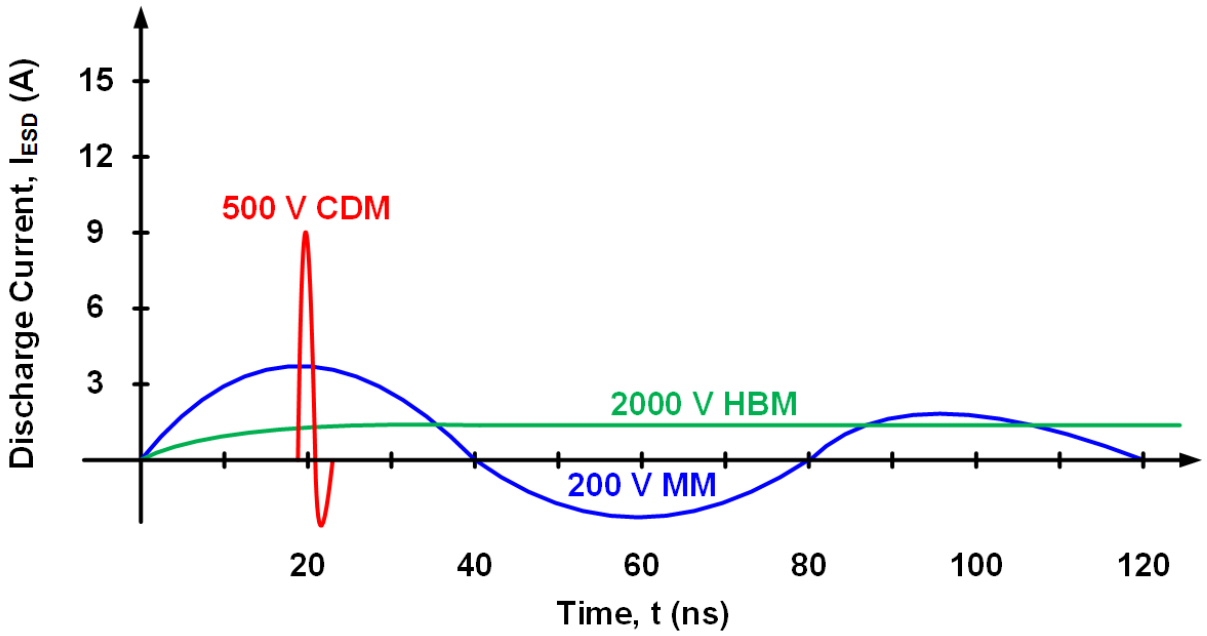


Fig. 1.4 Responses of the HBM, MM, and CDM ESD tests.

Table 1.1 Test standards of the HBM and MM ESD.

HBM Level	**MM Level**	**Impact on Manufacturing Environment**
500 V	> 30 V	➢ Basic ESD control methods allows safe manufacturing with proven margin
1 kV	> 30 V	
2 kV	> 30 V	
100 V to < 500 V	N/A	➢ Detailed ESD control methods are required

Table 1.2 Test standards of the CDM ESD.

CDM Level	ESD Control Requirements
$V_{CDM} \geq 250$ V	➢ Basic ESD control methods with grounding of metallic machine parts and control of insulators.
$125 \text{ V} \leq V_{CDM} < 250$ V	➢ Basic ESD control methods with grounding of metallic machine parts and control of insulators. ➢ Process specific measures to reduce the charging of the device or to avoid a hard discharge.
$V_{CDM} < 125$ V	➢ Basic ESD control methods with grounding of metallic machine parts and control of insulators. ➢ Process specific measures to reduce the charging of the device or to avoid a hard discharge. ➢ Charging/discharging measurements at each process step.

1.4 Traditional ESD Protection Design for Radio-Frequency Circuits

Fig. 1.5 is the photo of an RF circuit which was destroyed after ESD attack. The dark part is the burned-out traces. It can be seen from the photo that the on-chip ESD protection is necessary so that the RF circuit can have an immediate and effective path to discharge ESD current when ESD attack happened.

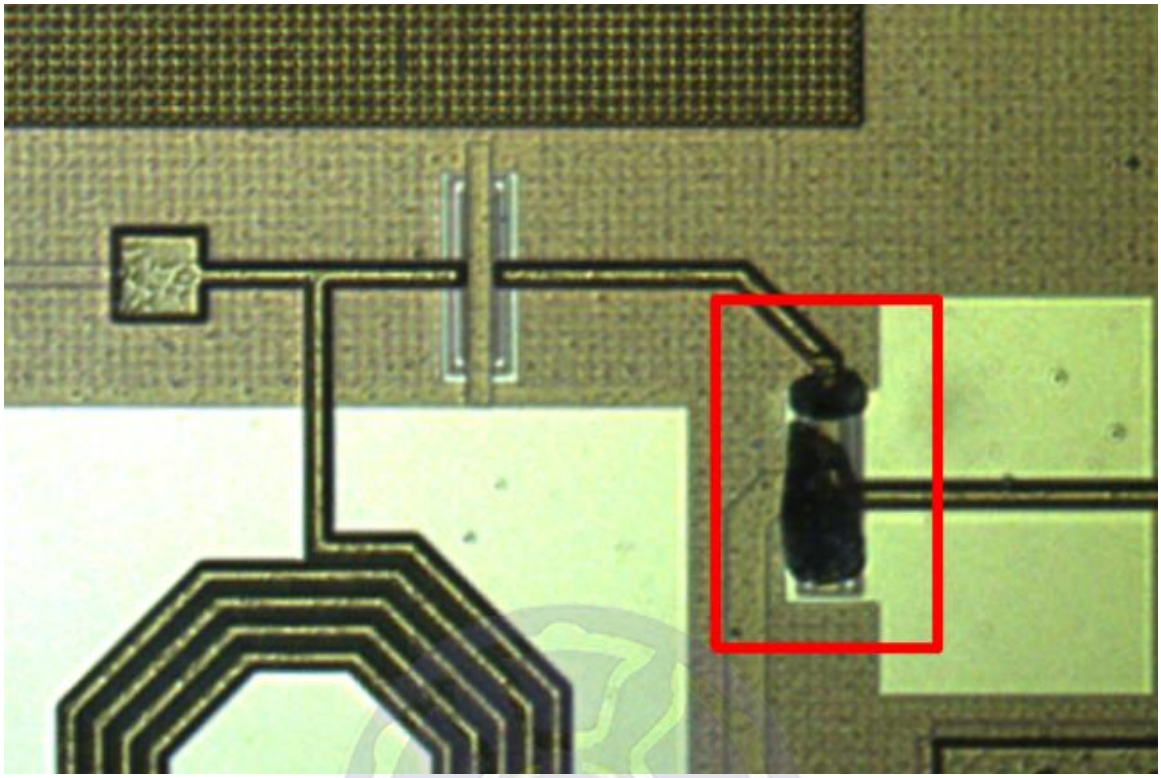


Fig. 1.5 The photo of an ESD damaged RF circuit without on-chip ESD protection.

In general, ESD protection components are designed to meet the ESD design window. As shown in Fig. 1.6, the ESD design window is surrounded by a number of boundary conditions, including the breakdown voltage of the internal circuit (V_{BD}), the power supply voltage (V_{DD}). These boundary conditions are determined by the internal circuit which is to be protected.

In the I-V curve of the ESD design window, the voltage of first snapback point is called the trigger voltage (V_{t1}). When the bias voltage is higher than V_{t1}, the protection circuit will begin conducting. In general, V_{t1} needs to be less than (1-10%)V_{BD} to avoid the internal circuits be failed before the conducting of the ESD protection circuits.

After passing the snapback point, the corresponding voltage and current of the holding point are called the holding voltage (V_h) and holding current (I_h), respectively.

In general, the holding voltage (V_h) is designed to be greater than (1 +10%)V_{DD} so that the ESD protection circuits may have the mechanism to terminate conduction after ESD stress. If the protection circuits cannot stop conducting, it may keep working until being burned out, and this phenomenon is called latch-up.

In the I-V curves of the protection components, the current of the second snapback point is called the secondary breakdown current, I_{t2}. Since ESD protection circuits cannot restore after the secondary breakdown, the physical meaning is that I_{t2} is the maximum current that the protection circuits can pass through. A larger I_{t2} indicates that the protection circuit itself has stronger robustness against the ESD stress.

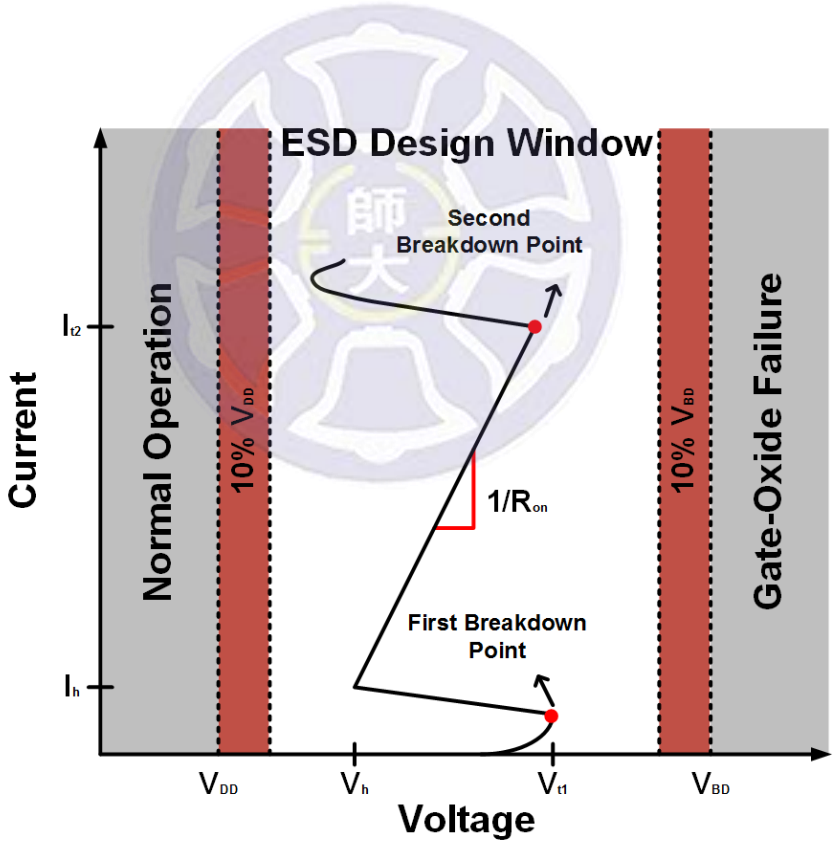


Fig. 1.6 The ESD design window.

For the design of ESD protection circuits, the best way is to provide a full-chip ESD protection because it cannot be estimated where the charges accumulate and

through which path the ESD stress will be released in the circuit, as shown in Fig. 1.7. For that purpose, there should be an ESD discharging path between the power lines. Such an ESD protection circuit is called the power clamp circuit. It basically has to maintain the voltage between the power lines when the circuit under protection is working properly. When the ESD attack occurs, the protection circuit should be able to provide two discharging paths with one for V_{DD}-to-V_{SS} and the other for V_{SS}-to-$V_{DD.}$ In addition, the protection circuit must meet the rules of the ESD design window and make V_h greater than (1 + 10%)V_{DD} to avoid the problems of latch-up.

In addition, there should also be a discharging path between the input (output) terminal and the power lines. The holding voltage of the protection component, V_{t1}, needs to be less than (1-10%)V_{BD} to protect the internal circuit when ESD events occur. For RF circuits, since the signal lines are very sensitive, the ESD protection circuits between the input or output terminals and the power supply lines need to be more carefully designed as compared to those between the power lines. The designed ESD protection circuits should avoid not only the problem of latch-up but also the signal distortion. They also need to minimize the parasitic capacitance in order not to degrade the circuit performance.

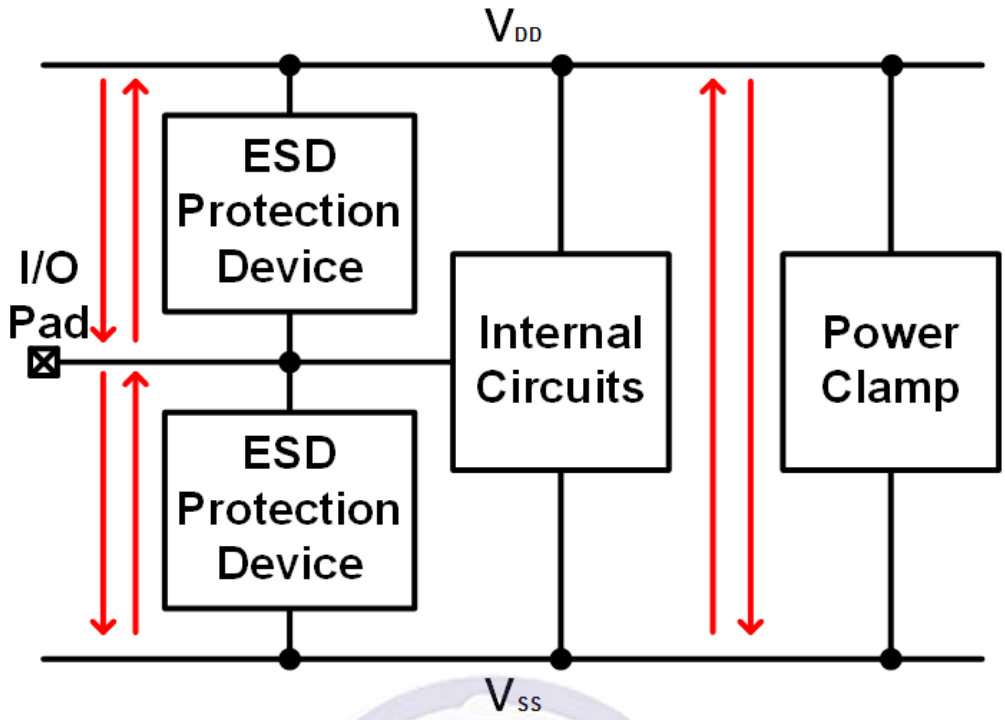


Fig. 1.7 The full-chip ESD protection configuration.

In the past, ESD protection of RF circuits using matching networks has been proposed [9]. A usual approach is to connect an inductor in parallel followed by a capacitor in series to the possible entrance of the ESD to prevent the internal circuits from ESD attack, as shown in Fig. 1.8. Or alternatively, the port that ESD may enter can be shunted with inductor, capacitor, and diode elements to provide a discharging path for circuit protection, as depicted in Fig. 1.9. In practical applications, the above ESD protection circuits can also be combined to achieve both impedance matching and ESD protection. The one shown in Fig. 1.10 is one of the examples with the transformer also used in the circuit design.

ESD protection circuits using capacitors and inductors usually occupy a large chip area, causing a higher manufacturing cost. This makes the off-chip components another possible choice in protection circuit designs. However, a drawback of using off-chip protection components is that before connecting to them, the internal circuits

have no electrostatic discharging path and thus could be attacked by the ESD stress. Once the IC chip accumulate enough static charges and form a discharging path, the on-chip circuits can be damaged by the ESD. Since such a damage is irreversible, the function of the internal circuit cannot be restored even the off-chip components are connected to provide the ESD protection. Thus to solve the ESD attack problems, the direct and effective approach is to integrate the designs of the internal circuit and the protection device on the same IC chip.

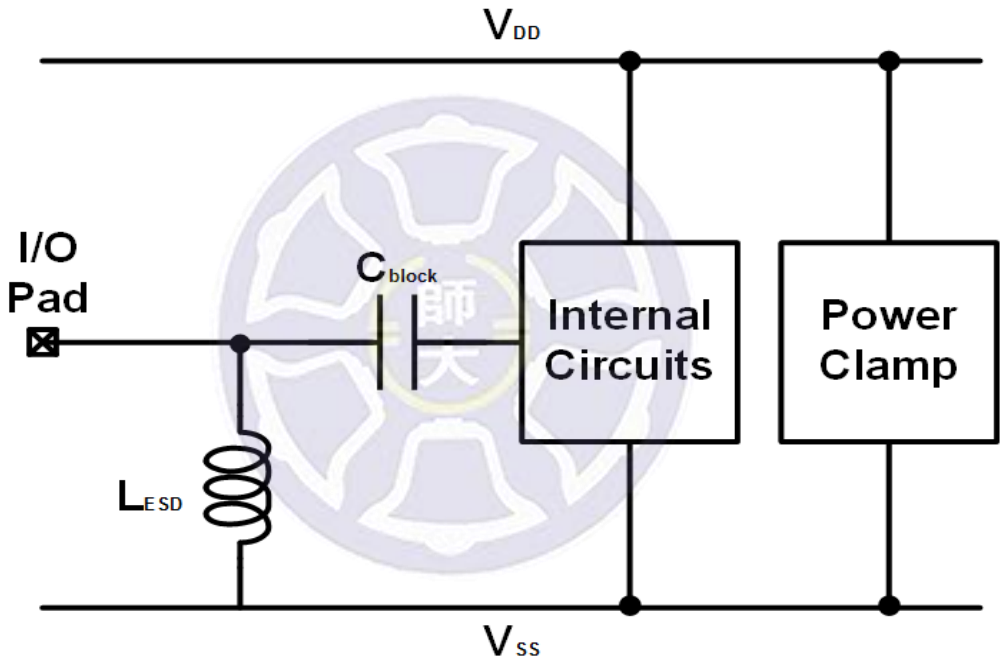


Fig. 1.8 The ESD protection circuit designed using a shunt capacitor followed by a series inductor.

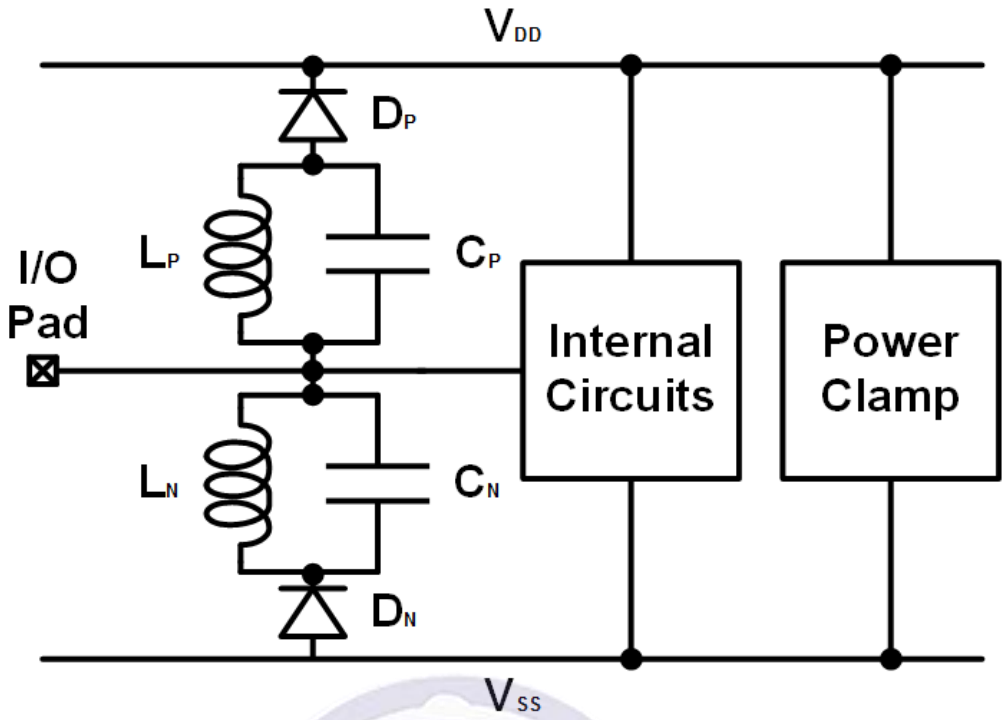


Fig. 1.9 The ESD protection circuit designed using a series diode and an LC tank.

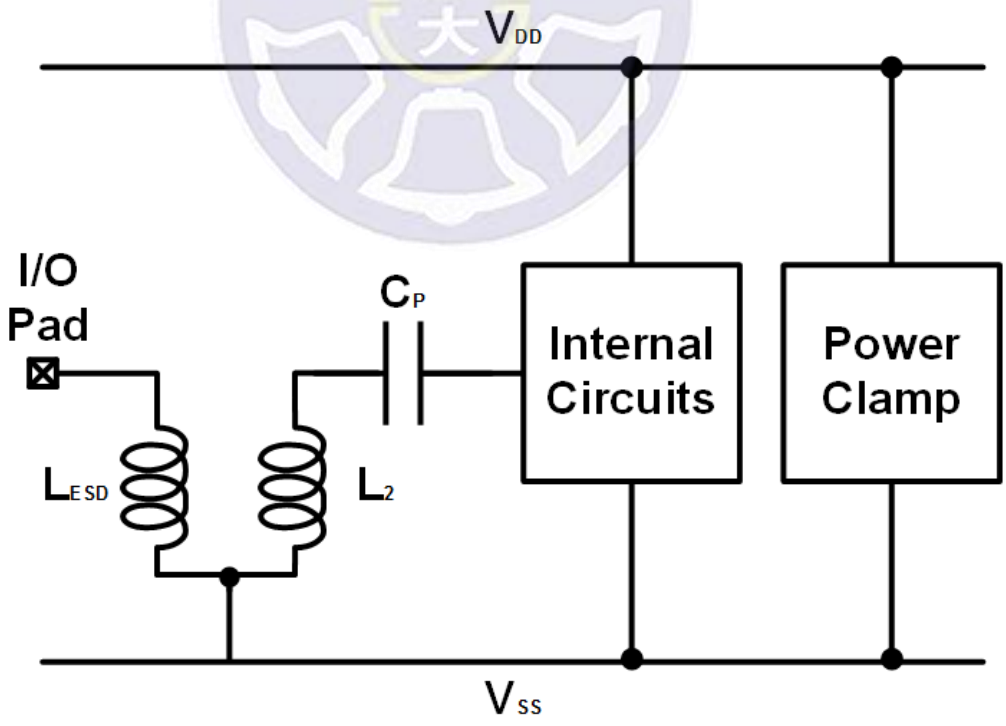


Fig. 1.10 The ESD protection circuit designed using the combination of a transformer, a capacitor and the power clamp circuit.

1.5 Introduction of Power Amplifiers

In this thesis, the efforts will be placed on the design of the protection circuits for RF power amplifiers (PAs), thus RF PAs will be briefly introduced in this section. PAs play a very important role in RF transmitters. They are usually located between the mixer and the antenna, as shown in Fig. 1.11. For application in wireless communication systems, the number of PAs in a single cell phone increases from 3.4 to 7 as the communication protocol steps from 3G to 4G. The required number of PAs is expected to be even larger as the wireless communication protocol migrates from 4G to 5G. Thus the need of ESD protection circuits in PAs will also be increased.

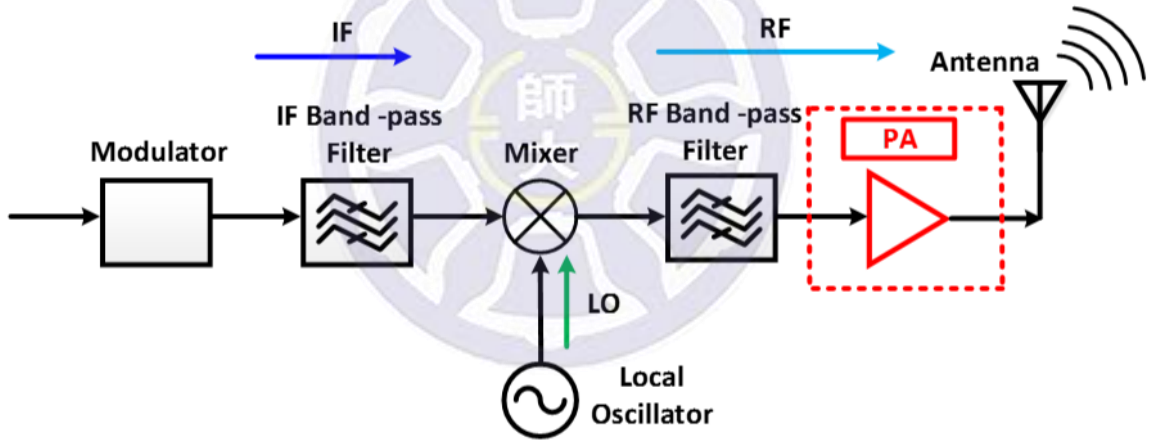


Fig. 1.11 The block diagram of an RF transmitter.

Conventionally, PAs are categorized into four classes, namely, class A, B, AB, and C. Such a classification is according to the collector current waveform that results when an input signal is applied. Among them, class A PA stage conducts for the entire cycle of the input signal, with the conduction angle being 360°; class B stage conducts for only half the cycle of the input signal, resulting in a conduction angle of 180°; class AB is an intermediate class between A and B, which conducts for an interval slightly

greater than half a cycle; class C conducts for an interval shorter than that of a half cycle, and its conduction angle is less than 180°. The main function of the PA is to amplify the signals from the output of the mixer with good linearity and deliver the required amount of power to the antenna in an efficient manner [10]. In this thesis, class AB power amplifiers will be adopted as the internal circuits for ESD protection design. Detailed design configuration and circuit verification will be presented in the following chapters.

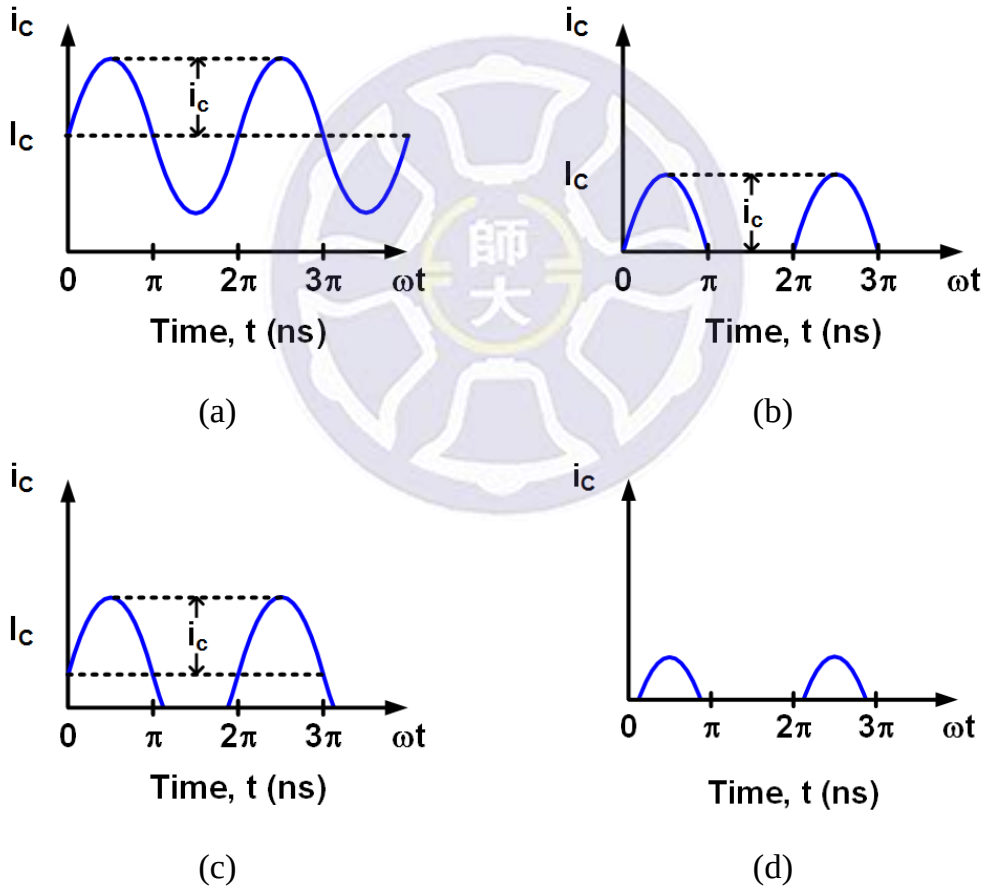


Fig. 1.12 Collector current waveforms for PA transistors operating in (a) class A, (b) class B, (c) class AB, and (d) class C stages.

1.6 Thesis Organization

This thesis consists of 4 chapters and is outlined as follows. Chapter 1 presents the literature survey, the research motivation, and the background and models of ESD. In Chapter 2, the ESD protection designs for large-swing PAs are presented. Three ESD circuit configurations including diode string (DS), diode-triggered silicon-controlled rectifier (DTSCR), and the newly proposed diode string with embedded silicon-controlled rectifier (DSSCR) are designed and measured. Their performances are also compared. In Chapter 3, three ESD protection architectures for 2.4-GHz RF PA are proposed and designed. The PA with ESD protection circuits are realized using 0.18-μm CMOS process. The fabricated PA circuits are validated by measurement.

Finally, it is concluded in Chapter 4 the work completed in this research and some proposals for future research are given.

Chapter 2

Novel ESD Protection Design for Large-Swing Power Amplifier

2.1 Consideration of ESD Protection for Large-Swing Power Amplifier

For ESD protection of radio-frequency (RF) circuits, the parasitic capacitance effect of ESD protection devices is one of the most important issues to be considered [11]. In circuit design, it is needed to reduce the effect of the protection element to avoid the degradation of circuit performance [12]. For power amplifiers, since the signal swing is large, care should be taken to prevent the output signal from being distorted when the protection element is added. The power amplifier is located at the end of the overall RF circuit and is usually one of the main entrances of the ESD stress, so how to meet the electrostatic protection requirement without affecting the performance of the power amplifier is a big challenge of design work.

In general, design of the ESD protection on the signal lines is more difficult than that between the power-lines [13]-[15]. For designing the ESD protection of large-signal-swing power amplifiers, the maximum value of the signal swing need to be notice, since the ESD protection circuits is easy to result the distortion of the PAs. Thus the boundary condition of the ESD design window is mainly provided by the maximum value of the signal swing.

RF ESD protection circuits are often designed using diodes since the diodes

have a lower parasitic capacitance. A diode can offer ESD protection by providing an electrostatic discharging path when forward biased and prevent the path from conducting under normal circuit operating condition for which it is reversed biased. For an ESD protection circuit, the parasitic capacitance mainly comes from two parts, one is from the PN junctions in the substrate, as shown in Fig. 2.1; the other is from the metal layer above the substrate, as shown in Fig. 2.2 [16]. The parasitic capacitance of the former is determined by the width of the depletion region which in turn varies with the bias and the doping concentration of the PN junction. A forward-bias will make the parasitic capacitance of a PN junction larger, whereas a reverse-bias will make it smaller. In addition, the larger the doping concentration on both sides of the PN junction, the narrower the width of the depletion region, and thus the larger the parasitic capacitance. The parasitic capacitance of the latter refers to the metal layout, where the parasitic capacitance is formed between the metal layers above the substrate, and this part may vary for different layouts.

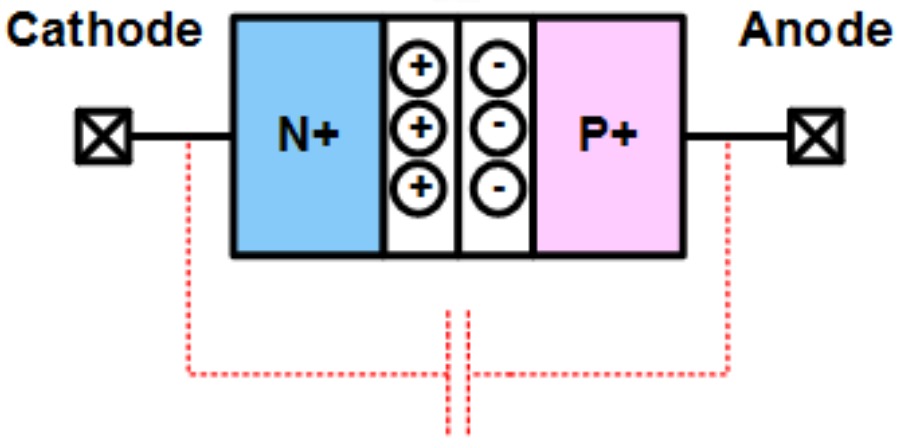


Fig. 2.1 The parasitic capacitance of a PN junction.

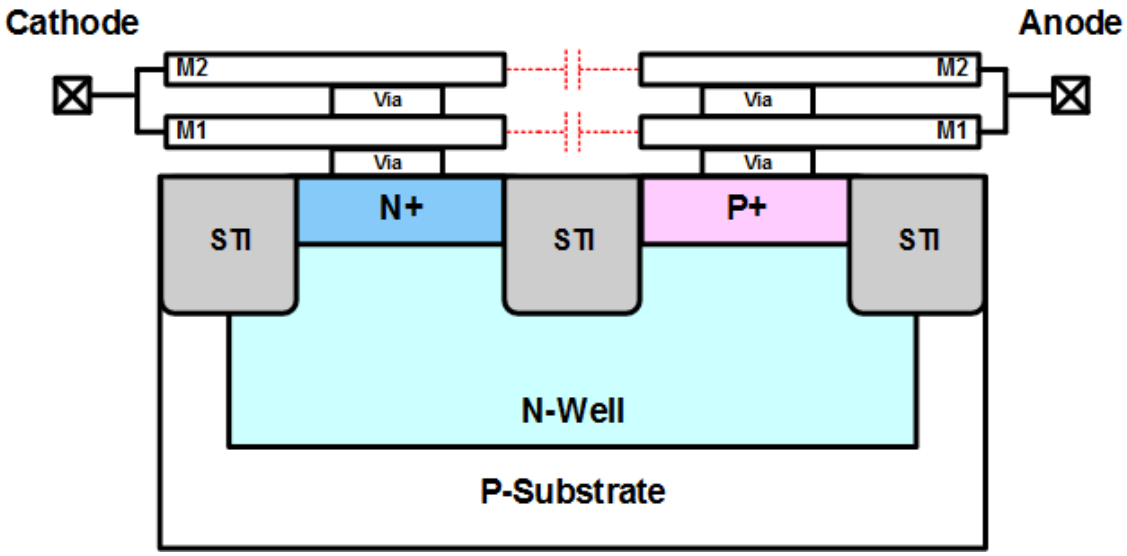


Fig. 2.2 The parasitic capacitance between metal layers.

The I-V curve of a diode is shown in Fig. 2.3, with its forward-biased region in the first quadrant and the reverse-biased region in the third quadrant. When the forward bias of a diode is higher than the cut-in voltage (usually about 0.7 V), the diode will be turned on and conduct current. The diode will turn off when reversed biased. However, when the reversed bias reaches the breakdown voltage or higher, the diode will be in its reverse conducting condition with large reverse current flowing through, as the operation shown in the third quadrant of the I-V curve. Comparison of the diode operations in the first quadrant and the third quadrant shows that when flow the same current, the power dissipated in the diode operating in the third quadrant is much larger than that in the first quadrant. This is because the diodes require a large reverse bias to operate in the reverse conducting region. If the reverse conducting characteristic of diodes in the third quadrant is employed to discharge the ESD current, it may not be able to provide an instant and effective discharging path due to its slower switching time.

Besides, the voltage across the ESD circuit, which is induced by the ESD discharging current can be too large to damage the circuit. Therefore, most of the ESD protection designs only use the diode in its forward conduction region to discharge the ESD current; that is, the operation region in the first quadrant of the I-V curve.

For diodes widely used in the ESD protection circuit of power amplifiers, their large parasitic resistance needs to be reduced. When an ESD occurs, the protection diode discharges current and meanwhile produces a large voltage across the cathode and the anode. Since the diodes for the ESD protection circuit are located between the drain of the PA and V_{SS}, this large voltage may cause damage to the drain of the PA. So reducing the parasitic resistance of the diodes is one of the primary research interests.

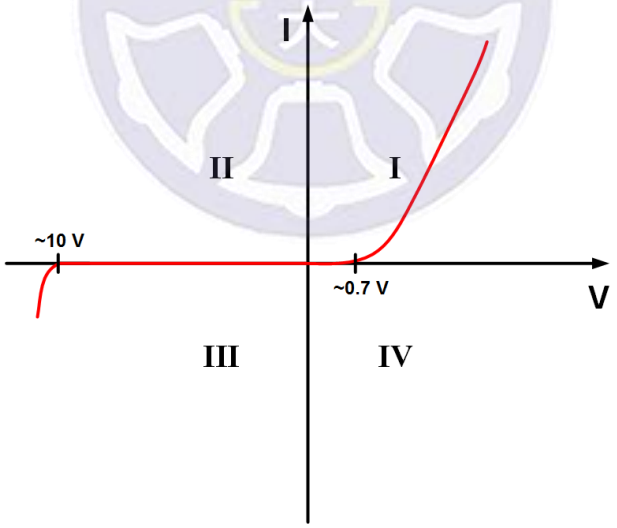


Fig. 2.3 The I-V curve of a diode.

Another often used RF ESD protection component is the silicon-controlled rectifier (SCR) [17]. The SCR is a four-layered PNPN structure. Figs. 2.4(a) and 2.4(b) show the equivalent circuit and the structural cross-sectional schematic of

the SCR, respectively. An SCR can be structurally equivalent to the cross-coupled structure of a p-n-p BJT and an n-p-n BJT, with the collector of p-n-p BJT connected to the base of the n-p-n BJT and the collector of n-p-n BJT connected to the base of the p-n-p BJT. This cross-coupled structure allows the SCR to form a positive feedback mechanism which gives a very low clamping voltage when it is conducting. This feature promises SCR good current discharging characteristic and very suitable for use as an ESD protection component.

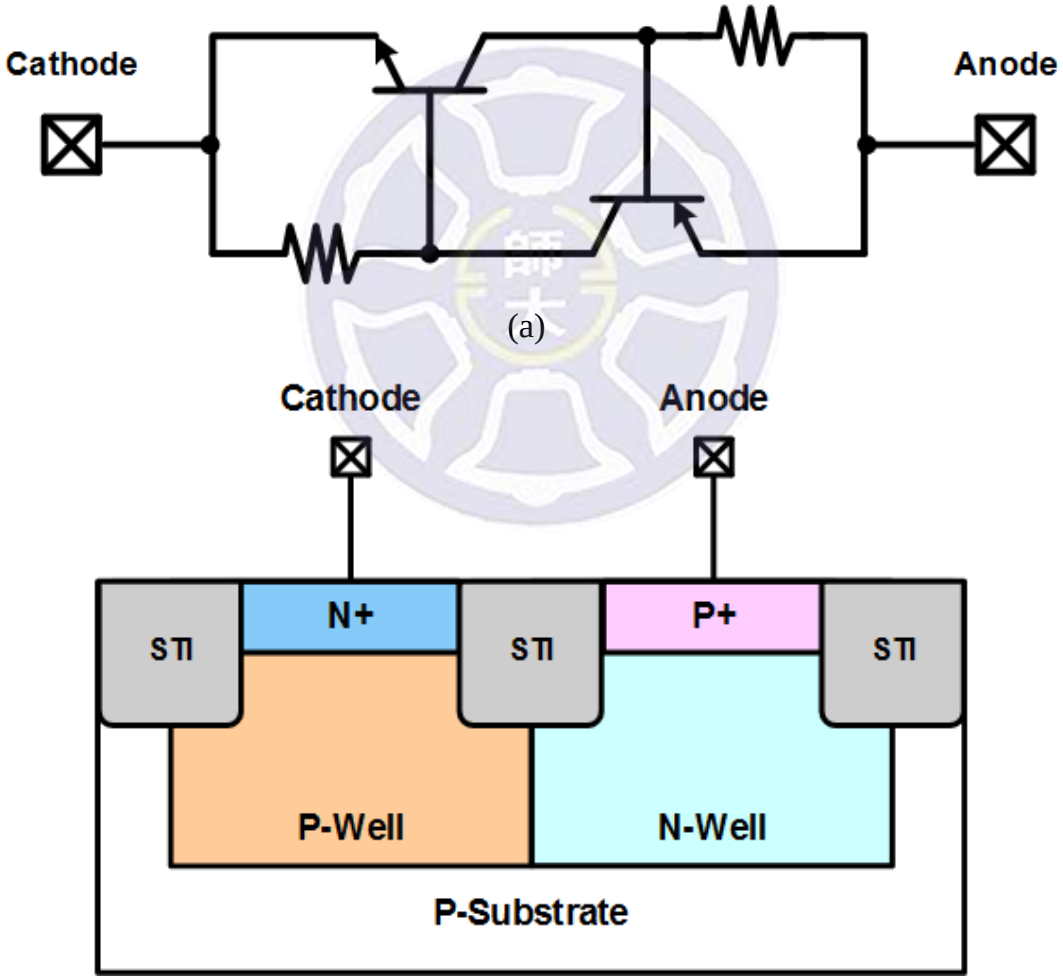
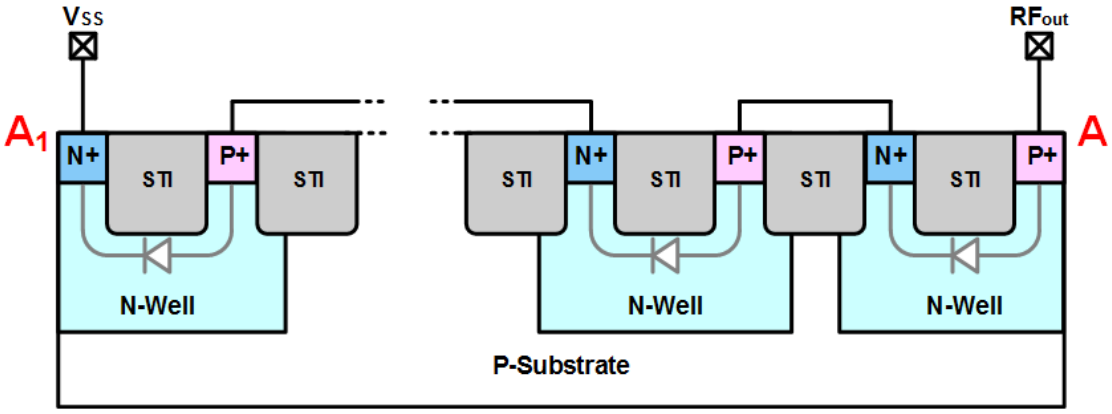


Fig. 2.4 (a) The schematic and (b) the cross-sectional view of an SCR.

2.2 Design of ESD Protection Devices

In this section, three electrostatic protection circuit designs are proposed. The first one presented here is composed of P-type diodes which are in series connection, as shown in Fig. 2.5(a), and is called the diode string (DS). Fig. 2.5(b) shows the cross-sectional view of the DS. It is seen that each P-type diode is composed of three layers, namely, the P+, N-Well, and N+ layers and the PN junction of the diodes is formed between the P+ layer and the N-Well. For the DS electrostatic protection device connected between RF_{out} and V_{SS} increasing the number of the stacked diodes can avoid distortion of the large-signal-swing power amplifier and meanwhile reduce the overall parasitic capacitance of the protection device.

(a)



(b)

Fig. 2.5 (a) Schematic and (b) cross-sectional view of the DS.

For the design of the DSs, 9 devices with different number of diodes and diode dimensions were presented. For the variation of diode dimension, three cases were considered, namely, width W_1 = 25, 50, and 100 μm, with length L_1 fixed at 0.89 μm, which corresponds to a diode cross-sectional area of 22.25, 44.5, and 89 μm^2, respectively (see Fig. 2.6). For the number of diodes in series, 4, 8, and 12 were used in this design. Fig. 2.6 shows the top view of the layout for DS with four stacked diodes.

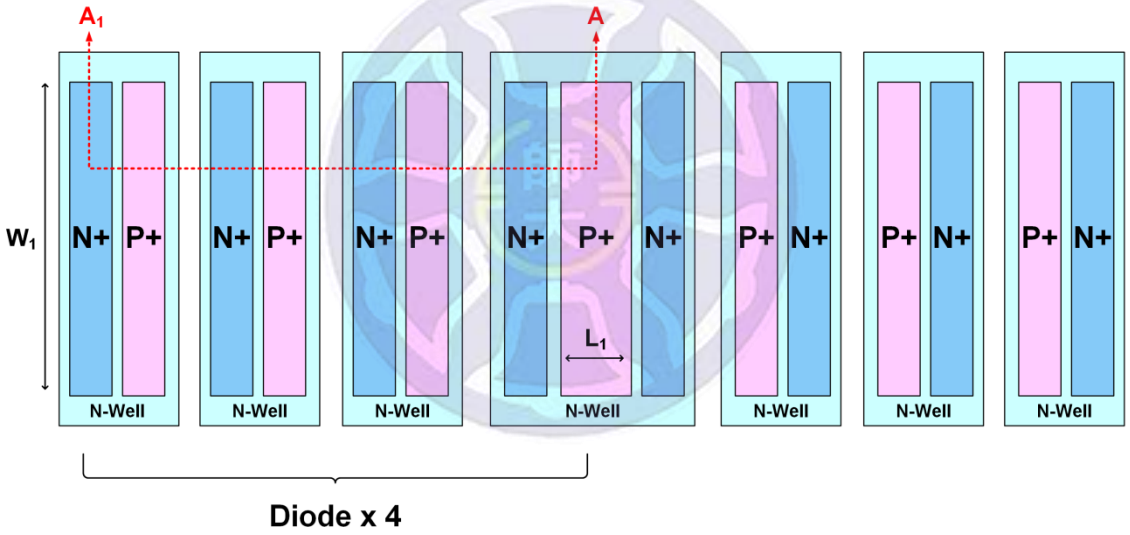


Fig. 2.6 Layout top view of the DS with 4 diodes in series.

Table 2.1 shows the notation for the 9 designed DSs with different width and number of diodes. For example, the one named DS_W100_D12 represents a DS with 12 series diodes having diode width W_1 = 100 μm.

Table 2.1 Notation and size of the designed DSs.

Notation	Width of the Diode (μm)	Number of the Stacked Diodes
DS_W25_D4	25	4
DS_W25_D8	25	8
DS_W25_D12	25	12
DS_W50_D4	50	4
DS_W50_D8	50	8
DS_W50_D12	50	12
DS_W100_D4	100	4
DS_W100_D8	100	8
DS_W100_D12	100	12

In addition to the DS, an ESD protection circuit which is composed of silicon-controlled rectifier (SCR) and diodes is also designed. Its circuit configuration is shown in Fig. 2.7(a) and it is called the diode-triggered SCR (DTSCR). For the proposed DTSCR, the structure of the SCR is formed by the P+, N-Well, P-Well, and N+ layers, as shown in Fig. 2.7(b). Since a conventional SCR needs a higher trigger voltage, it may response slower and unable to provide an instant and effective ESD discharging path when ESD occurs. To alleviate this problem, using the number of the stacked diodes can determine the trigger voltage level of the DTSCRs. In DTSCR structure, the series diodes are

connected in parallel between the N-Well and N+ layer of the SCR. When the voltage is higher than the turn-on voltage of the diode string, the SCR will be switched on and allowing current to flow through the N-Well of the SCR and the DS. Since the N-Well is just the base of the parasitic p-n-p BJT in SCR, the current can effectively reduce the trigger voltage level of the SCR [18]-[19].

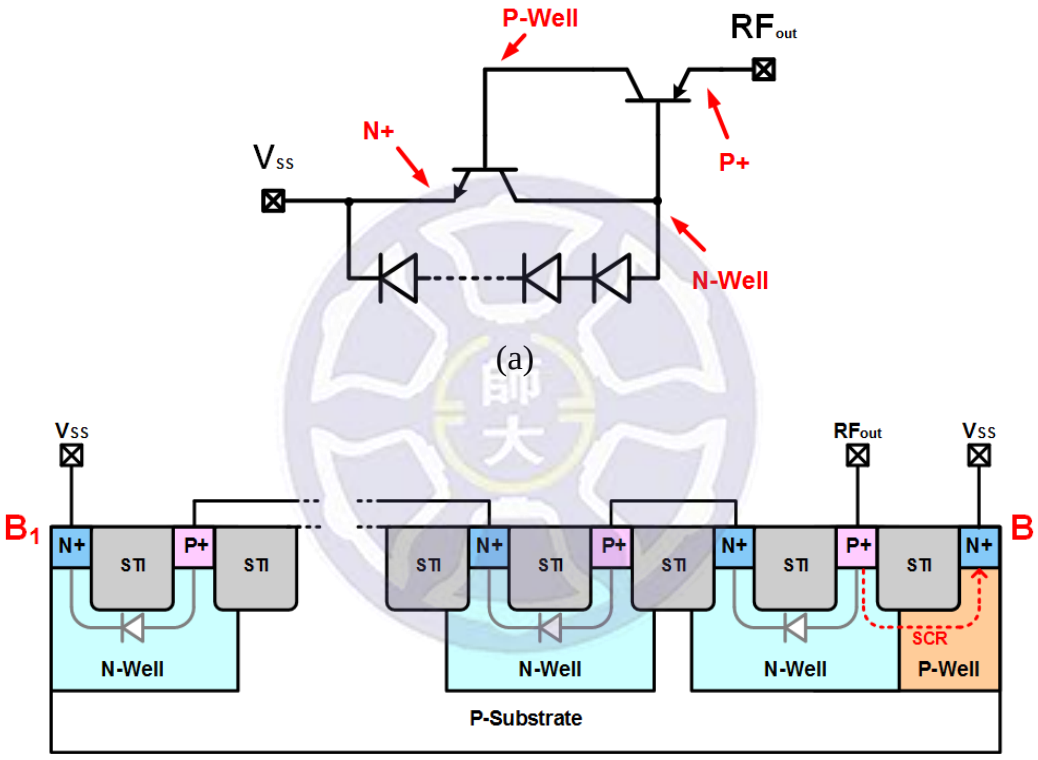


Fig. 2.7 (a) The schematic and (b) the cross-section view of the DTSCR.

For the design of the DTSCR, a total of nine different cases are also proposed. The number of diodes in series used is 4, 8 and 12, with each trigger diode having length L_2 = 0.89 μm and width W_2 = 5 μm (that is, the diode cross-sectional area is 4.45 μm^2). For the SCR, three cases of W_3 = 25, 50, and

100 μm are adopted, with L_3 fixed at 1.92 μm (see Fig. 2.8 as one of the cases). In the circuit design, to provide SCR the sufficient trigger current, the size of the trigger diodes should be increased accordingly with the increasing SCR size. Also, for the SCR be triggered uniformly by the diode strings, the diode strings should be located properly on the SCR. Three different sizes of the SCR will be used with 1, 2, and 4 strings of trigger diodes in this design.

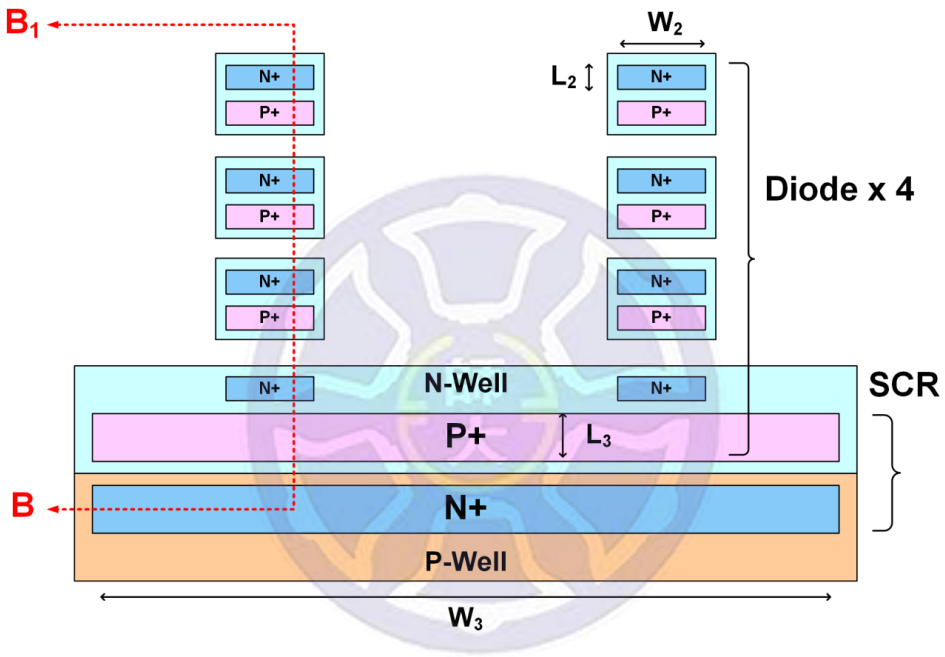


Fig. 2.8 Layout top view of DTSCR_W50_D4.

Table 2.2 shows the notations and corresponding sizes of the 9 DTSCRs. For the case of DTSCR_W100_D12, it means that the DTSCR is composed of an SCR with W_3 = 100 μm and 4 diode strings, each having 12 series-connected diodes are used. Shown in Fig. 2.8 is the top view of the layout of DTSCR_W50_D4, where one can see two evenly distributed diode strings implemented on the SCR.

Table 2.2 Notation and size of the designed DTSCRs.

Notation	Width of the SCR (μm)	Width of the Diode (μm)	Number of the Stacked Diodes
DTSCR_W25_D4	25	5	4
DTSCR_W25_D8	25	5	8
DTSCR_W25_D12	25	5	12
DTSCR_W50_D4	50	10	4
DTSCR_W50_D8	50	10	8
DTSCR_W50_D12	50	10	12
DTSCR_W100_D4	100	20	4
DTSCR_W100_D8	100	20	8
DTSCR_W100_D12	100	20	12

Besides the two electrostatic protection devices stated above, a newly designed circuit for electrostatic protection is also proposed in this thesis. The new device consists of surface diodes and a parasitic SCR, and is denoted by diode string with embedded SCR (DSSCR). Fig. 2.9(a) shows the circuit schematic of the DSSCR. Shown in Fig. 2.9(b) is the cross-sectional view. The DSSCR has a surface P-type diode (P+ layer/N-Well) and an N-type diode (P-Well/N+ layer) to form the trigger circuit that provides the SCR trigger current. The path below the surface P-type and N-type diodes can effectively form an SCR element, with its structure consists of P+/N-Well/P-Well/N+ layers.

The parasitic SCR provides the main electrostatic discharging path. The trigger voltage level of the DSSCR is determined by the series surface diodes and the clamping voltage is determined by the parasitic SCR [20]-[21]. The design and structure of the DSSCR are relatively simple. Unlike that using diode string, the DSSCR can reduce the excessive voltage drop when ESD occurs and meanwhile keep the advantage of the flexible design as that using the stacked diodes for DS to avoid large signal distortion of the PAs.

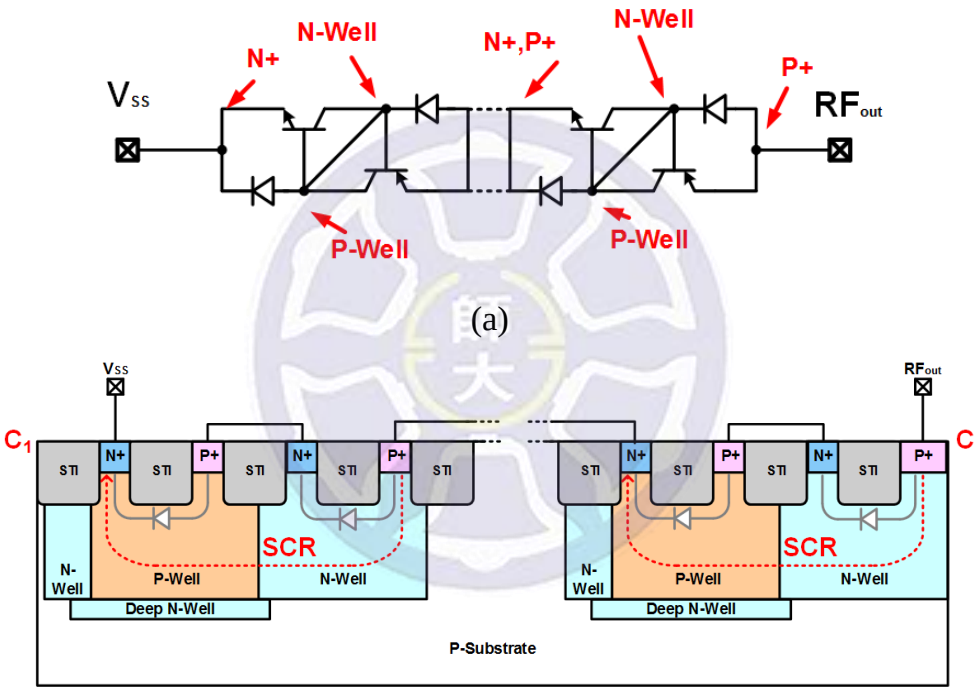


Fig. 2.9 (a) The schematic and (b) the cross-sectional view of the DSSCR.

There are also 9 cases for the DSSCR design, with length L_4 and width W_4 of each trigger diode fixed at 0.89 μm and 5 μm, respectively, corresponding to a diode cross-sectional area of 4.45 μm^2 (refer to Fig. 2.10 for structural notations). The number of diodes in series used is 4, 8, and 12. The width W_3 of the SCR is

25, 50, and 100 μm, with the length L_5 fixed at 1.92 μm. In order to provide SCR with sufficient trigger current, the size of the diode should be increased with the increasing SCR size. Also, in order for the SCR be triggered evenly, the trigger diode string will be uniformly located on the SCR. In this design, SCRs with three different sizes will be used. Each with 1, 2, or 4 diode strings implemented as the trigger circuit.

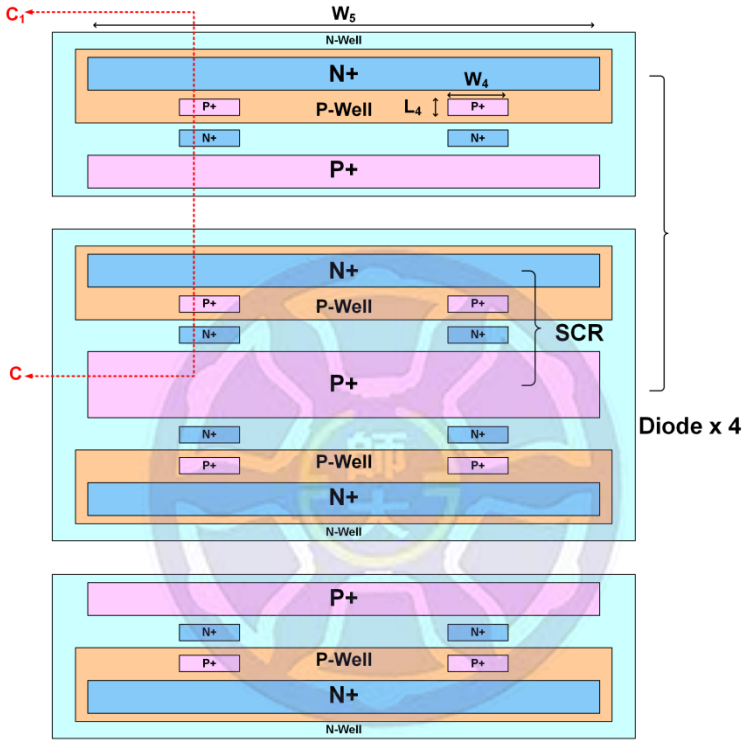


Fig. 2.10 Layout top view of DSSCR_W50_D4.

Table 2.3 lists all the 9 designed DSSCRs with notation and their corresponding size. For the case of DSSCR_W100_D12, it means that the width of the SCR is W_3 = 100 μm, and 4 strings, 12 series-connected trigger diodes are used. Shown in Fig. 2.10 is the layout top view of DSSCR_W50_D4, where the two strings of diodes are uniformly located on the SCR, as can be seen.

Table 2.3 Notation and size of the designed DSSCRs.

Notation	Width of the SCR (μm)	Width of the Diode (μm)	Number of the Stacked Diodes
DSSCR_W25_D4	25	5	4
DSSCR_W25_D8	25	5	8
DSSCR_W25_D12	25	5	12
DSSCR_W50_D4	50	10	4
DSSCR_W50_D8	50	10	8
DSSCR_W50_D12	50	10	12
DSSCR_W100_D4	100	20	4
DSSCR_W100_D8	100	20	8
DSSCR_W100_D12	100	20	12

2.3 Measurement Methods and Results of ESD Protection Devices

In this section, the RF integrated circuit (RFIC) measurement system will be employed to obtain the *S*-parameters of the DS and the DTSCR, and then use the measured *S*-parameters for de-embedding of the effect of the PAD and the metal lines with the aid of necessary matrix calculation. Since the *S*-parameters of cascaded circuits cannot be directly obtained by multiplying the *S*-parameter matrices of the individual circuits, it is needed to convert the *S*-parameter matrices into *T*-parameter matrices or *ABCD* matrices before performing matrix multiplication. Then the calculated total *T*-parameter or *ABCD* parameters should

be converted back to the *S*-parameters to complete the matrix calculation of the cascaded circuit (as illustrated in equations (1) through (4)).

Taking the two-port cascaded network shown in Fig. 2.11 as an example, the measured total *T*-parameter matrix represents the three cascaded sub-circuits with two being PADs and another being the circuit in the dashed box that is composed of metal and protection elements. Once the *T*-parameter matrix of the PAD is known, its inverse matrix can be calculated and be used to solve for the *T*-parameter and thus the *S*-parameter matrix of the red-box circuit [22]. Finally, the formula can be used to deduct the metal effect and obtain the impedance of the designed ESD protection device for evaluating its parasitic capacitance, parasitic resistance, and loss. The high-frequency model of designed ESD protection device is shown in Fig. 2.12. The calculation procedure described above can be illustrated by the following equations [22]. The afore-mentioned measurement method was employed for measuring the ESD protection devices designed in this research, with results shown in Figs. 2.13-2.18.

$$[\text{Total circuit}]_S \Rightarrow [\text{Total circuit}]_T \tag{2.1}$$

$$[\text{Total circuit}]_T = [\text{PAD}]_T\,[\text{DUT+Metal}]_T\,[\text{PAD}]_T \tag{2.2}$$

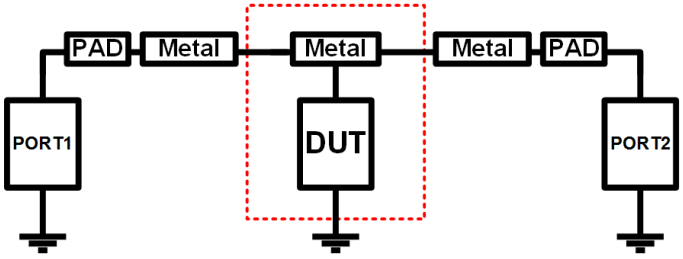
$$[\text{DUT+Metal}]_T = [\text{PAD}]^{-1}{}_T\,[\text{Total circuit}]_T\,[\text{PAD}]^{-1}{}_T \tag{2.3}$$

$$[\text{DUT+Metal}]_T \Rightarrow [\text{DUT+Metal}]_S \tag{2.4}$$

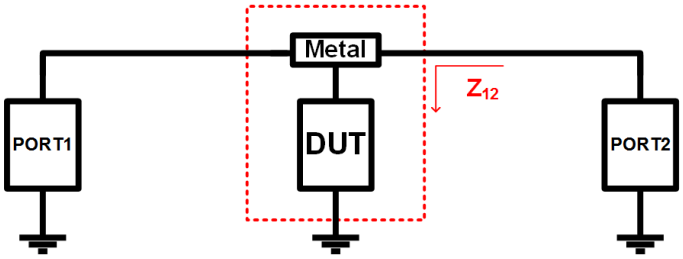
$$Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} \tag{2.5}$$

$$\mathrm{R} = \frac{1}{\mathrm{Re}\{\frac{1}{Z_{12}}\}} \tag{2.6}$$

$$\mathrm{C} = \frac{1}{2\pi f * \frac{1}{\mathrm{Im}\{\frac{1}{Z_{12}}\}}} \tag{2.7}$$



(a)



(b)

Fig. 2.11 (a) Block diagram of a cascaded two-port RFIC network; (b) the circuit after de-embedding.

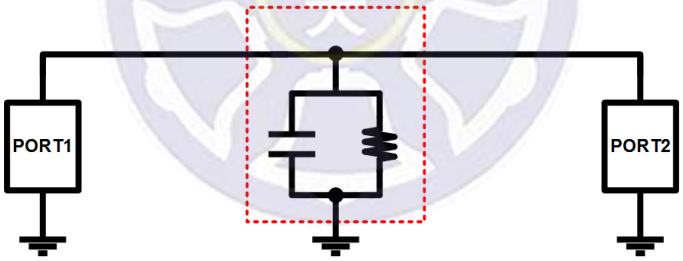


Fig. 2.12 The high-frequency model of the dashed box.

Figs. 2.13(a)-(c) show the losses of the DSs with the same diode width but different numbers of the stacked diodes. Figs. 2.13(d)-(f) show the losses of the DSs with the same number of the stacked diodes but different diode width. On the other hand, Figs. 2.14(a)-(c) show the parasitic capacitances of the DSs with the same diode width but different numbers of the stacked diodes and Figs. 2.14(d)-(f) show the parasitic capacitances of the DSs with the same number of

the stacked diodes but different diode width. The losses, parasitic capacitances and parasitic resistances of the designed DSs have also been shown in Table 2.4 for operating frequencies of 2.4 GHz and 5 GHz.

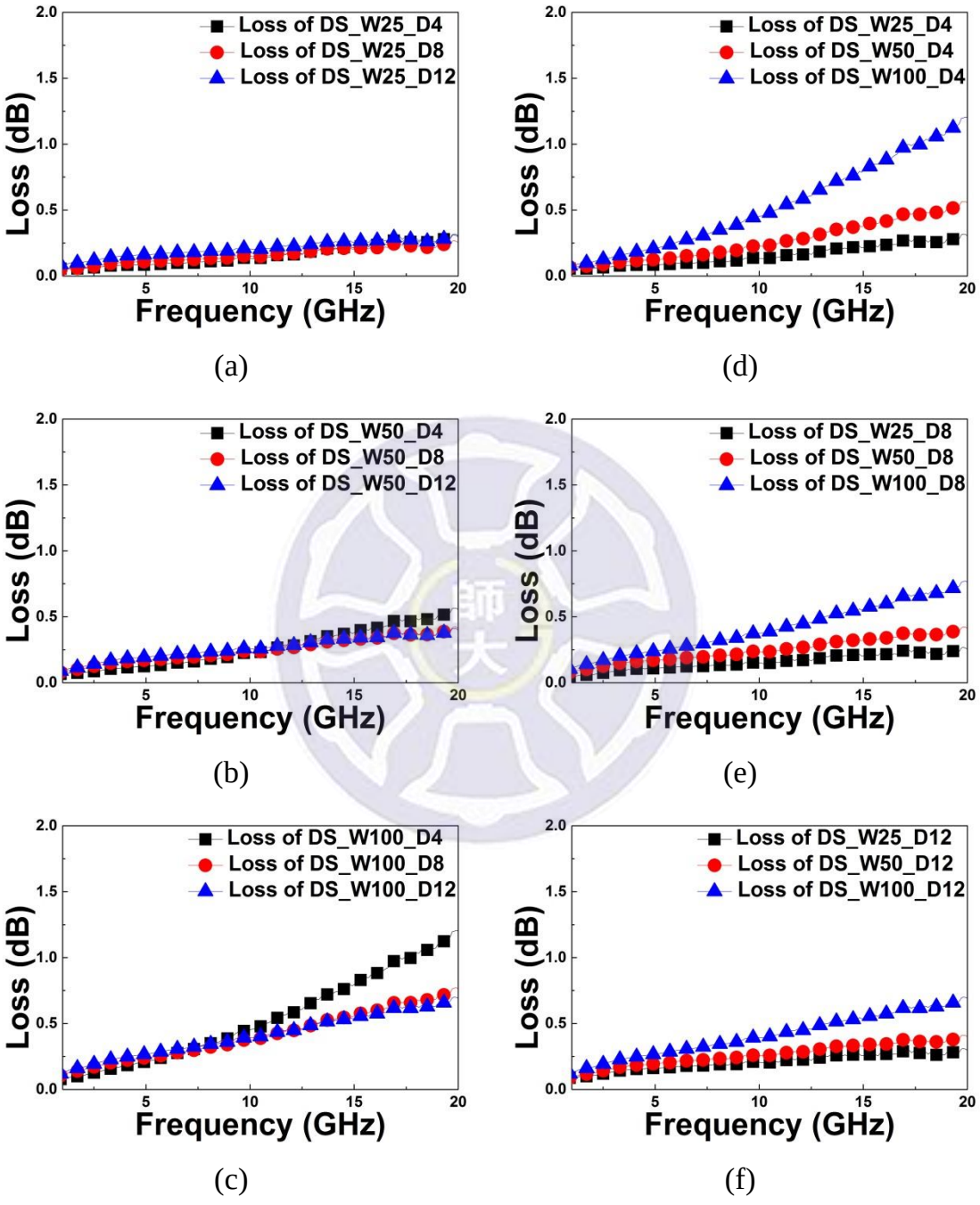


Fig. 2.13 Measured losses for the DSs having (a) 25 μm, (b) 50 μm, and (c) 100 μm diode width and different numbers of the stacked diodes; losses for the DSs having (d) 4, (e) 8, and (f) 12 stacked diodes and different diode width.

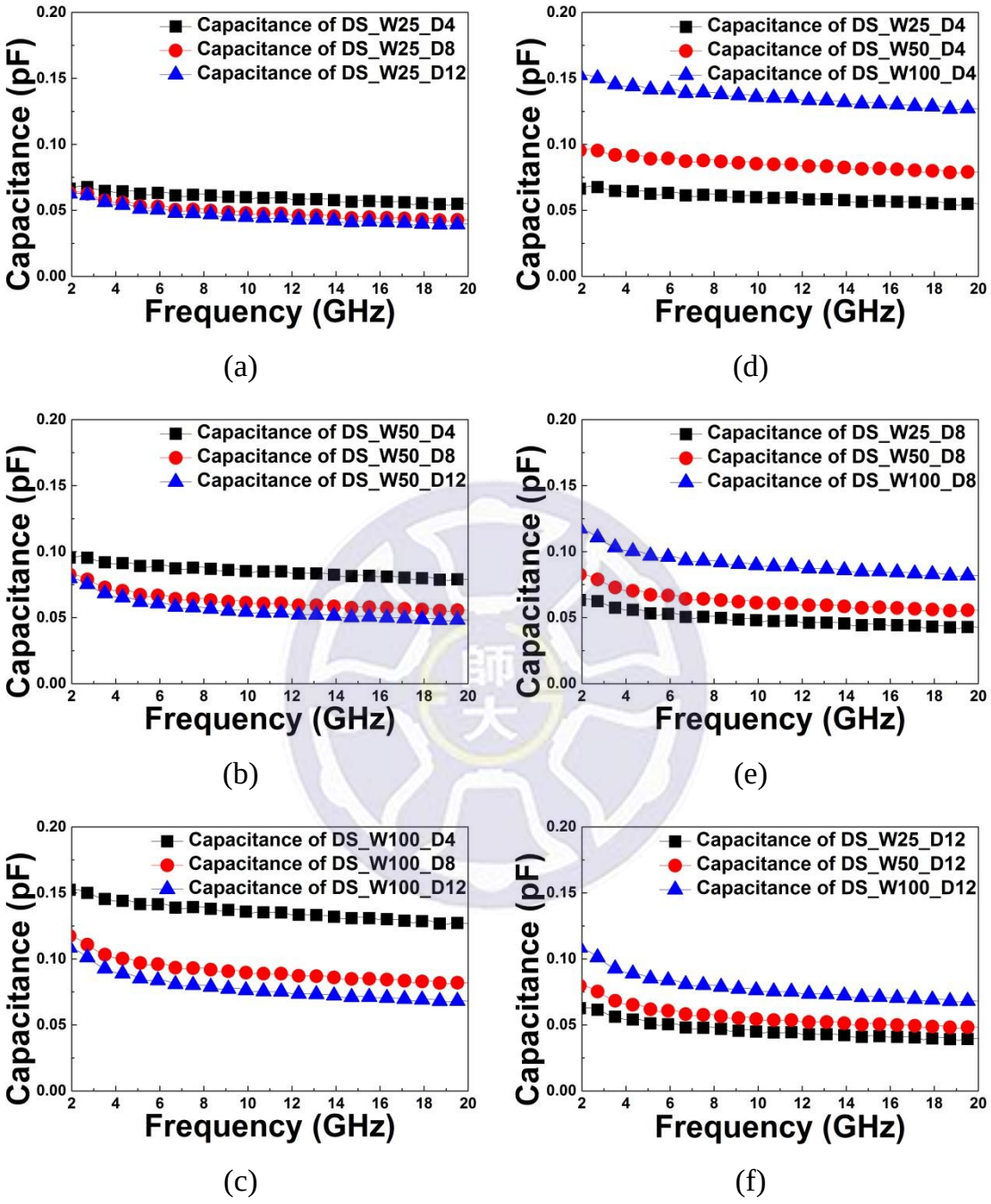


Fig. 2.14 Measured parasitic capacitance for the DSs having (a) 25 μm, (b) 50 μm, and (c) 100 μm diode width and different numbers of the stacked diodes; losses for the DSs having (d) 4, (e) 8, and (f) 12 stacked diodes and different diode width.

Table 2.4 Measured losses and parasitic capacitances of the DSs at different frequencies.

Width of the Diode (μm)	Number of the Stacked Diodes	Loss at 2.4 GHz (dB)	Loss at 5 GHz (dB)	Parasitic Capacitance at 2.4 GHz (fF)	Parasitic Resistance at 2.4 GHz (kΩ)
25	4	0.064	0.085	68	510.3
	8	0.072	0.11	64	10.5
	12	0.118	0.162	63	8.25
50	4	0.084	0.125	97	9.64
	8	0.122	0.169	81	3.56
	12	0.137	0.194	78	3.01
100	4	0.122	0.212	152	3.77
	8	0.168	0.239	114	1.97
	12	0.189	0.267	105	1.66

Figs. 2.15(a)-(c) show the losses of the DTSCRs with the same diode and SCR widths but different numbers of the stacked diodes. Figs. 2.15(d)-(f) show the losses of the DTSCRs with the same number of the stacked diodes but different diode and SCR widths. On the other hand, Figs. 2.16(a)-(c) show the parasitic capacitances of the DTSCRs with the same diode width but different numbers of the stacked diodes and Figs. 2.16(d)-(f) show the parasitic

capacitances of the DTSCRs with the same number of the stacked diodes but different diode width.

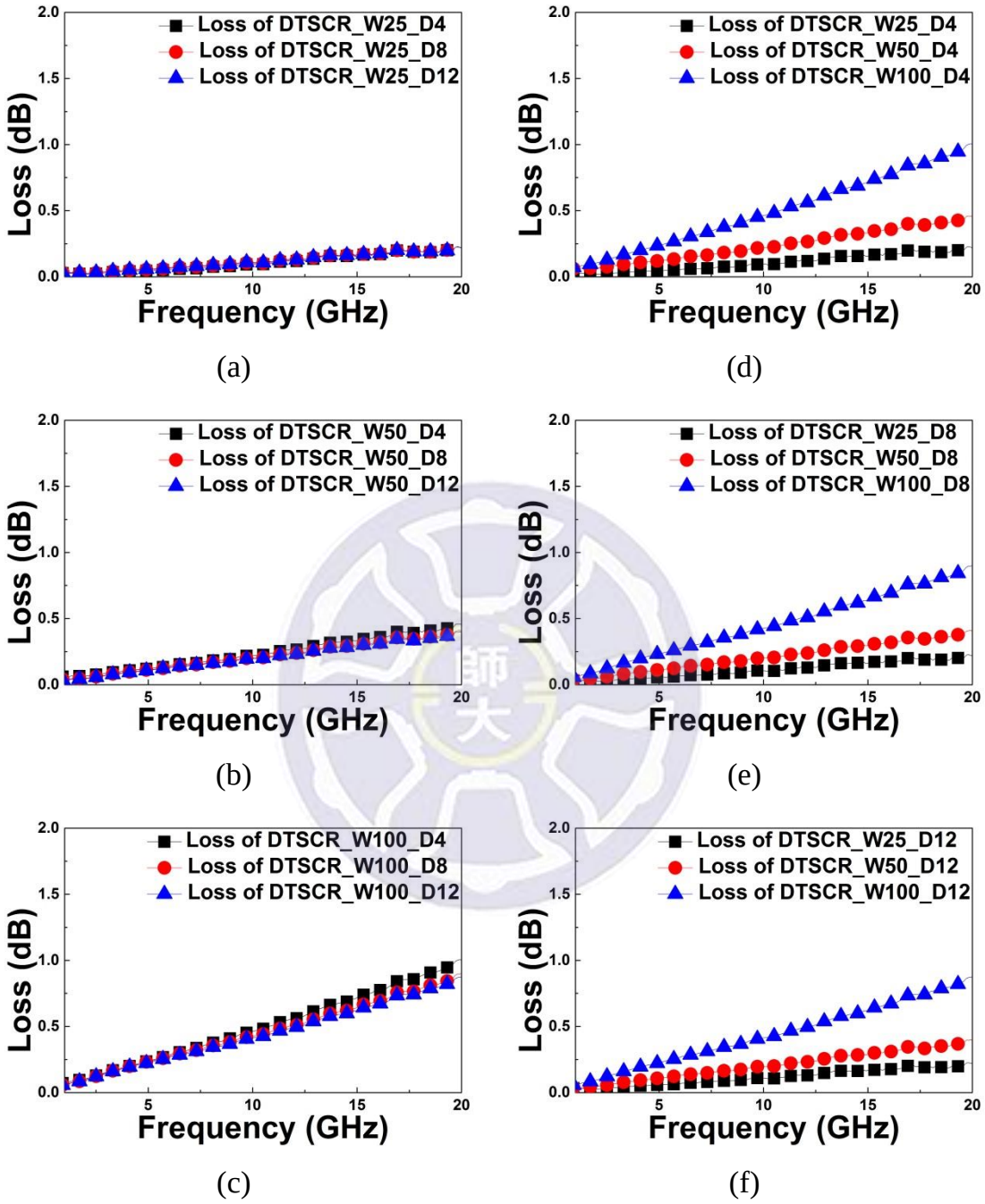


Fig. 2.15 Measured losses for the DTSCRs having (a) 25 μm, (b) 50 μm, and (c) 100 μm SCR width and different numbers of the stacked diodes; losses for the DTSCRs having (d) 4, (e) 8, and (f) 12 stacked diodes and different SCR widths.

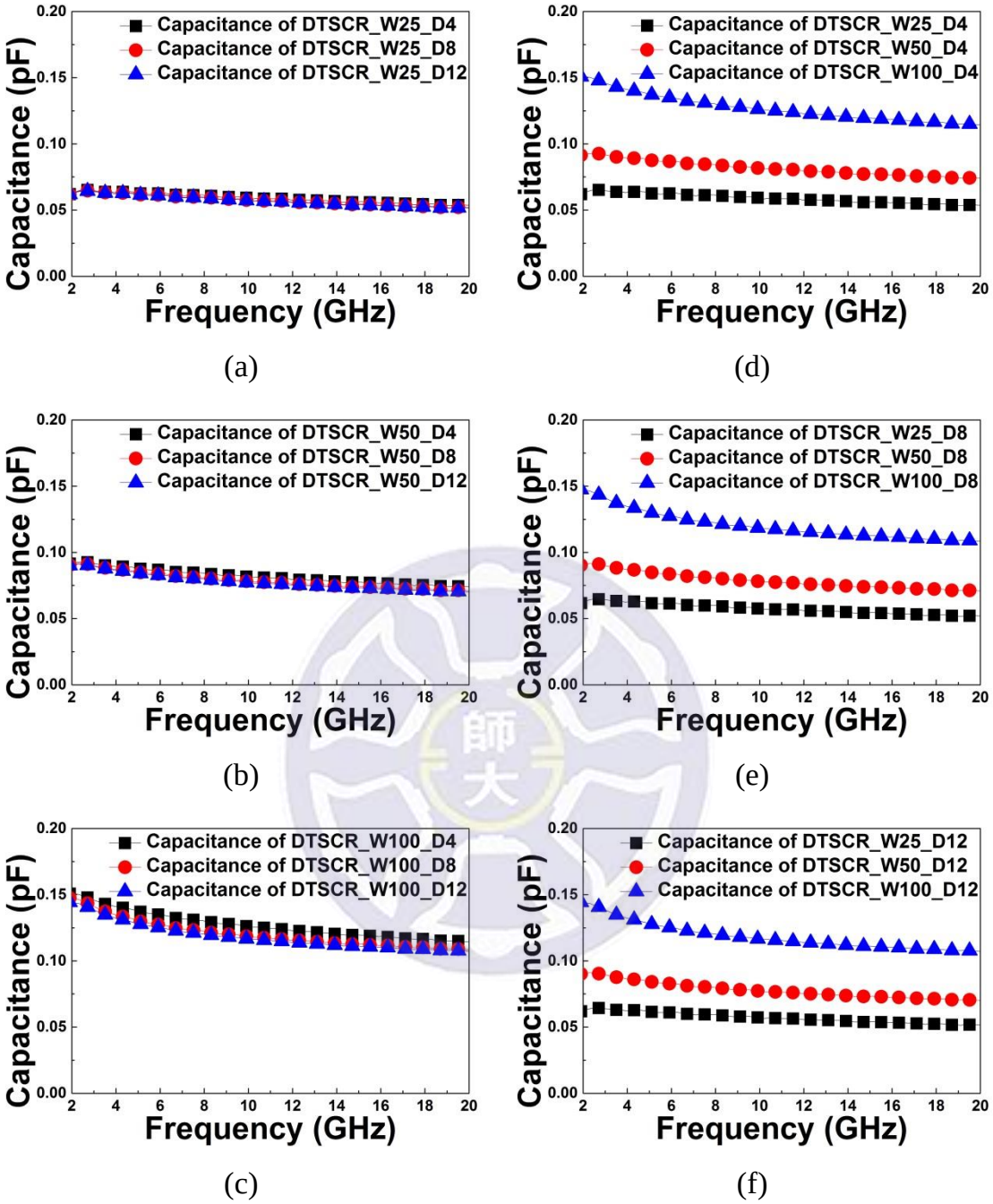


Fig. 2.16 Measured parasitic capacitance for the DTSCRs having (a) 25 μm, (b) 50 μm, and (c) 100 μm SCR width and different numbers of the stacked diodes; losses for the DTSCRs having (d) 4, (e) 8, and (f) 12 stacked diodes and different SCR widths.

Table 2.5 Measured losses and parasitic capacitances of the DTSCRs at different frequencies.

Width of the SCR (μm)	Number of the Stacked Diodes	Loss at 2.4 GHz (dB)	Loss at 5 GHz (dB)	Parasitic Capacitance at 2.4 GHz (fF)	Parasitic Resistance at 2.4 GHz (kΩ)
25	4	0.023	0.044	65	9.6
	8	0.029	0.055	64	10.9
	12	0.031	0.057	64	11.4
50	4	0.073	0.121	93	90.1
	8	0.057	0.112	92	59.5
	12	0.054	0.109	91	45.5
100	4	0.124	0.238	150	4.7
	8	0.119	0.234	146	3.7
	12	0.115	0.227	143	4.3

In the part of the DSSCRs, Figs. 2.17(a)-(c) show the losses of the DSSCRs with the same diode and SCR widths but different numbers of the stacked diodes. Figs. 2.17(d)-(f) show the losses of the DSSCRs with the same number of the stacked diodes but different diode and SCR widths. On the other hand, Figs. 2.18(a)-(c) show the parasitic capacitances of the DSSCRs with the same diode width but different numbers of the stacked diodes and Figs. 2.18(d)-(f) show the parasitic capacitances of the DSSCRs with the same number of the stacked

diodes but different diode width. The losses, parasitic capacitances, and parasitic resistances of the designed DTSCSs and DSSCRs have also been shown in Table 2.5 and Table 2.6, respectively, for operating frequencies of 2.4 GHz and 5 GHz.

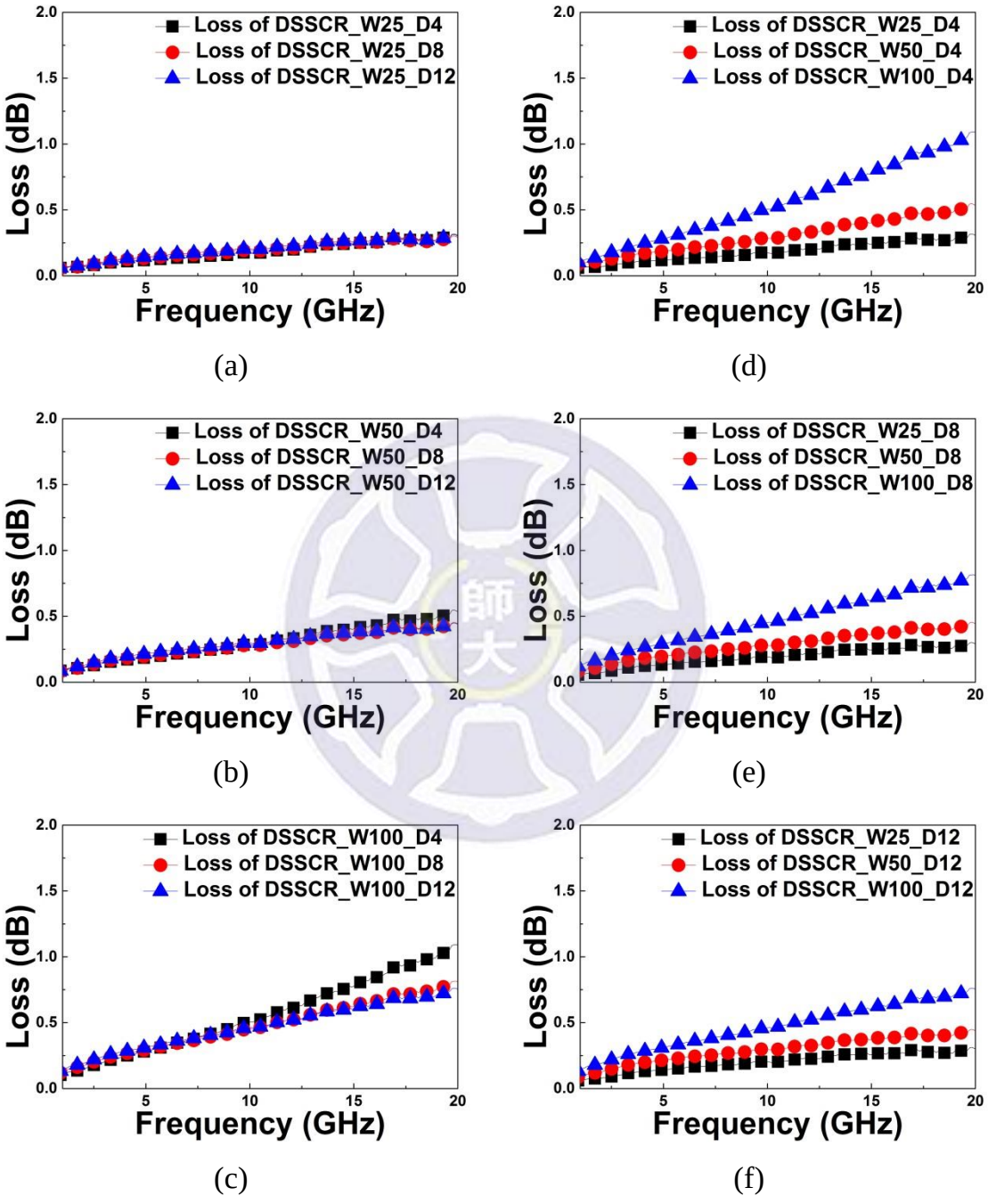


Fig. 2.17 Measured losses for the DSSCRs having (a) 25 μm, (b) 50 μm, and (c) 100 μm SCR width and different numbers of the stacked diodes; losses for the DSSCRs having (d) 4, (e) 8, and (f) 12 stacked diodes and different SCR widths.

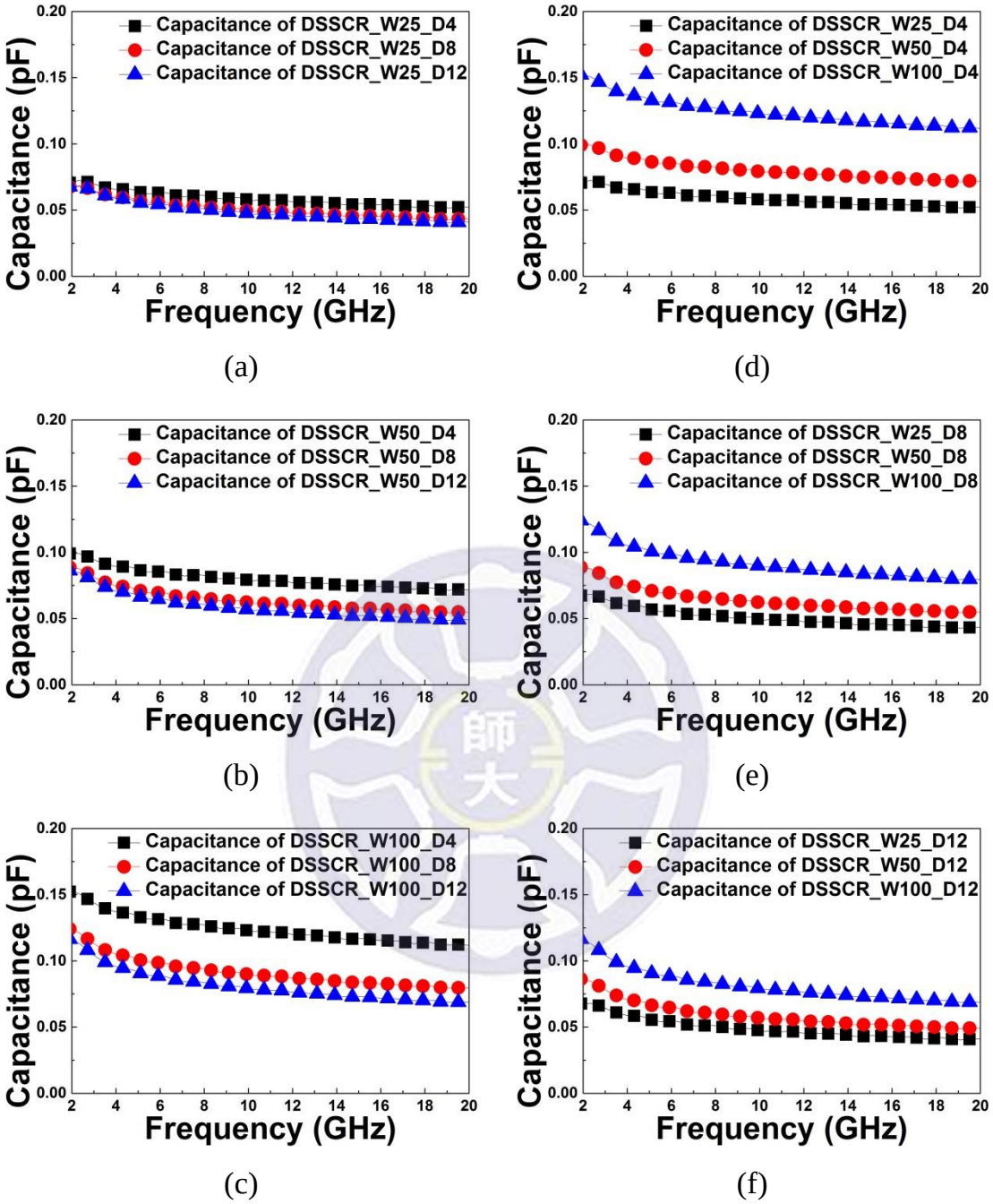


Fig. 2.18 Measured parasitic capacitance for the DSSCRs having (a) 25 μm, (b) 50 μm, and (c) 100 μm SCR width and different numbers of the stacked diodes; losses for the DSSCRs having (d) 4, (e) 8, and (f) 12 stacked diodes and different SCR widths.

Table 2.6 Measured losses and parasitic capacitances of the DSSCRs at different frequencies.

Width of the SCR (μm)	Number of the Stacked Diodes	Loss at 2.4 GHz (dB)	Loss at 5 GHz (dB)	Parasitic Capacitance at 2.4 GHz (fF)	Parasitic Resistance at 2.4 GHz (kΩ)
25	4	0.078	0.118	72	13.9
	8	0.083	0.133	68	7.8
	12	0.088	0.142	68	6.4
50	4	0.126	0.186	99	4.2
	8	0.13	0.196	87	2.8
	12	0.145	0.215	84	2.5
100	4	0.171	0.282	150	2.0
	8	0.197	0.293	120	1.5
	12	0.214	0.313	112	1.4

In the above results, the RFIC measurement system has been used for loss measurement. In the next, the transmission-line-pulse (TLP) testing technique will be adopted for measuring characteristics of the designed ESD devices in this thesis. TLP testing is a common measurement method for analyzing the high-current behavior of circuit devices when ESD occurs. Time-domain stresses are characterized by a narrow pulse width and fast rising and falling times which resembles those of ESD events. A 100-ns square pulse of a TLP system can be simulated by an HBM transient [23]-[27] and is usually used to simulate an ESD

event and inject a high-energy current pulse into a component in a short time. In other words, a narrow square pulse can be used to simulate a short ESD current pulse zapping a protection device. Thus, a time-domain reflectometry TLP system with a 100-ns pulse width is the most often used testing system [28]-[29].

In what follows, TLP testing technique will be used to measure the designed protection devices. The voltage at the first snapback point of the TLP I-V curve is defined as the first breakdown voltage (V_{t1}). In general, the robustness of a diode or an SCR is much stronger than that of a transistor in the internal circuit. Therefore, the second breakdown current (I_{t2}) of the protection element cannot be used as a standard for protecting the internal circuit from ESD attack effectively. Take the 0.18-μm CMOS process as an example, the breakdown voltage of the drain of the transistor is about 15 V. This means that the designed protection elements working in the part of the TLP I-V curve with breakdown voltage over 15 V will not be able to provide effective protection to the drain of the transistor. The current (I_{BV_15}) which corresponds to the 15-V point in the TLP I-V curve will be used as a measure of current-handling ability of the test circuit before the drain of the transistors breakdown [19]. Thus, I_{BV_15} represents the maximum discharging current that protection elements can offer before the drain of the transistor damaged. Similar to the definition of I_{BV_15}, the gate breakdown voltage of the transistor is 10 V, so the current (I_{BV_10}) which corresponds to the 10-V point in the TLP I-V curve is also defined as a measure of current-handling ability of the test circuit before the gate of a transistor damaged.

The measured results are shown in Figs. 2.19-2.21. Figs. 2.19(a)-(c) show the TLP I-V curves of the DSs having the same diode width but different numbers of the stacked diodes. Figs. 2.19(d)-(f) show the TLP I-V curves of the

DSs having the same number of the stacked diodes but different diode widths. V_{t1}, I_{BV_10} and I_{BV_15} of the DSs have also been shown in Table 2.7.

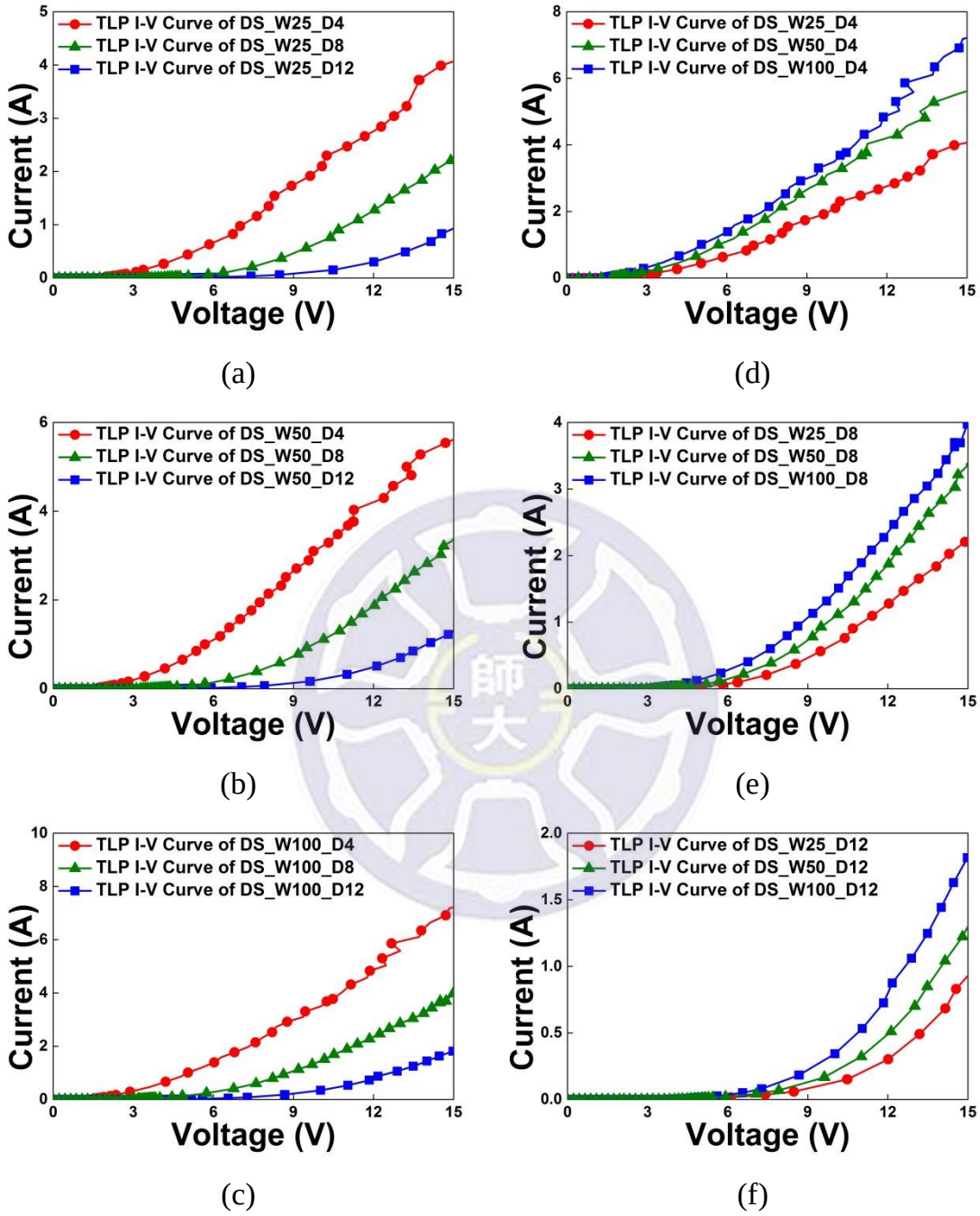


Fig. 2.19 Measured TLP I-V curves for the DSs having (a) 25 μm, (b) 50 μm, and (c) 100 μm diode width and different numbers of the stacked diodes; TLP I-V curves for the DSs having (d) 4, (e) 8, and (f) 12 stacked diodes and different diode width.

Table 2.7 Measured V_{t1}, I_{BV_10} and I_{BV_15} of the DSs.

Width of the Diode (μm)	Number of the Stacked Diodes	Trigger Voltage (V)	I_{BV_10} (A)	I_{BV_15} (A)
25	4	2	2.1	4.1
	8	3.1	0.7	2.2
	12	4	0.12	0.9
50	4	2	3.2	5.6
	8	3	1.1	3.3
	12	3.8	0.2	1.3
100	4	1.85	3.5	7.18
	8	2.9	1.45	3.97
	12	3.8	0.35	1.81

I_{BV_10} and I_{BV_15} correspond to the 10-V and 15-V points in the TLP I-V curve as a measure of current-handling ability of the test circuit before the gate and drain of the transistors breakdown respectively [19].

Shown in Figs. 2.20(a)-(c) are the TLP I-V curves of the DTSCRs with the same diode width but different numbers of the stacked diodes. Those in Figs. 2.20(d)-(f) are the TLP I-V curves of the DTSCRs with the same number of the stacked diodes but different diode widths.

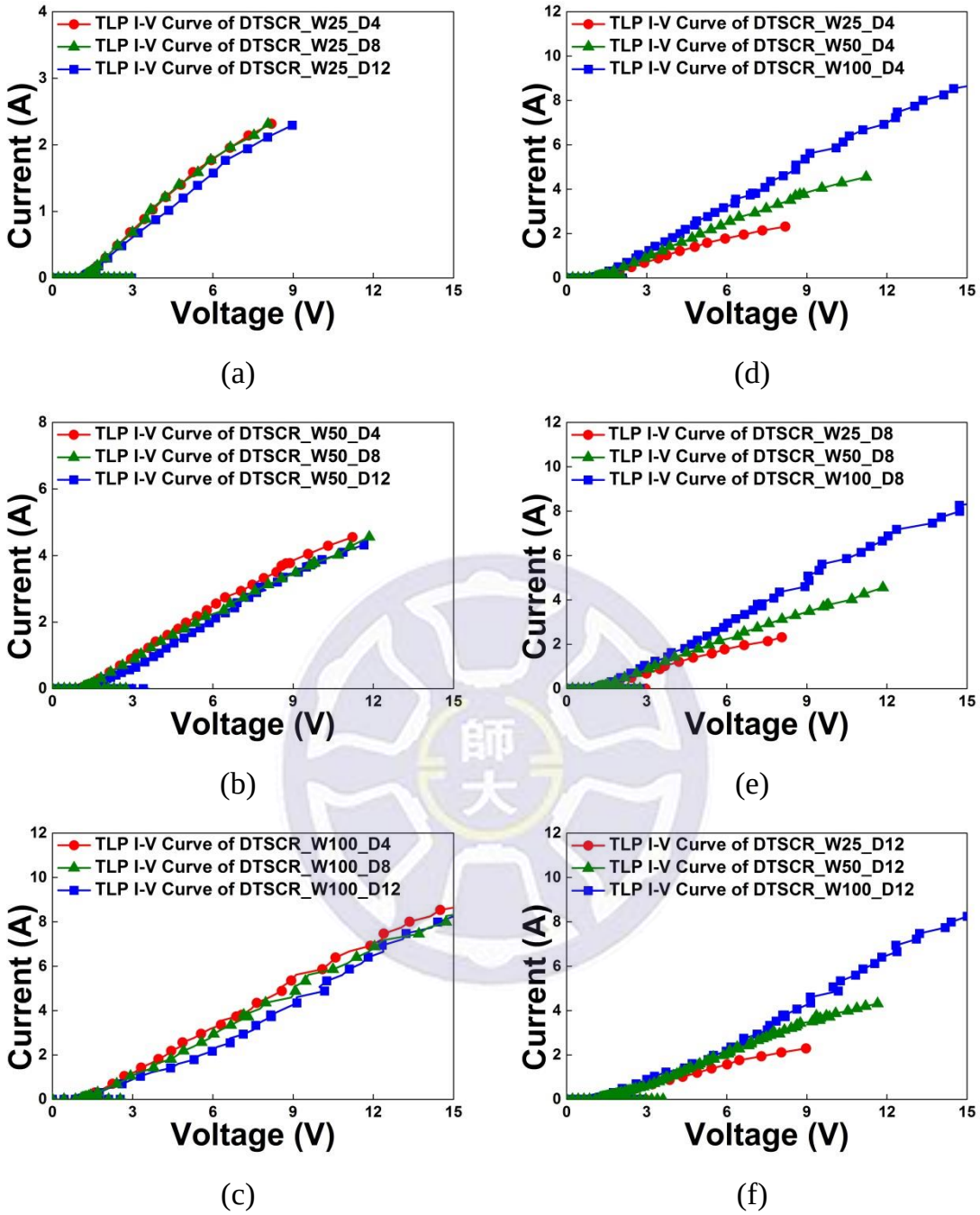


Fig. 2.20 Measured TLP I-V curves for the DTSCRs having (a) 25 μm, (b) 50 μm, and (c) 100 μm SCR width and different numbers of the stacked diodes; TLP I-V curves for the DTSCRs having (d) 4, (e) 8, and (f) 12 stacked diodes and different SCR widths.

Table 2.8 Measured V_{t1}, I_{BV_10} and I_{BV_15} of the DTSCRs.

Width of the SCR (μm)	Number of the Stacked Diodes	Trigger Voltage (V)	I_{BV_10} (A)	I_{BV_15} (A)
25	4	2.1	2.3*	2.3*
	8	3	2.3*	2.3*
	12	3	2.3*	2.3*
50	4	2.1	4.2	4.5*
	8	2.75	3.8	4.5*
	12	3.6	3.8	4.3*
100	4	2.1	5.8	8.6
	8	2.75	5.7	8.3
	12	2.75	4.8	8.3

I_{BV_10} and I_{BV_15} correspond to the 10-V and 15-V points in the TLP I-V curve as a measure of current-handling ability of the test circuit before the gate and drain of the transistors breakdown respectively [19]. (*represents the second breakdown current of test circuits.)

In Figs. 2.21(a)-(c), the TLP I-V curves of the DSSCRs with the same width but different numbers of the stacked diodes are plotted. Shown in Figs. 2.21(d)-(f) are the TLP I-V curves of the DSSCRs with the same number of the stacked diodes but different diode widths. V_{t1}, I_{BV_10} and I_{BV_15} of the DTSCRs and the

DSSCRs have also been shown in Table 2.8 and Table 2.9, respectively.

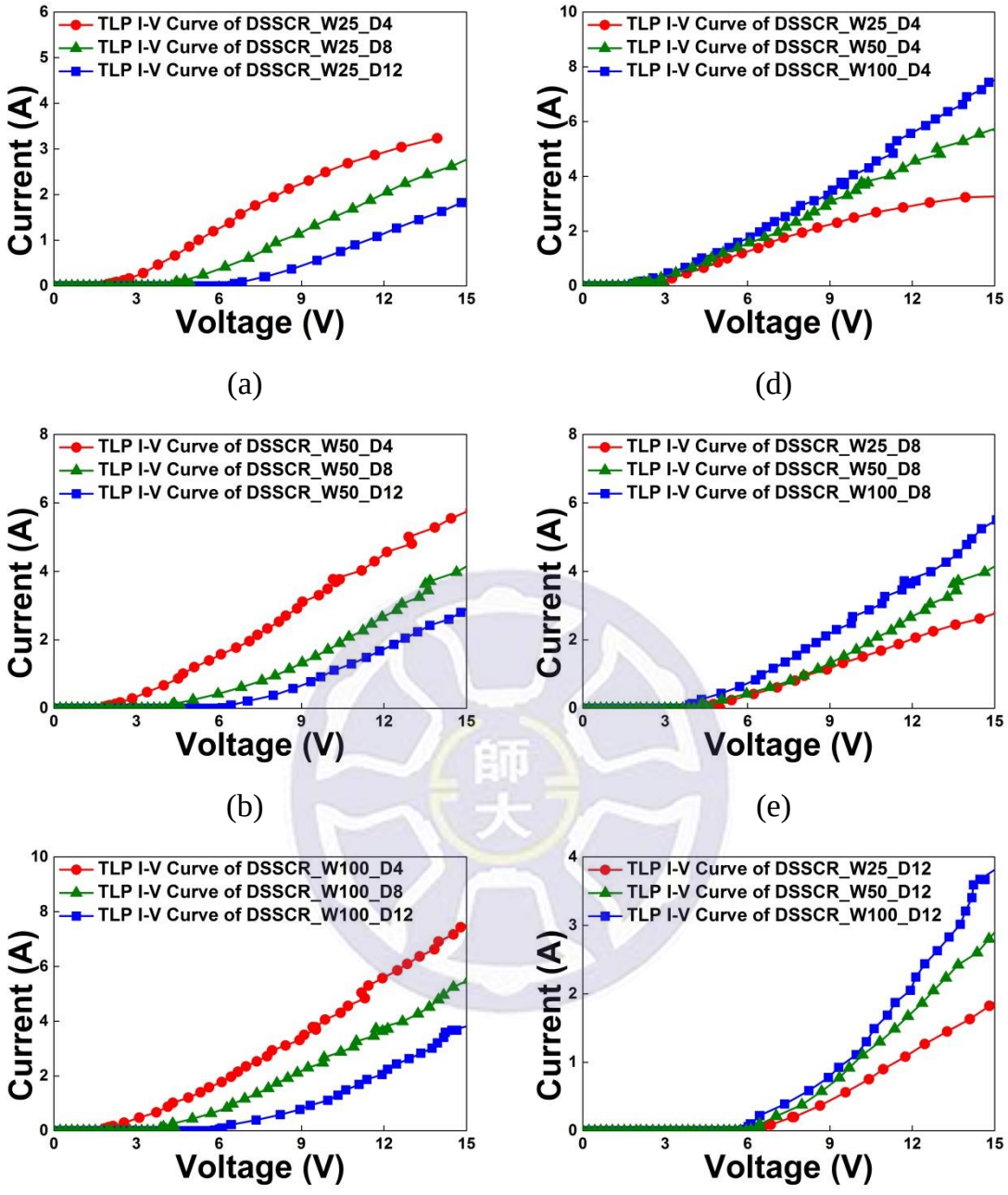


Fig. 2.21 Measured TLP I-V curves for the DSSCRs having (a) 25 μm, (b) 50 μm, and (c) 100 μm SCR width and different numbers of the stacked diodes; TLP I-V curves for the DSSCRs having (d) 4, (e) 8, and (f) 12 stacked diodes and different SCR widths.

Table 2.9 Measured V_{t1}, I_{BV_10} and I_{BV_15} of the DSSCRs.

Width of the SCR (μm)	Number of the Stacked Diodes	Trigger Voltage (V)	I_{BV_10} (A)	I_{BV_15} (A)
25	4	3	2.5	3.3
	8	4.8	1.4	2.7
	12	6.1	0.6	1.9
50	4	3	3.5	5.75
	8	4.7	1.7	4.1
	12	6.1	1	2.9
100	4	3	4.1	7.5
	8	4.5	2.7	5.4
	12	6.1	1.1	3.8

I_{BV_10} and I_{BV_15} correspond to the 10-V and 15-V points in the TLP I-V curve as a measure of current-handling ability of the test circuit before the gate and drain of the transistors breakdown respectively [19].

2.4 Comparison of Traditional and Novel ESD Protection Devices

For protection elements implemented on signal lines, the losses of those are a very important issue, so in this section the losses of the protection elements designed and measured in the previous sections will be first analyzed and compared. For the losses of the protection elements shown in Fig. 2.13, Fig. 2.15, and Fig. 2.17, it is observed that the loss appears to be more chaotic at low frequencies. The deviation could be due to measurement. It is also found that the overall loss at high frequencies is higher than that at low frequencies. Therefore, the influence of the measurement error at low frequencies is more pronounced than at high frequencies due to the relatively smaller loss when operated at low frequencies. Thus even if there is a $\pm$0.1 dB measurement error, it will not affect much the overall performance comparison at high frequencies. On the other hand, the de-embedding method is thinking the metal which is between pad and DUT as a resistor and inductor in series. The parasitic capacitor of the metal coupled by metal and substrate is not considered so the RC model of the DUT we assumed will be affect by it. But the overall characteristics of the comparison will still be quite close.

For the measured losses and parasitic capacitances of the DSs shown in Figs. 2.13(a)-(c) and Figs. 2.14(a)-(c), it can be found that the loss and parasitic capacitance decreases with the increasing number of the stacked diodes. For example, that of 4 stacked diodes is significantly larger than those of 8 or 12 stacked diodes. This is due to the close relationship of the loss and the parasitic capacitances of the protection elements. Fig. 2.22 shows the high-frequency equivalent circuit of a DS. The parasitic capacitance of a diode is formed by the P+/N-Well junction and is denoted by $C_{P+/N\text{-}Well}$. Accordingly, the parasitic

capacitance of n stacked diodes can be expressed as $C_{P+/N\text{-}Well}/n$. Theoretically, increasing the number of the stacked diodes can make the overall parasitic capacitance smaller. However, the parasitic capacitance of a protection element not only comes from the PN junction, but also from the parasitic capacitance between the metal leads. Therefore, the parasitic capacitance does not decrease proportionally to the number of the stacked diodes.

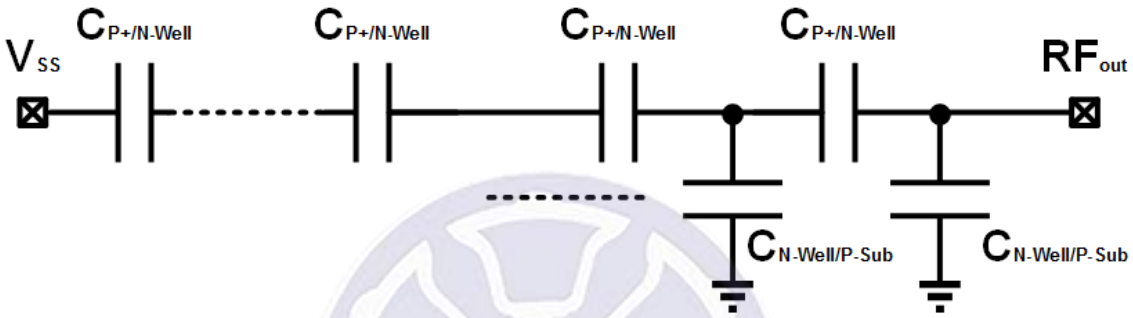


Fig. 2.22 The high-frequency model of the DS.

Also, there is no significant difference between the loss curves of the DSs with 8 and 12 stacked diodes. This is due to the fact that the parasitic capacitance of the DS is contributed by the P+/N-Well junction (namely, $C_{P+/\ N\text{-}Well}$) of the P-type diode and the N-Well/P-Sub (i.e., $C_{\ N\text{-}Well/\ P\text{-}Sub}$) junction just below the RF_{out}. As the number of the stacked diodes increased, the parasitic capacitance contributed by the series of the $C_{P+/N\text{-}Well}$s will be reduced progressively, so that the overall parasitic capacitance of the stacked diodes is dominated by the junction capacitance $C_{N\text{-}Well/P\text{-}Sub}$. Due to this fact, the loss curves for 8 stacked diodes and 12 stacked diodes have no significant difference. On the other hand, a diode with a small cross-sectional area (for instance, the diode with a 25-μm width) will result in a very small parasitic capacitance $C_{P+/\ N\text{-}Well}$. Thus reducing

the parasitic capacitance by stacking diodes of small size is usually not very effective, as shown in Fig. 2.14(a).

For the DTSCR, the measured losses and parasitic capacitances are different from that of the DS. Figs. 2.15(a)-(c) and Figs. 2.16(a)-(c) show that of the DTSCRs with the same SCR cross-sectional area do not vary significantly with the number of the stacked diodes. The loss of the DTSCR with 4 stacked diodes is only slightly larger than that of the DTSCR with 8 and 12 stacked diodes. The reasoning for this behavior is just like the one that was previously mentioned. Since the size of the trigger diodes of the DTSCR is very small relative to that of the DS, the difference in loss for the DTSCRs with 4 and 8 (or 12) stacked diodes is smaller than that for the DS.

Fig. 2.23 shows the high-frequency equivalent circuit of the DTSCR. Its parasitic capacitance is mainly from the various junctions in the SCR (that is, P+/ N-Well, N-Well/P-Well, and P-Well/N+) and from P+/N-Well junction of the trigger diode. The layout top view of DTSCR_W50_D8 shown in Fig. 2.8 indicates that the cross-sectional area of the SCR is much larger than that of the trigger diode. Thus with the number of the stacked diodes kept the same, the parasitic capacitance of the DTSCR increases greatly as the width of the SCR is getting larger, resulting in a significant increase in the loss of protection elements, as shown in Figs. 2.15(d)-(f).

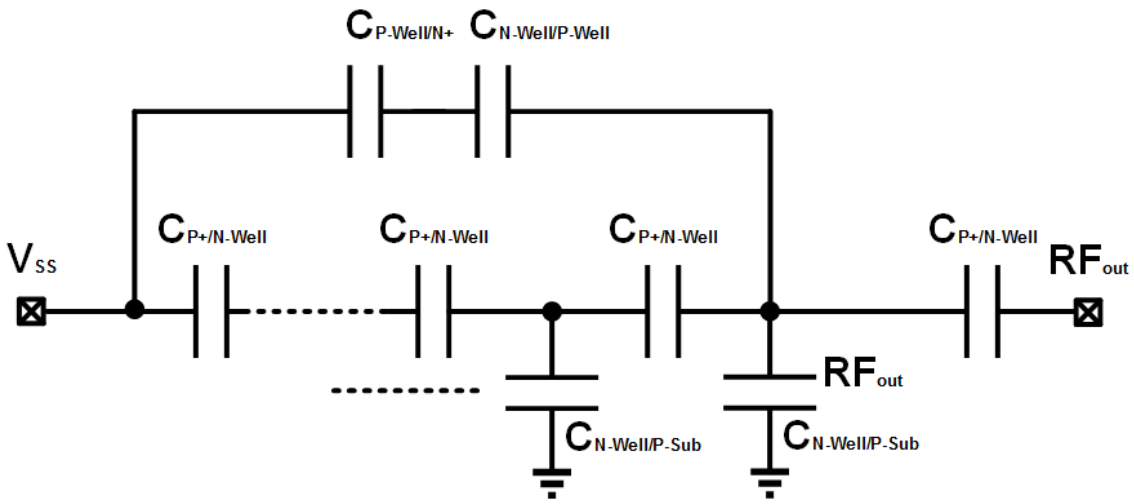


Fig. 2.23 The high-frequency model of the DTSCR.

For the DSSCR, its parasitic capacitance is mainly provided by the trigger diode on the surface of the element and the parasitic SCR below it, as shown in Fig. 2.24. By comparing the losses of the DSSCRs having the same SCR cross-sectional area but different numbers of stacked trigger diodes, it can be found that the measured losses and parasitic capacitances of the one with 4 stacked diodes is significantly larger than that of the one with 8 and 12 stacked diodes, as shown in Figs. 2.17(a)-(c) and Fig. 2.18(a)-(c). The reasoning for that has been stated previously. Since the parasitic capacitance due to the stacked trigger diodes of the DSSCR is similar to that of the DS, the total capacitance is reduced by the series connection of diodes, rendering the loss of the whole protection element smaller.

However, besides the parasitic capacitances of the DSSCR that come from junctions of P+/N-Well and P-Well/N+, there is an additional parasitic capacitance (due to N-Well/P-Sub junction) directly below RF_{out}, as shown in Fig. 2.24. With the increasing number of the stacked diodes, the equivalent parasitic capacitance of the DSSCR will be reduced, and eventually the overall parasitic

capacitance of the DSSCR will be dominated by $C_{N\text{-}Well/P\text{-}Sub}$ below RF_{out}. This is why there is no significant difference in losses of the DSSCRs with 8 and 12 stacked trigger diodes, as shown in Fig. 2.17(b) and Fig. 2.17(c). On the other hand, for the DSSCR with the SCR width 25 μm, since the diode parasitic capacitance $C_{P+/N\text{-}Well}$ itself is very small, reducing the parasitic capacitance by increasing the number of the stacked diodes is not very noticeable, as shown in Fig. 2.17(a) and Fig. 2.18(a).

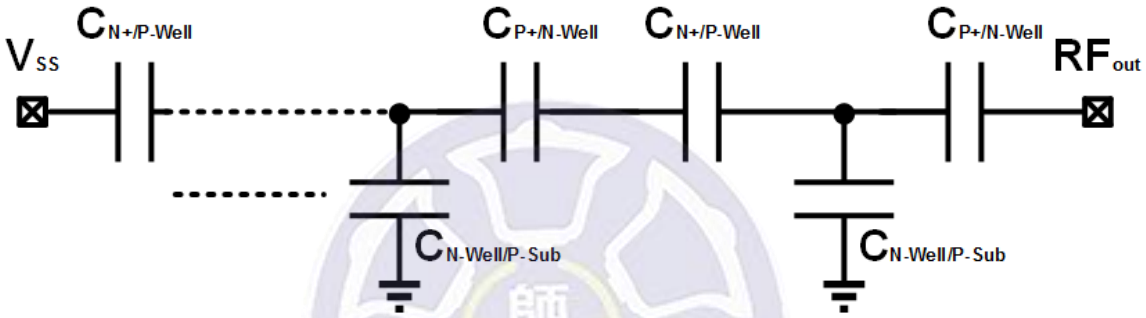


Fig. 2.24 The high-frequency model of the DSSCR.

Besides the doping concentration of the PN junction, the cross-sectional area is definitely a key factor which determines the scale of the parasitic capacitance. It can be seen in Figs. 2.18(d)-(f) that the parasitic capacitance increases greatly with the increase of the diode size of the DSSCR while the number of the stacked diodes is fixed, and thus results in significant increase in the loss of the protection element.

The characteristic of the protection element is the most important part of the ESD protection design. After analyzing the loss of the components, the data obtained using the TLP measurement system in the next will be analyzed and compared.

Both the DS and the DTSCR have cascaded P-type diodes, and in general the structure of the P-type diode has the parasitic p-n-p BJT (consisting of P+/N-Well/P-Sub layers). When cascading the P-type diodes, the parasitic p-n-p BJTs are also cascaded, and this will lead to the Darlington effect. That is, the emitter of one parasitic p-n-p BJT is connected to the base of another that follows it. For such a case, the current of the diode string will be decreased β times with the increasing number of the stacked diodes as compared with that of an individual diode. As the number of the stacked diodes is continuously increased, the current flowing through the diode string is getting smaller, and eventually less than the current of the collector below. Under such a condition, the collector current is dominant and will be used to determine the trigger voltage across the component [30].

In this research, the ADS software is also used for simulation of the Darlington effect. To do that, the p-n-p BJT of 1.8V_10x10 is used as the parasitic transistor in the DS structure, and the parasitic resistance between the N-Well and P-Sub layer is set to be 50 ohm. Since the collector current of the p-n-p BJT will ultimately flows through the parasitic diode (namely, the P-Sub/N-Well junction) that is closest to the cathode, the parasitic diode was also considered in the simulation. In simulation, the current is divided into two independent paths for performance observation and comparison. The parasitic architecture of the simulated DS is shown in Fig. 2.25. The emitter of each p-n-p BJT is connected to the base of the preceding BJT, and the base is connected to the emitter of the subsequent BJT. Simulation shows that the overall current (namely, $I_1 + I_2$) decreases with the increasing number of the stacked diodes, which is due to the longer discharging path. The current ratio (I_2 / I_1) was

observed to increase with the increasing number of the stacked diodes, that is, the influence of the parasitic path on the conduction voltage increases when the number of the stacked diodes is increased, as shown in Table 2.10.

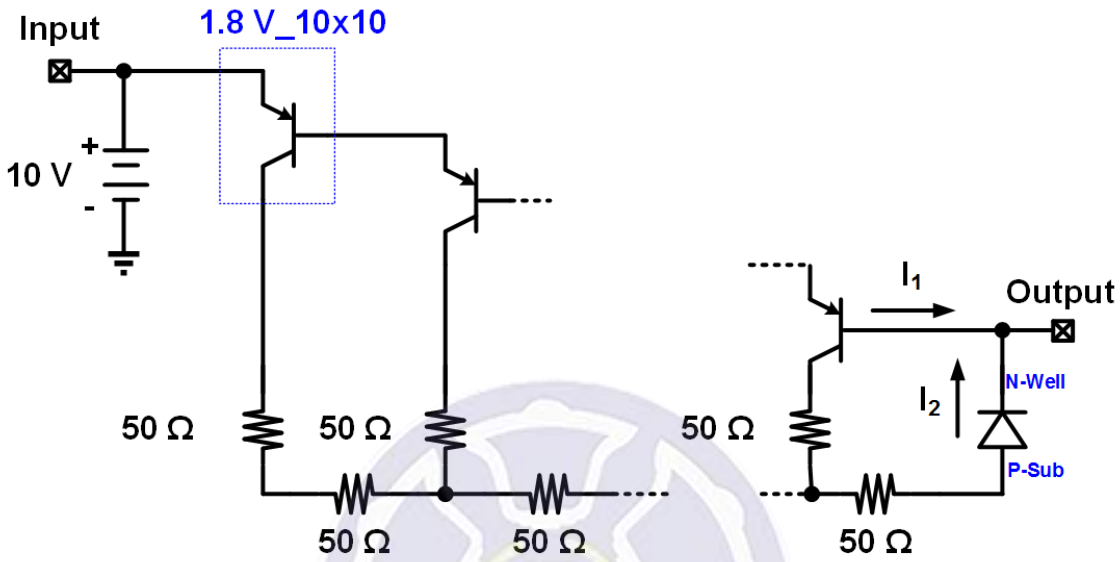


Fig. 2.25 The equivalent circuit of the parasitic p-n-p BJT in diode string.

Table 2.10 Simulated I_1 and I_2 of the parasitic p-n-p BJT in diode string.

Number of the Stacked Diodes	Branch Current (mA)	Current (mA)	I_2/ I_1
4	I_1	80.5	0.472
	I_2	38	
8	I_1	23.4	0.649
	I_2	15.2	
12	I_1	5.59	1.112
	I_2	6.22	

Figs. 2.19-2.21 are the TLP I-V curves of the designed protection elements. Fig. 2.19 shows the TLP I-V curve of the DS. In Figs. 2.19(a)-(c), it can be found that V_{t1} of the DS increases with the number of the stacked diodes. This is due to the fact that in order to avoid the influence of Darlington effect on V_{t1} of the designed DS, the distance between the P-type diodes in the DS has been increased to reduce the collector current of the parasitic p-n-p BJT as much as possible so that V_{t1} will not be affected.

For the ESD protection DS, with the size of the diode fixed, $1/R_{on}$ of the TLP I-V curve will be affected by the number of the stacked diodes. This is because that the main discharging path is just the DS itself, and the distance of the discharging path increases with the increasing number of the stacked diodes, rendering the overall parasitic resistance of the discharging path larger. On the other hand, for the DSs having the same number of the stacked diodes but different diode size, their voltage drops can be different even the DSs are flowing the same current. It is seen in Figs. 2.19(d)-(f) that the larger the diode's size, the smaller the voltage across the protection element. This means that the parasitic resistance of the protection element (DS) is reduced with the increasing diode cross section.

However, providing the ESD protection of the power amplifier using series-connected diodes is not an ideal way since the parasitic resistance of the protection DS increases as the number of the stacked diodes increases. Fig. 2.19(c) shows the TLP I-V curve of the DSs with different number of the stacked diodes. The red, green, and blue curves are for the cases of 4, 8, and 12 stacked diodes, respectively. In the figure, it is found that if the DS current is fixed at 0.3

A, the voltages across the DSs of the above three cases (corresponding to the red, green, and blue curves) are 3.7 V, 7.2 V, and 9.6 V, respectively. It indicates that a smaller number of the stacked diodes will result in a smaller voltage across of the DS under the same operating current, and the dissipated power will also be relatively smaller. The resistance R_{on} for 4, 8, and 12 stacked diodes can be evaluated from Fig. 2.19(c) to be 4.98, 7.9, and 12.2 ohms, respectively. This shows that the larger the number of the stacked diodes, the larger the R_{on}. In contrast, R_{on} will be smaller.

The situation stated above is a serious problem to the ESD protection design of power amplifiers using DS. On one hand, more diodes in series is needed to avoid distortion of the large-swing signal; but on the other hand, the parasitic resistance of the DS will also be increased and it may result in a large enough voltage to damage the internal circuit when the static current flowing through the DS. In short, there may exist a special situation that the internal circuit under ESD protection is damaged before the protection elements when the electrostatic attack occurs.

The shortcoming of the DS can be improved by using DTSCR in protection device design. Fig. 2.20 shows the TLP I-V curve of the DTSCR. In design of the DTSCR, its trigger-diodes is similar to the DS. In order to avoid the Darlington effect of the DTSCR, the separation between the P-type diodes is also made larger. However, V_{t1} of the DTSCR in Table 2.8 shows that it does not increase proportionally to the increase of the stacked diodes. In order to know the reasoning for that, the DS structure in Fig. 2.5(b) and the DTSCR in Fig. 2.7(b) were compared. In DTSCR, the parasitic p-n-p BJT that is closest to RF_{out} is composed of P+, N-Well, and P-Well layers. This is different from the structure

of the parasitic p-n-p BJT in DS. This difference leads to a higher beta gain of the parasitic p-n-p BJT in DTSCR and makes the Darlington effect more pronounced. Therefore, the trigger voltage is almost the same for the DTSCRs with 8 and 12 stacked diodes.

Another difference between the DTSCR and the DS is that increasing the number of the stacked diodes does not cause a significant change in R_{on} of the DTSCR because the trigger diode is not the main ESD discharging path [31], [32]. The holding voltage, V_h, of the DTSCR is also found to be almost fixed in Fig. 2.20. This is due to that the main discharging path of the DTSCR is provided by the SCR, not the stacked diodes. When the SCR is triggered on, it will maintain a low and fixed voltage across the element and provide a low-resistance discharging path. Since there is only one SCR in the structure of the DTSCR, it will determine the V_h of the DTSCR. It is seen in Figs. 2.20(d)-(f) that with the number of the stacked diodes fixed, the larger the SCR size, the smaller the voltage across the protection element DTSCR. It means that the parasitic resistance of the protection element is reduced as the SCR size is increased.

Fig. 2.21 shows the TLP I-V curves of different DSSCRs. It can be seen that V_{t1} of the DSSCR increases as the number of the stacked diodes increases, as shown in Figs. 2.21(a)-(c). With the same diode width, the number of the stacked diodes will determine R_{on} of the DSSCR. In addition, the DSSCR is different from the DS that besides the trigger diodes in the upper part of the element, the DSSCR have an SCR discharging path in parallel, so that the equivalent resistance of the DSSCR is smaller than that of the DS with the same length of the discharging path. With the increased number of the stacked diodes, the parasitic SCRs in the lower part of the element structure are also cascaded and

thus lengthen the discharging path, making the overall parasitic resistance of discharging path growing. With the number of the stacked diodes fixed, R_{on} and the current of the DSSCR is reduced as the diode size increases. It can be seen in Figs. 2.21(d)-(f) that the larger the SCR size, the smaller the voltage across the protection element. This means that the total parasitic resistance of the protection element is reduced. This can be explained as that in the DSSCR, the parasitic SCR is in parallel with the stacked diodes. When the SCR size is increased, its resistance will be reduced, and this also reduces the parallel resistance of the DSSCR, rendering the decrease in the whole parasitic resistance of the protection element.

Fig. 2.26 also implies the effective conduction of the parasitic SCR in the DSSCR. If the DS and the DSSCR were compared, it would be found that R_{on} of DSSCR is significantly smaller than that of the DS. The structure of the DSSCR is composed of series P-type and N-type diodes, but the DS is composed of all P-type diodes. It is known that R_{on} of the N-type diode is larger than that of the P-type diode. So if the parasitic SCR in the lower part of the protection element is not turned on, the TLP I-V curve of the DSSCR will be similar to that of the DS. But in Fig. 2.26, R_{on} of the DSSCR is less than that of the DS, implying that the parasitic SCR in DSSCR is indeed conducting.

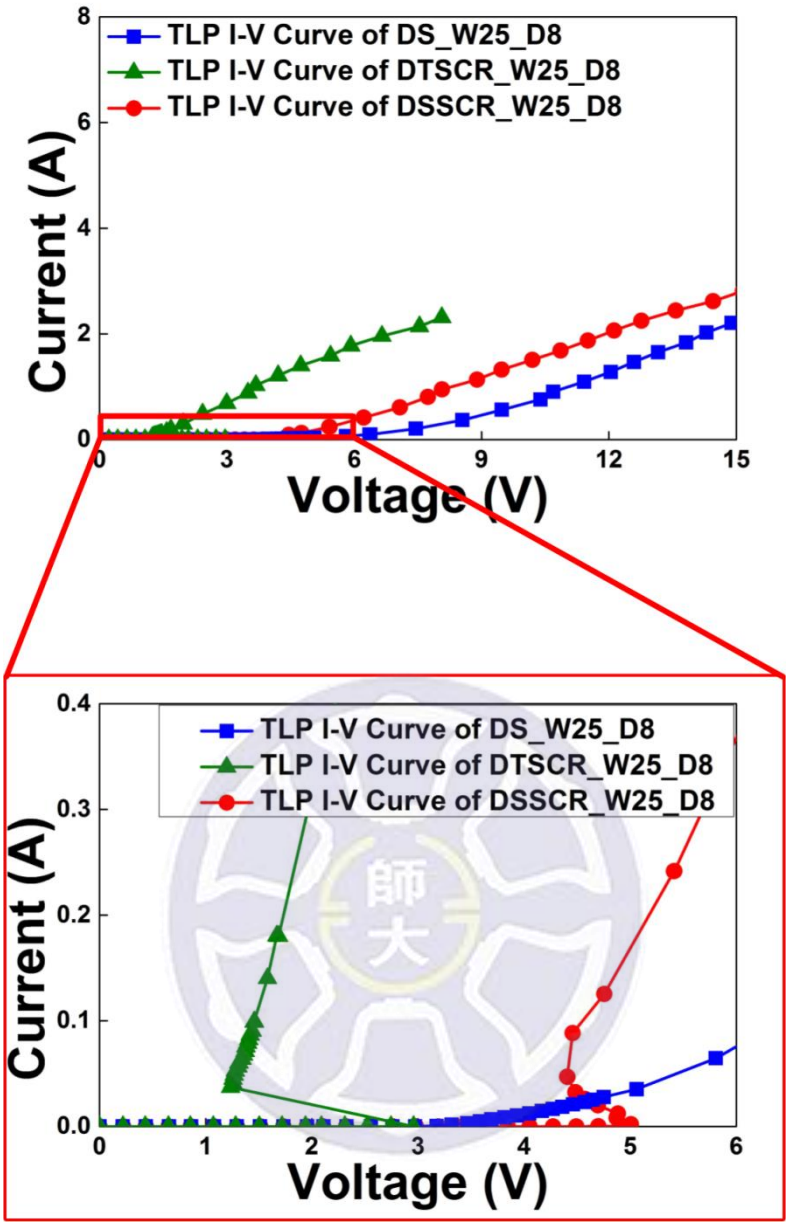


Fig. 2.26 Comparison among TLP I-V curves of DS_W25_D8, DTSCR_W25_D8, and DSSCR_W25_D8.

Next, the comparison of the TLP I-V curves of three protection devices will be examined. Fig. 2.26, Fig. 2.27, and Fig. 2.28 show that the sequence of R_{on} values from large to small are DS, DSSCR, and DTSCR, respectively. The difference in R_{on} can be attributed to different discharging paths of three designed protection devices. It is seen in this figure that DTSCR_W50_D8 provides

essentially a single path the parasitic SCR is turned on and its holding voltage is about 1.1 V. However, since DSSCR_W50_D8 has four parasitic SCRs in series, and the structure of each parasitic SCR is the same as that of the DTSCR, the holding voltage of the DSSCR is about 4 times that of the DS (namely, 4.4 V).

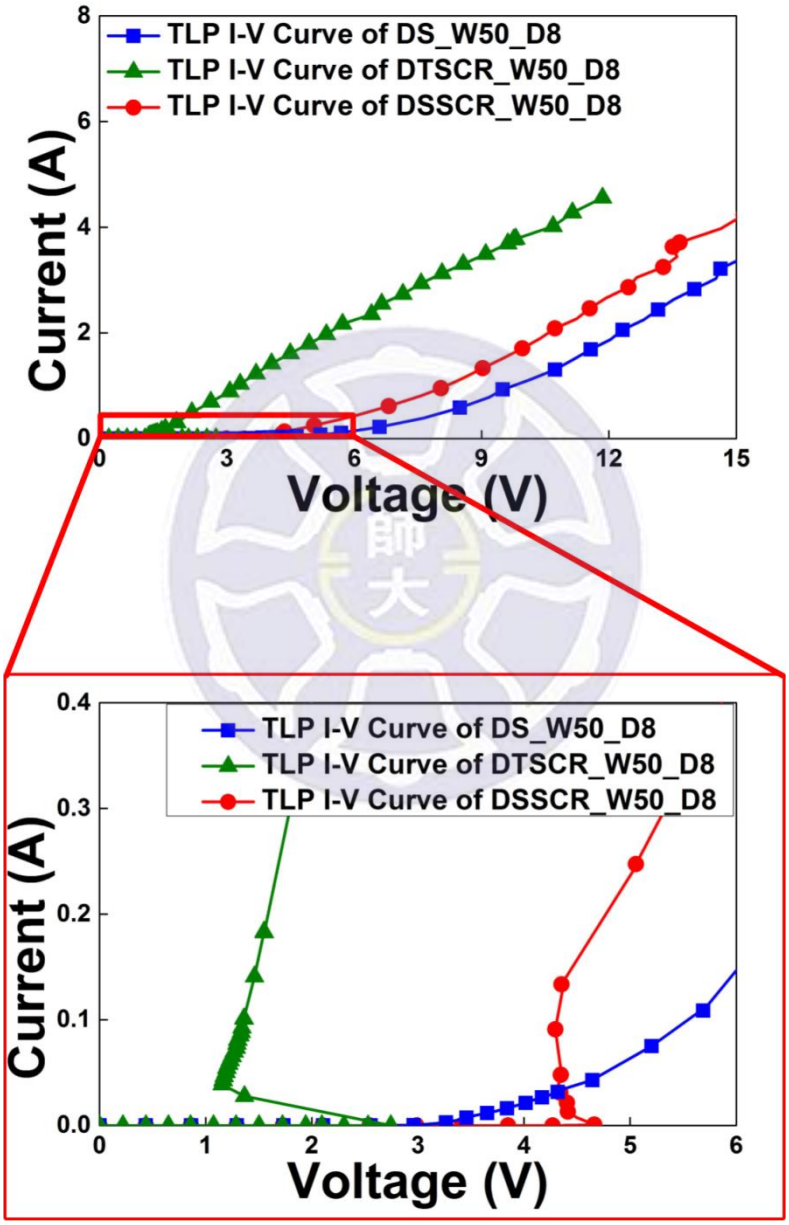


Fig. 2.27 Comparison among TLP I-V curves of DS_W50_D8, DTSCR_W50_D8, and DSSCR_W50_D8.

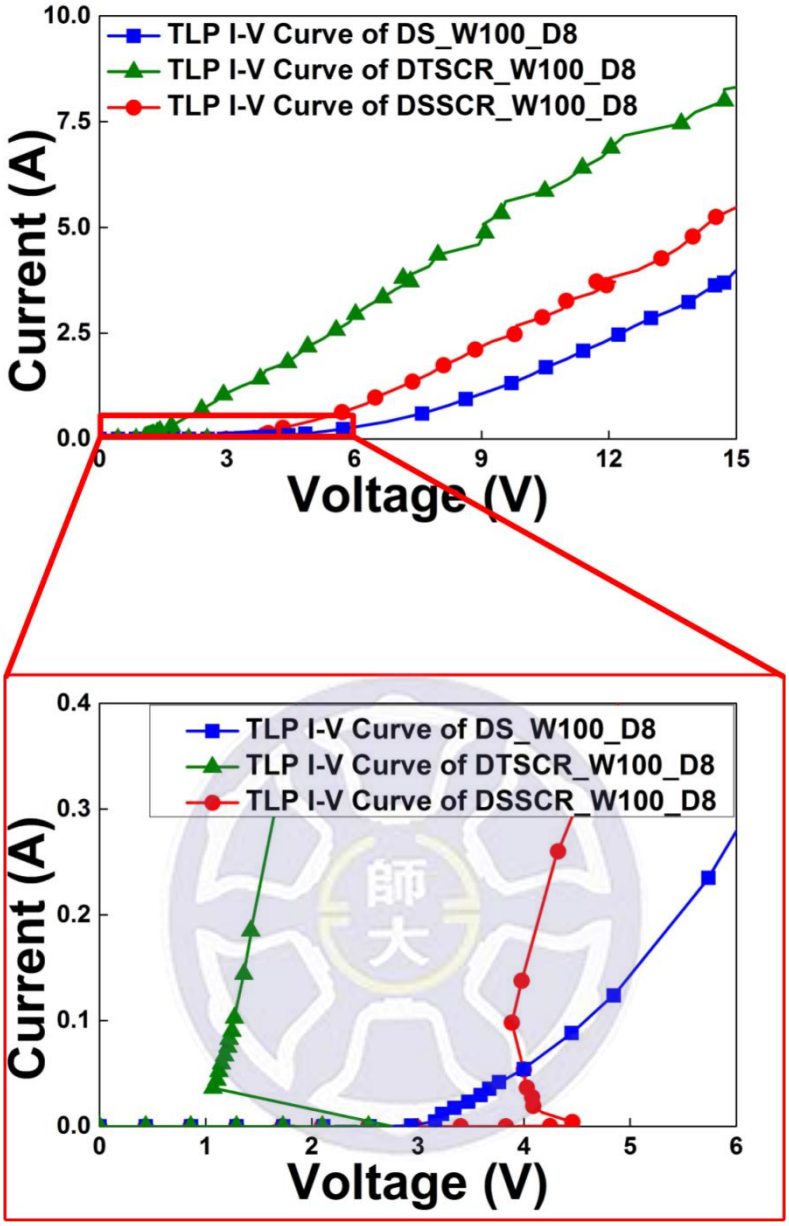


Fig. 2.28 Comparison among TLP I-V curves of DS_W100_D8, DTSCR_W100_D8, and DSSCR_W100_D8.

Since this study is aimed at the ESD protection circuits connected between RF_{out} and V_{SS}, the best ESD protection circuit needs to meet the requirement of the ESD design window provided by PAs and meanwhile possesses the best protection capability. From the above conditions, a figure of merit (FOM) related to I_{BV} and V_h can be defined, as shown in Eq. (2.8). The holding voltage of the

ESD protection circuits is defined as the voltage values of TLP I-V curve under 0.1 A operating current. The constant 3.6 represents the operating voltage between the RF_{out} and V_{SS}. The denominator of the Eq. (2.8) should be positive and smaller, indicating that the power by the ESD protection circuit is relatively smaller. If the denominator of the Eq. (2.8) is negative, the ESD protection circuit will have the risk of latch-up. The I_{BV} in the numerator is positively correlated with the protection capability. So the greater the FOM is, the higher the effectiveness of the ESD protection circuit is.

$$\text{FOM} = \frac{I_{BV}}{V_h - 3.6} \tag{2.8}$$

FOM of the designed circuits have also been shown in Table 2.11. Table 2.11 shows that DTSCRs have the risk of latch-up problem. FOM of the DS_W50_D8 is 2.06 mho and FOM of the DSSCR_W50_D8 is improved to 6.83 mho. FOM of DSSCR_W50_D8 is over three times that of DS_W50_D8.

Table 2.11 The FOM of all ESD protection circuits.

Notation	FOM (mho)	Notation	FOM (mho)	Notation	FOM (mho)
DS_W25_D4	-5.85	DTSCR_W25_D4	-1.04	DSSCR_W25_D4	-2.53
DS_W25_D8	1.15	DTSCR_W25_D8	-1.09	DSSCR_W25_D8	3
DS_W25_D12	0.25	DTSCR_W25_D12	-1.09	DSSCR_W25_D12	0.59
DS_W50_D4	-5.09	DTSCR_W50_D4	-1.95	DSSCR_W50_D4	-3.83
DS_W50_D8	2.06	DTSCR_W50_D8	-1.87	DSSCR_W50_D8	6.83
DS_W50_D12	0.40	DTSCR_W50_D12	-1.86	DSSCR_W50_D12	1.03
DS_W100_D4	-4.48	DTSCR_W100_D4	-3.58	DSSCR_W100_D4	-4.16
DS_W100_D8	4.41	DTSCR_W100_D8	-3.77	DSSCR_W100_D8	10.8
DS_W100_D12	0.54	DTSCR_W100_D12	-3.45	DSSCR_W100_D12	1.52

$$\text{FOM} = \frac{I_{BV}}{V_h - 3.6}$$

2.5 Summary of This Chapter

To close this chapter, the above analysis and comparison of the three designed protection devices are summarized. First of all, if the element size is the same, the losses and parasitic capacitance of the DSSCR and the DS are almost

the same, while that of the DTSCR is smaller than the other two. For I_{BV}, the measured data can offer a sequence of DTSCR > DSSCR > DS.

In the comparison of the FOM, all the DTSCRs are negative values may cause the latch-up problem to the PA. Both FOM of the DSSCRs and DSs are positive values and FOM of the DSSCRs are better than the DSs in the same size, which indicates DSSCRs can discharge more current than DSs without latch-up problem.

Finally, for the ESD protection, the traditional DS avoids PA signal distortion by increasing the number of the stacked diodes. But this also increases the parasitic resistance and eventually may not be able to provide effective ESD protection to the internal circuit. The DTSCR has lots of advantages in loss and I_{BV}, but its V_h is too low that may cause the circuit latch-up problem. The preceding analysis also shows that the trigger voltage of the DTSCR cannot be designed by merely varying the number of staked diodes and there may exist miss-triggering problem due to the serious Darlington effect. In particular, the DTSCR cannot be designed with a higher V_{t1}, and hence is not suitable for ESD protection of large-swing-signal PAs. Compared with the above two ESD protection devices, the DSSCR can simultaneously avoid large-swing-signal distortion of PAs and improve the protection capability. Therefore, it is a better choice for ESD protection.

Chapter 3

2.4 GHz Power Amplifier with Novel ESD Protection Design

3.1 Reliability of CMOS Power Amplifier

For implementation and fabrication of integrated RF circuits, the gallium arsenide (GaAs) process has better performance than that of the CMOS. But the CMOS process has more advantages of circuit integration and lower cost. This makes the CMOS process one of the mainstreams in IC design. With the advance of fabrication process, the size of the RF circuits keeps reducing [33]. However, the reliability of the RF circuits decreases with the size. Thus, circuit size reduction renders the problem of reliability knotty.

In addition, ESD is an important part of numerous reliability issues. For RF circuits, the power amplifier is the back-end circuit and is often an entrance of the ESD stress. Therefore, protection circuit design for RF power amplifiers is one of the primary interests for researchers in this area. In this chapter, three configurations of the ESD protection design are proposed for applications in power amplifiers. The designed circuits are realized using 0.18-μm CMOS process. The reliability issue will be discussed and the measured results will be examined and analyzed.

3.2 Design of Power Amplifiers

For a PA, since it usually handles relatively large signals, the small-signal approximations and models either are not applicable or must be used with care. This is different from that of the general RF amplifier circuits. Nevertheless, linearity remains a very important requirement for PAs. As the input signal of the PA becomes larger and larger, the output signal can be saturated eventually, causing a non-linear relationship between the input and the output signals. On the other hand, PA has a large-swing signal that causes difficulties in the ESD protection design. To measure the linearity, the OP_{1dB} (namely, the 1-dB gain compression point which indicates the power level that causes the gain to drop by 1 dB from its small signal value) is a common standard which are used to estimate the upper limitation of the linear operating region of a PA.

In this chapter, since the class AB power amplifier can virtually eliminates the crossover distortion and has other advantages, it will be designed and used as a verification circuit for the ESD protection designs. On designing a power amplifier, it needs first to determine the operating voltage of the transistor. Different operating voltage will determine the type of the power amplifier. For the standard 0.18-μm CMOS process, the drain voltage of a single transistor is 1.8 V, which is the maximum allowable value of drain voltage in transistors provided by the foundry factory. In Fig. 3.1, it shows that the gate bias voltage should be set at about 0.8 V in order to design a class AB PA.

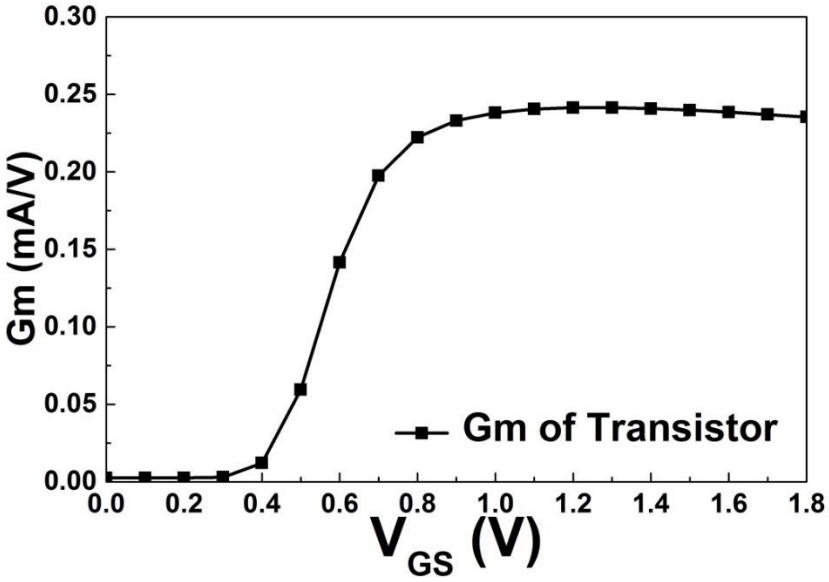


Fig. 3.1 Response of G_m versus V_{GS} of the MOSFET.

Since the amplifier is used for amplifying the input signal, the MOSFET must operate in the saturation region (i.e., the linear region). The I-V equation and the transconductance, G_m, of the MOSFET for the saturation region are listed in Eq. (3.1) and Eq. (3.2), respectively.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{3.1}$$

$$G_m = \mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th}) \tag{3.2}$$

When the bias voltage is fixed, to obtain higher output power of PA, the bias current should be larger. In Eq. (3.2), it indicates that the transconductance (and thus the gain) is higher when the channel length of the MOSFET is shorter. Due to this, the channel length would be chosen as 0.18 μm and V_{DD} be chosen as 1.8 V. The maximum gate width of the NMOS_RF (that the foundry can offer) is 8 μm and the number of fingers is 64. If a larger current is needed, a transistor of larger size should be used.

In the design of the power amplifier, the cascode configuration, as shown in

Fig. 3.2 is adopted because its gain and high frequency response are relatively better than that of the single-stage common source (CS) amplifier.

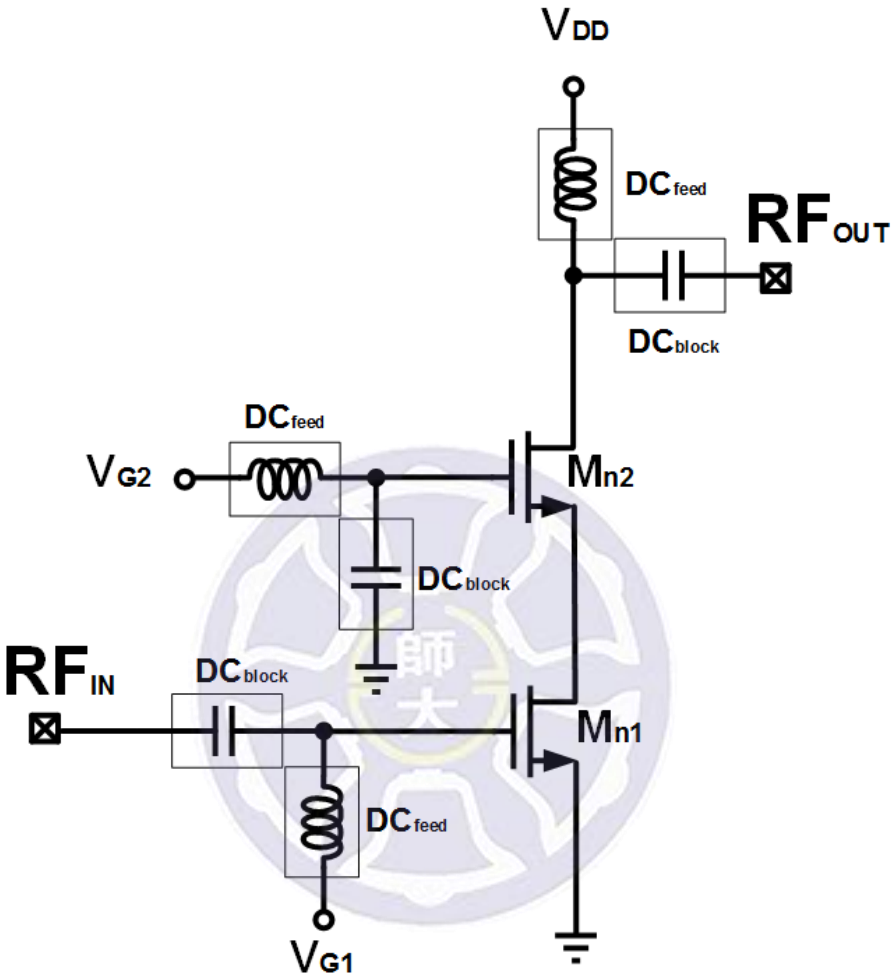


Fig. 3.2 The cascode amplifier configuration.

The input bypass circuit is composed of two capacitors and one resistor, as shown in Fig. 3.3. It is seen in Fig. 3.3 that the bypass circuit produces a transmission zero at its resonant frequency of 10.6 GHz which is calculated by taking into consideration the parasitic inductance of the components, as shown in Fig. 3.4.

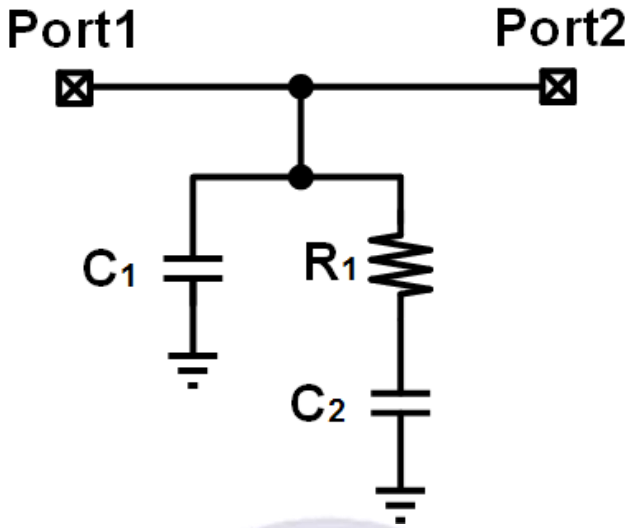


Fig. 3.3 The configuration of the bypass circuit.

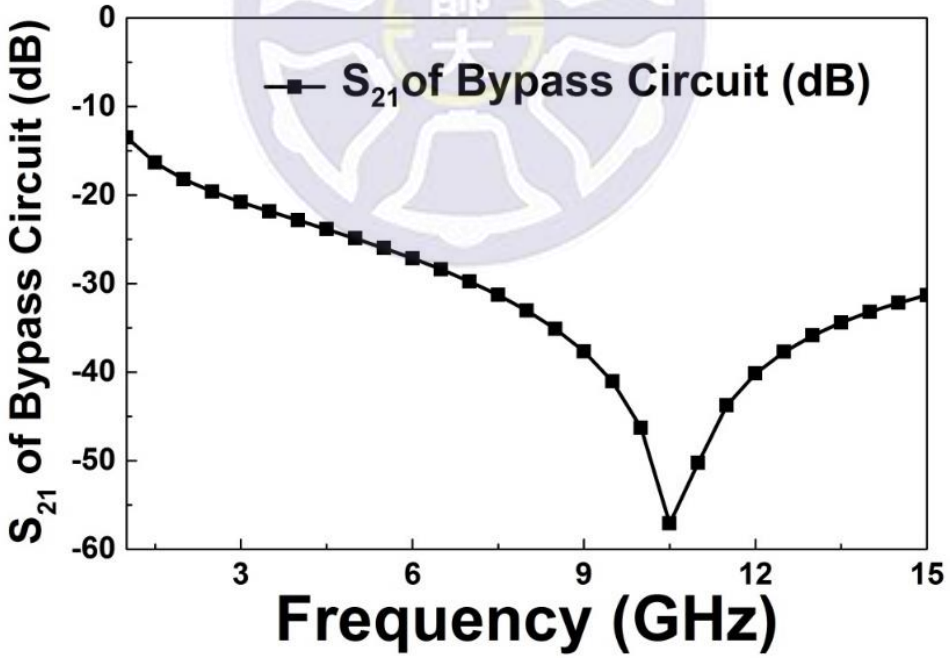


Fig. 3.4 S_{21} of the bypass circuit. Note that a transmission zero is seen at 10.6 GHz.

For impedance matching of the PA, the conjugate matching method is used for the input matching network, whereas the output matching network is used to convert the load impedance R_L to the optimal output impedance, $Z_{optimal}$, seen from the drain of the transistor into the input of the output matching network, as shown in Fig. 3.5. With the output impedance being optimal, PA can deliver the maximum output power.

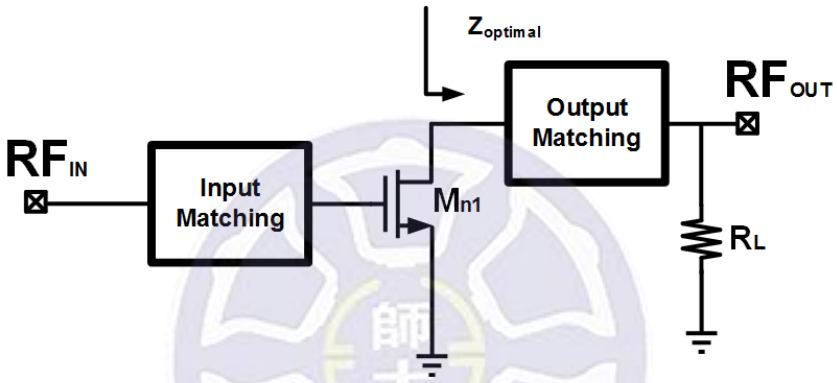


Fig. 3.5 The amplifier with matching networks.

Because it is desirable to simulate the PA in a case without output matching network, the output matching network will be implemented on the PCB rather than on the wafer, as shown in Fig. 3.6. The size of the components and the power supplies used in the PA circuit are summarized in Table 3.1.

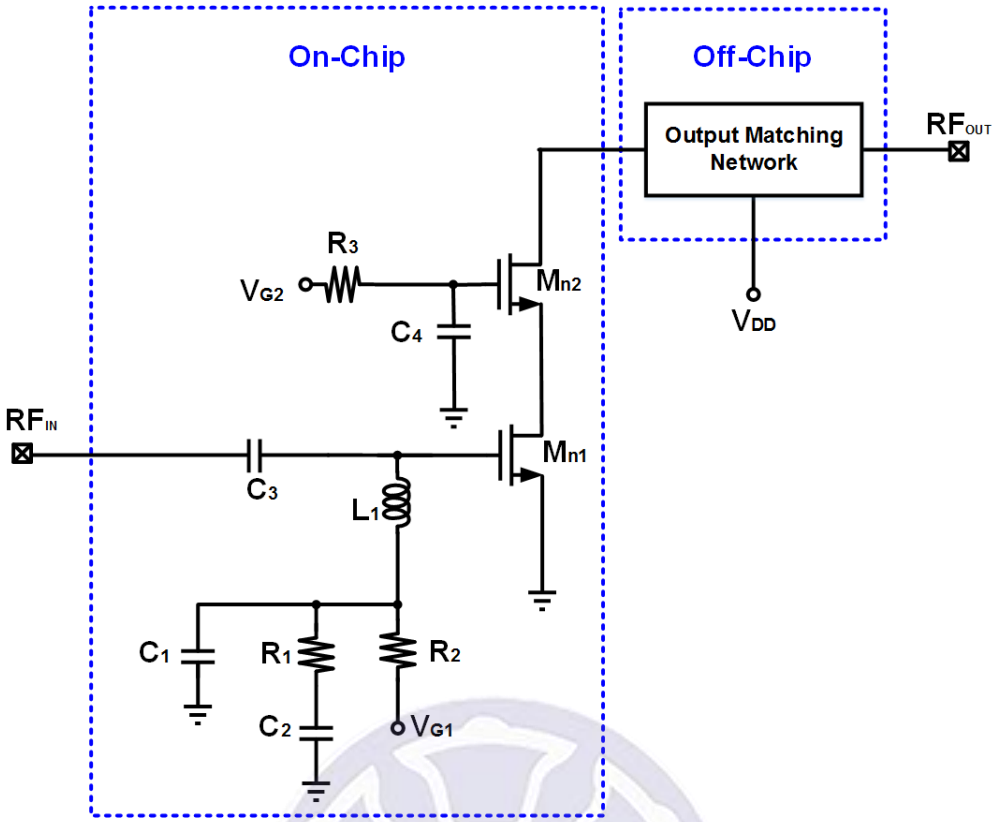


Fig. 3.6 The configuration of power amplifier with off-chip matching circuit.

Table 3.1 Component sizes of the power amplifier.

Device	Value (pF)
C_1	15.22
C_2	15.22
C_3	0.71
C_4	11.41

Device	Value (Ω)
R_1	4.9
R_2	337.3
R_3	2.01k

Device	Value (nH)
L_1	3.11

Device	Value (V)
V_{G1}	0.8
V_{G2}	2.6
V_{DD}	3.6

In the output matching network, the size of the surface-mount devices (SMD) components is summarized in Table 3.2. The photo of the output matching network among SMA connector, SMD components, and PCB is shown in Fig. 3.7. Also, the parasitic effects on PCB are taken into account. The parasitic inductance of each element and the via hole on PCB are estimated to be 0.6 nH and 1 nH, respectively. The sub miniature version A (SMA) connector is equivalent to a 4-Ω resistor and a 0.6-nH inductor in series shunt a 2-pF capacitor.

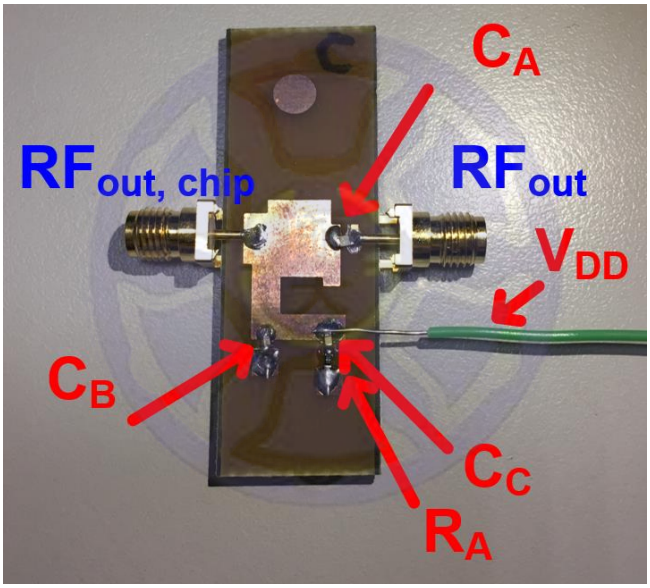
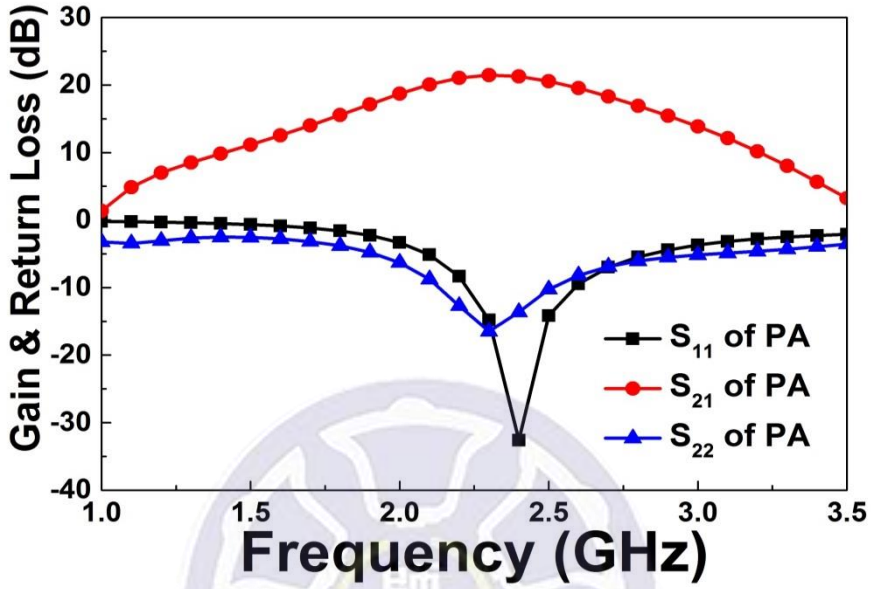


Fig. 3.7 The photo of the output matching network among SMA connector, SMD components, and PCB.

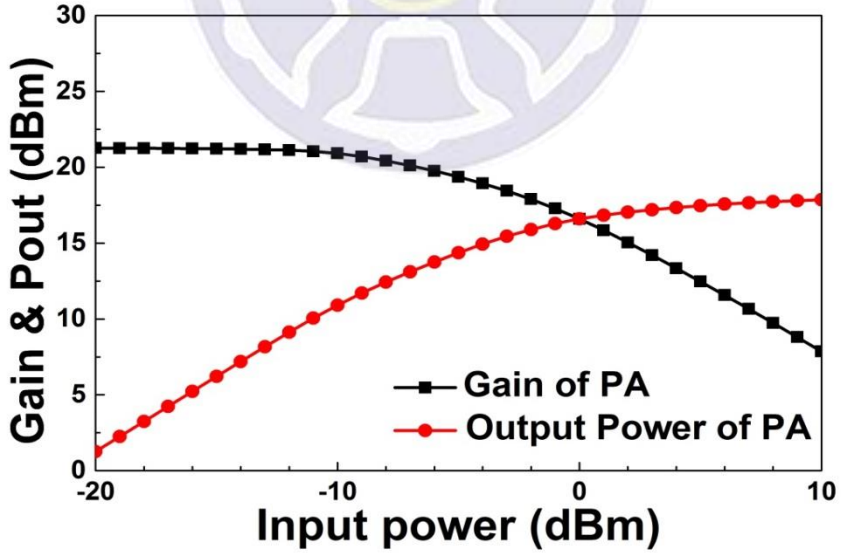
Table 3.2 The sizes of the SMD components.

Device	C_A	C_B	C_C	R_A
Value	15 pF	20 pF	20 pF	22 Ω

The simulated *S*-parameters and power sweep of the designed PA with PCB consideration are shown in Fig. 3.8(a) and Fig. 3.8(b). The value of S_{21}, S_{11}, and S_{22} is, respectively, 21.2 dB, -32.6 dB, and -13.6 dB at 2.4 GHz. In Fig. 3.8, it indicates that the OP_{1dB} is 13.1 dBm.



(a)



(b)

Fig. 3.8 The simulated (a) *S*-parameters and (b) power sweep of the designed power amplifier with PCB consideration.

3.3 Architecture of the PA with ESD Protection Designs

As stated in the previous sections, the ESD protection has been an important task on the reliability of CMOS IC's. Besides the input and output ESD protection circuits implemented around the input and output pads, unexpected ESD damages may still exist in the internal circuits of CMOS IC's beyond the input and output ESD protections. Due to this, a whole-chip ESD protection is required to fully protect the RF PA designed in this study without causing unexpected ESD damage in the input, output, and internal circuits. In general, a whole-chip ESD protection circuit consists of three parts, namely, the power clamp circuit, the N-type diode, and the designed protection circuit. Fig. 3.9 shows the architecture of the PA with a whole-chip ESD protection circuit. For the ESD protection circuits, three different configurations are presented and studied in this thesis, namely, the diode string (denoted by DS), the diode-triggered SCR (DTSCR), and the diode string with embedded SCR (DSSCR). As for the N-type diodes, it can be constructed using N+ and P-Well layers. Finally, the power clamp circuit can be composed of resistor, capacitor, inverter, and MOSFET (M_{clamp}).

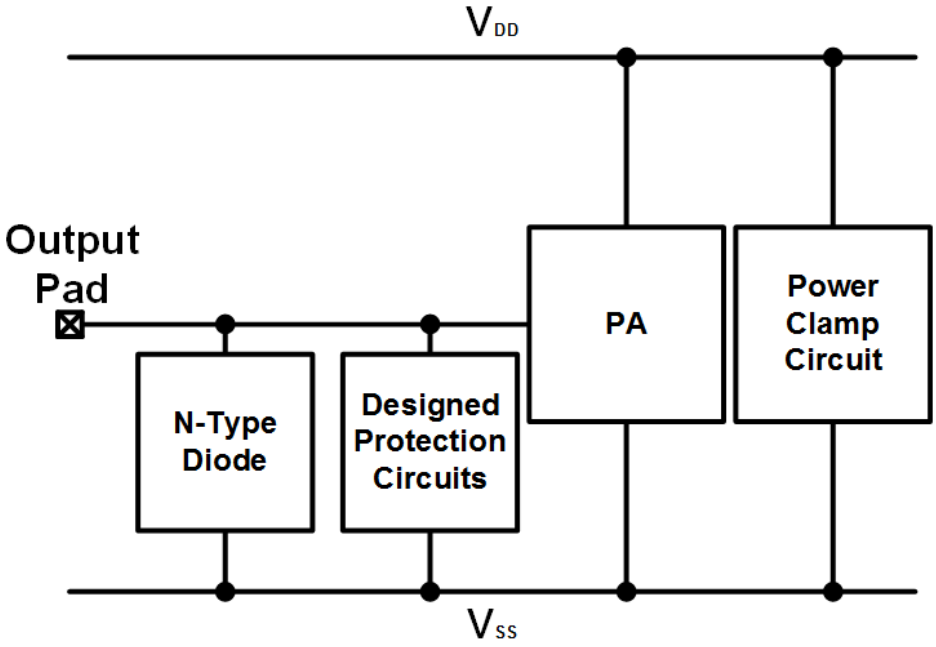


Fig. 3.9 The architecture of the PA with a whole-chip ESD protection circuit.

The designed power clamp circuit is a conventional ESD-transient detection circuit, as shown in Fig. 3.10. Since the rising time of an ESD stress is about nanosecond and the rising time of normal power-on events is about millisecond, the time constant of the RC detector can be designed about microsecond in order to distinguish the ESD events from the normal power-on events. In addition, the element M_{clamp} of the power clamp is the main ESD discharging device which can offer two ESD discharging paths including V_{DD}-to-V_{SS} and V_{SS}-to-V_{DD} when ESD event occurs. It also clamps the ESD voltage between V_{DD} and V_{SS} of the power lines after the ESD-transient detection circuit is triggered.

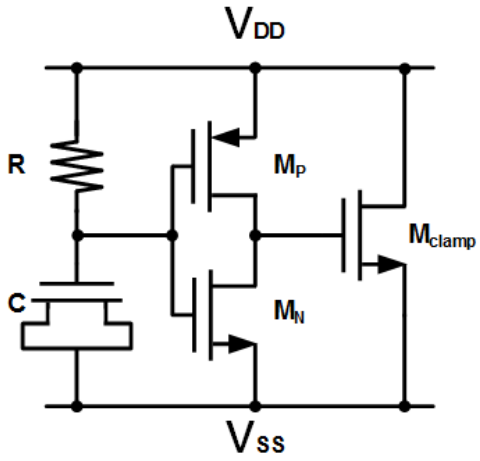


Fig. 3.10 Schematic of power clamp circuit.

The whole-chip ESD protection circuits provide six ESD discharging paths, including positive-to-V_{DD} mode (PD-mode), positive-to-V_{SS} mode (PS-mode), negative-to-V_{DD} mode (ND-mode), negative-to-V_{SS} mode (NS-mode), V_{DD}-to-V_{SS} mode, and V_{SS}-to-V_{DD} mode. All the ESD discharging paths are shown in Fig. 3.11 and Fig. 3.12.

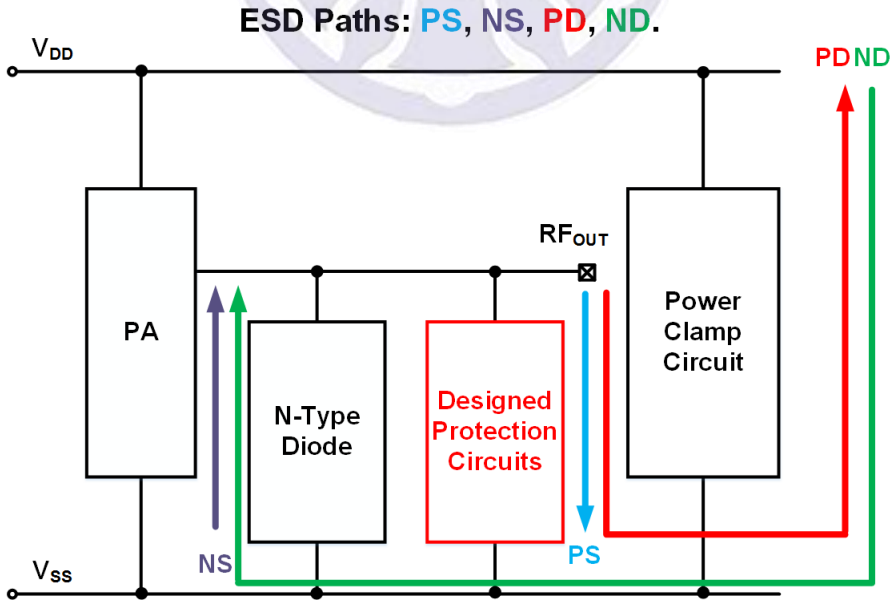


Fig. 3.11 The ESD discharging paths among PS, NS, PD, and ND of the whole-chip ESD protection circuit.

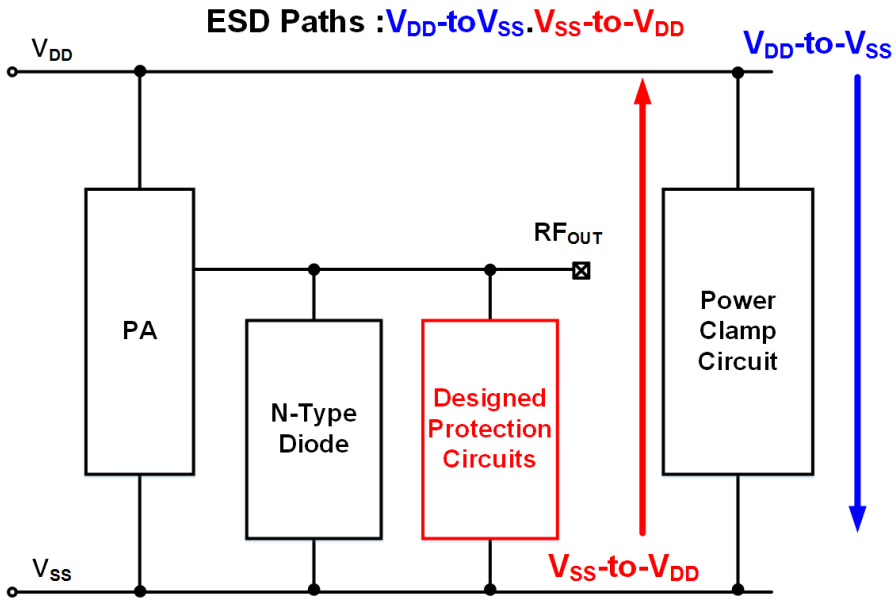


Fig. 3.12 The ESD discharging paths among V_{DD}-to-V_{SS} and V_{SS}-to-V_{DD} of the whole-chip ESD protection circuit.

3.4 Measured Results of the PAs with and without ESD Protection Circuits

Three different configurations of the whole-chip ESD protection circuits were designed in this research and the PA with three proposed circuits are denoted by PA with DS, PA with DTSCR and PA with DSSCR, respectively. The ESD protection circuits of PA with DS is composed of the DS_W50_D8, the N-type diode, and the power clamp circuit; the ESD protection circuits of PA with DTSCR consists of the DTSCR_W50_D8, the N-type diode, and the power clamp circuit; the ESD protection circuits of PA with DSSCR is constructed using the DSSCR_W50_D8, the N-type diode, and the power clamp circuit. Figs. 3.13-3.16 are the chip micrographs of designed PA, PA with DS, PA with DTSCR, and PA with DSSCR. The layout area of each one is 500.6 μm ×

607.245 μm.

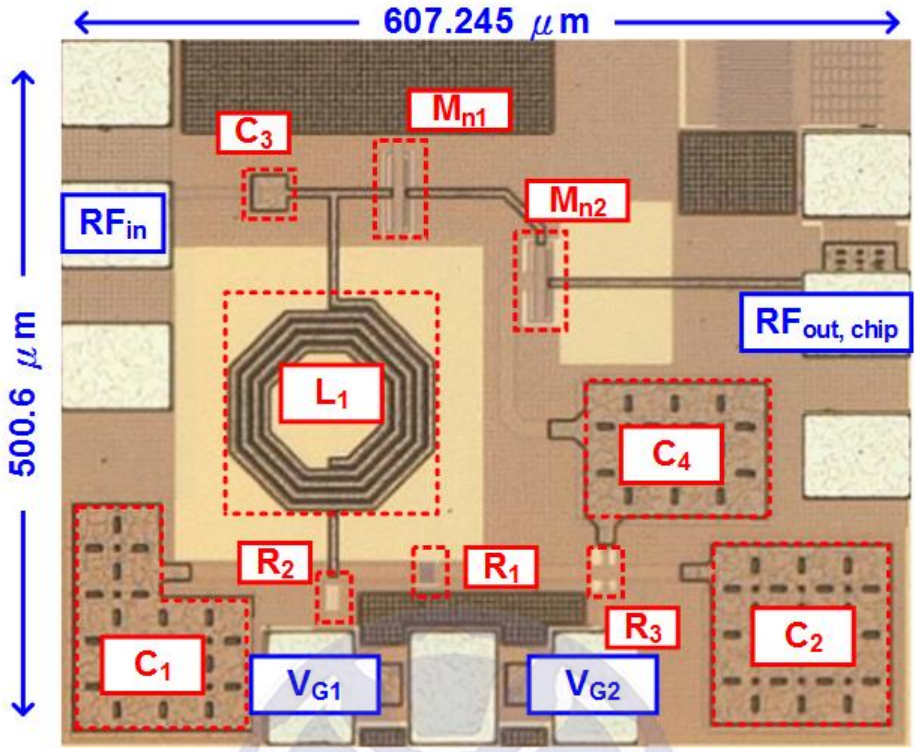


Fig. 3.13 The chip micrographs of PA.

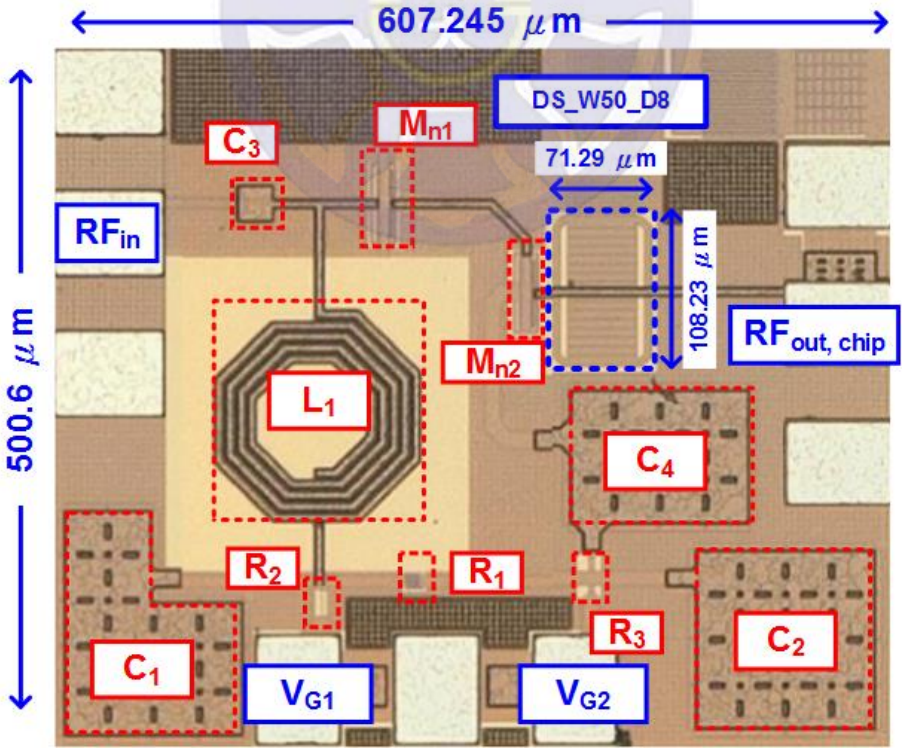


Fig. 3.14 The chip micrographs of PA with DS.

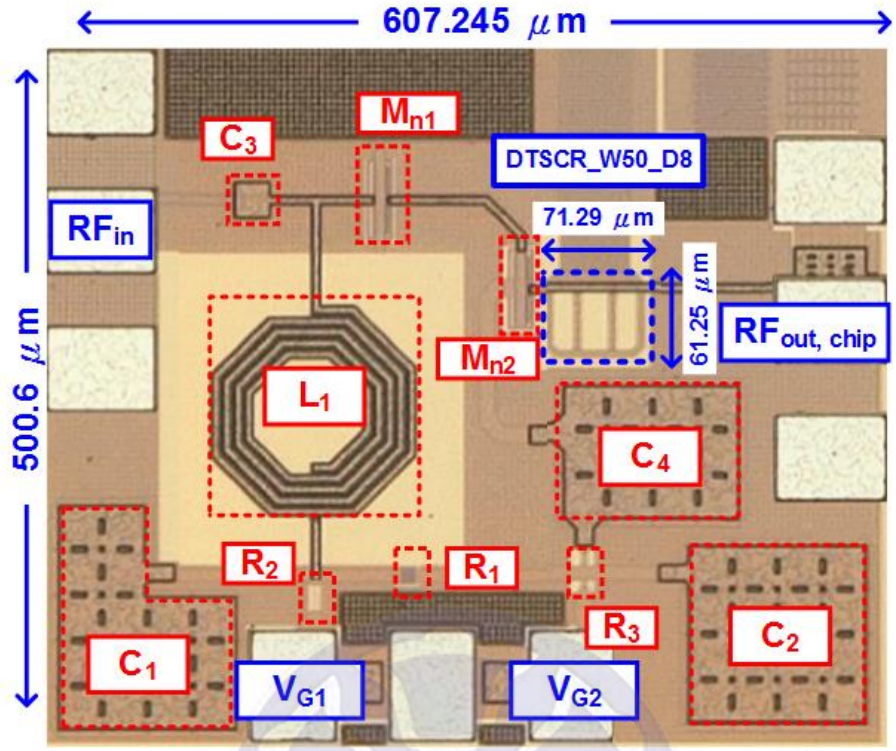


Fig. 3.15 The chip micrographs of PA with DTSCR.

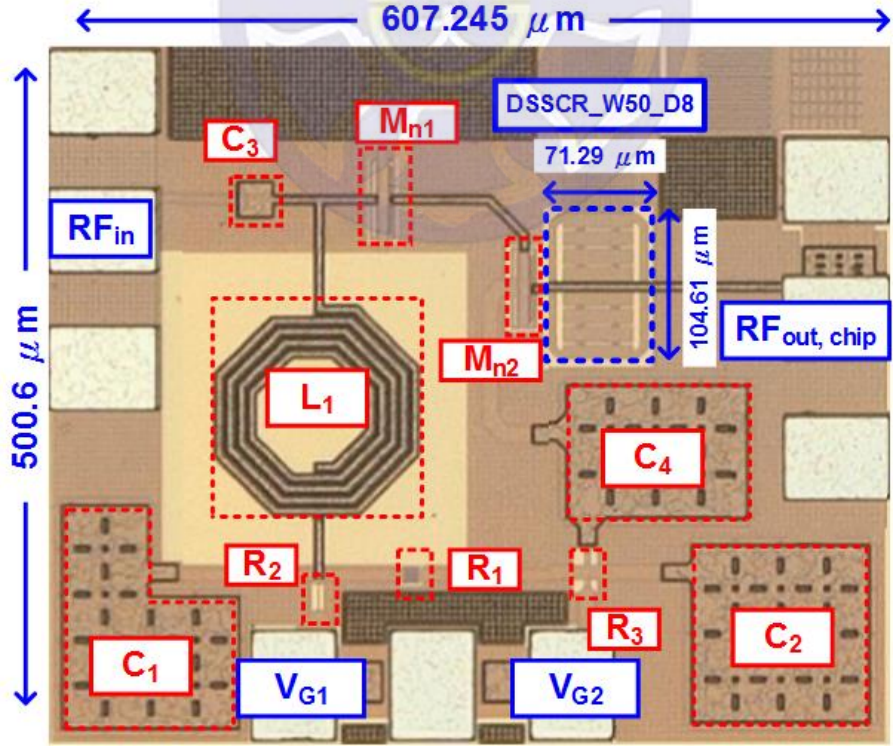


Fig. 3.16 The chip micrographs of PA with DSSCR.

In order to evaluate the capability of the PA with/without ESD protection circuit against the ESD damage, the human-body-model (HBM) of different ESD stresses level will be employed for test.

The measured S_{21} of the PA, the PA with DS, the PA with DTSCR, and the PA with DSSCR are shown in Fig. 3.17. Fig. 3.18 shows the measured S_{21} of the PA before and after the HBM test. Figs. 3.19-3.21 show the S_{21} of the PA with DS, DTSCR, and DSSCR, respectively, before and after the HBM test. The measured gains of the PA, the PA with DS, the PA with DTSCR, and the PA with DSSCR are shown in Fig. 3.22. Fig. 3.23 shows the measured gains of the PA before and after HBM test. Figs. 3.24-3.26 show the gains of the PA with DS, DTSCR, and DSSCR before and after the HBM test, respectively. The measured output powers of the PA, the PA with DS, the PA with DTSCR, and the PA with DSSCR are shown in Fig. 3.27. Fig. 3.28 shows the measured output powers of the PA before and after HBM test. Figs. 3.29-3.31 show the output powers of the PA with DS, DTSCR, and DSSCR before and after HBM test, respectively.

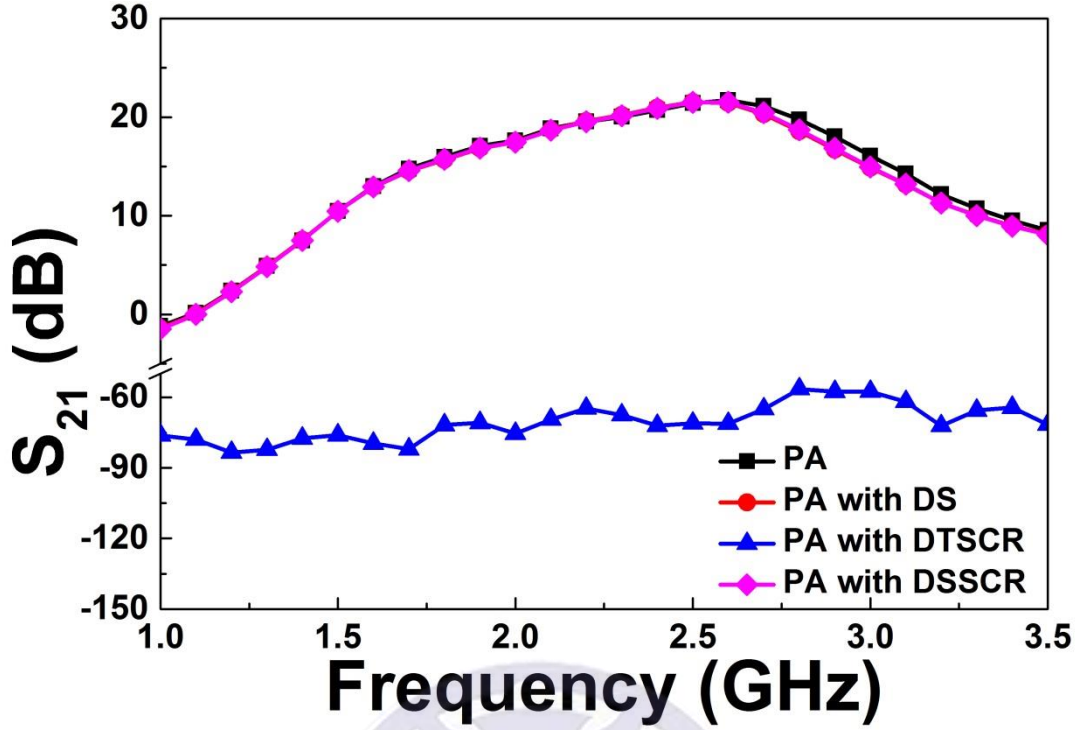


Fig. 3.17 Measured S_{21} of the PAs with and without ESD protection circuit.

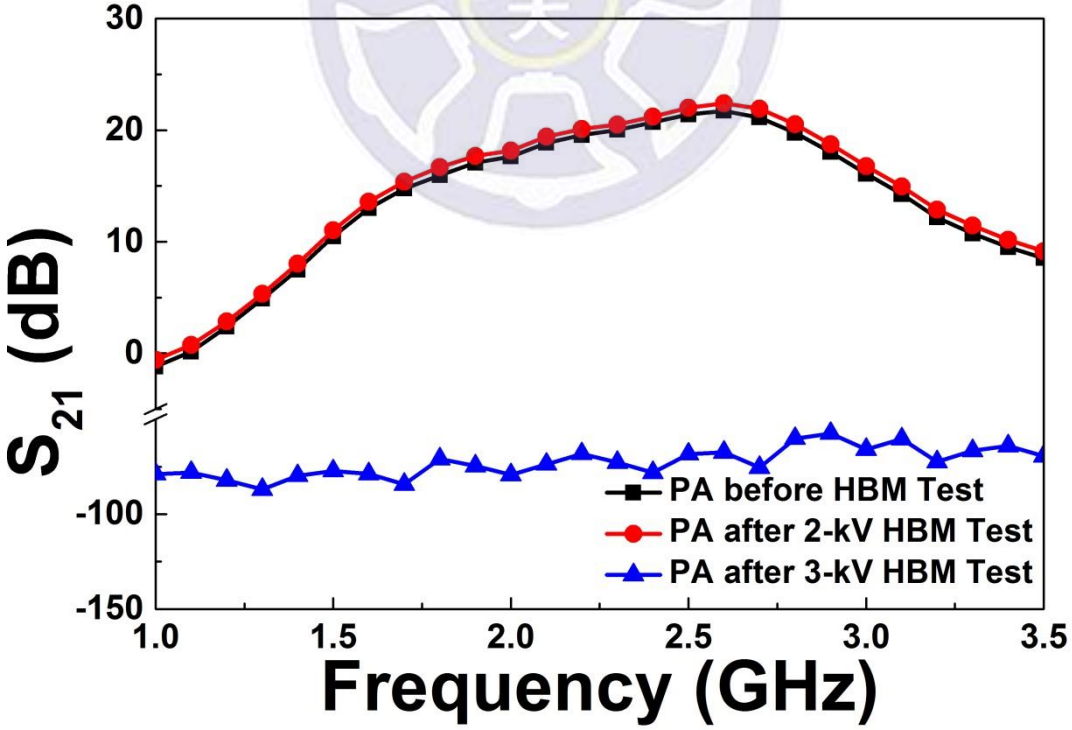


Fig. 3.18 Measured S_{21} of the PA before and after HBM test.

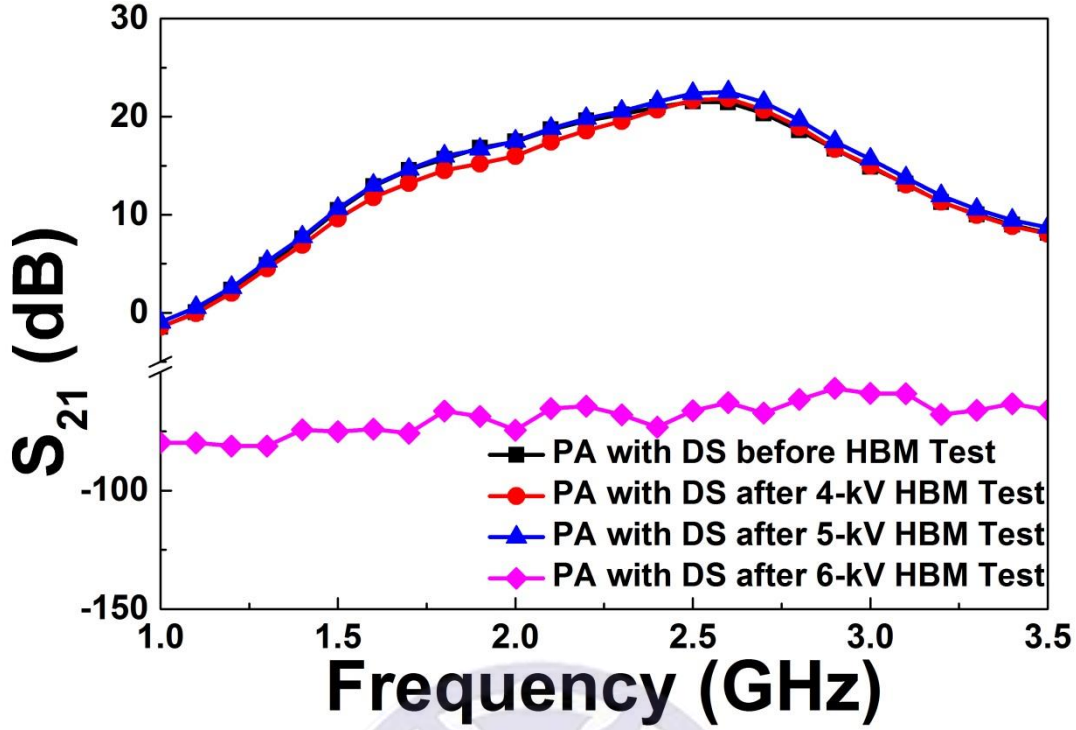


Fig. 3.19 Measured S_{21} of the PA with DS before and after HBM test.

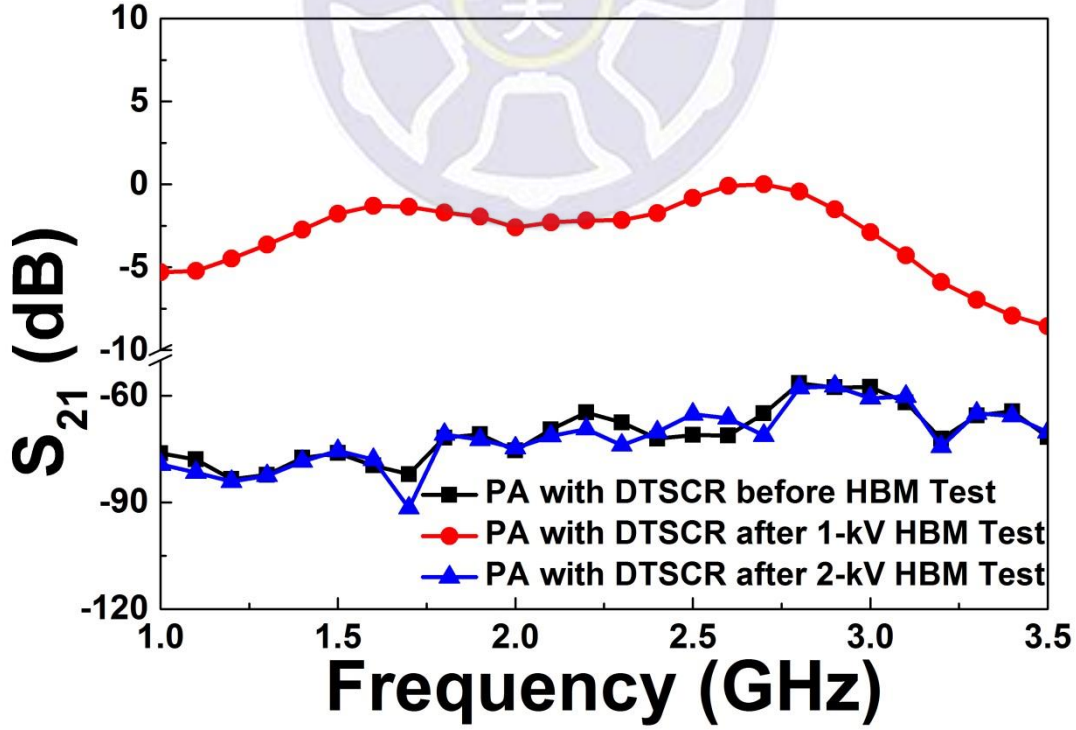


Fig. 3.20 Measured S_{21} of the PA with DTSCR before and after HBM test.

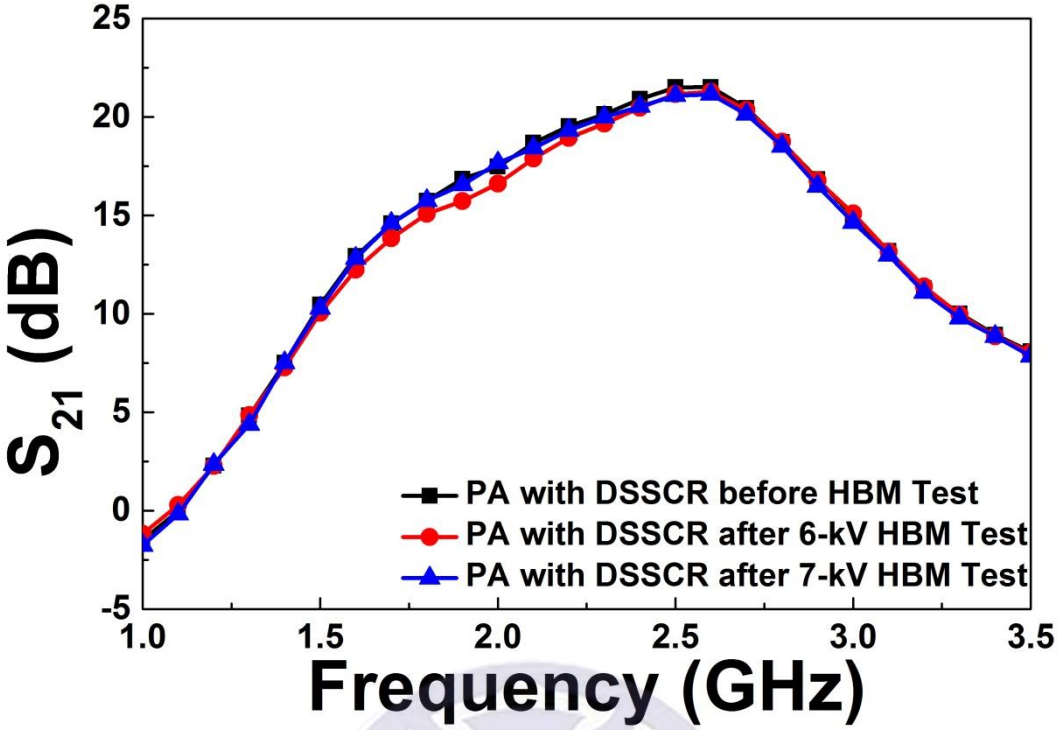


Fig. 3.21 Measured S_{21} of the PA with DSSCR before and after HBM test.

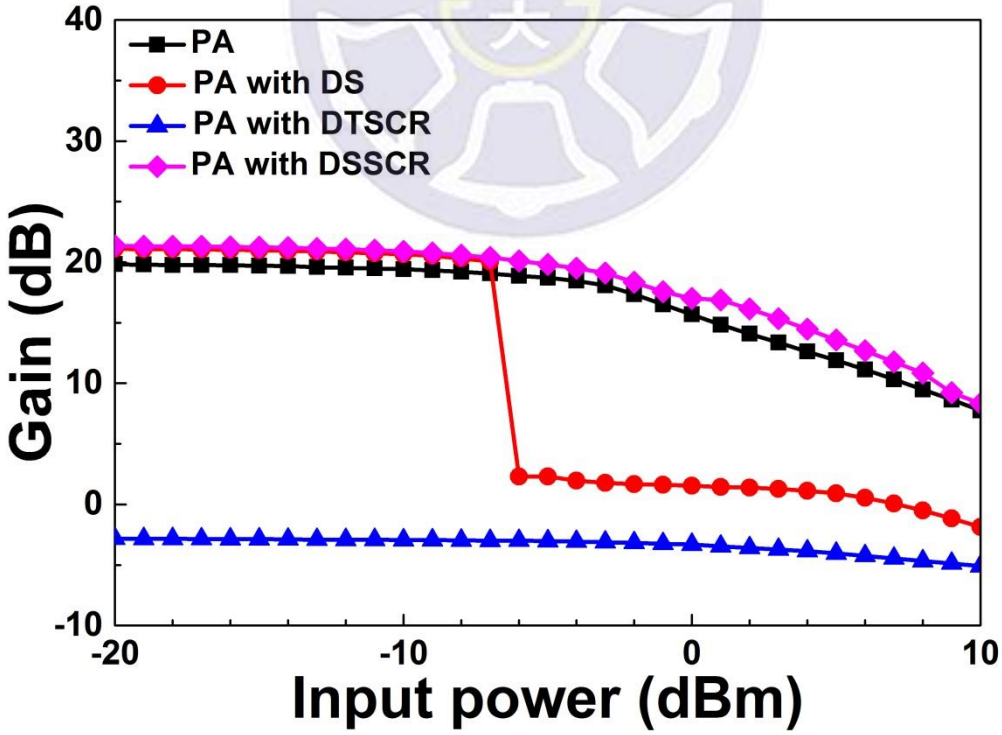


Fig. 3.22 Measured gains of the PAs with and without ESD protection circuit.

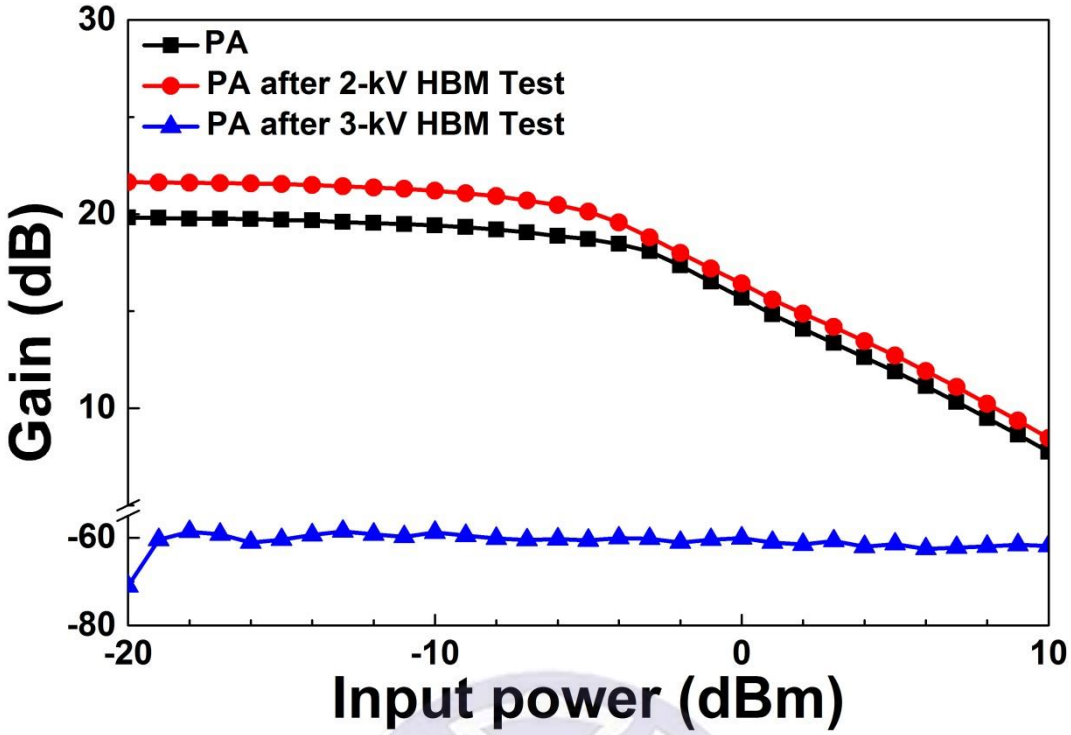


Fig. 3.23 Measured gains of the PA before and after HBM test.

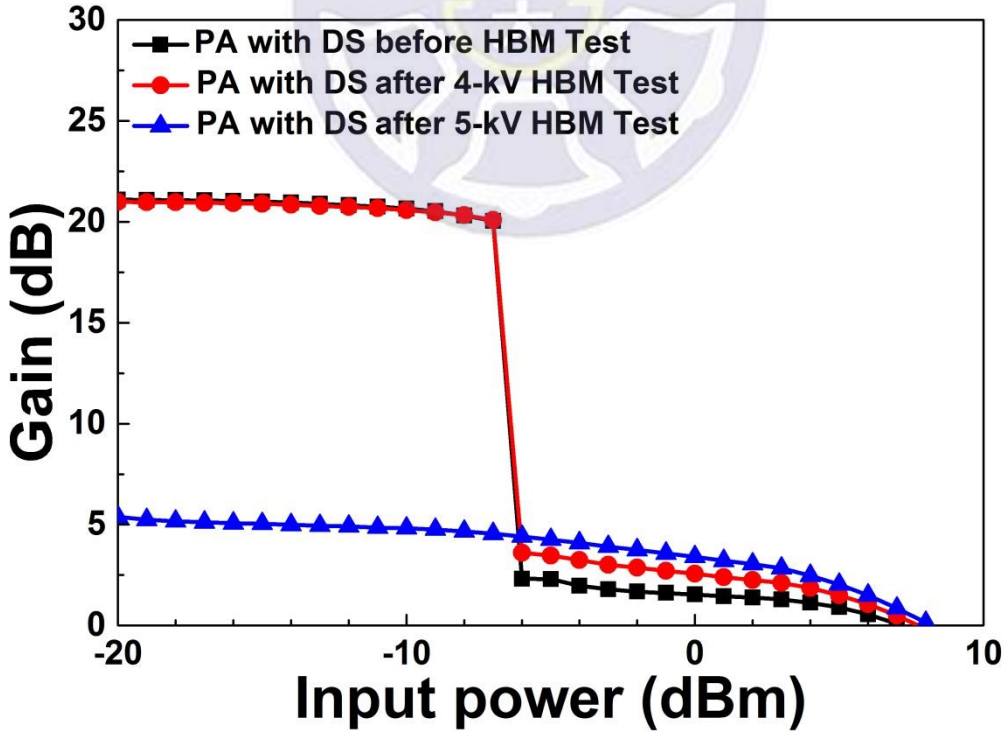


Fig. 3.24 Measured gains of the PA with DS before and after HBM test.

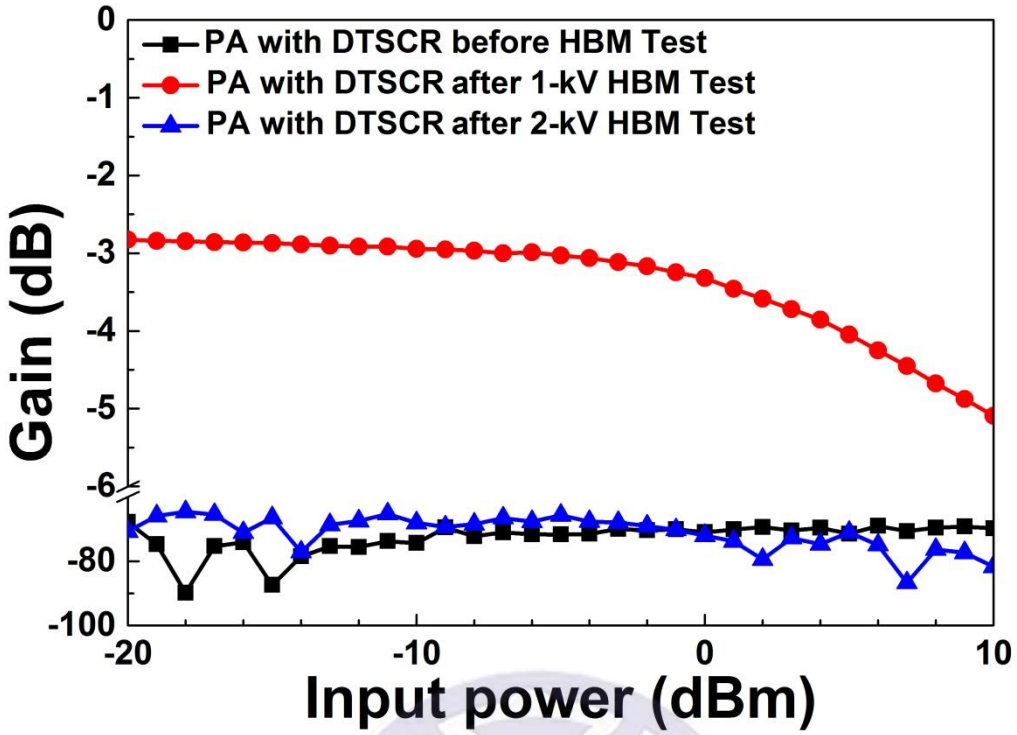


Fig. 3.25 Measured gains of the PA with DTSCR before and after HBM test.

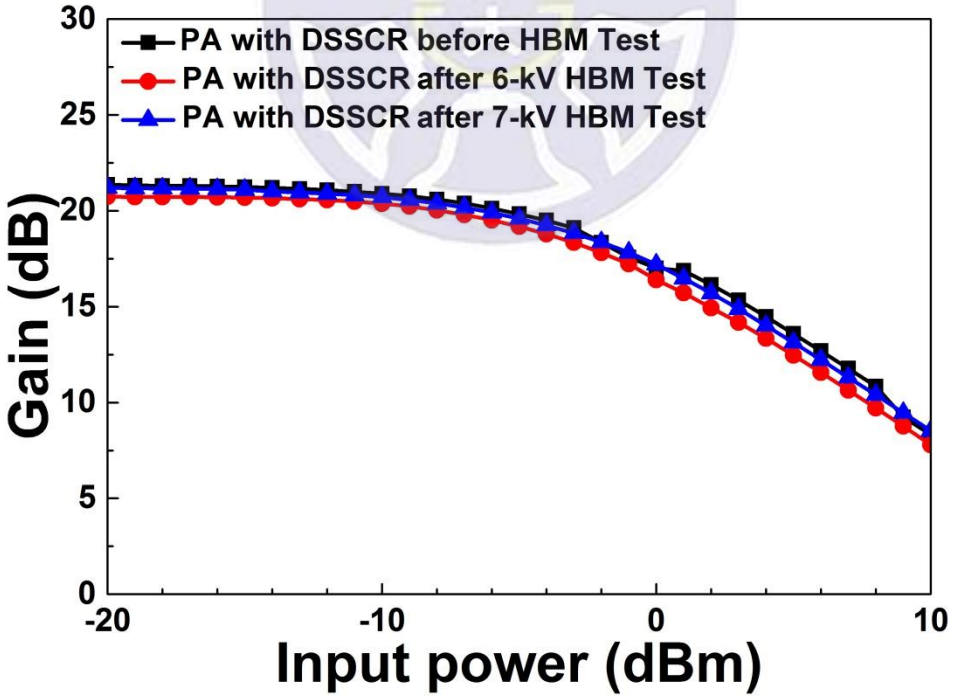


Fig. 3.26 Measured gains of the PA with DSSCR before and after HBM test.

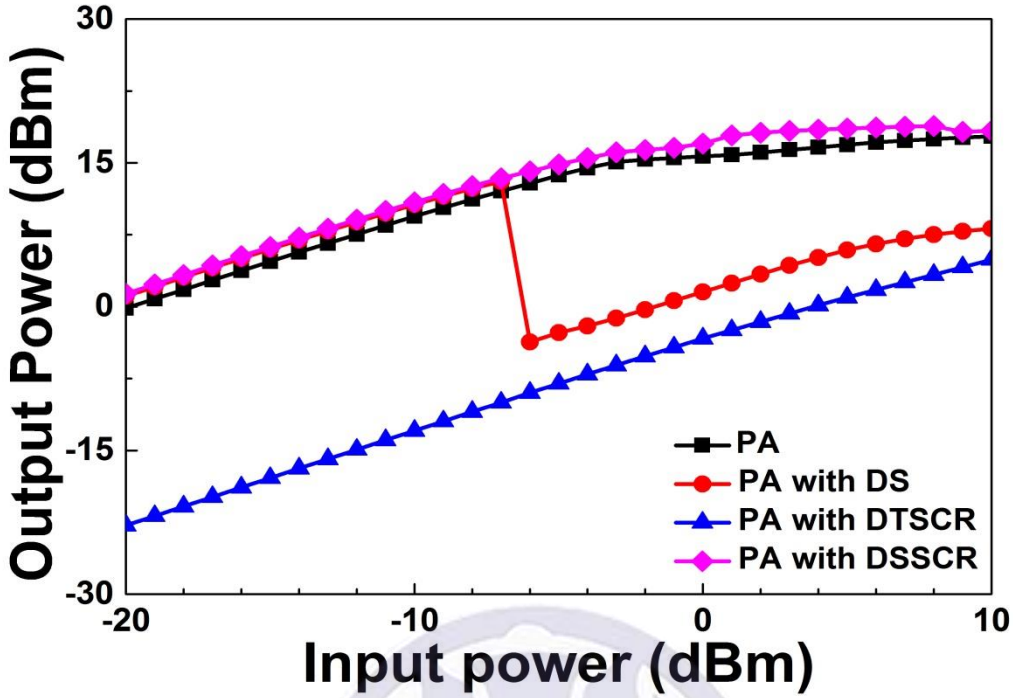


Fig. 3.27 Measured output powers of the PAs with and without ESD protection circuit.

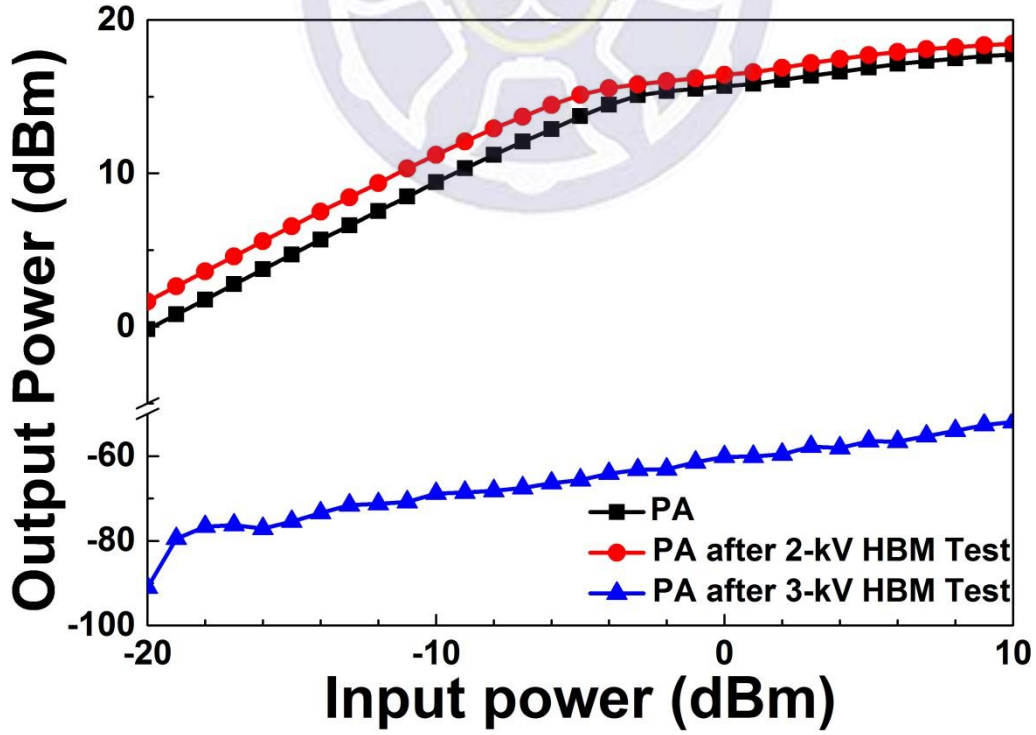


Fig. 3.28 Measured output powers of the PA before and after HBM test.

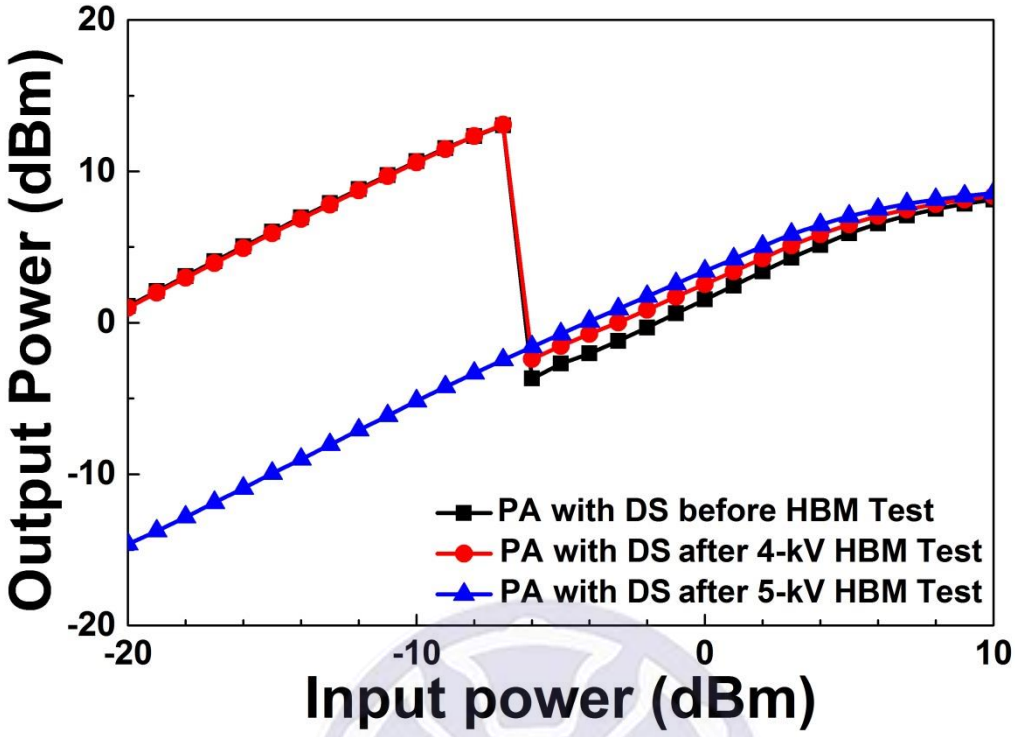


Fig. 3.29 Measured output powers of the PA with DS before and after HBM test.

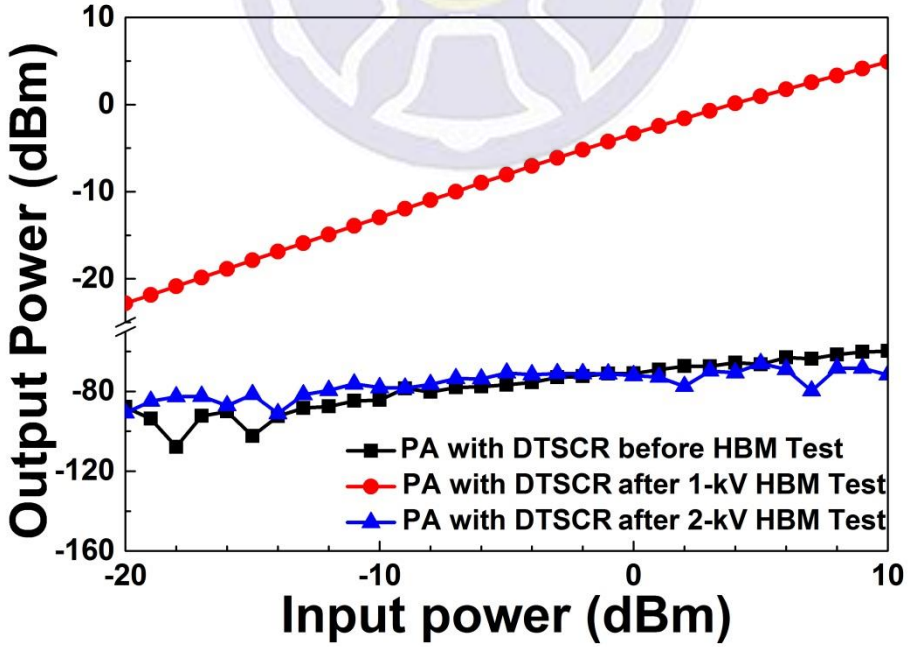


Fig. 3.30 Measured output powers of the PA with DTSCR before and after HBM test.

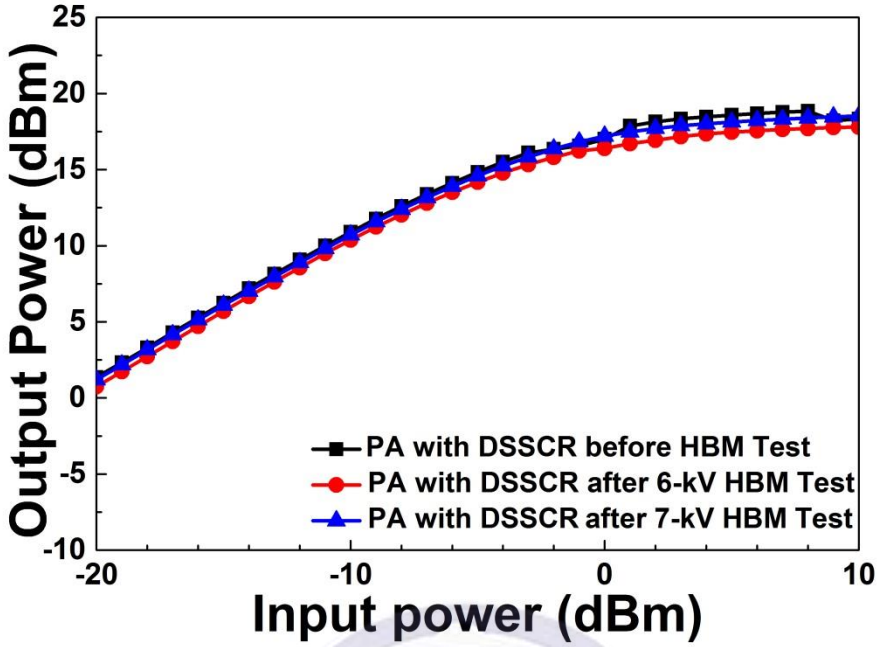


Fig. 3.31 Measured output powers of the PA with DSSCR before and after HBM test.

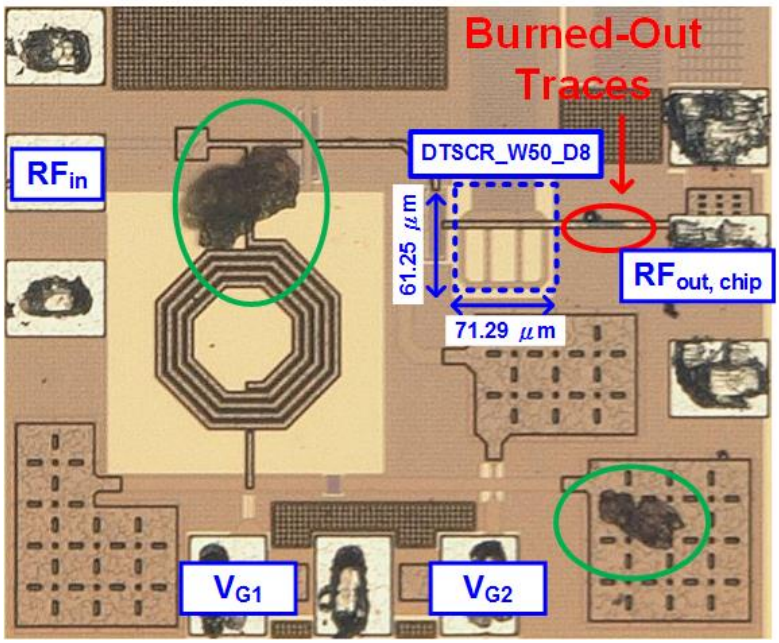
3.5 Comparison between The Designed PAs with and without ESD Protection

The effects that come from ESD protection circuits are not what power amplifiers need. So in this section the measured performances of the power amplifiers with and without ESD protection circuits in the previous section will be examined and discussed.

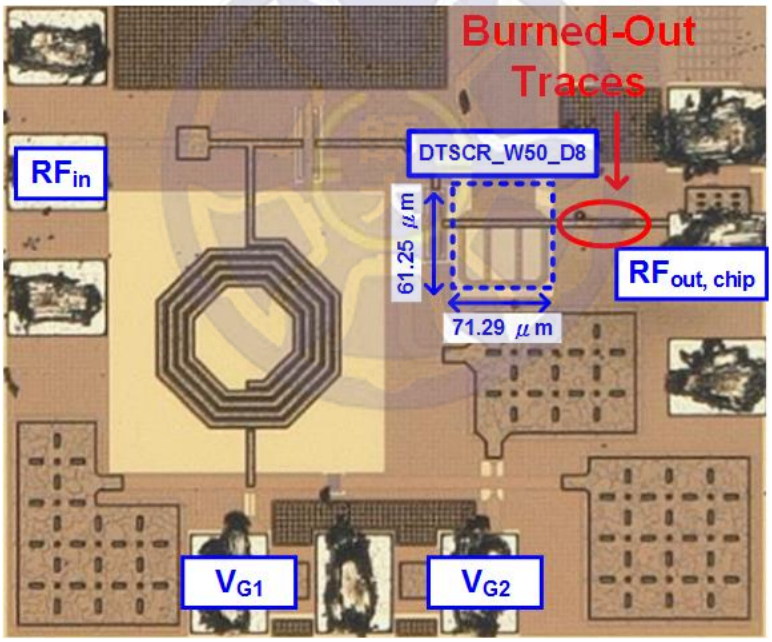
Figs. 3.17-3.31 indicate that the PA without ESD protection circuit can only bear 2-kV HBM test, the PA with DS can bear 4-kV HBM test, that with DTSCR cannot resist 1-kV HBM test and even cause the PA damaged, and the one with DSSCR can provide up to 7-kV HBM ESD robustness. It is seen that all the designs except DTSCR do not cause undesirable degradation of circuit performance at 2.4 GHz and can maintain linear relationship between the input

signal and the output signal when input signal power is between -20 dBm and -6 dBm.

For the measured S_{21} parameters of the PAs with and without ESD protection circuit shown in Fig. 3.17, it is observed that the S_{21} parameters have a maximum difference of only 0.3 dB among the PAs at 2.4 GHz. However, the S_{21} of the PA with DTSCR is -72.08 dB at 2.4 GHz. In other words, the measured gain of the PA with DTSCR is different from that of the others. For analysis of this phenomenon, the chip micrographs of PA with DTSCR before and after HBM test are shown in Fig. 3.32 and the de-layered chip micrograph of PA with DTSCR before and after HBM test are shown in Fig. 3.33. In view of the structure, the DTSCR has an SCR which can also serve as the latch-up structure. The SCR of the DTSCR_W50_D8 turns on at 2.75 V (see Table 2.8) and locks the potential between the $RF_{out,\,chip}$ (namely, the location at the drain of M_{n2}) and V_{SS} at 1.1 V (namely, the holding voltage of the DTSCR_W50_D8). While the power supply still provides a bias of 3.6 V, this will cause the signal line failed further. This also explains why the damage region of the PA with DTSCR is located at the signal line between the DTSCR_W50_D8 and pads, as shown in Fig. 3.32(a) and Fig. 3.32(b). No damage region found in transistor M_{n2} (see Fig. 3.33(a) and Fig. 3.33(b)) also verifies the above statement. In addition to the damage region, the other two stains near the inductor L_1 and capacitor C_2 can be respectively found and marked with green circles in Fig. 3.32(a). In Fig. 3.32(a), the shapes of the two stains in green circles are different from other shapes of ESD damage. Other than that, the PA with DTSCR is not tested by HBM. Based on this, the stains are rust that are caused by water vapor.

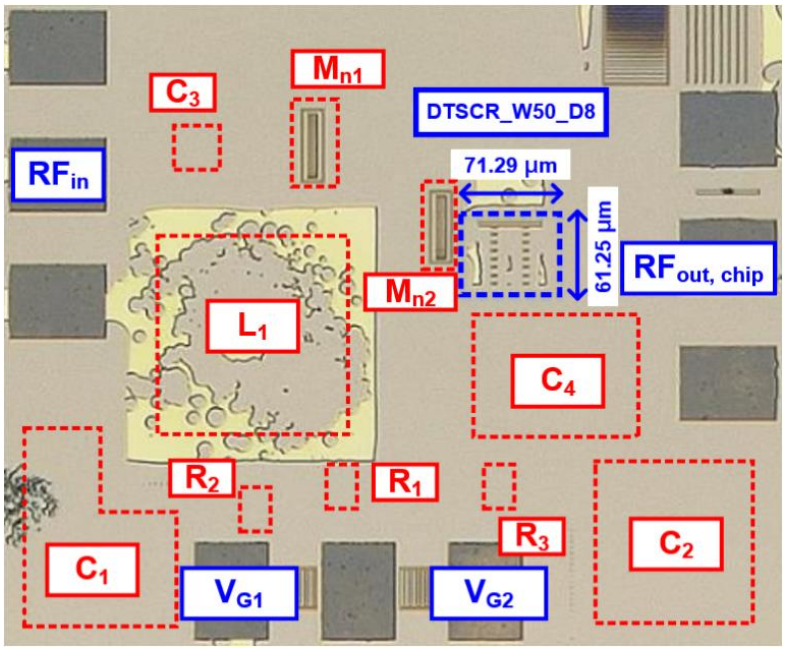


(a)

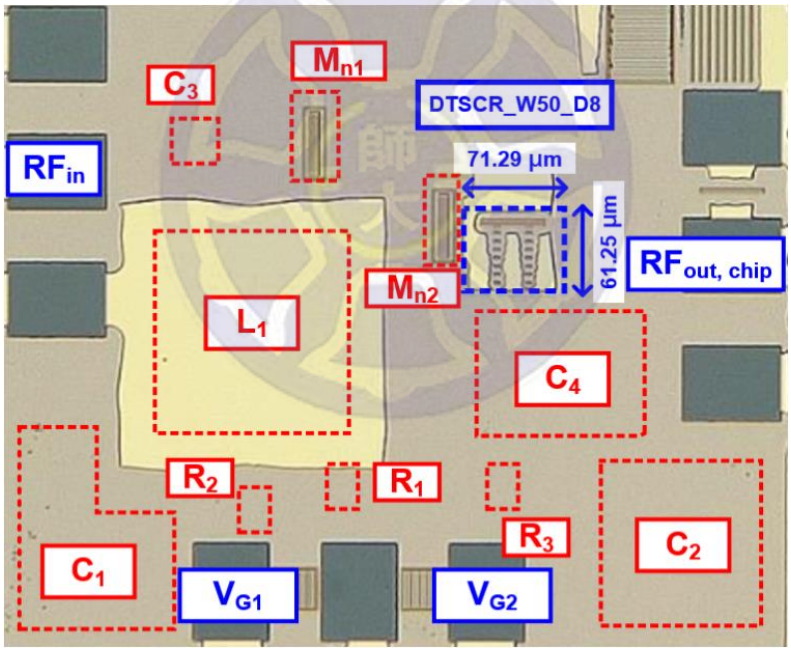


(b)

Fig. 3.32 The chip micrographs of (a) the PA with DTSCR before HBM test and (b) the PA with DTSCR after 7-kV HBM test.



(a)



(b)

Fig. 3.33 The de-layered chip micrographs of (a) the PA with DTSCR before HBM test and (b) the PA with DTSCR after 7-kV HBM test.

After discussing performance of the PA with DTSCR, we will now focus on the measured gains and output powers of the PA with DS shown in the Fig. 3.24 and Fig. 3.29, respectively. It is seen in both figures that there appears a discontinuity when the input power is about -6 dBm. Note that the signal voltage (see Fig. 3.34) at the $RF_{out,\ chip}$ which is located between the drain of M_{n2} transistor and the off-chip matching network (see Fig. 3.35) has a simulated maximum value of 5 V when input power is -6 dBm. Such a maximum signal voltage usually serves as an important reference voltage level for the design of the ESD protection circuits. However, since the trigger voltage of the DS_W50_D8 is lower than the estimated value which is assuming to be about 5.6 V, the DS_W50_D8 is conducted and the operating voltage of the drain in the PA is decreased.

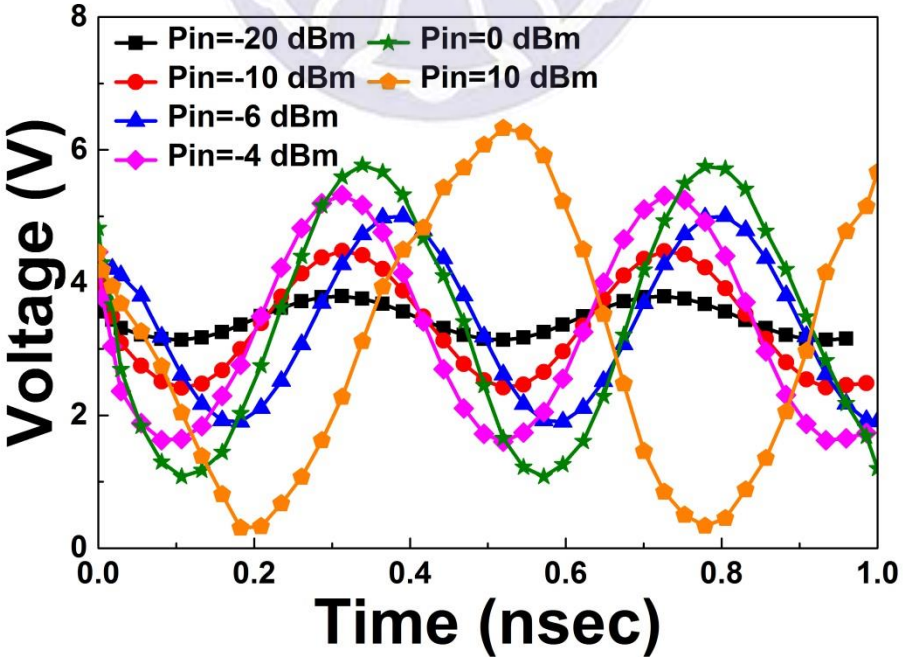


Fig. 3.34 The signal waveform on drain-end signal line.

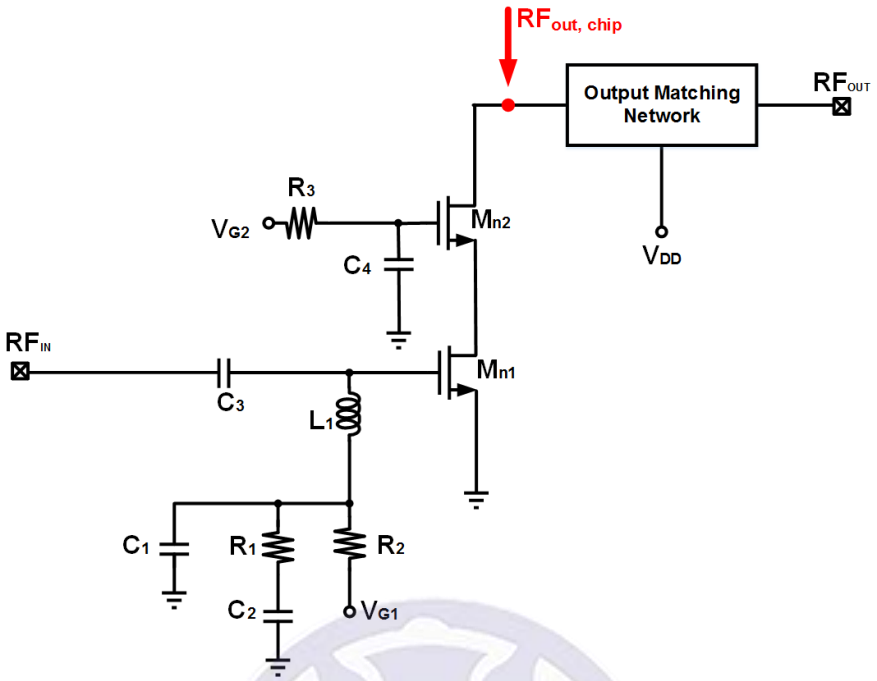


Fig. 3.35 The location of the signal waveform on signal line.

Differently, such signal distortion would not happen to the PA with DSSCR because its trigger voltage is higher than that of the PA with DS. In other words, because the trigger voltage of DSSCR_W50_D8 in PA with DSSCR is higher than that of DS_W50_D8 in PA with DS, the signal distortion like that occurs in the PA with DS will not be observed in the PA with DSSCR. Although the trigger voltage of the DSSCR_W50_D8 is also lower than 5 V, the pulse of the TLP system is a bit different from the RF signal in cycle and energy. Based on the above reasoning, the response of the PA with DSSCR does not have a discontinuity point like the PA with DS in power sweep. Similar to the PA with DS, the PA with DTSCR has the same problem of mis-triggering. But since the DS does not have the structure like SCR, it will not cause circuit latch-up and failed after conducting. The fact that there is no damage region found in the PA

with DS can verify the above statement. In addition, the fact that the PA with DS can be tested by measurement system to obtain the same data repeatedly also provides the evidence of the difference between DS and DTSCR. Table 3.3 summarizes the HBM ESD robustness of PAs and other works from references.

Table 3.3 The comparison among the PAs and other works from references.

Specification \ Parameter		Freq. (GHz)	Technology (μm)	V_{DD} (V)	Gain (dBm)	HBM ESD Robustness (kV)
This Works	PA with DS	2.4	0.18	3.6	21.09	4
	PA with DTSCR				-2.82	0
	PA with DSSCR				21.35	7
Reference [34]				1.8	8.2	5.3
Reference [35]				1.8	8	3
Reference [36]				unknown	20.2	5

3.6 Summary of This Chapter

In order to evaluate the effectiveness of proposed ESD protection circuits, the PAs with and without ESD protection circuits have been implemented, measured, analyzed, and discussed.

Among the whole-chip ESD protection circuits presented in this chapter, the PA with DS can bear 4-kV HBM test, but the PA with DS can only keep amplifier linearity in a small input power range, namely, between -20 dBm and

-6 dBm. The linear operation region can be made wider by increasing the number of the stacked diodes and meanwhile the ESD protection effectiveness is reduced as itself. So the DSs are indeed not an ideal ESD protection design for large-swing power amplifiers.

The measured results show that the PA with DTSCR cannot bear any HBM test and even cause the circuit damaged before ESD events occur. Besides, a higher beta-gain (β) of the parasitic p-n-p BJT in DTSCR makes the Darlington effect more pronounced. Therefore, the trigger voltage of the DTSCR will not be proportional to the number of the stacked diodes and will reach saturation at the voltage of 2.7 V. Due to the fact that the DTSCR does not possess a larger trigger voltage, it is not suitable for use as the ESD protection device for large-swing PAs.

The PA with DSSCR can bear over 7-kV HBM test. The DSSCRs which is verified to be an effective ESD protection circuit for power amplifiers because it produce lower voltage across RF_{out} and V_{SS} to avoid the PN junction breakdown in the drain of NMOS in the PA when ESD events occur. Also, the DSSCRs do not cause the signal distortion of the power amplifier like that by DSs or cause the PA damage like that by DTSCRs.

Chapter 4

Conclusions and Future Works

4.1 Conclusion

In this research, a novel ESD protection circuit configuration has been proposed for large-signal-swing power amplifiers. The proposed ESD protection circuits and those for comparison have been realized in a 0.18-μm CMOS process. The fabricated protection circuits were measured for verification and for performance comparison.

In chapter 2, the losses and TLP I-V curves of the DS, the DTSCR, and the DSSCR, respectively, have been measured and analyzed. The losses of the DSSCR and the DS are almost the same, while that of the DTSCR is smaller than the other two. In the judgment of protection effectiveness, the I_{BV_15} and I_{BV_10} have been used as references. Measured results show that the comparison results in DTSCR > DSSCR > DS for either I_{BV_15} or I_{BV_10}. In particular, the DTSCR which exists miss-triggering problem due to the serious Darlington effect cannot be designed with a higher V_{t1}, and hence is not suitable for ESD protection of large-swing-signal PAs. In addition, the large-signal models of the designed ESD protection elements should be established in order to avoid latch-up problems caused by the designed ESD protection elements in the future. For example, I_h of the DTSCR_W50_D8 is only 38 mA which is lower than the operating current of the PA. Thus, PA with DTSCR latches up.

In chapter 3, three different configurations of the whole-chip ESD protection circuits consisting of the local clamp circuit, the power clamp circuit, and the

designed protection devices (namely, the DS, the DTSCR, and the DSSCR, respectively) have been designed, fabricated, and measured. Results show that PA with DS can bear 4-kV HBM test, but the PA with DS can only keep linearity within a small input power range; the PA with DTSCR cannot bear any HBM test and even causes the circuit damaged before ESD events occur; the PA with DSSCR can bear the HBM test of voltage higher than 7 kV. The measured results also show that the DSSCR does not cause signal distortion of the RF power amplifier like that by the DS or cause the PA damage like that by DTSCR.

Results obtained in this work can find practical applications in ESD protection for the RF PAs. For future development of the power amplifiers, the signal-swing is expected to increase in order to resist attenuation due to the higher operating frequency. It has been demonstrated in this research that the DSSCR can serve as a very good ESD protection component for large-signal-swing power amplifiers. It is expected to be very suitable for even higher-speed or higher-frequency ESD protection applications without degrading the performance of the circuits.

4.2 Future Works

From this research, it is known that the output end (RF_{out}) of the power amplifier exhibits high operating voltage and current, and also large-swing signal that make the electrostatic protection design of the RF PA quite difficult. Increasing the holding voltage is a common practice to solve the latch-up problem. However, such a problem can also be solved through increasing the holding current of the ESD protection circuit, as shown in Fig. 4.1. With such an idea in mind, a new and improved ESD protection circuit can be proposed, as

shown in Fig. 4-2.

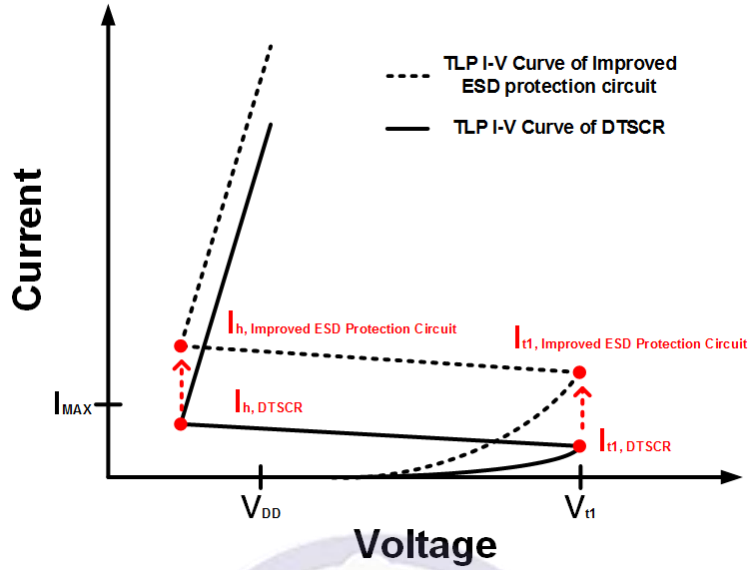


Fig. 4.1 The TLP I-V curves of the DTSCR and improved ESD protection circuit.

The improved ESD protection circuit for the RF PA has a structure resembles that of the DTSCR and the DSSCR. By increasing the resistance R shown in Fig. 4-2(a), I_h and I_{t1} of the improved ESD protection circuit can be improved directly. Also, connecting the P+ and N+ layers together allows for decreasing the resistance between the emitter and the base of the parasitic p-n-p BJT in the SCR, and this will result in increasing of I_h and I_{t1}. V_{t1} of the improved ESD protection circuit can be determined by the number of diodes in series. The improved ESD protection circuit is expected to have lower V_h and higher I_{BV}. Besides, the structure of such an improved ESD protection circuit has an additional parasitic diode that can offer another discharging-path (V_{SS}-to-RF_{out}) as compared with that of the DTSCR and the DSSCR. This implies that the N-type

diode located between RF_{out} and V_{SS} can be removed (since it is no longer needed to serve as a discharging path) and the parasitic capacitance of ESD protection circuit can be reduced. Eventually, the effect of the ESD protection circuit on the PA output end RF_{out} can be reduced. The above-mentioned design idea of the improved ESD protection circuit for the RF PA can be a promising topic for further study.

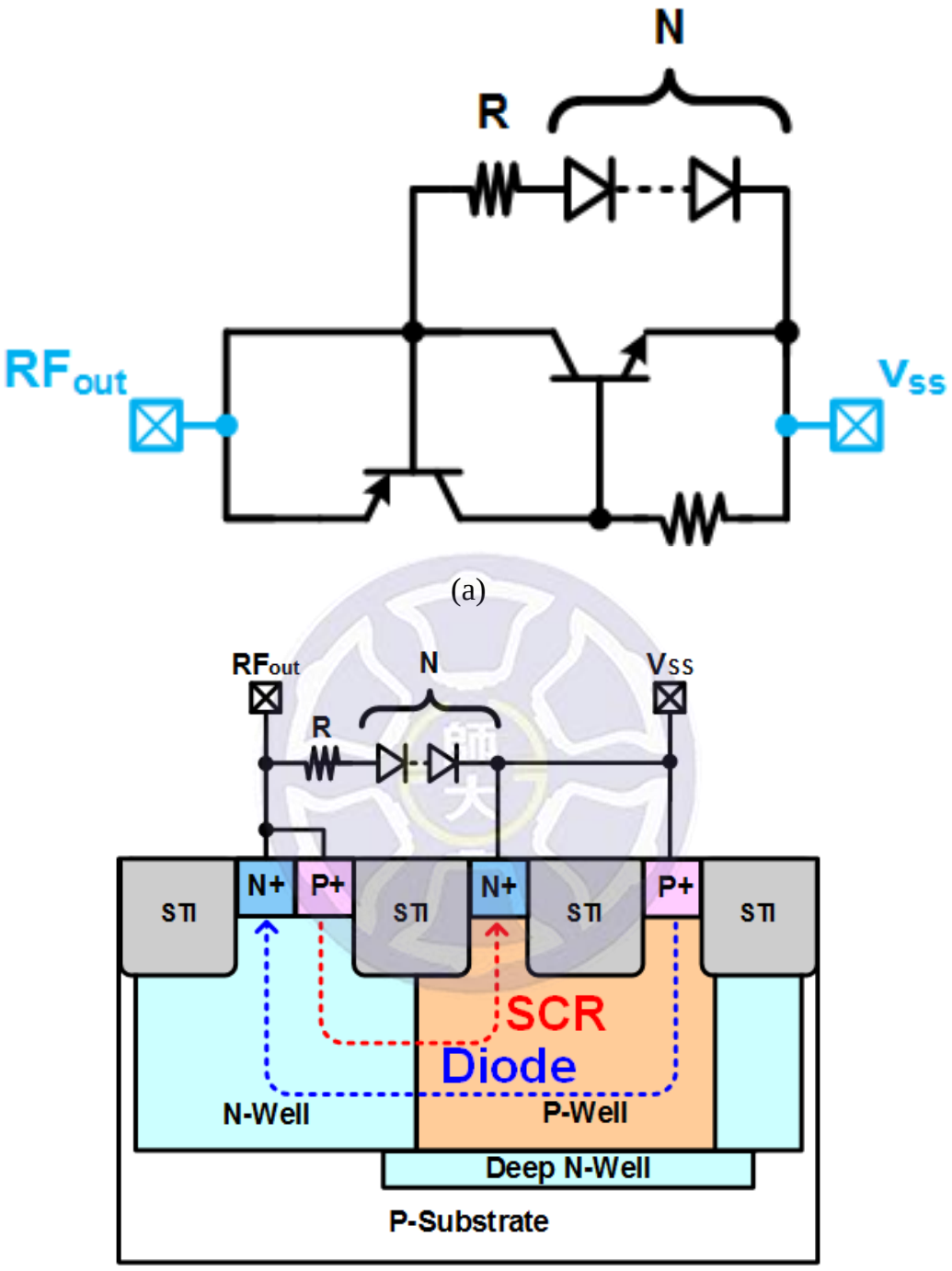


Fig. 4.2 (a) The schematic and (b) the cross-sectional view of the improved ESD protection circuit.

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Publication List

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