國立臺灣師範大學電機工程學系

碩士論文

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元件層級及系統層級之靜電放電防護設計

Component-Level and System-Level ESD Protection Design

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摘　　要

隨著製程演進，積體電路中電晶體尺寸逐漸縮小，靜電放電 (ESD) 容易造成晶片內部不可逆之破壞，因此積體電路產品中靜電放電防護的可靠度議題必須被深入探討。

現今的積體電路在出廠時需要做元件層級的靜電放電測試，當積體電路安裝在電子產品後，又需要做系統層級的靜電放電測試。因系統層級靜電放電的測試規範 (IEC 61000-4-2) 的嚴格要求，積體電路產品常通過了元件層級靜電放電的測試標準，也可能無法達到系統層級的靜電放電的標準，因此本論文進行元件層級和系統層級的靜電放電防護研究。

在論文第二章使用雙極性電晶體 (BJT)、二極體 (diode)、閘極接地 N 型金屬氧化物半導體場效電晶體 (GGNMOS)、靜電放電箝制 (power clamp) 作為靜電放電防護電路的研究基礎，並在 0.18um 1.8 V 的 Bi CMOS 製程下實現。這些防護電路使用傳輸線觸波產生器 (TLP) 系統、人體放電模式 (HBM) 儀器、靜電槍 (ESD gun) 進行測試，測試結果證明二極體和靜電放電箝制有較好的元件層級的防護能力。瞬態電壓抑制 (TVS) 二極體被用來提升系統層級的靜電放電防護能力。

在論文第三章提出了一項創新使用二極體串嵌入式矽控整流器 (DSESCR) 之靜電放電防護元件，因傳統式的二極體串聯 (TDS) 和改善

型二極體串 (IDS) 有較高箝制電壓及高漏電流，故 DSESCR 被用來改善缺點。此元件在 0.18um 1.8 V 的 CMOS 製程下實現。這些防護電路使用 TLP 系統、HBM 儀器、ESD gun 進行測試，測試結果證明能有效改善漏電過大及箝制電壓過大的缺點。

本論文第二章及第三章所設計的元件，可以依其特性應用在各種的電路上，能夠有效的防護內部電路。

關鍵字: 雙極性電晶體，元件層級靜電放電，二極體，靜電放電，金屬氧化物半導體，矽控整流器，系統層級靜電放電

Component-Level and System-Level ESD Protection Design

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Abstract

With the continuous evolution of semiconductor integrated circuits (ICs) process, electrostatic discharge (ESD) events are likely to cause IC products suffered irreversible damage. All microelectronic products must meet the reliability specifications. Therefore, ESD must be taken into consideration.

Nowadays, when the IC chip is produced, it must test the robustness of component-level ESD. When the IC chip is mounted on the electronics products, it also needs to test the robustness of system-level ESD. The component-level and system-level ESD qualifications are needed to test based on a set of corresponding standardization documents. System-level ESD is an increasingly important reliability issue in CMOS IC products. It has been also reported that reliability issues still exist in CMOS ICs under system-level ESD tests, even though IC products have passed component-level ESD specifications. Therefore, the component-level and system-level ESD robustness are analyzed in this thesis.

In chapter 2, the ESD protection circuits of bipolar junction transistor (BJT), diode, gate-grounded NMOS (GGNMOS), and power clamp are studied. These ESD protection circuits have been fabricated in 0.18-μm 1.8V BiCMOS process. The transmission-line-pulsing (TLP) system, human-body-model (HBM), and ESD gun are used to verify ESD protection circuits. The experimental results of diodes and power clamp show better component-level ESD robustness. Transient-voltage-suppression (TVS) diode is used to improve the system-level ESD robustness.

In chapter 3, a novel design of diode string with embedded silicon-controlled rectifier (DSESCR) device is proposed for ESD protection. The traditional diode string (TDS) and improved diode string (IDS) have drawbacks of a high clamp voltage and a high leakage current, so DSESCR is proposed to improve these drawbacks. These ESD protection circuits have been fabricated in 0.18-μm 1.8V CMOS process. The TLP system, HBM, and ESD gun are used to verify IDS and DSESCR device. DSESCR can improve the clamp voltage and leakage current.

In chapter 2 and chapter 3, according to their characteristics of the ESD protection devices, the devices can be used to protect different internal circuits.

Keywords: bipolar junction transistor (BJT), component-level ESD, diode, electrostatic discharge (ESD), metal-oxide-semiconductor (MOS), silicon-controlled rectifier (SCR), system-level ESD

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傅偉豪 謹誌於師大

中華民國一零六年六月

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Chapter 1

Introduction

1.1 Motivation

Nowadays, the electrostatic discharge (ESD) events of IC products have attracted more and more attention [1]-[5]. Many IC manufacturers face the challenge that they are requested to provide the products which are robust against ESD events [6].

Lots of the electronic components or systems are caused failure and damage by ESD [7]-[9]. The factors of ESD are mostly caused by human, machine, and component itself. Such as electronic components or systems during manufacture, production, assembling, testing, storage, and handling, etc., the electrostatic can accumulate in human body, instruments, equipment, and electronic component itself. A current discharging path is formed when these objects contact with each other, and the electronic components are destroyed by ESD. A general specification for a commercial IC is 2000V for ESD robustness of the human-body-model (HBM) [10]. Thus, ICs with the design of ESD protection should be used to prevent the ICs from destruction of ESD. The specification not only let the user reassurance, but the specification also let the user know the sufficient durability of the electronic products. Reliability of ICs product is the most important part, so all the electronic components or systems need to be designed with ESD protection. To ensure and certify the reliability of the electronics systems, both the component-level and system-level ESD qualifications are needed to test based on a set of corresponding standardization

documents. The electronics products need to pass the testing of component-level and system-level ESD specifications [11]. Therefore, when the IC chip is produced, it must test the robustness of component-level ESD. When the IC chip is mounted on the electronics products, it also needs to test the robustness of system-level ESD.

1.2 Background of ESD

The phenomenon of ESD occurs when an electrostatic voltage slowly develops between an object and its surrounding environment, commonly referred to as ground, then spontaneously discharges as an electrical current impulse [12].

1.3 Testing Methods

Basically, there are two types of ESD test. One is component-level ESD specification, and the other is system-level ESD specification. In component-level ESD specification, three models are shown bellow: human-body-model (HBM), machine-model (MM), and charge-device-model (CDM). The secondary specification is system-level ESD specification.

Nowadays, the IC manufacturers adopt IEC 61000-4-2 standard [13]. The devices under test (DUT) with or without power supply are the main difference by component-level and system-level ESD specification.

1.3.1 Component-Level ESD Test

Component-level ESD specification is used to test for ESD robustness of ICs product. ESD models are currently classified into three categories: (1) human-body-model (HBM), (2) machine-mode (MM), and (3) charge-device-model (CDM).

(A) Human-Body-Model (HBM)

The human-body-model represents friction of the person or other factors that has accumulated electrostatic. When the person touches the ICs, the ESD can destroy the IC. As shown in Fig. 1.1., the equivalent circuit of HBM ESD test has a 100pF equivalent capacitor and a 1.5kΩ equivalent resistor [14]. The new specifications of component-level ESD for HBM are shown in Table 1.1[15].

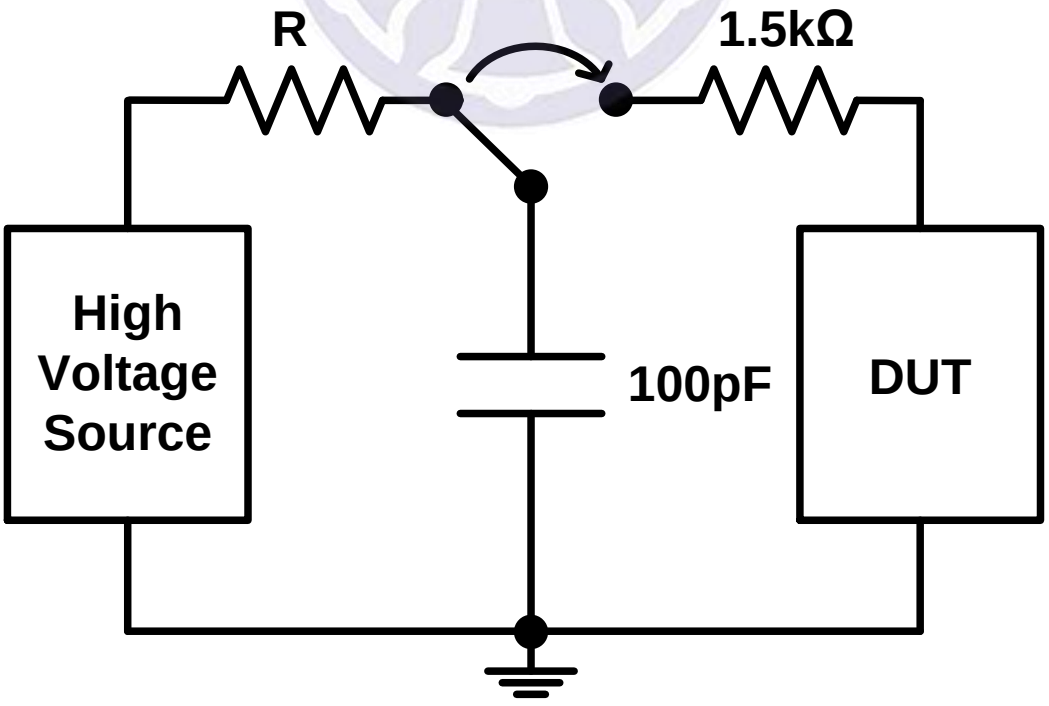


Fig. 1.1. Equivalent circuits of HBM ESD test.

(B) Machine-Mode (MM)

The MM refers to the machine itself that has accumulated electrostatic. When the machine contacts the ICs, the electrostatic discharge will damage the ICs. As shown in Fig. 1.2, the equivalent circuit of MM ESD test has a 200 pF equivalent capacitor with no resistive device [16]. The new specifications of component-level ESD for MM are shown in Table 1.1 [15].

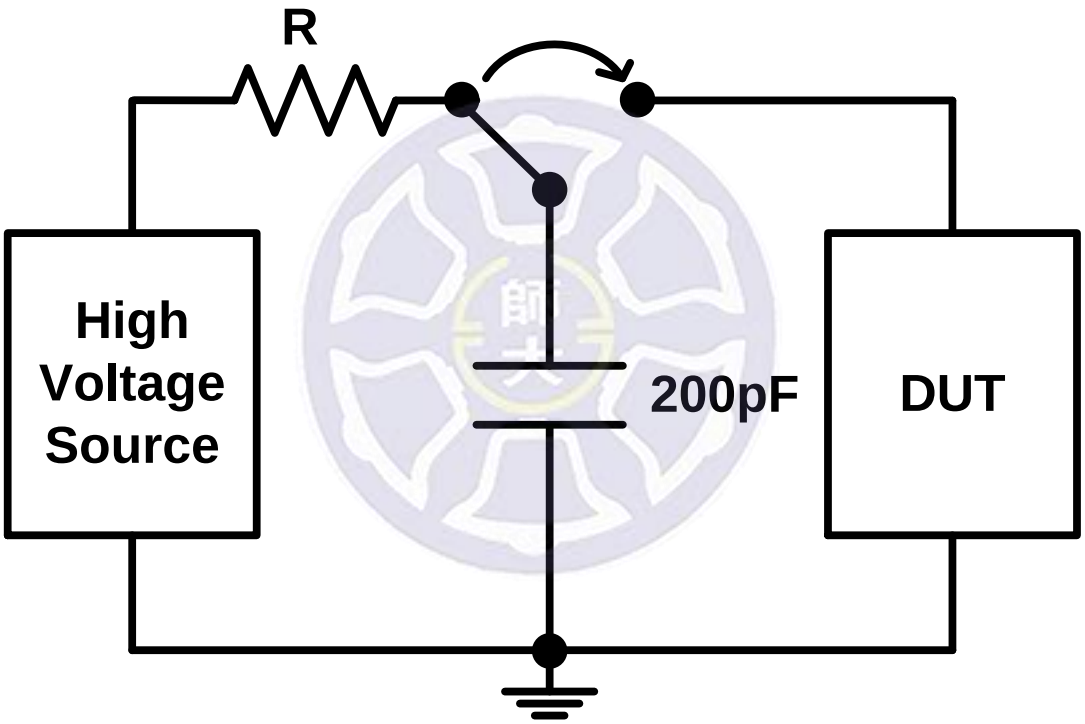


Fig. 1.2. Equivalent circuits of MM ESD test.

(C) Charge-Device-Model (CDM)

As shown in Fig. 1.3, the equivalent circuit of CDM ESD test has a no resistive device and different kinds of equivalent capacitance. The ICs always have different kinds of equivalent capacitance because the ICs are difference of the angle, the position and the package [17]. The new specifications of component-level ESD for CDM are shown in Table 1.2 [18].

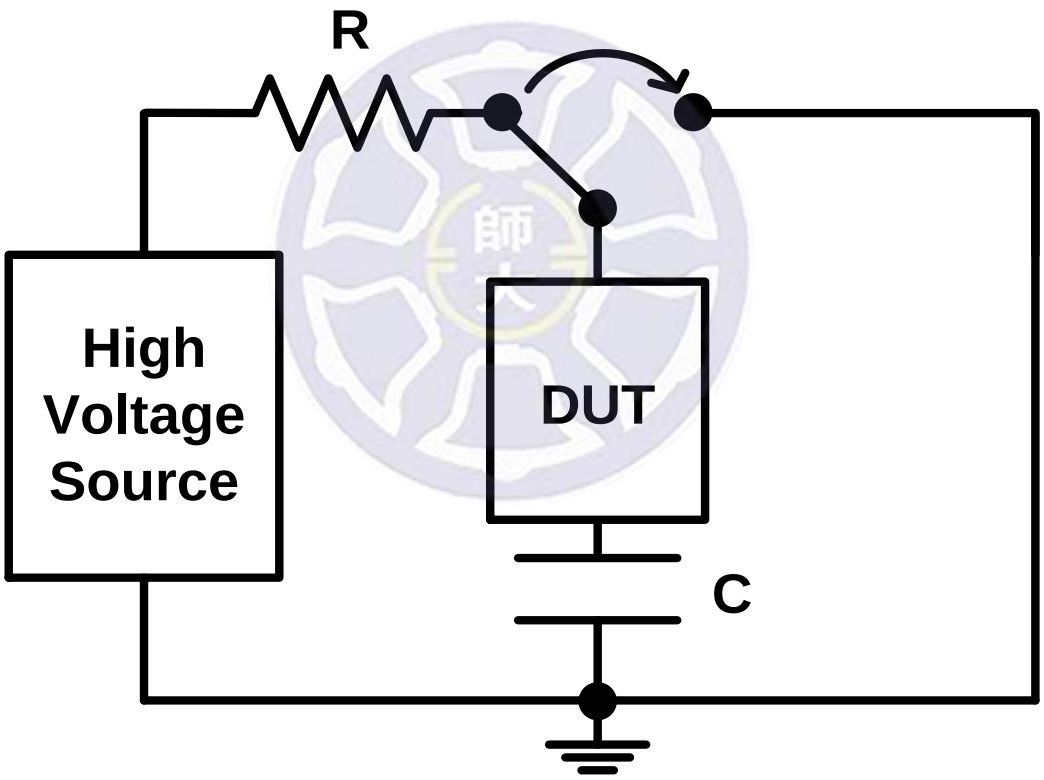


Fig. 1.3. Equivalent circuits of CDM ESD test.

Table 1.1

Component-level ESD specifications for HBM and MM.

HBM level	MM level	Impact on manufacturing environment
2kV	>30V	Basic ESD control methods allow safe manufacturing with proven margin.
1kV	>30V	
500V	>30V	
100V to <500V	N/A	Detailed ESD control methods are required.

Table 1.2

Component-level ESD specifications for CDM.

CDM level	ESD control requirements
$V_{CDM} \geq 250V$	✧ Basic ESD control methods with grounding of metallic machine parts and control of insulators.
$125V \leq V_{CDM} < 250V$	✧ Basic ESD control methods with grounding of metallic machine parts and control of insulators. ✧ Process specific measures to reduce the charging of the device or to avoid a hard discharge.
$V_{CDM} < 125V$	✧ Basic ESD control methods with grounding of metallic machine parts and control of insulators. ✧ Process specific measures to reduce the charging of the device and to avoid a hard discharge. ✧ Charging/discharging measurements at each process step.

1.3.2 System-Level ESD Test

System-level ESD test has become an important issue of reliability in electronic products. The system-level ESD test must follow the rules of IEC 61000-4-2 specification. The definition of IEC 61000-4-2 specification is used to simulate the human-body ESD. The IEC 61000-4-2 specification is similar to the JESD22-A114E specification [19], but only difference is the size of the capacitor and the resistor. According to the standard of IEC 61000-4-2, the ESD gun is used to evaluate the system-level ESD robustness. The equivalent circuit of ESD gun is shown in Fig. 1.4 [20]. As shown in Fig. 1.4, equivalent capacitance and resistance of IEC 61000-4-2 are 150 pF (1.5 times of JESD22-A114E) and 330Ω (1/5 times of JESD22-A114E), respectively. Therefore, such a situation of large energy storage capacitor and small discharge resistor, the damage of ESD is more serious.

Comparing component-level ESD test (JESD22-A114E) with system-level ESD test (IEC 61000-4-2), as shown in Fig. 1.5. Both of the capacitors charging voltage is 1000V, and the system-level ESD current can reach peak value of 4A approximately six times of the component-level ESD current [21]-[22]. Therefore, ICs are more destroyed by system-level ESD test. That is why electronic products pass component-level ESD and they can sometimes not pass the system-level ESD test [23]-[24]. ESD gun is used for system-level ESD test, including the following two methods:

(A) Contact Discharge

This test method simulates phenomenon of ESD when the metal tools touch the electronic product. The ESD gun discharge head is composed of a metal tip for contact discharge test, as shown in Fig. 1.6.

(B) Air Discharge

This test method simulates phenomenon of ESD when the person's finger touch the electronic product. In this situation, the ESD gun will use discharge head of 8mm for air discharge test, as shown in Fig. 1.6. The air discharge test is used without contacting the electronic product.

Table 1.2 shows the test level of system-level ESD specifications with contact discharge and air discharge. Comparing Table 1.3 with Table 1.2, the system-level ESD test voltage is bigger than component-level ESD, whether under contact discharge or air discharge test modes [25].

According to phenomena of test voltage, the system-level ESD test will influence the system operation of the electronic products more important than component-level ESD test.

Table 1.4 displays the evaluation of system-level ESD test. The determination of the results of the system-level ESD test are divided into four levels, including class A, class B, class C, and class D. General recommendations, commercial electronic products must pass verification of class A or class B specification at least, in order to be accepted by the mass market.

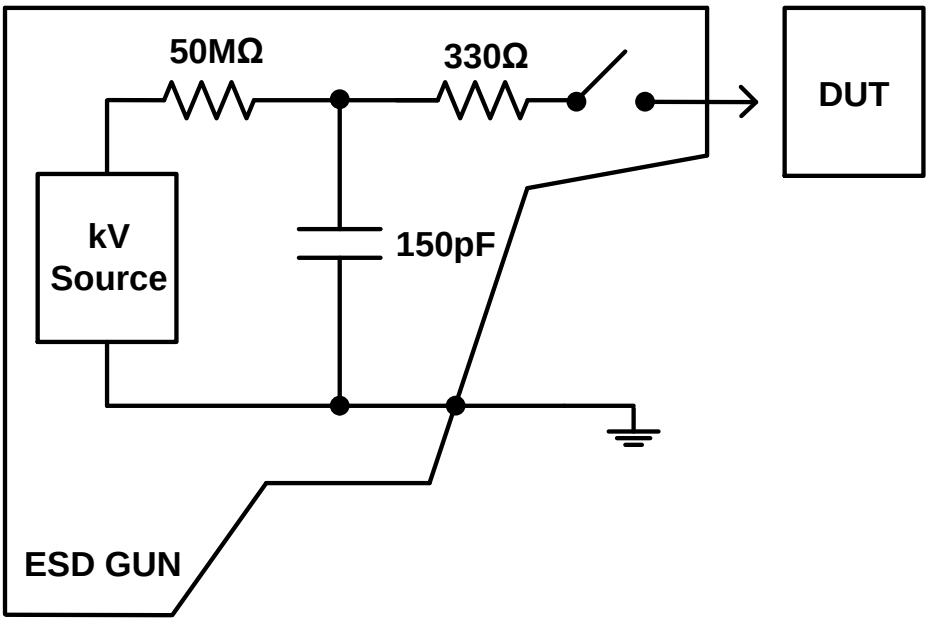


Fig. 1.4. Equivalent circuits of ESD gun under system-level ESD test.

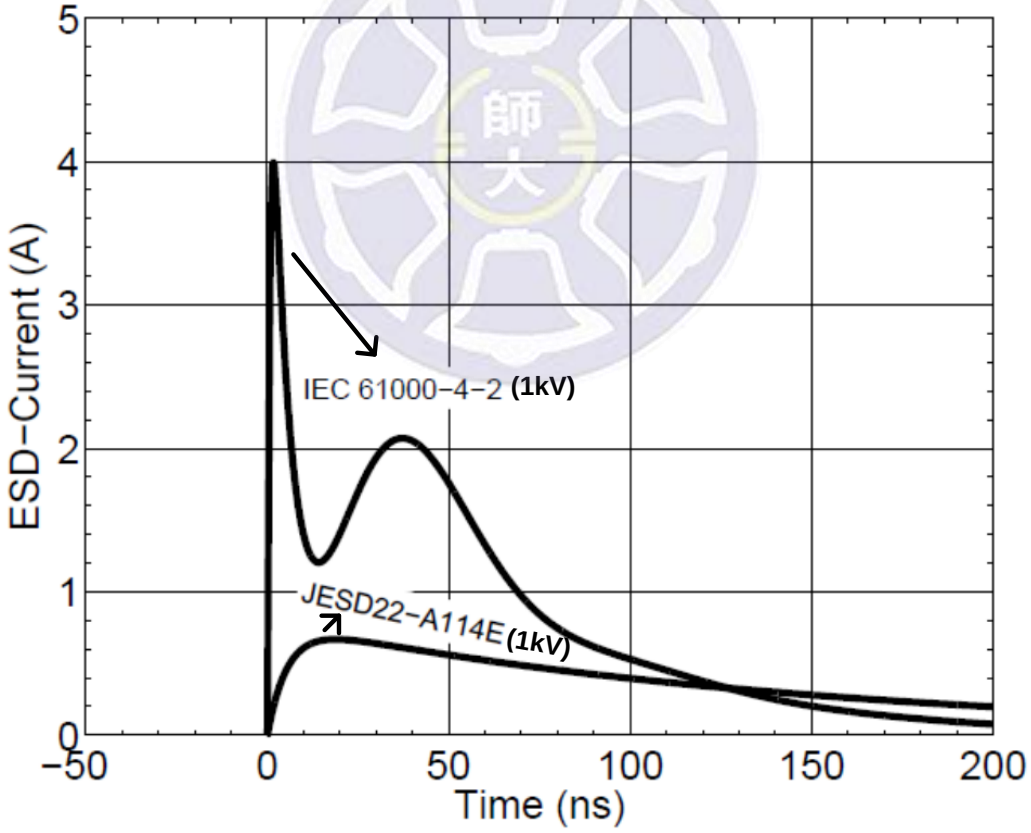


Fig. 1.5. ESD current comparison chart of component-level and system-level ESD test [22].

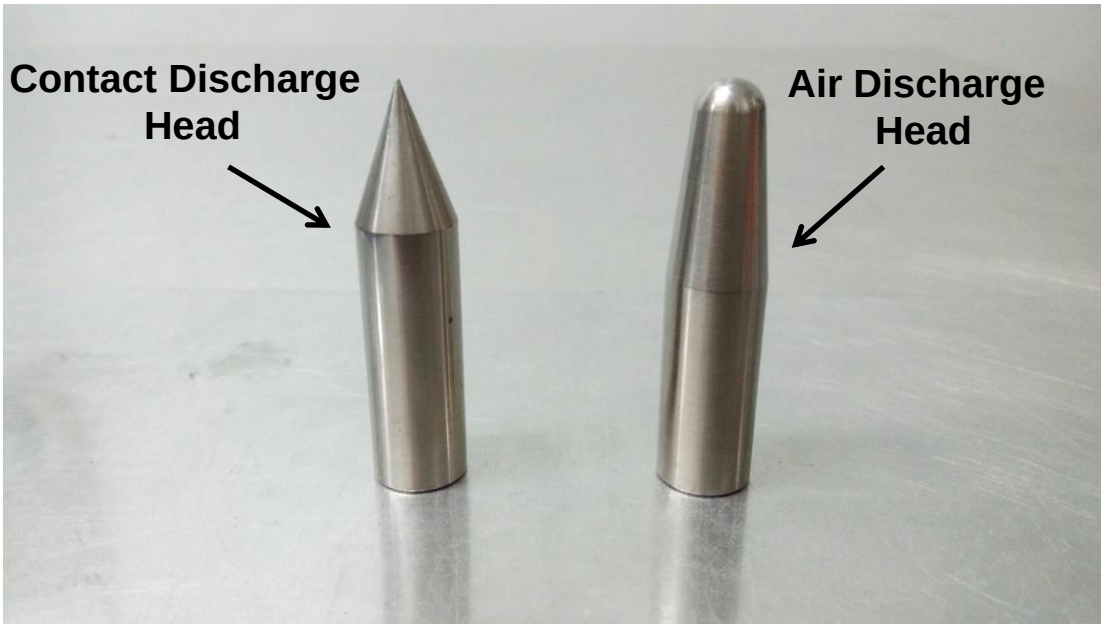


Fig. 1.6. ESD gun is used under system-level ESD test with contact discharge head and air discharge head.

Table 1.3

System-level ESD specifications.

Contact discharge		Air discharge	
Level	Test voltage	Level	Test voltage
1	±2kV	1	±2kV
2	±4kV	2	±4kV
3	±6kV	3	±8kV
4	±8kV	4	±15kV
X	Specified by customer	X	Specified by customer

Table 1.4

Recommended classifications of system-level ESD test results.

Criterion	Classification	Result
Level A	The DUT is unaffected by ESD stress.	Pass
Level B	The DUT works abnormally after ESD stress, but it will reset automatically.	Pass
Level C	The DUT works abnormally after ESD stress, but it needs to be reset manually.	Failure
Level D	The DUT failure.	Failure

There are some problems of ESD protection design. The first one is ESD design optimization and prediction, which necessitate comprehensive mixed-mode ESD simulation to address the complex coupling effects among device, process, layout and circuit. Second, ESD protection device will introduce parasitic effects, such as leakage current (I_{leak}), resistance, and capacitance (C_{ESD}), etc., which will unfavorably affect IC chip performance [46].

To guarantee the effectiveness of an ESD protection design, it has been approved that the I-V characteristics of ESD protection devices should locate within the ESD protection window. The ESD-critical parameters, typical ESD discharging I-V characteristics, and the ESD design window are shown in Fig. 1.7

An ESD protection circuit needs accurate design of ESD-critical parameters, including the ESD triggering voltage (V_{t1}) and current (I_{t1}), the ESD holding voltage (V_h), the ESD discharging resistance (R_{ON}), and thermal breakdown voltage and current (V_{t2}, I_{t2}) [47].

The ESD protection window is defined that trigger voltage (V_{t1}) should be smaller than breakdown voltage of internal circuits ($V_{BD,\ Internal}$). To ensure successful protection, the snapback holding voltage (V_{hold}) should be higher than the operational voltage (VDD) to avoid a possible latch-up issue [48].

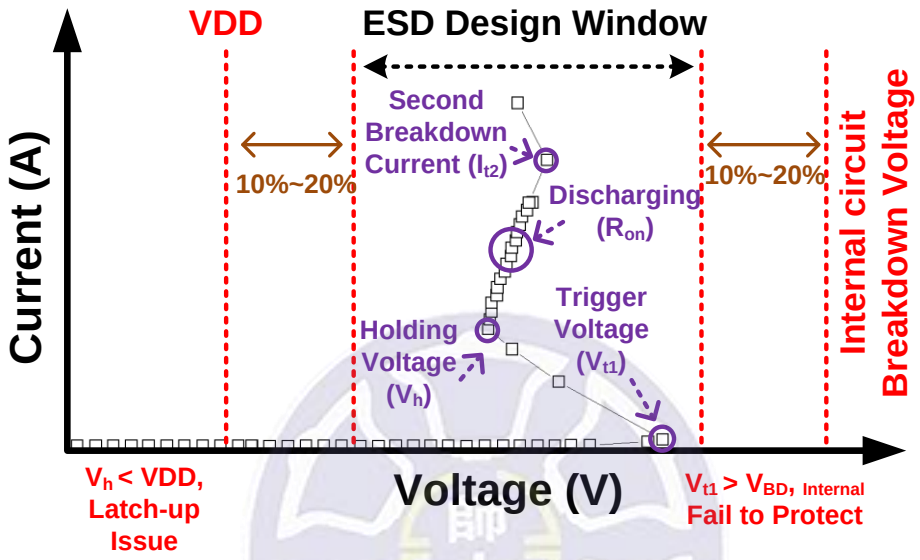


Fig. 1.7. A typical ESD protection window of ESD protection device.

1.4 Thesis Organization

In Chapter 1, the background and testing methods of ESD is introduced.

In Chapter 2, ESD protection design by using BJT, diodes, and GGNMOS will be introduced in detail. In this Chapter, all testing circuits are fabricated in 0.18um BiCMOS process.

In Chapter 3, ESD protection design by using improved diode string, diode string with embedded SCR will be introduced. In this study, all testing devices are fabricated in 0.18um CMOS process.

In chapter 4, recapitulates the major consideration of this thesis and concludes with suggestions for future investigation.

Chapter 2

Study of On-Chip ESD Protection Circuits in BiCMOS Process

Component-level ESD and system-level ESD both are the major reliability problems of electronics products. Industrial standards need to satisfy on-chip ESD protection for all ICs and systems, which becomes a constantly increasing IC design challenge for complex ICs using advanced IC technologies [26]-[27].

As shown in Fig. 2.1, the typical design of on-chip ESD protection circuits is a whole-chip ESD protection design on chip of ICs. With the design of considering the possible ESD damage sites, the ESD current discharging paths need to be created and constructed.

The ESD testing modes at input-output (I/O) pads with respect to VDD or VSS pins, VDD-to-VSS and pin-to-pin ESD stresses have been specified to judge the whole-chip ESD robustness. Under the ESD stress condition, the VDD-to-VSS ESD clamp circuit can provide a low impendence path to discharge the ESD current between the VDD and VSS power lines.

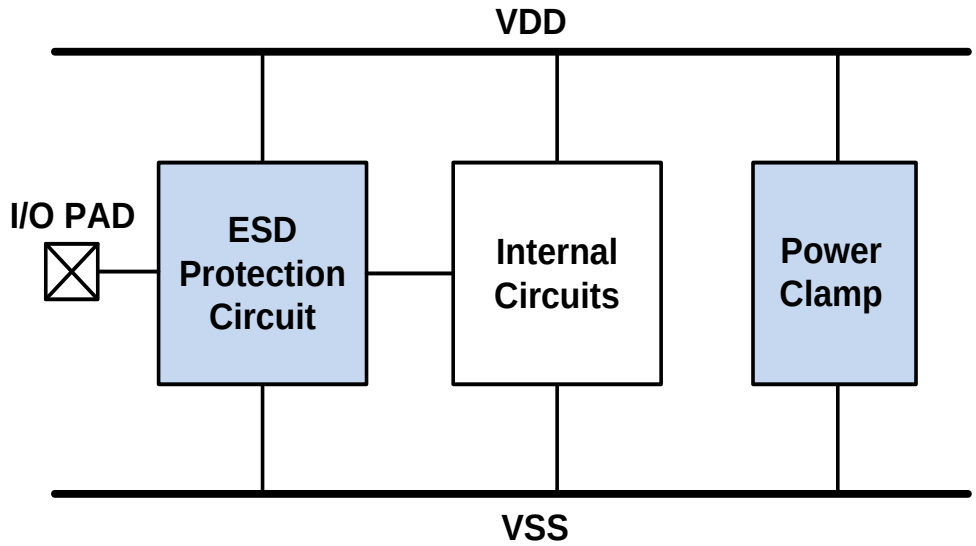


Fig. 2.1. Typical design of on-chip ESD protection circuits.

2.1 ESD Protection Design by Using BJT, Diodes, and GGNMOS

(A) Design of NPN BJT

In this work, an NPN BJT (NBJT) circuits are designed in I/O pad to VSS pad as an ESD current discharging paths. Cross-sectional view of NBJT is shown in Fig. 2.2. NBJT with its base connects to the emitter has been used for on-chip ESD protection [28], as shown in Fig. 2.3 (a). Another NBJT with on-chip resistance (R_{be}) to improve its trigger ability has also been used [29], as shown in Fig. 2.3 (b). The design parameters of NBJT display in Table 2.1. The BJT circuits are used the dimension of 60μm, 180um, and 360um. An on-chip resistance is 0Ω, 100kΩ, and 500kΩ under each dimension, respectively.

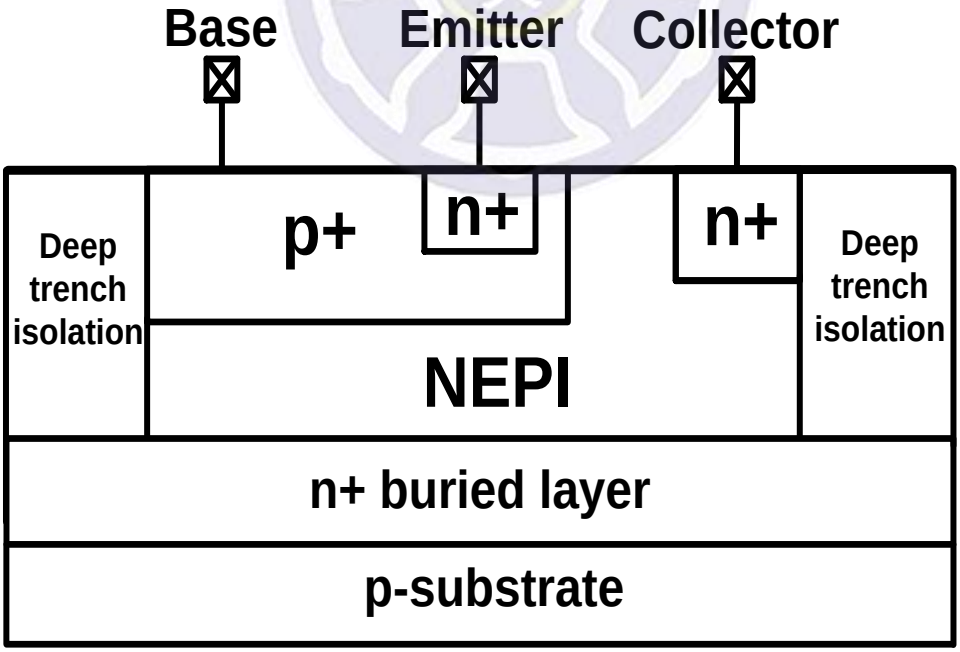
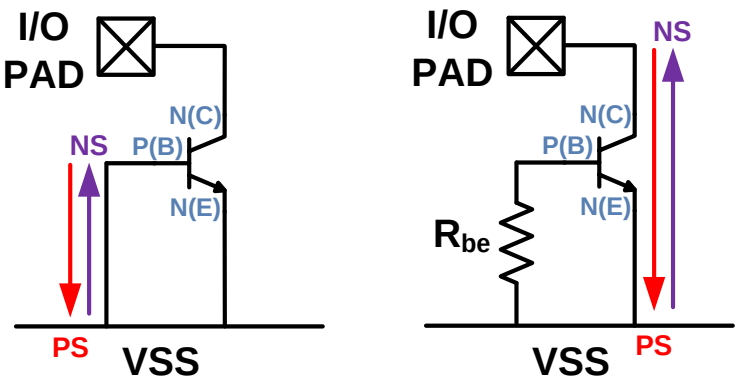


Fig. 2.2. Cross-sectional view of NBJT.



(a) (b)

Fig. 2.3. On-chip ESD protection design of NBJT with (a) base connects to emitter and (b) on-chip resistance (R_{be}).

Table 2.1

Design parameters of NBJT.

Test device	NBJT length (um)	R_{be} (kΩ)
NBJT_60_R0	60	0
NBJT_60_R100k		100
NBJT_60_R500k		500
NBJT_180_R0	180	0
NBJT_180_R100k		100
NBJT_180_R500k		500
NBJT_360_R0	360	0
NBJT_360_R100k		100
NBJT_360_R500k		500

(B) Design of diodes with power clamp

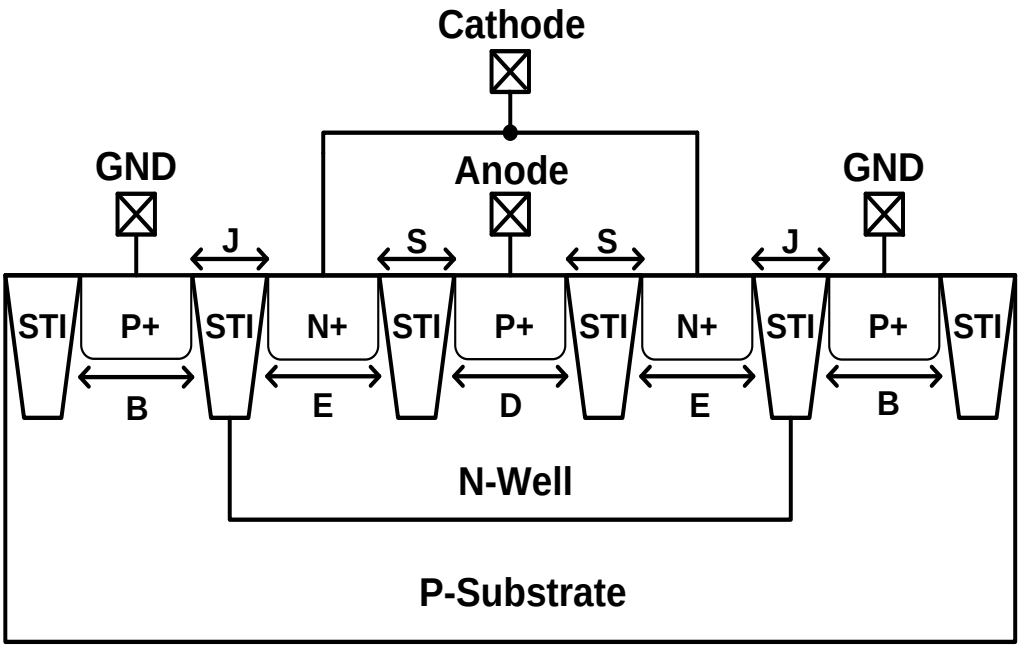
Diodes are the easiest voltage-clamping components. It has some advantages of higher current handling capability, lower trigger (cut-in) voltage, lower turn-on resistance, and smaller parasitic loading effect in the forward-biased. However, diodes exists shortcoming of poorer voltage clamping and higher on-resistance in the reverse-biased [30]-[36]. Therefore, the diodes can be used as on-chip ESD protection devices.

As shown in Fig. 2.4, the p-type diode (DP) and n-type diode (DN) are p+/n-well diodes and n+/p-well diodes, respectively. Both of diodes are operating in the reverse-biased under normal circuit operating conditions. When ESD happened, the ESD discharging current can pass through Anode P+/Cathode N+ paths in the forward-biased diodes. Therefore, the ESD discharging current passing through paths will put a few metal contacts under layout of diodes in order to prevent overcurrent from burning diodes devices. Generally, the RC-based power-rail ESD clamp (PC) circuit between the VDD and VSS is widely used as on-chip ESD protection to protect the internal circuits. It consists of a capacitor, a resistor, inverter, and ESD clamp NMOS transistor. When ESD stress happened, the NMOS transistor of ESD clamp will be turned on. The NMOS transistor can be turned off under normal circuit operation condition. The turn-on time of the NMOS transistor of ESD clamp will be adjusted by the RC-time constant of the RC-based ESD transient detection circuit to satisfy the half-energy discharging time of the HBM ESD stress [37]-[38].

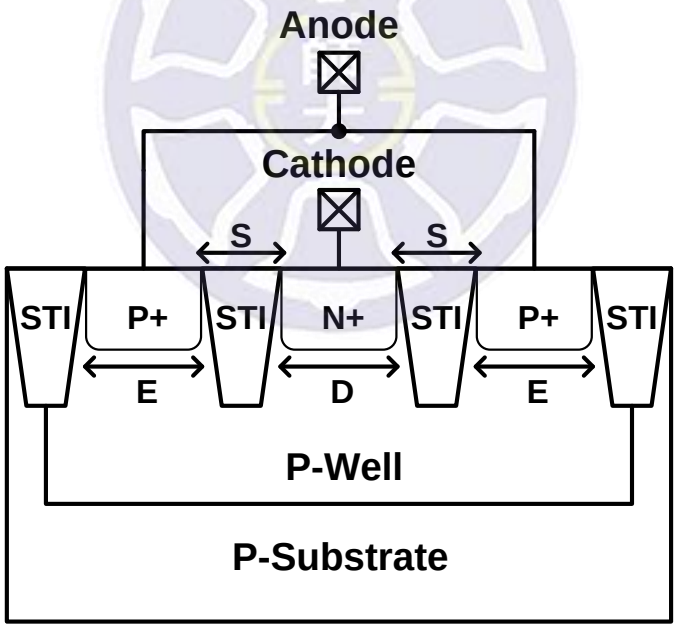
In this work, cross-sectional view of inverter and ESD clamp NMOS are shown in Fig. 2.5. The length adjustment of the ploy gate is used for the design of inverter. When ESD stress happened, the ESD discharging current can pass through the ESD clamp NMOS transistor. On-chip ESD protection design of

diodes with power clamp are shown in Fig. 2.6. When ESD stress appears in I/O pads with respect to VDD or VSS pins and VDD-to-VSS, the ESD protection circuits must give a path of ESD discharging current. Therefore, 6-types modes of the ESD current discharging paths are designed in Fig. 2.6. When positive electrostatic discharge form I/O pads to VSS pads (positive-to-VSS, PS), electrostatic current will flowing through the DP and then discharge by the power-rail ESD clamp circuit. When negative electrostatic discharge form I/O pads to VSS pads (negative-to-VSS, NS), electrostatic current will discharge by the forward-biased DN. When positive electrostatic discharge form I/O pads to VDD pads (positive-to-VDD, PD), electrostatic current will discharge by forward-biased DP. When negative electrostatic discharge form I/O pads to VDD pads (negative-to-VDD, ND), electrostatic current will pass through the power-rail ESD clamp circuit and then discharge by the forward-biased DN. When positive electrostatic discharge form VDD (Power) pads to VSS pads (VDD-to-VSS, PW+), electrostatic current will discharge by the power-rail ESD clamp circuit. When negative electrostatic discharge VDD (Power) pads to VSS pads (VSS-to-VDD, PW-), electrostatic current will discharge by the forward-biased diode of ESD clamp NMOS transistor.

The design parameters of DP and DN diodes are listed in Table 2.2. Table 2.3 shows design parameters of power-rail ESD clamp (PC). One DP, one DN, one PC are merged together to form on-chip ESD protection circuit that are diodes with power clamp.

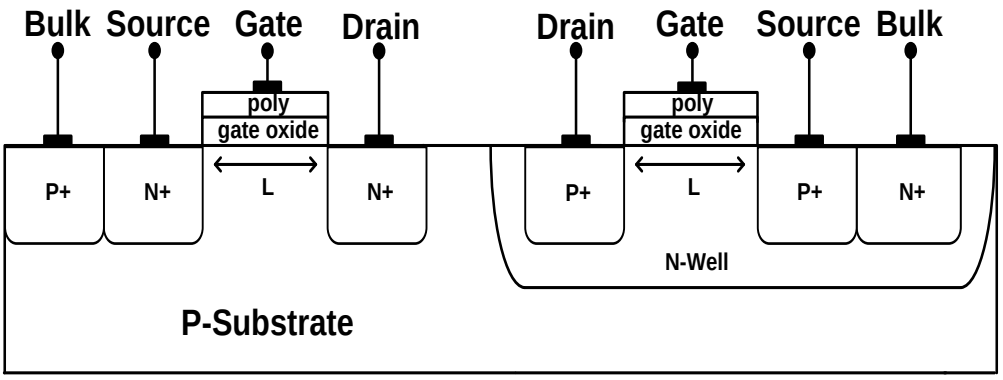


(a)

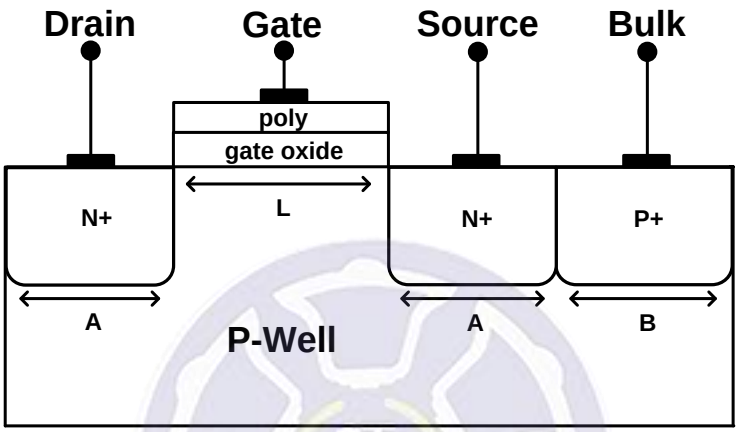


(b)

Fig. 2.4. Cross-sectional view of (a) p-type diode (DP) and (b) n-type diode (DN).



(a)



(b)

Fig. 2.5. Cross-sectional view of (a) inverter and (b) ESD clamp NMOS.

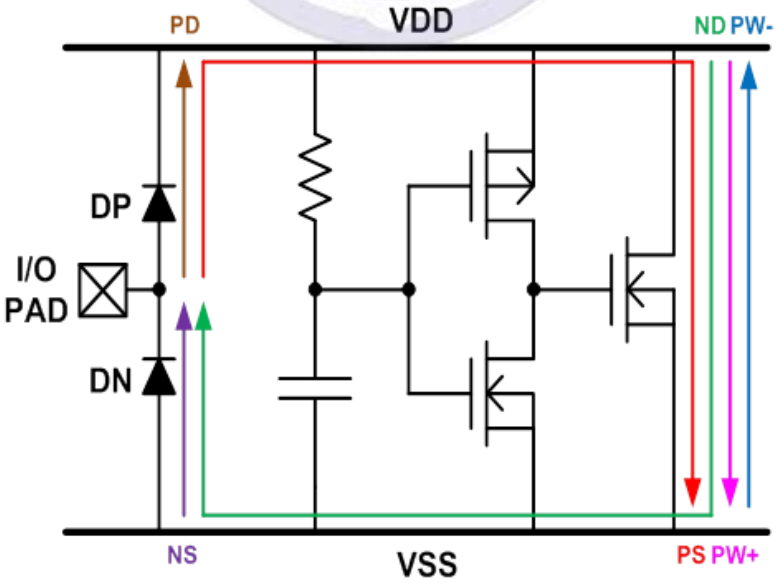


Fig. 2.6. On-chip ESD protection design of diodes with power clamp.

Table 2.2

Design parameters of diodes.

Test device	DP width (um)	DN width (um)	S (um)	J (um)	D (um)	E (um)	B (um)
DP_DN_w30	30	30	0.44	0.36	1.92	0.92	0.42
DP_DN_w60	60	60					
DP_DN_w90	90	90					

Table 2.3

Design parameters of power clamp.

Test device	Power clamp width (um)	Inverter PMOS width (um)	Inverter NMOS width (um)	L (um)	A (um)	B (um)	C (pF)	R (kΩ)
PC_w2000	2000	200	3	0.36	1.42	0.42	10	100
PC_w4000	4000	400						
PC_w8000	8000	800						

(B) Design of GGNMOS with power clamp

A gate-grounded NMOS (GGNMOS) has been widely used as ESD protection device. GGNMOS has some advantages of simple structure, snapback characteristics, and higher current handling capability under ESD stress. However, GGNMOS has potential risk of non-uniform turn-on under ESD stress [39]-[43]. The structure of GGNMOS is made from the standard NMOS structure by grounding the gate terminal, as shown in Fig. 2.7. The ESD protection device of GGNMOS can't work under normal circuit operating conditions. When positive ESD happened, the ESD discharging current can pass through drain to source in a parasitic n-p-n BJT path. An extra resist-protection-oxide (RPO) layer or silicide-blocking is used to block the silicide diffusion in the structure of GGNMOS [44]-[45]. It makes easier to turn on parasitic n-p-n BJT path of GGNMOS.

When negative ESD happened, the ESD discharging current can pass through bulk to drain in the parasitic diode path.

In Fig. 2.8, it also marked the electrostatic discharge path of 6-types when the circuit is influenced under ESD stress. Generally, GGNMOS is often used in the industry.

The design parameters of GGNMOS (GGN) are listed in Table 2.4. Table 2.5 shows design parameters of power-rail ESD clamp (PC). One GGN, one PC are merged together to form on-chip ESD protection circuit that is GGNMOS with power clamp.

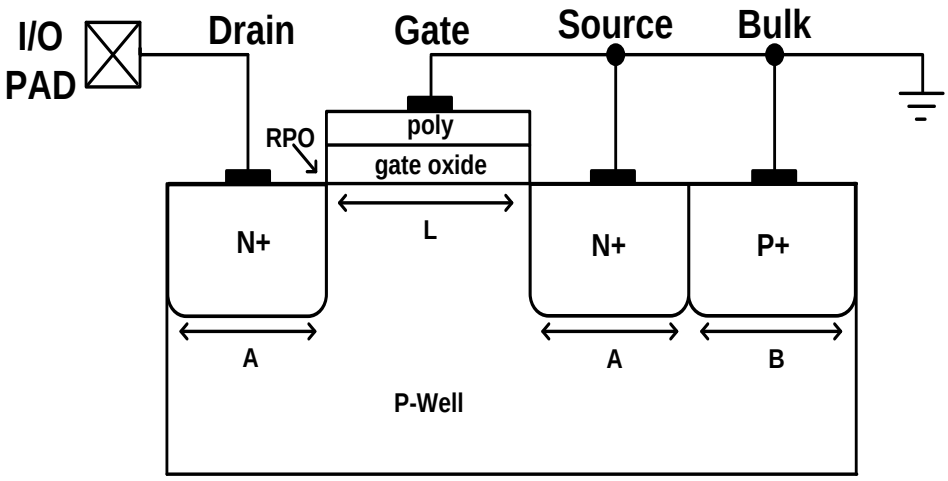


Fig. 2.7. Cross-sectional view of gate-grounded NMOS (GGNMOS).

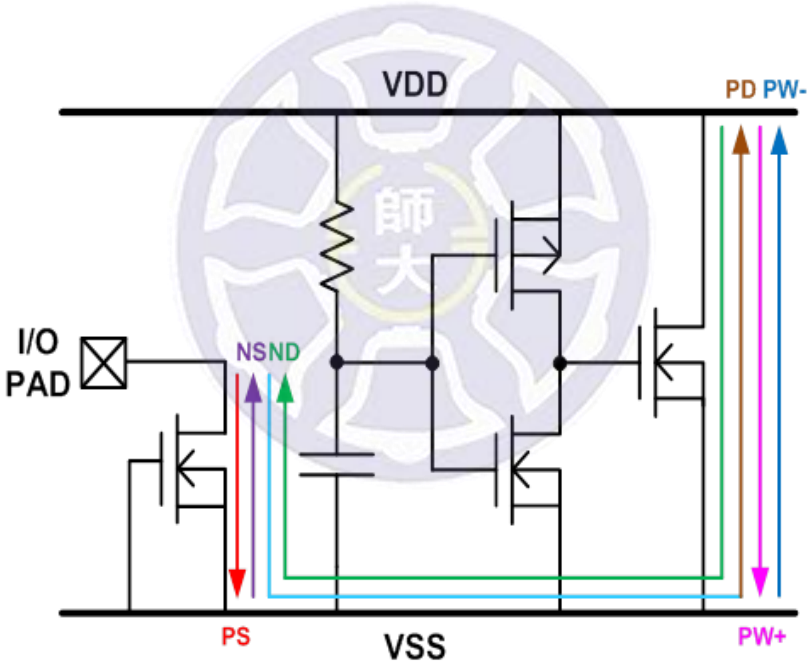


Fig. 2.8. On-chip ESD protection design of GGNMOS with power clamp.

Table 2.4

Design parameters of GGNMOS.

Test device	GGNMOS width (um)	L (um)	A (um)	B (um)
GGN_w90	90	0.36	1.42	0.42
GGN_w180	180			
GGN_w270	270			

Table 2.5

Design parameters of power clamp.

Test device	Power clamp width (um)	Inverter PMOS width (um)	Inverter NMOS width (um)	L (um)	A (um)	B (um)	C (pF)	R (kΩ)
PC_w2000	2000	200	3	0.36	1.42	0.42	10	100
PC_w4000	4000	400						
PC_w8000	8000	800						

2.2 Experimental Results under DC Voltage Supply

2.2.1 Measured Leakage Currents

To observe the leakage current and the trigger phenomenon, the leakage current of diodes with power clamp and GGNMOS with power clamp are measured.

The leakage current is swept from 0V-3.3V operating voltage under I/O-to-VSS, VDD-to-I/O, and VDD-to-VSS. The diodes with power clamp and GGNMOS with power clamp are measured under I/O-to-VSS, as shown in Fig. 2.9. In Fig. 2.9, different diodes width and different power clamps width are used to compare leakage current in Fig. 2.9 (a)-Fig. 2.9 (c) and different GGNMOS width with different power clamps width are also compared leakage current in Fig. 2.9 (d)-Fig. 2.9 (f).

In Fig. 2.9 (a)-Fig. 2.9 (c), the leakage current and trigger phenomenon of 30um diode are almost the same because the diodes width is the same. Power clamp width is different, so the leakage current is different. In Fig. 2.9 (d)-Fig. 2.9 (f), GGNMOS width is the same, so the leakage current and trigger phenomenon have almost the same.

In Fig. 2.10-Fig. 2.11, the diodes with power clamp and GGNMOS with power clamp are also measured under VDD-to-I/O and VDD-to-VSS, respectively. Different diodes with different power clamp are used to compare leakage current. GGNMOS with power clamp are also compared leakage current.

The measured leakage currents of diodes with power clamps and GGNMOS with power clamps under normal operating voltage of 1.8V are shown in Table 2.7 and Table 2.8, respectively.

Under I/O-to-VSS, VDD-to-I/O, and VDD-to-VSS, the leakage current will increase along with the different width of diodes, GGNMOS, and power clamp

under operating voltage 1.8V. If the width of diodes, GGNMOS, and power clamp are the same, the leakage current has also almost the same. The safe operating area (SOA) is defined as the leakage current shown shifting over 10%~20% from its original leakage current. Therefore, the measurement results have been achieved expectation.

As shown in Fig. 2.12 (a)-Fig. 2.12 (c), the leakage current of NBJT are measured. The leakage current is swept under operating voltage from 0 to 12V.

In Fig. 2.12 (a), the test device of NBJT_60_R0 has lower leakage current than NBJT_60_R100k and NBJT_60_R500k. In Fig. 2.12 (b), the test device of NBJT_180_R0 has higher leakage current than NBJT_180_R100k and NBJT_180_R500k. In Fig. 2.13 (c), the test device of NBJT_360_R100k has higher leakage current than NBJT_360_R0 and NBJT_360_R500k. The DC-IV characteristics of NBJT measured results under normal operating voltage of 1.8V are shown in Table 2.6.

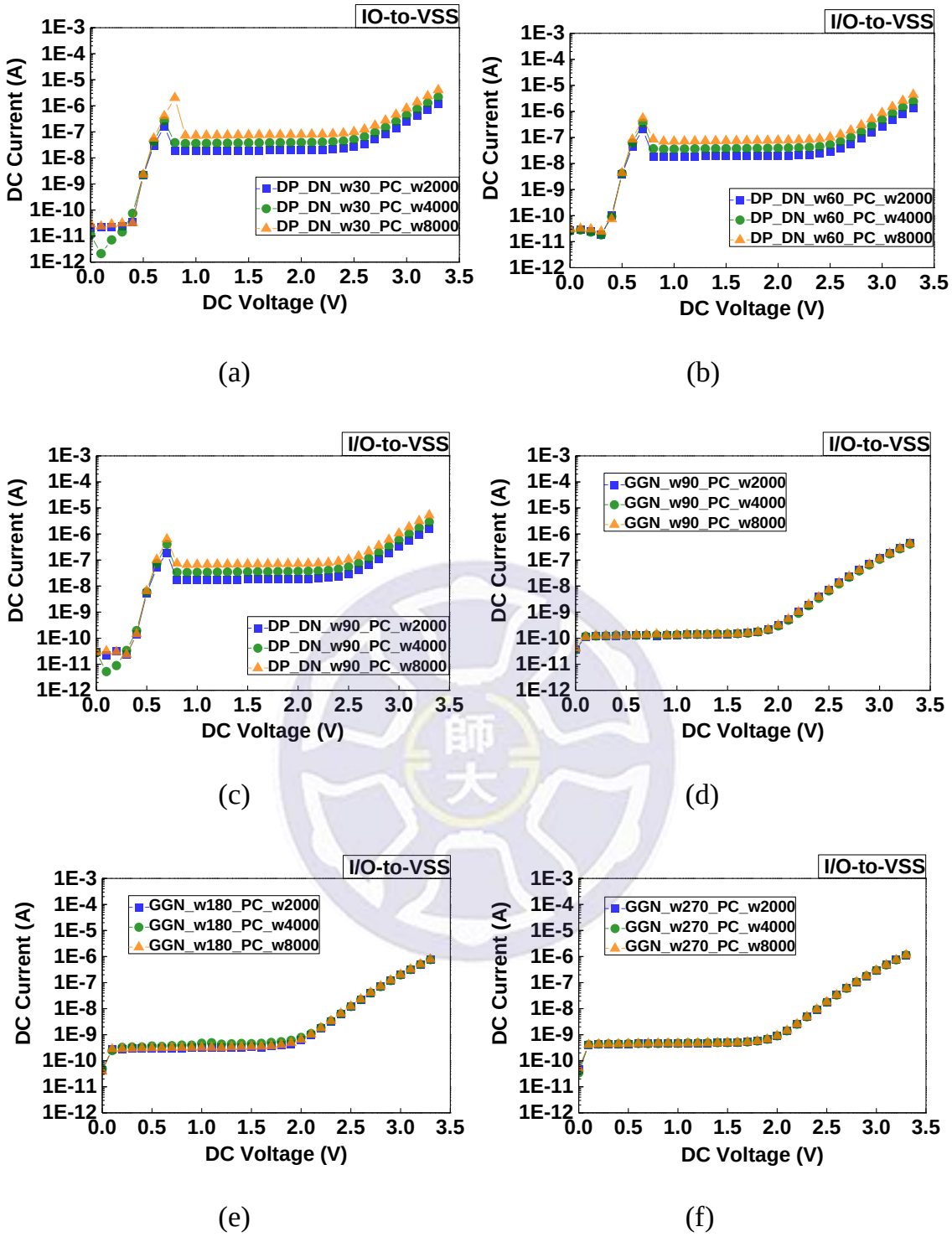


Fig. 2.9. Measured leakage currents of (a) 30um diodes with power clamps under I/O-to-VSS mode, (b) 60um diodes with power clamps under I/O-to-VSS mode, (c) 90um diodes with power clamps under I/O-to-VSS mode, (d) 90um GGNMOS with power clamps under I/O-to-VSS mode, (e) 180um GGNMOS with power clamps under I/O-to-VSS mode, and (f) 270um GGNMOS with power clamps under I/O-to-VSS mode.

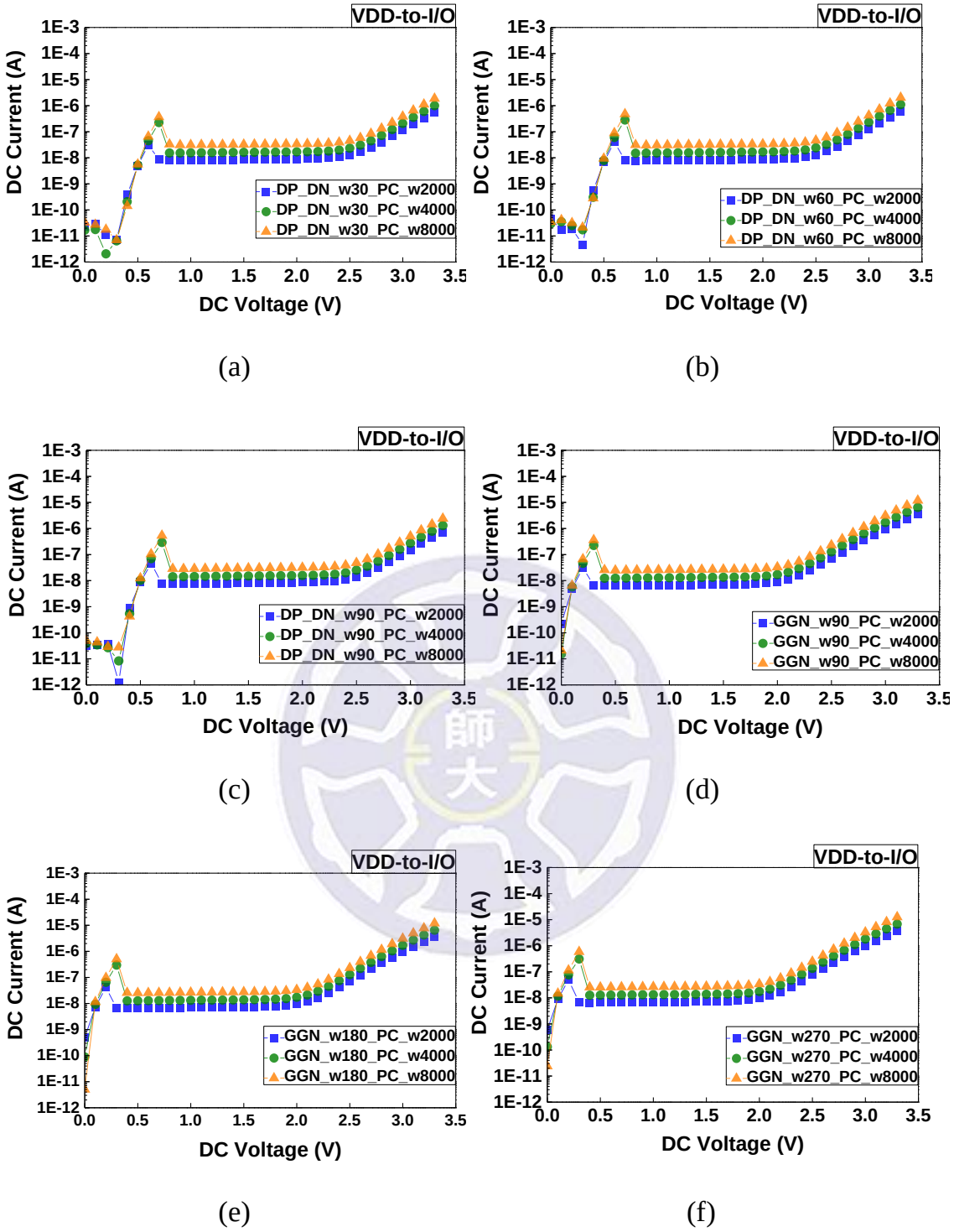


Fig. 2.10. Measured leakage currents of (a) 30um diodes with power clamps under VDD-to-I/O mode, (b) 60um diodes with power clamps under VDD-to-I/O mode, (c) 90um diodes with power clamps under VDD-to-I/O mode, (d) 90um GGNMOS with power clamps under VDD-to-I/O mode, (e) 180um GGNMOS with power clamps under VDD-to-I/O mode, and (f) 270um GGNMOS with power clamps under VDD-to-I/O mode.

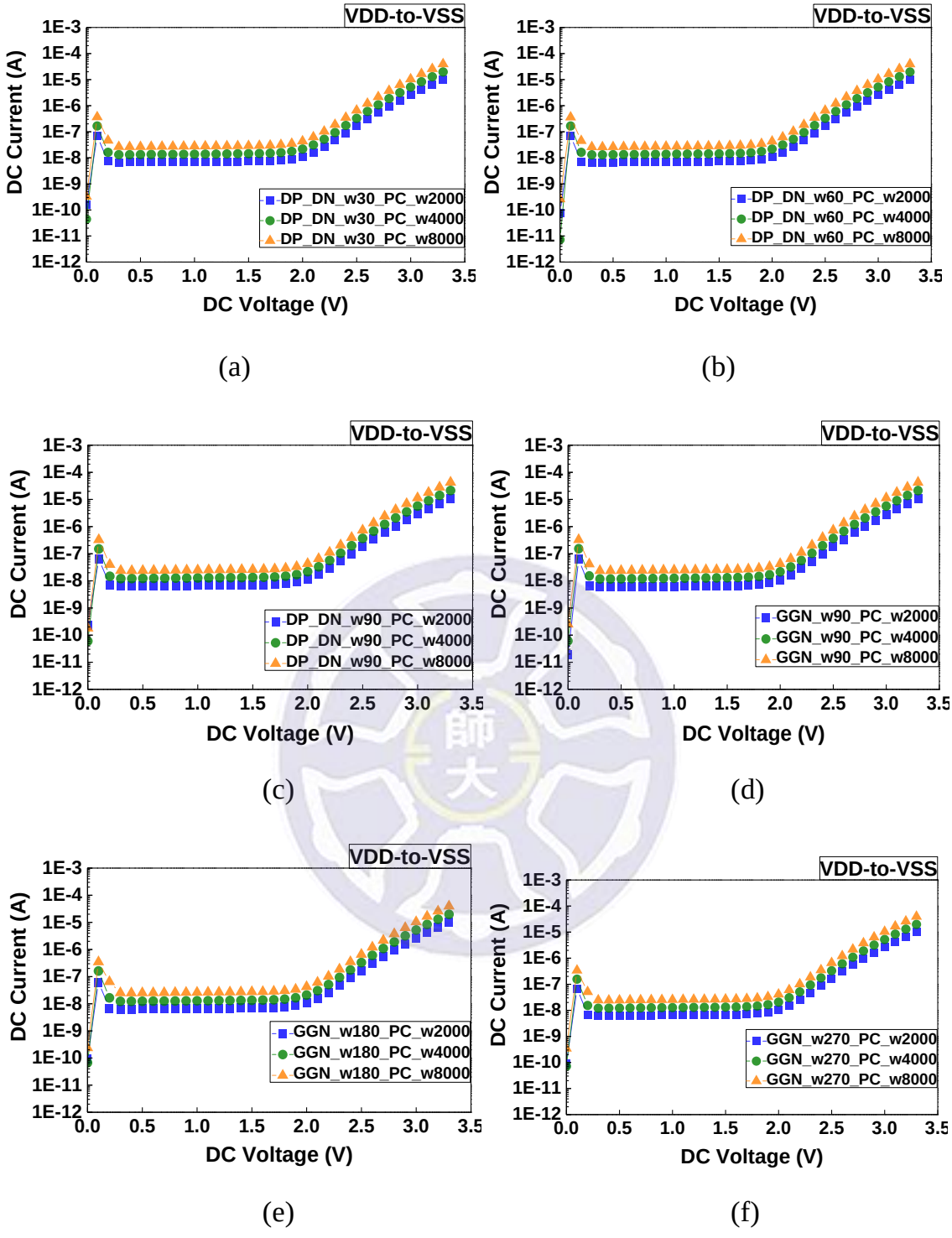
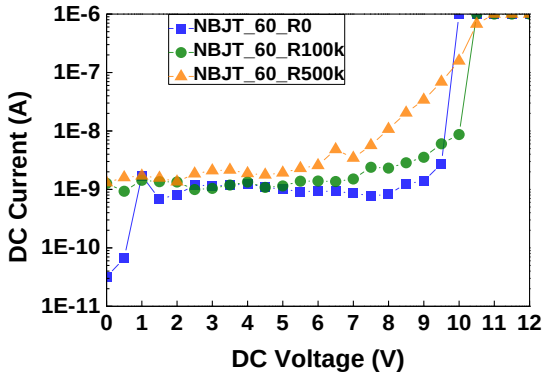
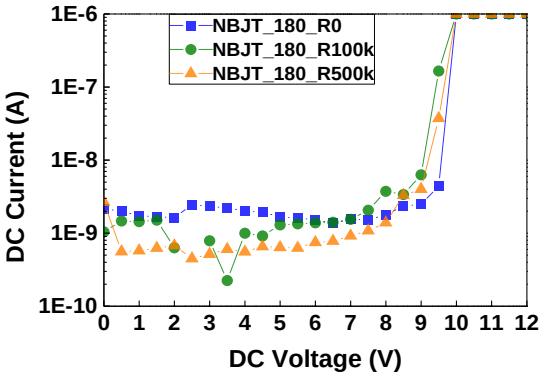


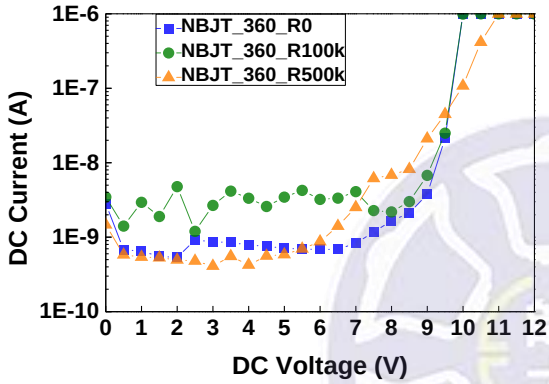
Fig. 2.11. Measured leakage currents of (a) 30um diodes with power clamps under VDD-to-VSS mode, (b) 60um diodes with power clamps under VDD-to-VSS mode, (c) 90um diodes with power clamps under VDD-to-VSS mode, (d) 90um GGNMOS with power clamps under VDD-to-VSS mode, (e) 180um GGNMOS with power clamps under VDD-to-VSS mode, and (f) 270um GGNMOS with power clamps under VDD-to-VSS mode.



(a)



(b)



(c)

Fig. 2.12. Measured leakage currents of (a) 60um NBJT with 0Ω, 100kΩ, and 500kΩ resistances under I/O-to-VSS mode, (b) 180um NBJT with 0Ω, 100kΩ, and 500kΩ resistances under I/O-to-VSS mode, (c) 360um NBJT with 0Ω, 100kΩ, and 500kΩ resistances under I/O-to-VSS mode.

Table 2.6

The measured leakage currents of NBJT under normal operating voltage of 1.8V.

Test device	Leakage current (nA) at 1.8 V
NBJT_60_R0	0.8
NBJT_60_R100k	1.3
NBJT_60_R500k	1.3
NBJT_180_R0	1.6
NBJT_180_R100k	0.6
NBJT_180_R500k	0.6
NBJT_360_R0	0.5
NBJT_360_R100k	4.7
NBJT_360_R500k	0.5

Table 2.7

The measured leakage currents of diodes with power clamps under normal operating voltage of 1.8V.

Test device	Leakage current (nA) at 1.8 V		
	I/O-to-VSS	VDD-to-I/O	VDD-to-VSS
DP_DN_w30_PC_w2000	19.7	8.6	8.1
DP_DN_w30_PC_w4000	38.7	16.6	15.8
DP_DN_w30_PC_w8000	77.3	33.2	31.5
DP_DN_w60_PC_w2000	19.7	8.4	7.9
DP_DN_w60_PC_w4000	38.3	16.4	15.7
DP_DN_w60_PC_w8000	76.0	32.8	31.0
DP_DN_w90_PC_w2000	18.4	8.3	7.9
DP_DN_w90_PC_w4000	36.2	15.5	14.9
DP_DN_w90_PC_w8000	71.0	30.9	29.1

Table 2.8

The measured leakage currents of GGNMOS with power clamps under normal operating voltage of 1.8V.

Test device	Leakage current (nA) at 1.8 V		
	I/O-to-VSS	VDD-to-I/O	VDD-to-VSS
GGN_w90_PC_w2000	0.17	7.5	7.4
GGN_w90_PC_w4000	0.17	14.3	14.5
GGN_w90_PC_w8000	0.17	28.2	28.9
GGN_w180_PC_w2000	0.39	7.8	7.7
GGN_w180_PC_w4000	0.54	14.6	14.8
GGN_w180_PC_w8000	0.40	28.9	30.1
GGN_w270_PC_w2000	0.56	7.8	7.5
GGN_w270_PC_w4000	0.57	14.6	14.6
GGN_w270_PC_w8000	0.56	28.8	29.1

2.2.2 Measured DC I-V Characteristics

To understand relationship of the trigger voltage and holding voltage, the test devices need to be further explored. In this work, snapback holding voltage of the NBJT and diodes with power clamp has been investigated by DC curve tracer. The measurement was carried out with Tektronix 370A DC curve tracer as shown in Fig. 2.13. All these measurement results are listed in Table 2.9.

As shown in Fig. 2.13. (a), NBJT_180_R0 is 180um NBJT with 0Ω resistance under I/O-to-VSS mode. The turn on phenomenon is mainly through the collector-base path. NBJT_180_R0 has no snapback phenomenon and its holding voltage is equivalent to trigger voltage.

As shown in Fig. 2.13. (b)-Fig. 2.13. (c), NBJT_180_R100k and NBJT_180_R500k both have the R_{be} under IO-to VSS mode. The turn on phenomenon is mainly through the BJT collector-emitter path. NBJT_180_R100k and NBJT_180_R500k both have snapback phenomenon. NBJT_180_R100k has snapback from 9.85V trigger voltage to 3.3V holding voltage. NBJT_180_R500k has snapback from 10V trigger voltage to 3.2V holding voltage.

As shown in Fig. 2.13. (d)-Fig. 2.13. (f), DP_DN_w90_PC_w2000 has snapback a little from 6.35V to 5.05V. DP_DN_w90_PC_w4000 has snapback a little from 6.35V to 5V. DP_DN_w90_PC_w8000 has snapback a little from 6.4V to 5V. They have almost the same.

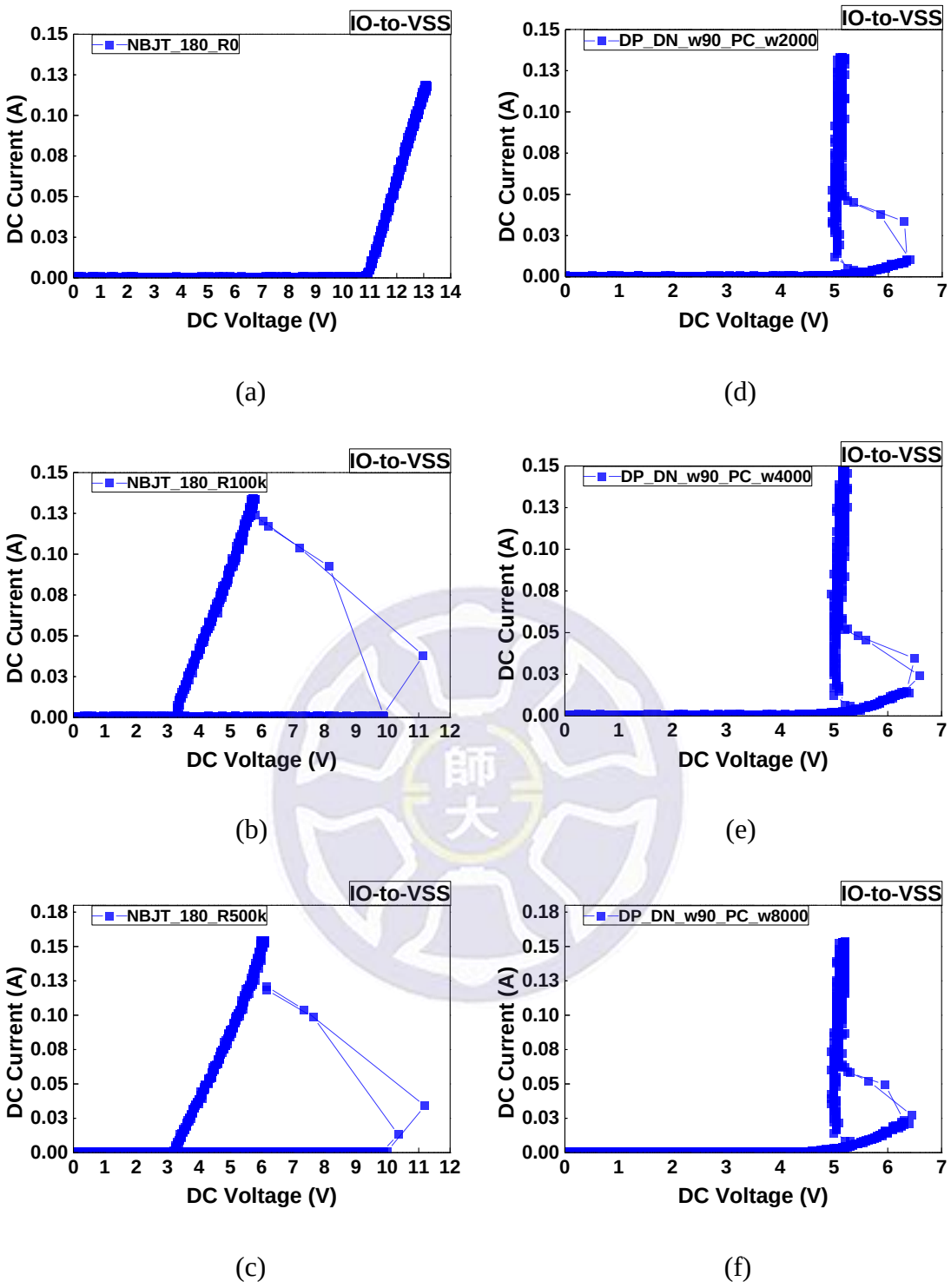


Fig. 2.13. Measured DC-IV characteristics of (a) 180um NBJT with 0Ω resistance under I/O-to-VSS mode, (b) 180um NBJT with 100kΩ resistance under I/O-to-VSS mode, (c) 180um NBJT with 500kΩ resistance under I/O-to-VSS mode, (d) 90um diode with 2000um power clamp under I/O-to-VSS mode, (e) 90um diode with 4000um power clamp under I/O-to-VSS mode, and (f) 90um diode with 8000um power clamp under I/O-to-VSS mode.

Table 2.9

The measured DC-IV characteristics of NBJT and diodes with power clamps under I/O-to-VSS mode.

Test device	I/O-to-VSS	
	V_{t1} (V)	V_h (V)
NBJT_180_R0	11	11
NBJT_180_R100k	9.85	3.3
NBJT_180_R500k	10	3.25
DP_DN_w90_PC_w2000	6.35	5.05
DP_DN_w90_PC_w4000	6.35	5
DP_DN_w90_PC_w8000	6.4	5

2.3 Experimental Results under Component-Level ESD Test

In this section, human-body-model (HBM) and transmission-line-pulsing (TLP) is used to measure component-level ESD robustness, which means it alone do the test for on-chip ESD protection device.

2.3.1 Measured TLP I-V Curves

The transmission-line-pulsing (TLP) system with 10-ns rise time and 100-ns pulse width is used to understand the turn-on behavior and the I-V characteristics in high-current regions of the ESD protection devices.

Each on-chip ESD protection device has been tested by TLP tester. The failure criterion is defined as leakage current shown between the test pads shifting over 30% from its original leakage current.

The TLP-measured I-V characteristics of NBJT, diodes with power clamp, and GGNMOS with power clamp are shown in Fig. 2.14-Fig. 2.19. In Fig. 2.14 (a)-Fig. 2.14 (c), TLP-IV characteristics of NBJT are measured under PS mode ESD stress. The NBJT_60_R0, NBJT_180_R0, and NBJT_360_R0 have not R_{be} under PS mode. The current discharging path is mainly through the collector-base path which is a reverse-biased diode.

The NBJT_60_R100k, NBJT_60_R500k, NBJT_180_R100k, NBJT_180_R500k, NBJT_360_R100k, and NBJT_360_R500k have R_{be} under PS mode so that they have a lower trigger voltage and a higher current handling ability. With the help of R_{be}, the current discharging path is mainly through the collector-emitter path, so the ESD protection ability of the BJT circuits can be improved.

In Fig. 2.14 (d)-Fig. 2.14 (f), TLP-IV characteristics of NBJT are measured

under NS mode ESD stress. The current discharging path of the NBJT_60_R0, NBJT_180_R0, and NBJT_360_R0 under NS mode is mainly through the base-collector path which is a forward-biased diode.

They have a higher current handling ability than the NBJT_60_R100k, NBJT_60_R500k, NBJT_180_R100k, NBJT_180_R500k, NBJT_360_R100k, and NBJT_360_R500k under NS mode. If the higher current handling ability is required under NS mode, the designer can increase guard ring of the NBJT.

In Fig. 2.15 (a)-Fig. 2.15 (f), TLP-IV characteristics of diodes with power clamp and GGNMOS with power clamp are measured under PS mode ESD stress. The V_{t1} of all diodes with power clamp about 1.6V-1.8V. The V_{t1} is defined as voltage value of current 10mA. The V_h is also about 1.6V-1.8V because the diodes have no "snapback" phenomenon. The V_h is equal to V_{t1}. The addition of dimension will cause lower R_{on} and higher I_{t2}. The V_{t1} and V_h of all GGNMOS with power clamp have almost the same. The addition of dimension will cause lower R_{on} and higher $I_{t2.}$

In Fig. 2.16 (a)-Fig. 2.16 (c), TLP-IV characteristics of diodes with power clamp are measured under NS mode ESD stress. The V_{t1} of all diodes with power clamp are about 0.94V-1V. The V_{t1} is defined as voltage value of current 10mA. The V_h is also about 0.94V-1V. The V_h is equal to V_{t1}. The addition of dimension will result in lower R_{on} and higher I_{t2}. Under NS mode ESD stress, the leakage current will increase by the different width of diodes with power clamp because different width of power clamp relate to leakage current. In Fig. 2.16 (d)-Fig. 2.16 (f), the addition of dimension will also result in lower R_{on} and higher I_{t2}. Under NS mode ESD stress, GGNMOS is similar to diodes. The V_{t1} and V_h are also the same.

In Fig. 2.17 (a)-Fig. 2.17 (c), TLP-IV characteristics of diodes with power

clamp are measured under PD mode ESD stress. The V_{t1} of all diodes with power clamp are about 0.94V-1.11V. The V_{t1} is defined as voltage value of current 10mA. The V_h is also about 0.94V-1.11V. The V_h is equal to V_{t1}. The addition of dimension will result in lower R_{on} and higher I_{t2}. Under PD mode ESD stress, the leakage current will increase by the different diodes with power clamp because different power clamps can influence leakage current. In Fig. 2.17 (d)-Fig. 2.17 (f), the addition of dimension will also result in lower R_{on} and higher I_{t2}. The GGNMOS have "snapback" phenomenon. This phenomenon can result in distinctive of trigger voltage and holding voltage. Under operating voltage 1.8V, the GGNMOS circuits have not "latch up" phenomenon. The "latch up" will cause the internal circuits working abnormality. The addition of dimension will also result in lower R_{on} and higher I_{t2}.

In Fig. 2.18 (a)-Fig. 2.18 (c), TLP-IV characteristics of diodes with power clamp are measured under ND mode ESD stress. The V_{t1} of all diodes with power clamp about 1.59V-1.81V. The V_{t1} is defined as voltage value of current 10mA. The V_h is also about 1.59V-1.81V. The V_h is equal to V_{t1}. The addition of dimension will result in lower R_{on} and higher I_{t2}. In Fig. 2.18 (d)-Fig. 2.18 (f), the addition of dimension will also result in lower R_{on} and higher I_{t2}.

In Fig. 2.19 (a)-Fig. 2.19 (f), TLP-IV characteristics of diodes with power clamp and GGNMOS with power clamp are measured under PW+ mode ESD stress. The V_{t1} of all power clamp about 0.73V-1.09V and 0.74V-0.83V. The V_{t1} is defined as voltage value of current 10mA for power clamp. The V_h is also equal to V_{t1}. Under PW+ mode ESD stress, the addition of dimension will also result in lower R_{on} and higher I_{t2}.

In Fig. 2.20 (a)-Fig. 2.20 (f), TLP-IV characteristics of diodes with power clamp and GGNMOS with power clamp are measured under PW- mode ESD

stress. Under PW- mode ESD stress, parasitic diodes of NMOS will turn-on as ESD current discharging path. The V_{t1} of all power clamp about 0.52V-0.69V and 0.52V-0.73V. The V_{t1} is defined as voltage value of current 10mA for power clamp. The V_h is also equal to V_{t1}. Under PW- mode ESD stress, the addition of dimension will also result in lower R_{on} and higher I_{t2}.

TLP-IV characteristics of all test circuits are measured under PS, NS, PD, ND, PW+, and PW- mode ESD stress. All these TLP measurement results are also listed in Table 2.10, Table 2.11, Table 2.12, Table 2.13, Table 2.14, Table 2.15, and Table 2.16.

Some leakage currents are higher and others are lower after TLP-IV characteristics are measured in PS mode of diodes with power clamps. Metal of guard ring of p-type diode (DP) was probably burned to short after the devices are measured by TLP due to metal of guard ring of p-type diode (DP) connects to the VSS. Thus, the leakage current can pass through two type paths. One pass from DP to power clamp and the other pass from DP to VSS that could not pass the power clamp. The pulsed current can pass from DP to VSS that can cause the metal of guard ring of DP to burn from shorting to opening. The leakage currents could reduce after TLP-IV curves was measured.

After measuring TLP-IV curves, the leakage current of 90um GGNMOS with power clamps is lower than leakage current of 180um and 360um GGNMOS with power clamps under PD mode. The metal of GGNMOS was burned to short after the devices are measured by TLP. The 0.8A in TLP-IV curve have slightly shifted that can prove the GGNMOS destruction. The pulsed current can pass through the metal of GGNMOS until the metal burned out from shorting to opening. The metal opening can cause the leakage current to reduce.

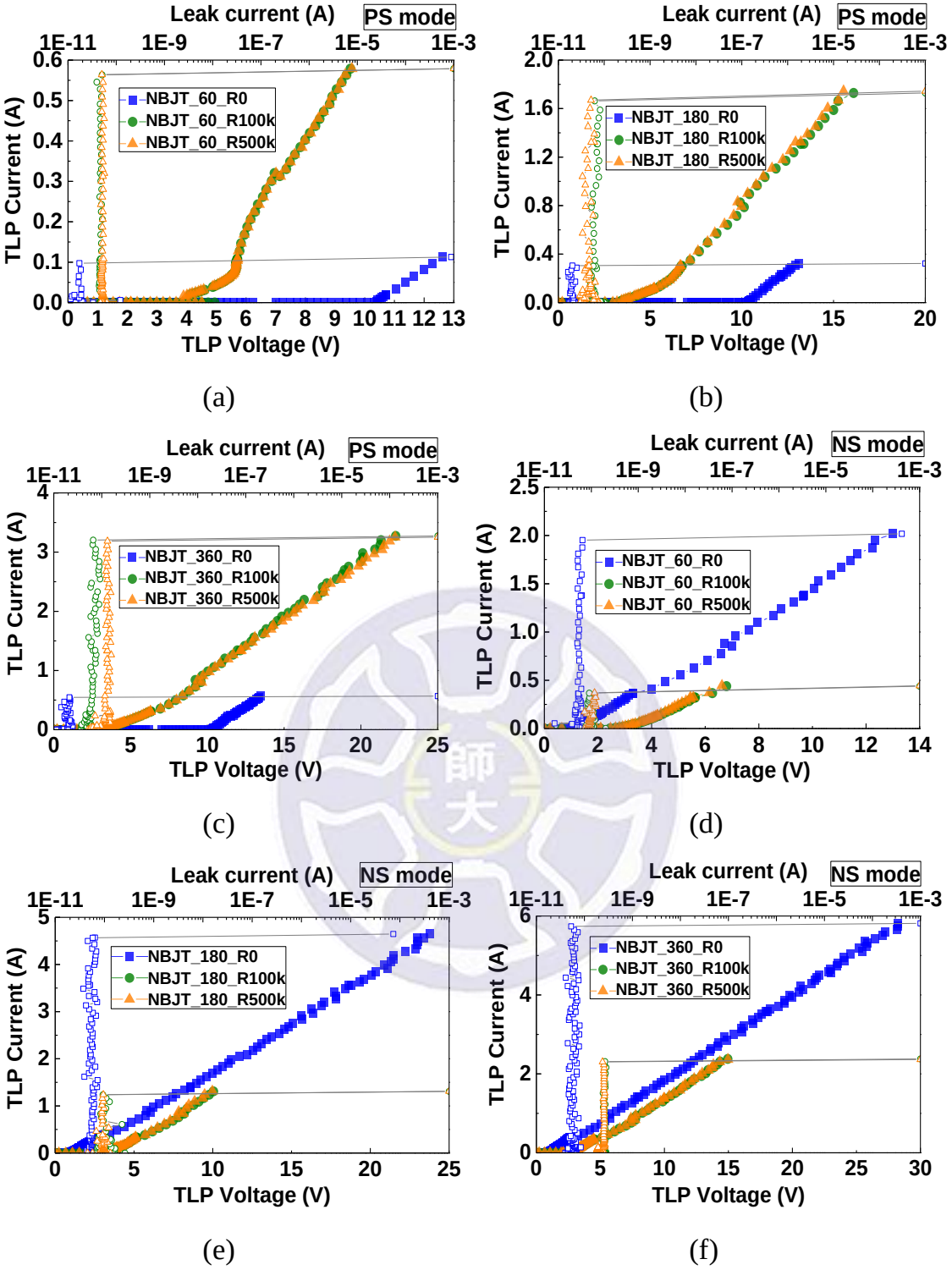


Fig. 2.14. Measured TLP-IV characteristics of (a) 60um NBJT with 0Ω, 100kΩ, and 500kΩ resistances under PS mode, (b) 180um NBJT with 0Ω, 100kΩ, and 500kΩ resistances under PS mode, (c) 360um NBJT with 0Ω, 100kΩ, and 500kΩ resistances under PS mode, (d) 60um NBJT with 0Ω, 100kΩ, and 500kΩ resistances under NS mode., (e) 180um NBJT with 0Ω, 100kΩ, and 500kΩ resistances under NS mode, (f) 360um NBJT with 0Ω, 100kΩ, and 500kΩ resistances under NS mode.

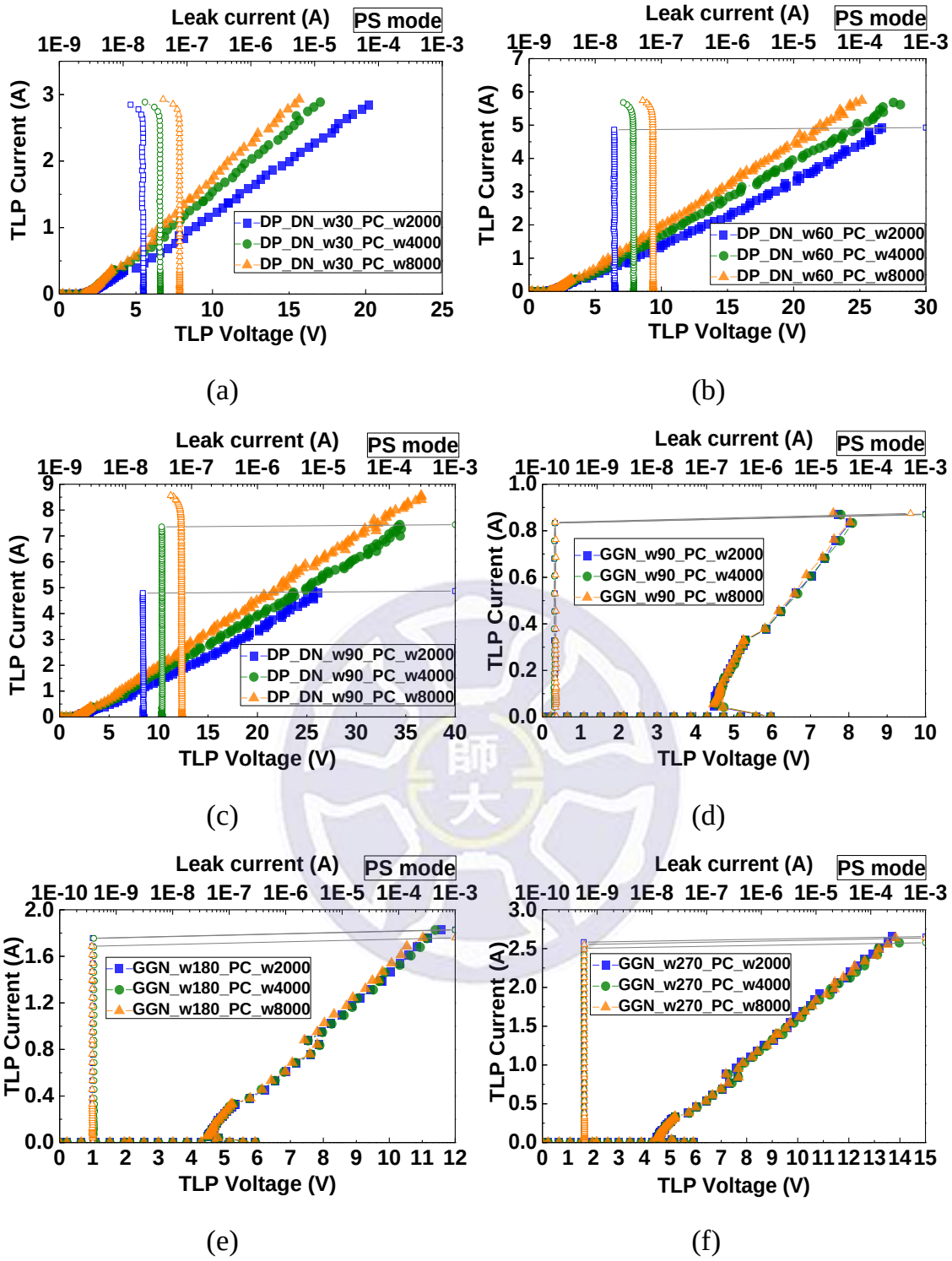


Fig. 2.15. Measured TLP-IV characteristics of (a) 30um diodes with power clamps under PS mode, (b) 60um diodes with power clamps under PS mode, (c) 90um diodes with power clamps under PS mode, (d) 90um GGNMOS with power clamps under PS mode, (e) 180um GGNMOS with power clamps under PS mode, and (f) 270um GGNMOS with power clamps under PS mode.

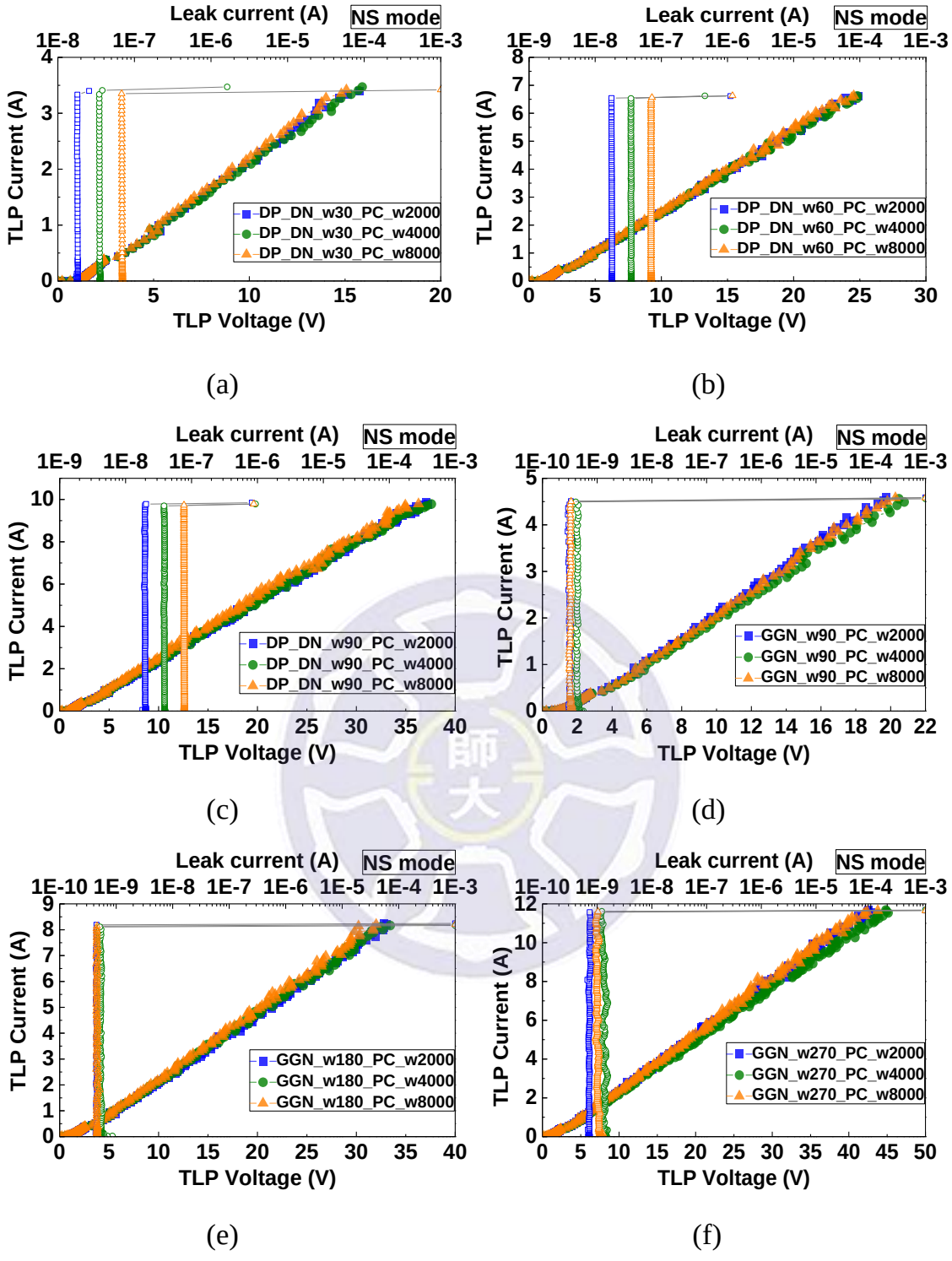


Fig. 2.16. Measured TLP-IV characteristics of (a) 30um diodes with power clamps under NS mode, (b) 60um diodes with power clamps under NS mode, (c) 90um diodes with power clamps under NS mode, (d) 90um GGNMOS with power clamps under NS mode, (e) 180um GGNMOS with power clamps under NS mode, and (f) 270um GGNMOS with power clamps under NS mode.

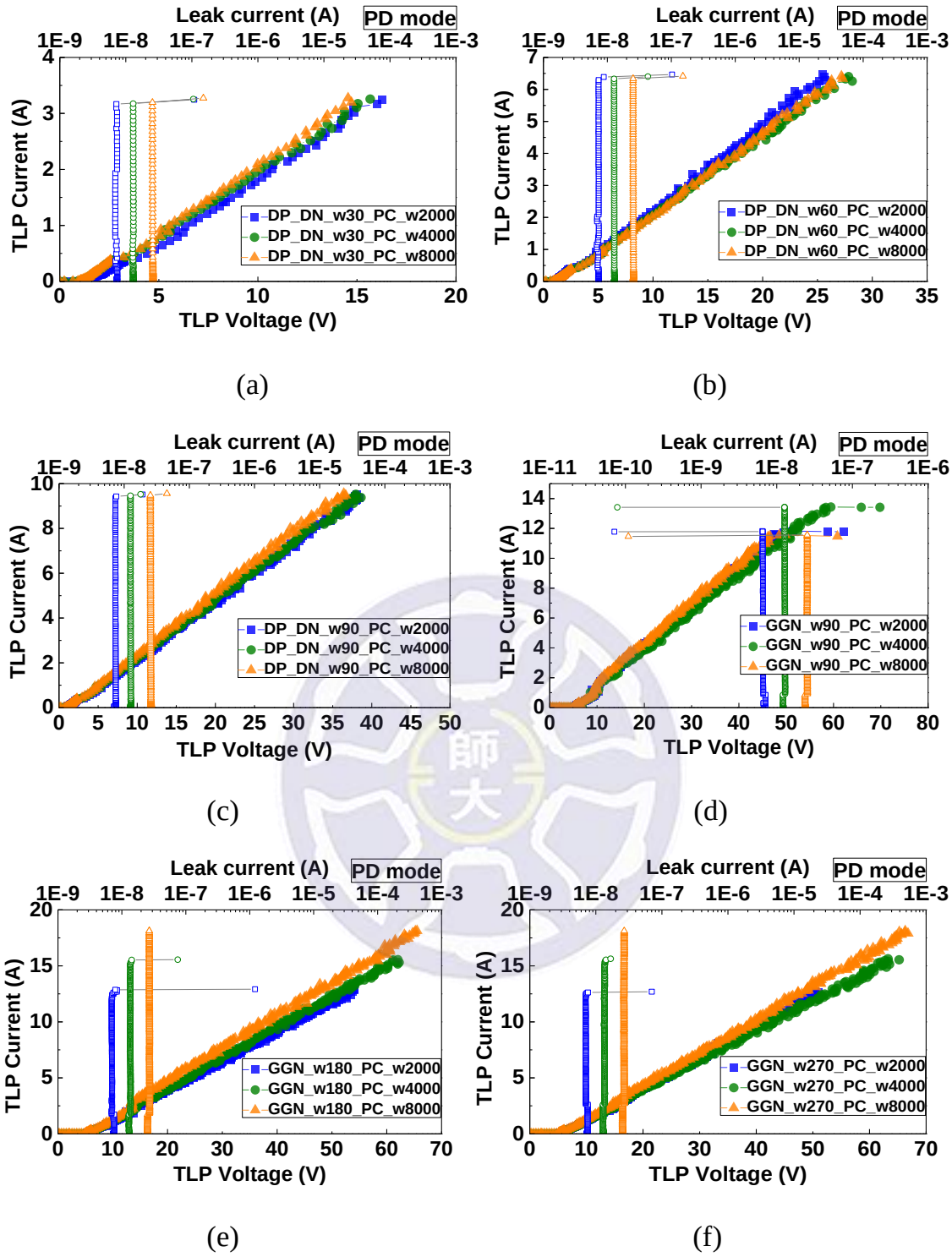


Fig. 2.17. Measured TLP-IV characteristics of (a) 30um diodes with power clamps under PD mode, (b) 60um diodes with power clamps under PD mode, (c) 90um diodes with power clamps under PD mode, (d) 90um GGNMOS with power clamps under PD mode, (e) 180um GGNMOS with power clamps under PD mode, and (f) 270um GGNMOS with power clamps under PD mode.

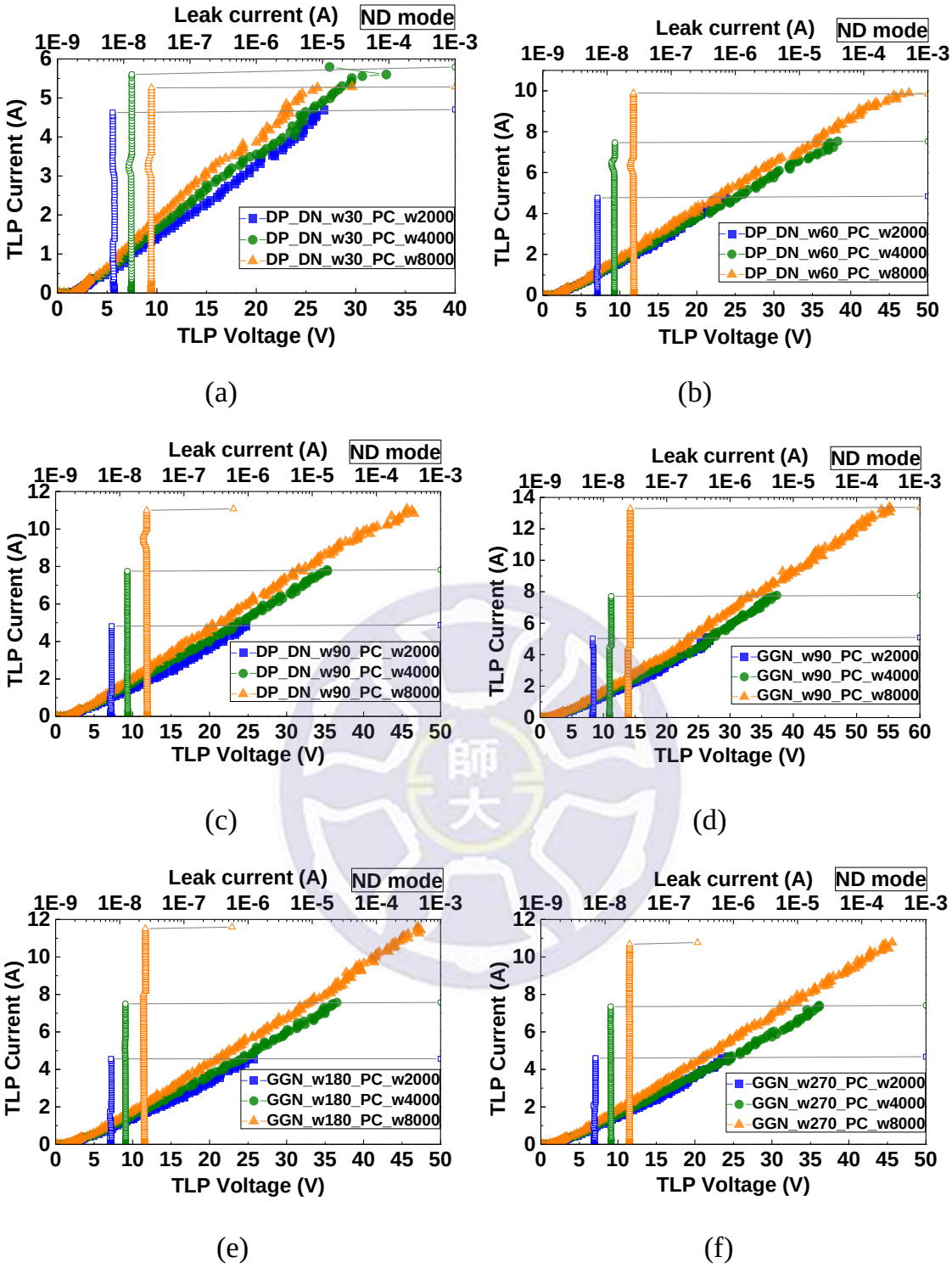


Fig. 2.18. Measured TLP-IV characteristics of (a) 30um diodes with power clamps under ND mode, (b) 60um diodes with power clamps under ND mode, (c) 90um diodes with power clamps under ND mode, (d) 90um GGNMOS with power clamps under ND mode, (e) 180um GGNMOS with power clamps under ND mode, and (f) 270um GGNMOS with power clamps under ND mode.

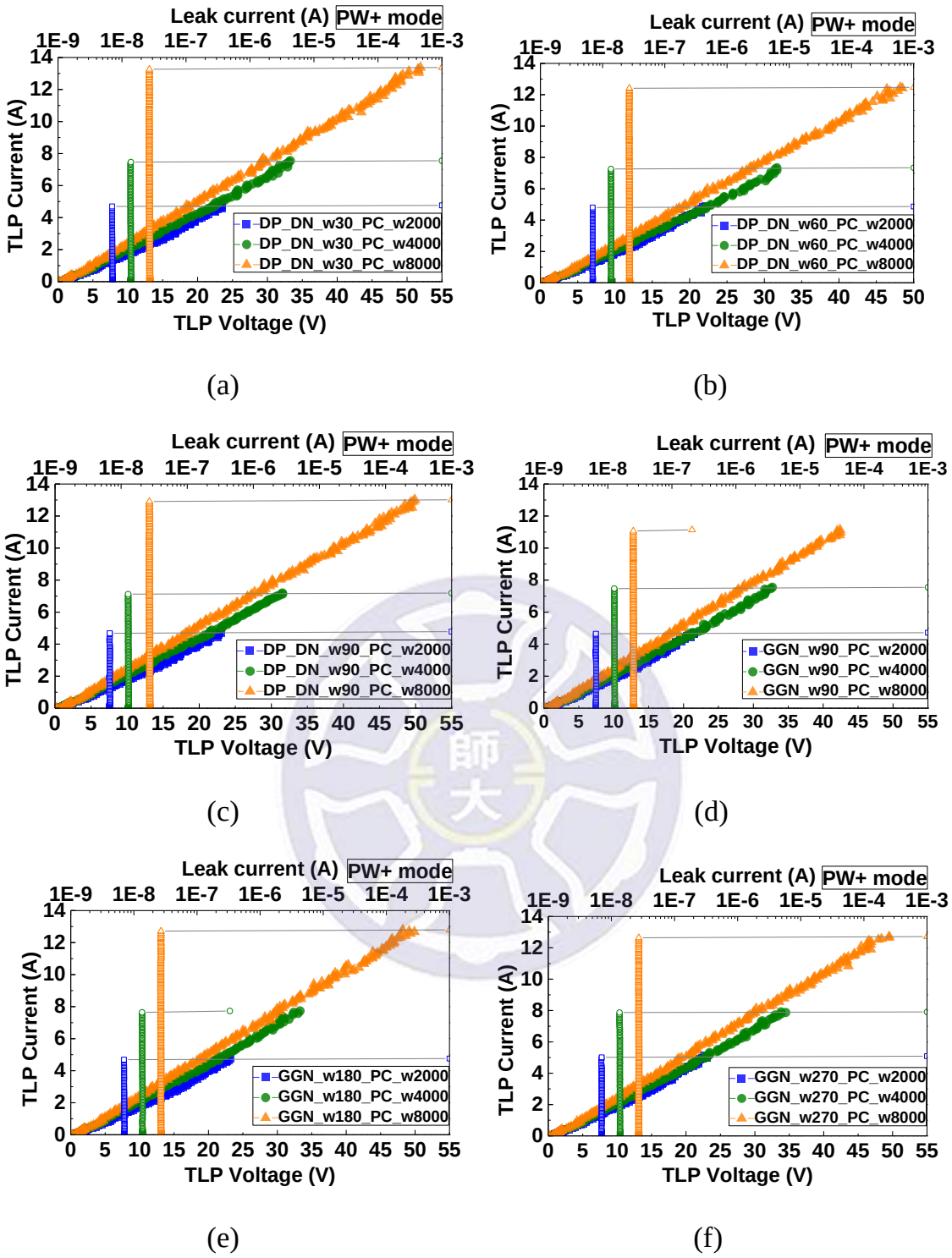


Fig. 2.19. Measured TLP-IV characteristics of (a) 30um diodes with power clamps under PW+ mode, (b) 60um diodes with power clamps under PW+ mode, (c) 90um diodes with power clamps under PW+ mode, (d) 90um GGNMOS with power clamps under PW+ mode, (e) 180um GGNMOS with power clamps under PW+ mode, and (f) 270um GGNMOS with power clamps under PW+ mode.

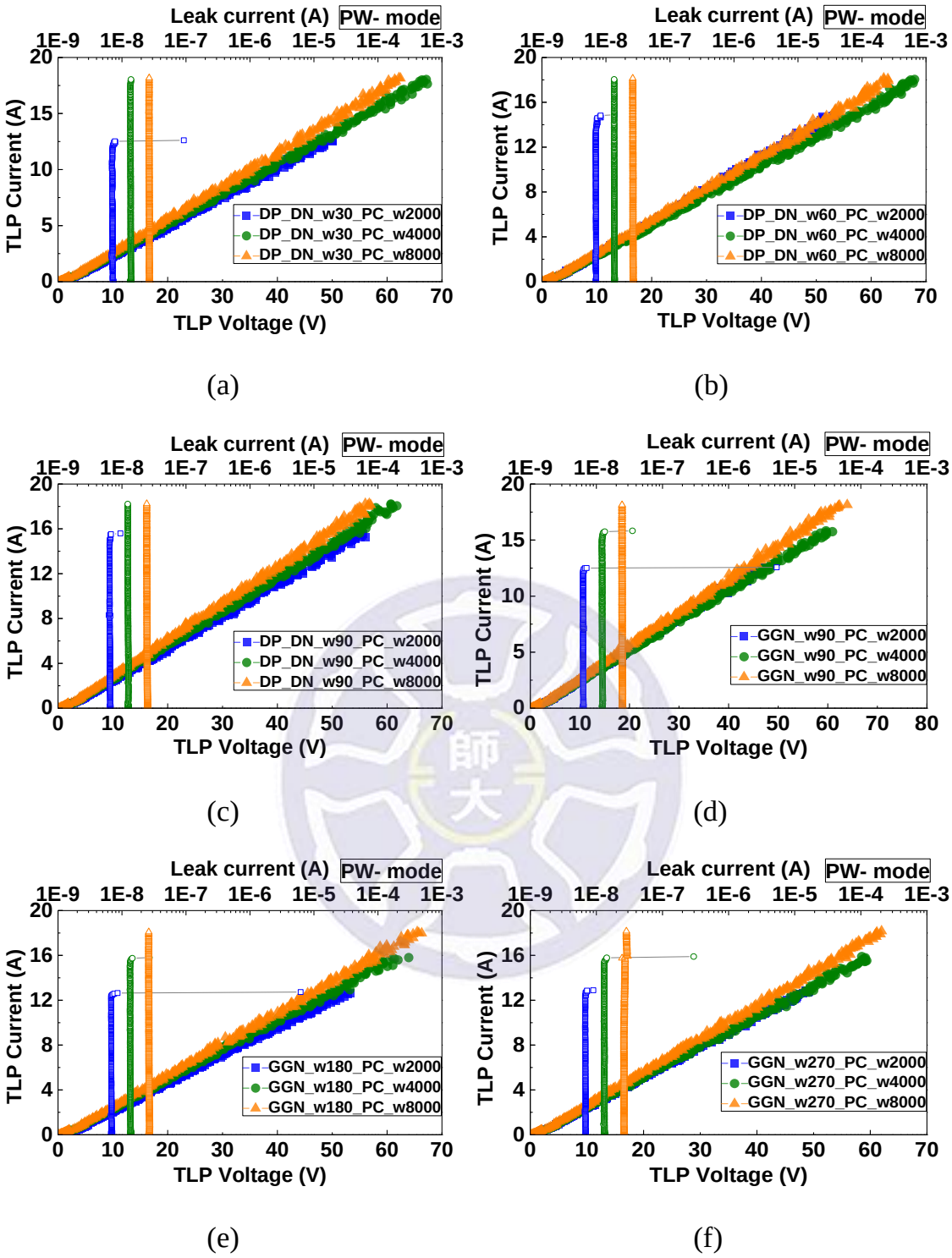


Fig. 2.20. Measured TLP-IV characteristics of (a) 30um diodes with power clamps under PW- mode, (b) 60um diodes with power clamps under PW- mode, (c) 90um diodes with power clamps under PW- mode, (d) 90um GGNMOS with power clamps under PW- mode, (e) 180um GGNMOS with power clamps under PW- mode, and (f) 270um GGNMOS with power clamps under PW- mode.

Table 2.10

TLP-measured characteristics of NBJT under PS and NS mode.

Test device	TLP							
	PS mode				NS mode			
	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
NBJT_60_R0	10.57	10.57	0.1	19.2	0.97	0.97	1.95	5.9
NBJT_60_R100k	4.94	4.12	0.56	10.4	2.80	2.80	0.37	9.0
NBJT_60_R500k	4.5	3.89	0.56	9.9	2.80	2.80	0.37	8.5
NBJT_180_R0	10.4	10.4	0.3	9.2	0.92	0.92	4.57	5.2
NBJT_180_R100k	3.84	3.45	1.66	7.4	2.65	2.65	1.14	6.2
NBJT_180_R500k	3.84	3.45	1.66	7.2	2.66	2.66	1.15	5.8
NBJT_360_R0	10.39	10.39	0.55	6.1	0.89	0.89	5.73	4.8
NBJT_360_R100k	3.40	3.31	3.20	5.9	2.6	2.6	2.3	5.2
NBJT_360_R500k	3.40	3.40	3.18	5.89	2.6	2.6	2.3	5.1

Table 2.11
TLP-measured characteristics of diodes with power clamps under PS and NS mode.

Test device	TLP							
	PS mode				NS mode			
	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
DP_DN_w30_PC_w2000	1.74	1.74	2.78	5.81	1.00	1.00	3.33	3.92
DP_DN_w30_PC_w4000	1.76	1.76	2.81	5.31	1.00	1.00	3.41	3.95
DP_DN_w30_PC_w8000	1.80	1.80	2.85	5.17	0.99	0.99	3.35	3.88
DP_DN_w60_PC_w2000	1.60	1.60	4.86	4.54	0.97	0.97	6.54	3.52
DP_DN_w60_PC_w4000	1.73	1.73	5.62	4.49	0.96	0.96	6.53	3.48
DP_DN_w60_PC_w8000	1.76	1.76	5.67	4.44	0.96	0.96	6.56	3.42
DP_DN_w90_PC_w2000	1.57	1.57	4.79	4.48	0.95	0.95	9.78	3.76
DP_DN_w90_PC_w4000	1.71	1.71	7.35	4.44	0.94	0.94	9.69	3.77
DP_DN_w90_PC_w8000	1.74	1.74	8.52	4.35	0.94	0.94	9.73	3.60

Table 2.12
TLP-measured characteristics of diodes with power clamps under PD and ND mode.

Test device	TLP							
	PD mode				ND mode			
	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
DP_DN_w30_PC_w2000	1.11	1.11	3.17	4.20	1.59	1.59	4.62	5.65
DP_DN_w30_PC_w4000	1.00	1.00	3.17	4.11	1.78	1.78	5.60	4.88
DP_DN_w30_PC_w8000	1.00	1.00	3.20	4.07	1.81	1.81	5.26	4.02
DP_DN_w60_PC_w2000	0.96	0.96	6.39	4.12	1.69	1.69	4.77	5.32
DP_DN_w60_PC_w4000	0.96	0.96	6.33	4.22	1.72	1.72	7.47	4.33
DP_DN_w60_PC_w8000	0.97	0.97	6.34	4.30	1.78	1.78	9.83	4.38
DP_DN_w90_PC_w2000	0.95	0.95	9.43	3.91	1.59	1.59	4.82	4.60
DP_DN_w90_PC_w4000	0.95	0.95	9.46	3.78	1.72	1.72	7.75	4.24
DP_DN_w90_PC_w8000	0.94	0.94	9.48	3.48	1.76	1.76	11.00	3.66

Table 2.13
TLP-measured characteristics of diodes with power clamps under PW+ and PW- mode.

Test device	TLP							
	PW+ mode				PW- mode			
	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
DP_DN_w30_PC_w2000	0.73	0.73	4.70	4.80	0.68	0.68	12.52	3.73
DP_DN_w30_PC_w4000	0.78	0.78	7.47	4.58	0.56	0.56	17.99	3.63
DP_DN_w30_PC_w8000	0.82	0.82	13.26	3.52	0.52	0.52	18.14	3.41
DP_DN_w60_PC_w2000	0.74	0.74	4.80	4.70	0.68	0.68	14.81	3.58
DP_DN_w60_PC_w4000	0.79	0.79	7.26	4.15	0.56	0.56	17.99	3.67
DP_DN_w60_PC_w8000	0.82	0.82	12.41	3.65	0.52	0.52	18.08	3.55
DP_DN_w90_PC_w2000	0.75	0.75	4.68	5.17	0.69	0.69	15.52	3.43
DP_DN_w90_PC_w4000	0.78	0.78	7.12	4.32	0.56	0.56	18.16	3.42
DP_DN_w90_PC_w8000	1.09	1.09	12.91	3.59	0.52	0.52	18.24	3.02

Table 2.14
TLP-measured characteristics of GGNMOS with power clamps under PS and NS mode.

Test device	TLP							
	PS mode				NS mode			
	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
GGN_w90_PC_w2000	5.97	4.48	0.83	4.54	0.86	0.86	4.51	3.87
GGN_w90_PC_w4000	5.95	4.49	0.83	4.75	0.86	0.86	4.49	3.96
GGN_w90_PC_w8000	5.86	4.47	0.84	4.45	0.86	0.86	4.50	3.86
GGN_w180_PC_w2000	5.93	4.49	1.76	3.92	0.76	0.76	8.19	4.03
GGN_w180_PC_w4000	5.94	4.50	1.75	3.98	0.76	0.76	8.11	4.09
GGN_w180_PC_w8000	5.93	4.48	1.69	3.77	0.76	0.76	8.14	3.72
GGN_w270_PC_w2000	5.91	4.47	2.58	3.56	0.70	0.70	11.57	3.67
GGN_w270_PC_w4000	5.90	4.54	2.50	3.68	0.70	0.70	11.61	3.78
GGN_w270_PC_w8000	5.91	4.52	2.55	3.57	0.70	0.70	11.60	3.34

Table 2.15
TLP-measured characteristics of GGNMOS with power clamps under PD and ND mode.

Test device	TLP							
	PD mode				ND mode			
	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
GGN_w90_PC_w2000	6.92	5.22	11.79	3.94	1.49	1.49	5.03	5.27
GGN_w90_PC_w4000	6.82	5.23	13.42	4.10	1.53	1.53	7.71	4.99
GGN_w90_PC_w8000	6.93	5.09	11.56	3.65	1.57	1.57	13.29	4.40
GGN_w180_PC_w2000	6.88	5.25	12.86	3.79	1.38	1.38	4.56	5.24
GGN_w180_PC_w4000	6.87	5.15	15.52	3.57	1.41	1.41	7.50	4.67
GGN_w180_PC_w8000	6.85	5.05	18.11	3.14	1.44	1.44	11.51	3.73
GGN_w270_PC_w2000	6.82	5.28	12.62	3.68	1.28	1.28	4.60	5.33
GGN_w270_PC_w4000	6.81	5.23	15.54	3.55	1.34	1.34	7.35	4.74
GGN_w270_PC_w8000	6.79	5.12	18.04	3.56	1.39	1.39	10.68	3.80

Table 2.16
TLP-measured characteristics of GGNMOS with power clamps under PW+ and PW- mode.

Test device	TLP							
	PW+ mode				PW- mode			
	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
GGN_w90_PC_w2000	0.74	0.74	4.65	4.84	0.68	0.68	12.50	3.72
GGN_w90_PC_w4000	0.79	0.79	7.47	4.30	0.56	0.56	15.75	3.66
GGN_w90_PC_w8000	0.83	0.83	11.07	3.85	0.52	0.52	18.10	3.09
GGN_w180_PC_w2000	0.73	0.73	4.69	4.60	0.73	0.73	12.64	4.03
GGN_w180_PC_w4000	0.78	0.78	7.64	4.06	0.56	0.56	15.75	3.69
GGN_w180_PC_w8000	0.82	0.82	12.72	3.78	0.52	0.52	18.00	3.46
GGN_w270_PC_w2000	0.73	0.73	5.01	4.68	0.68	0.68	12.86	3.74
GGN_w270_PC_w4000	0.78	0.78	7.87	4.00	0.56	0.56	15.79	3.43
GGN_w270_PC_w8000	0.82	0.82	12.64	3.82	0.52	0.52	18.06	3.41

2.3.2 Measured ESD Robustness

The human-body-model (HBM) ESD robustness of each circuit has been tested by the HBM tester. The failure criterion is defined as the I-V curves shown between the test pads shifting over 30% from its original curve after ESD stressed at every ESD test level. All these HBM test results are also listed in Table 2.17, Table 2.18, and Table 2.19.

The ESD robustness of human-body-mode in general commercial ICs must pass 2kV above. As shown in Table 2.17 and Table 2.18, basically, ESD robustness of the diodes with power clamp and GGNMOS with power clamp almost pass the 2kV above, except test devices of GGN_W90_PC_W2000, GGN_W90_PC_W4000, and GGN_W90_PC_W8000 in PS and PD mode ESD stress under normal operating voltage of 1.8V.

The test devices could not reach 2kV that the possible reasons divided into two types. First, dimension is not enough for GGNMOS. Second, GGNMOS has a non-uniformity turn-on phenomenon. If these problems solved, HBM ESD robustness of test devices will pass 2kV.

In Table 2.19, the ESD robustness of some NBJT could not reach 2kV. If the higher ESD robustness is required, the designer can increase the size of NBJT.

Table 2.17

Measured HBM ESD robustness of diodes with power clamps.

Test device	PS mode (kV)	NS mode (kV)	PD mode (kV)	ND mode (kV)	PW+ mode (kV)	PW- mode (kV)
DP_DN_w30_PC_w2000	6.75	6.25	6	6.25	>8	>8
DP_DN_w30_PC_w4000	6.75	6.25	6.25	6.25	>8	>8
DP_DN_w30_PC_w8000	7	6.25	6	6.25	>8	>8
DP_DN_w60_PC_w2000	>8	>8	>8	>8	>8	>8
DP_DN_w60_PC_w4000	>8	>8	>8	>8	>8	>8
DP_DN_w60_PC_w8000	>8	>8	>8	>8	>8	>8
DP_DN_w90_PC_w2000	>8	>8	>8	>8	>8	>8
DP_DN_w90_PC_w4000	>8	>8	>8	>8	>8	>8
DP_DN_w90_PC_w8000	>8	>8	>8	>8	>8	>8

Table 2.18

Measured HBM ESD robustness of GGNMOS with power clamps.

Test device	PS mode (kV)	NS mode (kV)	PD mode (kV)	ND mode (kV)	PW+ mode (kV)	PW- mode (kV)
GGN_w90_PC_w2000	1.5	5	1.5	5	>8	>8
GGN_w90_PC_w4000	1.5	5	1.25	5	>8	>8
GGN_w90_PC_w8000	1.5	5	1.25	5	>8	>8
GGN_w180_PC_w2000	3	>8	3	>8	>8	>8
GGN_w180_PC_w4000	3	>8	3	>8	>8	>8
GGN_w180_PC_w8000	3.25	>8	3	>8	>8	>8
GGN_w270_PC_w2000	4.5	>8	4.25	>8	>8	>8
GGN_w270_PC_w4000	4.5	>8	4.5	>8	>8	>8
GGN_w270_PC_w8000	4.5	>8	4.5	>8	>8	>8

Table 2.19

Measured HBM ESD robustness of NBJT.

Test device	HBM level	
	PS mode (kV)	NS mode (kV)
NBJT_60_R0	0.15	4
NBJT_60_R100k	1.15	0.65
NBJT_60_R500k	1.15	0.7
NBJT_180_R0	0.5	8
NBJT_180_R100k	3.5	1.9
NBJT_180_R500k	3.5	2.1
NBJT_360_R0	0.8	8
NBJT_360_R100k	6.6	4
NBJT_360_R500k	6.6	3.8

2.3.3 Comparison and Discussion

The comparison among various diodes with power clamp, NBJT, and GGNMOS with power clamp for BiCMOS on-chip ESD protection have been summarized in Table 2.20, Table 2.21, and Table 2.22, respectively. In Table 2.20, HBM ESD robustness of diodes with power clamp is higher than prior HBM ESD robustness of diodes with power clamp.

In Table 2.21, the trigger voltage (V_{t1}) and the holding voltage (V_h) of NBJT are lower than the prior Zener-triggered NBJT, except the NBJT_60_R0, NBJT_180_R0, and NBJT_360_R0. The thermal breakdown current (I_{t2}), and the ESD discharging resistance (R_{on}) have been compared. If the higher I_{t2} of

NBJT is required, the designer can increase the size of NBJT. R_{on} of NBJT is higher than the prior Zener-triggered NPN. The R_{ON} of NBJT must be finely designed to less and effectively discharging path.

In Table 2.22, the V_{t1}, V_h, I_{t2}, and R_{on} of GGNMOS have been compared. The V_{t1} of GGNMOS has lower than V_{t1} of the prior GGNMOS. Comparing with the prior GGNMOS, the V_h have almost the same. The designer can increase the size of GGNMOS to improve the I_{t2} of GGNMOS. The prior GGNMOS have lower R_{on}, except 120um GGNMOS in 90nm CMOS process.

Table 2.20

Comparison among the prior devices and diodes with power clamp.

Test device		Technology	Diodes width (um)	Power clamp width (um)	HBM ESD robustness					
					PS (kV)	NS (kV)	PD (kV)	ND (kV)	PW+ (kV)	PW- (kV)
Reference [49]	Dual diodes	65nm CMOS	40	N/A	2	2	2	2	N/A	N/A
DP_DN_w30_PC_w2000		0.18um BiCMOS	30	2000	6.75	6.25	6	6.25	>8	>8
DP_DN_w30_PC_w4000				4000	6.75	6.25	6.25	6.25	>8	>8
DP_DN_w30_PC_w8000				8000	7	6.25	6	6.25	>8	>8
DP_DN_w60_PC_w2000			60	2000	>8	>8	>8	>8	>8	>8
DP_DN_w60_PC_w4000				4000	>8	>8	>8	>8	>8	>8
DP_DN_w60_PC_w8000				8000	>8	>8	>8	>8	>8	>8
DP_DN_w90_PC_w2000			90	2000	>8	>8	>8	>8	>8	>8
DP_DN_w90_PC_w4000				4000	>8	>8	>8	>8	>8	>8
DP_DN_w90_PC_w8000				8000	>8	>8	>8	>8	>8	>8

Table 2.21

Comparison among the prior devices and NBJT.

Test device		Technology	Length (um)	R_{be} (kΩ)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
Reference [50]	Zener-triggered NPN with resistance	BiCMOS	500	1	9.6	9.4	1.6	3.3
	Zener-triggered NPN with resistance			infinity	8.5	7.9	1.8	3.5
PS mode	NBJT_60_R0	0.18um BiCMOS	60	0	10.57	10.57	0.1	19.2
	NBJT_60_R100k			100	4.94	4.12	0.56	10.4
	NBJT_60_R500k			500	4.5	3.89	0.56	9.9
	NBJT_180_R0		180	0	10.4	10.4	0.3	9.2
	NBJT_180_R100k			100	3.84	3.45	1.66	7.4
	NBJT_180_R500k			500	3.84	3.45	1.66	7.2
	NBJT_360_R0		360	0	10.39	10.39	0.55	6.1
	NBJT_360_R100k			100	3.40	3.31	3.20	5.9
	NBJT_360_R500k			500	3.40	3.40	3.18	5.89

Table 2.22

Comparison among the prior devices and GGNMOS with power clamps.

Test device		Technology	GGNMOS width (um)	Power clamp width (um)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
Reference [41]	GGNMOS	90nm CMOS	120	N/A	6.71	4.71	0.67	3.8
			240		6.59	4.52	1.1	1.8
		40nm CMOS	60		6.73	4.92	0.43	N/A
			240		6.31	4.49	1.77	N/A
			360		6.19	4.2	2.65	N/A
Reference [43]	Novel GGNMOS	0.13um CMOS	160		6.1	4.6	1.1	2.8
			240		6.2	4.6	1.1	2.7
			320		6.4	4.5	1.7	1.8
			480		6.5	4.5	1.8	1.3
PS mode	GGN_w90_ PC_w2000	0.18um BiCMOS	90	2000	5.97	4.48	0.83	4.54
	GGN_w90_ PC_w4000			4000	5.95	4.49	0.83	4.75
	GGN_w90_ PC_w8000			8000	5.86	4.47	0.84	4.45
	GGN_w180_ PC_w2000		180	2000	5.93	4.49	1.76	3.92
	GGN_w180_ PC_w4000			4000	5.94	4.50	1.75	3.98
	GGN_w180_ PC_w8000			8000	5.93	4.48	1.69	3.77
	GGN_w270_ PC_w2000		270	2000	5.91	4.47	2.58	3.56
	GGN_w270_ PC_w4000			4000	5.90	4.54	2.50	3.68
	GGN_w270_ PC_w8000			8000	5.91	4.52	2.55	3.57

2.4 Experimental Results under System-Level ESD Test

According to the standard of IEC 61000-4-2, the ESD gun is used to evaluate the system-level ESD robustness. Each on-chip ESD protection device has been tested under system-level ESD test. The failure criterion is defined as leakage current shown between the test pads shifting over 30% from its original leakage current. The system-level ESD robustness of diodes with power clamp and GGNMOS with power clamp are shown in Table 2.23 and Table 2.24.

Table 2.23

System-level ESD robustness of diodes with power clamp.

Test device	PS mode (kV)	NS mode (kV)	PD mode (kV)	ND mode (kV)	PW+ mode (kV)	PW- mode (kV)
DP_DN_w30_PC_w2000	1.5	1.5	1.5	1.5	2.2	6.5
DP_DN_w30_PC_w4000	1.5	1.5	1.5	1.5	4	9
DP_DN_w30_PC_w8000	1.5	1.5	1.5	1.5	4.2	8
DP_DN_w60_PC_w2000	2.5	3.5	3.5	2	2.4	8
DP_DN_w60_PC_w4000	3.5	3.5	3.5	3.5	4	9
DP_DN_w60_PC_w8000	3.5	3.5	3.5	3.5	4.4	8
DP_DN_w90_PC_w2000	2	5.5	5	2.5	2.4	8.5
DP_DN_w90_PC_w4000	3.5	5.5	5	4.5	4	10
DP_DN_w90_PC_w8000	4.5	5.5	5	5	5.2	9.5

Table 2.24

System-level ESD robustness of GGNMOS with power clamp.

Test device	PS mode (kV)	NS mode (kV)	PD mode (kV)	ND mode (kV)	PW+ mode (kV)	PW- mode (kV)
GGN_w90_PC_w2000	0.4	1.5	0.4	1	2	3.5
GGN_w90_PC_w4000	0.4	1.5	0.4	1.5	2.4	3
GGN_w90_PC_w8000	0.4	1	0.4	1	2	2.5
GGN_w180_PC_2000	0.9	2.5	0.9	2	2.2	5
GGN_w180_PC_w4000	0.9	2.5	0.9	2.5	2.4	3
GGN_w180_PC_w8000	0.9	2.5	0.9	2.5	2.4	2.5
GGN_w270_PC_w2000	1.3	3.5	1.4	2	2.2	4
GGN_w270_PC_w4000	1.3	4	1.4	2.5	2.8	3
GGN_w270_PC_w8000	1.3	3.5	1.4	2.5	3	2.5

The system-efficient ESD design (SEED) is a co-design methodology of on-board and on-chip ESD protection that system-level ESD robustness can be achieved and analyzed. SEED is also an optimized IEC protection co-design for external pins. This design methodology needs thorough understanding of the interactions between external ESD pulses, device pin characteristics and system level board design during an ESD stress event [51].

A two-stage system-level ESD protection scheme–fundamental SEED concept is shown in Fig. 2.21 [51]. It consists of the primary clamp, the secondary clamp, and the isolation impedance. This protection circuit can reduce the current flowing into the IC, and then the system level ESD robustness is improved. On-board protection or off-chip ESD protection (primary clamp), which means most of the ESD current can be discharged to the ground and prevent from flowing into the IC. The primary clamp protection circuitry might include clamping components such as polymers, varistors, transient voltage suppression (TVS) diodes, and so on. Next, on-chip ESD protection (secondary clamp) of an IC pin in the system, which means the residual pulse current can flow from the secondary clamp to the ground. Finally, isolation impedance also helps to prevent ESD flowing into the IC [51].

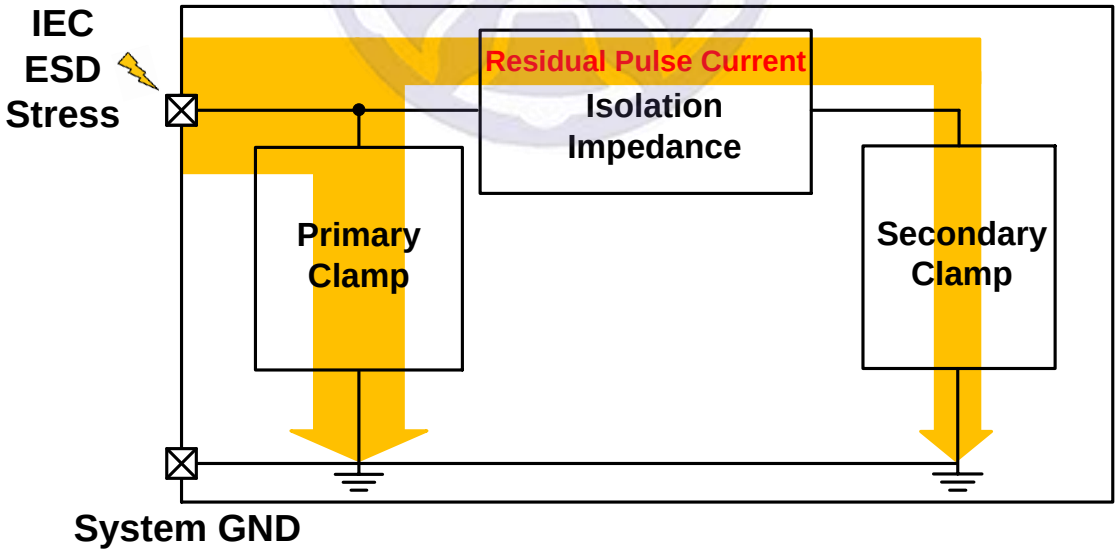


Fig. 2.21. Two-stage system-level ESD protection – fundamental SEED concept.

As shown in Fig. 2.22, the transient voltage suppression (TVS), the isolation impedance (R_{ESD}), and the NBJT are used as two-stage system-level ESD protection device.

The transient voltage suppressor (TVS) is used as primary clamp under system-level ESD test, which has the advantages of low capacitance, low leakage current, and low clamping voltage [52]-[53]. With the primary clamp of TVS, most of the ESD current can be discharged to the ground and prevent from flowing into the IC.

The isolation resistance (R_{ESD}) is used as the isolation impedance. R_{ESD} also helps to prevent ESD current flowing into the IC. TVS can discharge the main ESD current to the ground. R_{ESD} of 0Ω, 30Ω, 45Ω, 60Ω, and 100 Ω are used for the system-level ESD test.

The NPN BJT (NBJT) with on-chip resistance (R_{be}) is used as secondary clamp. The residual pulse current can flow from the secondary clamp to the ground.

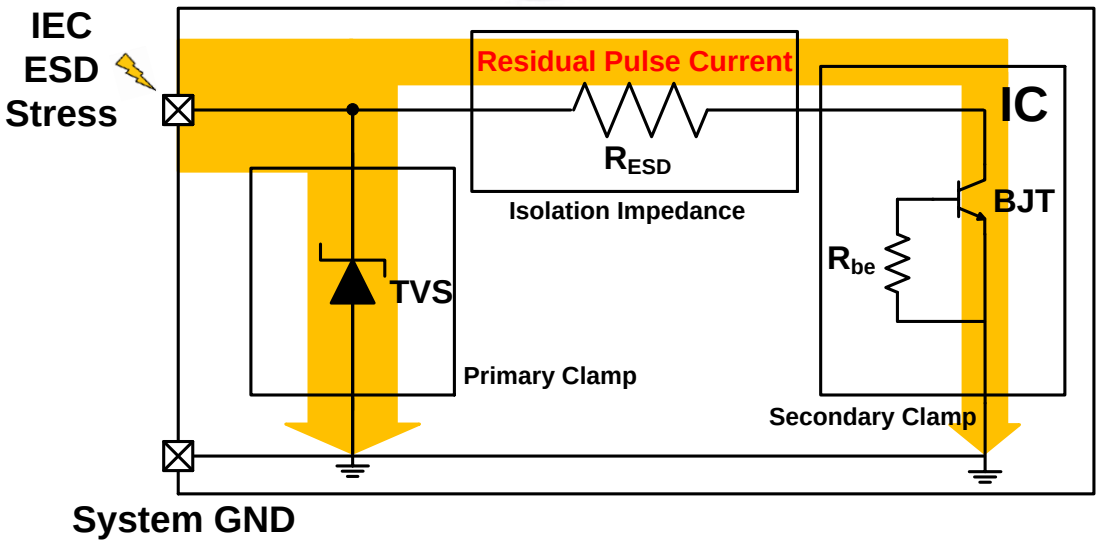


Fig. 2.22. Two-stage system-level ESD protection by TVS, R_{ESD}, and NBJT.

Table 2.25

System-level ESD robustness of NPN BJT (NBJT).

Test device	NBJT length (um)	R_{be} (kΩ)	System-level ESD robustness (kV)				
			with 0Ω R_{ESD}	with 30Ω R_{ESD}	with 45Ω R_{ESD}	with 60Ω R_{ESD}	with 100Ω R_{ESD}
NBJT_60_R0	60	0	<0.2	<0.2	<0.2	<0.2	0.2
NBJT_60_R100k		100	0.5	1.5	1.5	2	2
NBJT_60_R500k		500	0.75	1.5	1.5	1.8	1.5
NBJT_180_R0	180	0	0.2	0.2	0.2	0.8	1
NBJT_180_R100k		100	2	3	4	4	2
NBJT_180_R500k		500	1.2	3.5	3.5	4.5	2.6
NBJT_360_R0	360	0	0.5	0.2	1	1.5	1.3
NBJT_360_R100k		100	3.5	5.5	7	3.5	4
NBJT_360_R500k		500	1.5	7	4.5	3	3

According to the standard of IEC 61000-4-2, the ESD gun is used to evaluate the system-level ESD robustness. Each on-chip ESD protection device has been tested by SEED co-design methodology under system-level ESD test. The failure criterion is defined as leakage current shown between the test pads shifting over 30% from its original leakage current.

Table 2.25 shows the system-level ESD robustness of NBJT. With the help of TVS and R_{ESD}, the system-level ESD robustness of the NBJT_60_R0 can reach 0.2kV. The NBJT_60_R100k can be improved to have 2kV system-level ESD robustness. The NBJT_60_R500k can be improved to have 1.8kV system-level ESD robustness. The NBJT_180_R0 can be improved from 0.2kV to 1kV. The NBJT_180_R100k can be improved to have 4kV system-level ESD robustness. The NBJT_180_R500k can be improved to have 4.5kV system-level ESD robustness. The NBJT_360_R0 can be improved from 0.5kV to 1.5kV. The NBJT_360_R100k can be improved from 3.5kV to 7kV. The NBJT_360_R500k can also be improved from 1.5kV to 4.5kV system-level ESD robustness. The two-stage system-level ESD protection is analyzed. Different R_{ESD} can affect the system-level ESD robustness. These experimental results can provide the design guideline for ESD protection in BiCMOS technology.

2.4.1 Failure Analysis

The failure analysis (FA) has been finished to seek the failure location after the power clamp test system-level ESD. The FA pictures of the 4000um power clamp and the 8000um power clamp shown in Fig. 2.23-Fig. 2.24. After system-level ESD, the damaged regions are all located on the metal of ESD clamp NMOS. Therefore, the metal lines can be increased to improve the ESD protection ability of power clamps.

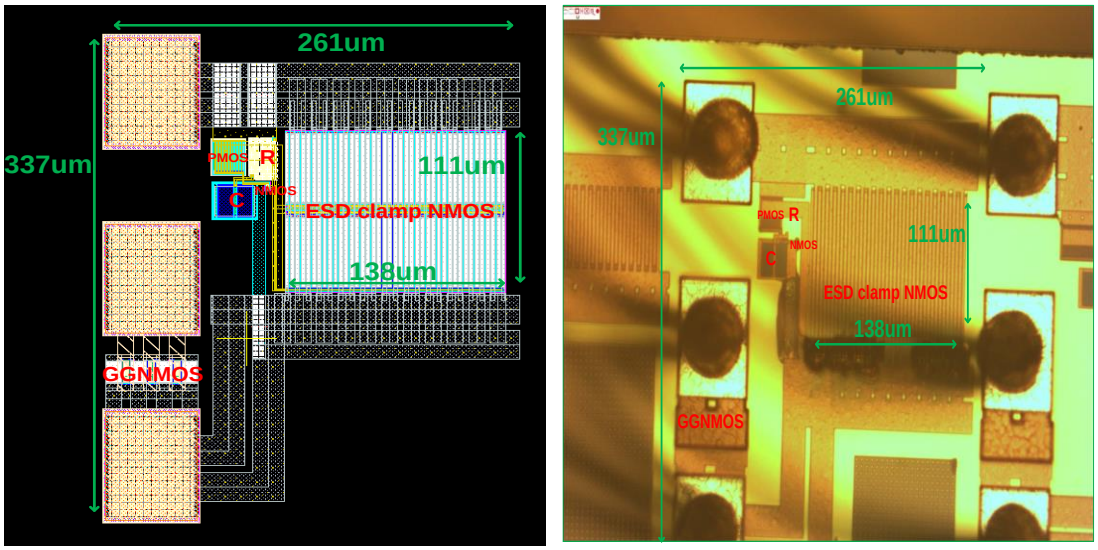


Fig. 2.23. The layout and OM picture of the 4000um power clamp after +2.4kV system-level ESD under PW+ mode.

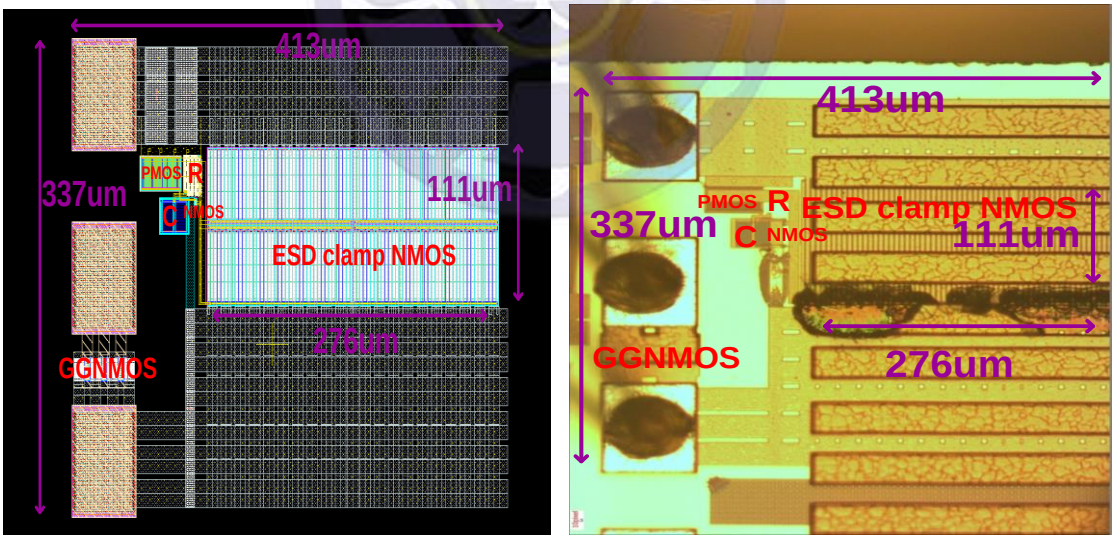


Fig. 2.24. The layout and OM picture of the 8000um power clamp after +2.4kV system-level ESD under PW+ mode.

2.5 Summary on On-Chip ESD Protection Circuits in BiCMOS Process

To protect the internal circuits for the component-level and system-level ESD, the ESD protection circuits of NBJT, diodes with power clamp, GGNMOS with power clamp was presented in this work. The component-level ESD robustness of the NBJT, diodes with power clamp, GGNMOS with power clamp are on-chip conducted. Verified in silicon chip, experimental results show that component-level ESD of NBJT with R_{be}, diodes with power clamp, GGNMOS with power clamp has the advantages of higher ESD robustness and lower trigger voltage. Analyze the two-stage system-level ESD protection characteristic. Different R_{ESD} of the NBJT can affect the system-level ESD robustness. These experimental results provide the design guideline for ESD protection in BiCMOS technology.

Chapter 3

Design of Improved Diode String with Embedded SCR in CMOS Process

Diode is widely used for on-chip electrostatic discharge (ESD) protection applications. Diode string has been utilized for on-chip protection against the electrostatic discharge (ESD) [54]. For example, the diode string can be used as the local ESD clamp for high-speed I/O. Besides, as the operation voltage reduced to ~1V, the diode string is possible to be used as the efficient power-rail ESD clamp. However, the traditional diode string (TDS) realized by the diodes of P+ with N-well (P+/NW) has some drawbacks, such as the high turn-on resistance, high clamping voltage, and large leakage current. Therefore, some modified designs on the diode string have been reported [55]-[63]. The diode string realized by the distributed ESD diodes is reported in [55] to enhance the ESD robustness. The diode string to reduce its clamping voltage is reported in [56] for RF circuits. The diode strings with reduced leakage currents are reported in [57]-[62]. Recently, the diode string realized by the diodes of P– with N+ (P–/N+) is reported in [63] to have the low leakage current and small layout area. However, its clamping voltage can be further improved. The traditional diode string (TDS) schematic circuit diagram is shown in Fig. 3.1. The cross-sectional view of traditional diode string (TDS) is shown in Fig. 3.2.

To reduce the clamping voltage of diode string, the design of the traditional and improved diode strings will be presented. In this paper, the diode string-based ESD protection design in a 0.18μm CMOS technology is studied.

Fig. 3.1. Schematic circuit diagram of traditional diode string (TDS).

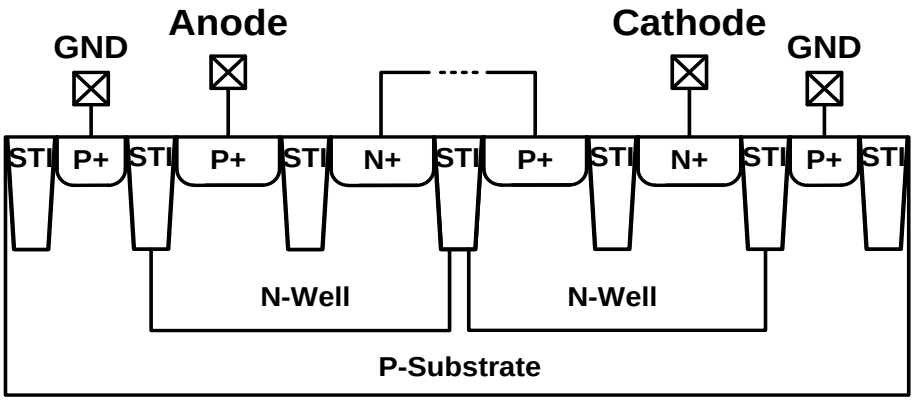


Fig. 3.2. Cross-sectional view of TDS.

3.1 ESD Protection Design by Using Improved Diode String

The improved diode string (IDS) utilizes P–/N+ diodes. Fig. 3.3 is the device cross-sectional view of improved diode string (IDS) in the standard CMOS technology. The P-type ESD implantation (P– implantation) under the N+ is used to reduce the junction breakdown voltage, and for earlier activation of the parasitic diode for ESD protection. The P– implantation is a standard step in CMOS process to enhance the ESD robustness of protection device [64]. The silicide block [65] is added on the surface between P+ and N+ (undoped region). Using more diodes can raise the blocking voltage of the IDS, but it also increases the overall clamping voltage and turn-on resistance during ESD stress, so it is adverse to ESD protection.

Design parameters of IDS display in Table 3.1. The IDS dimension of 20um, 60um, and 100um with diode counts of 2, 4, and 6 diodes, respectively, and those are used to compare with novel design devices.

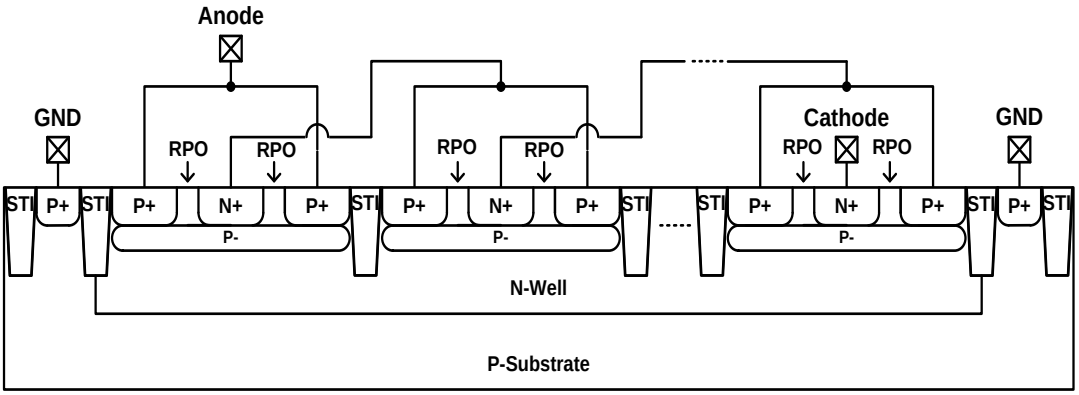


Fig. 3.3. Cross-sectional view of improved diode string (IDS).

Table 3.1

Test device of IDS.

Test device	Width (um)	Diode counts
IDS_w20_d2	20	2
IDS_w20_d4		4
IDS_w20_d6		6
IDS_w60_d2	60	2
IDS_w60_d4		4
IDS_w60_d6		6
IDS_w100_d2	100	2
IDS_w100_d4		4
IDS_w100_d6		6

3.2 ESD Protection Design by Using Diode String with Embedded SCR

The silicon-controlled rectifier (SCR) device is widely used for on-chip electrostatic discharge (ESD) protection applications. The SCR device has advantages of highly conductive and small layout area. However, the SCR device has a drawback of high trigger voltage. An efficient design is required to reduce the trigger voltage of the SCR device. The conventional SCR device consists of a P+, N-Well, P-Well, and N+, as shown in Fig. 3.4. The equivalent circuit of the SCR consists of a PNP BJT (Q_{PNP}) and an NPN BJT (Q_{NPN}), as shown in Fig. 3.5. When ESD happened, the positive-feedback regenerative mechanism of Q_{PNP} and Q_{NPN} results in the SCR device being highly conductive, therefore making SCR have higher against ESD stresses.

The proposed diode string with embedded SCR utilizes P+/NW and P–/N+ diodes. Fig. 3.6 is the device cross-sectional view diode string with embedded silicon-controlled rectifier (DSESCR). One P+/NW diode and one P–/N+ diode are merged together to form a silicon-controlled rectifier (SCR) path, that is P+/NW/P–/N+. The SCR device with low turn-on resistance, low clamping voltage, and high ESD robustness has been reported to be useful for ESD protection [66]. As utilizing the advantages of SCR, the DSESCR is expected to have reduced clamping voltage. As ESD stress, the diode path will quickly turn on to discharge the early part of current, and then the SCR path will turn on to discharge the primary part of current. The diode path also acts the trigger circuit of SCR device [67], because the current drawn from N-Well (injected into P–) of diode can also trigger the SCR. Since the primary part of ESD current will be released through the SCR path in this design, the clamping voltage of the DSESCR can be lowered. Besides, by butting the P+/NW and P–/N+ diodes, the

N+ and P+ can be directly connected by the silicide. The metal routing in the DSESCR can be simplified.

The equivalent circuit of the DSESCR is shown in Fig. 3.7. Fig. 3.8 is the device overhead view of novel diode string with embedded SCR which means DSESCR. The width of DSESCR can be modulated. Besides, each device layout space is the minimum value. Design parameters of DSESCR are shown in Table 3.2.

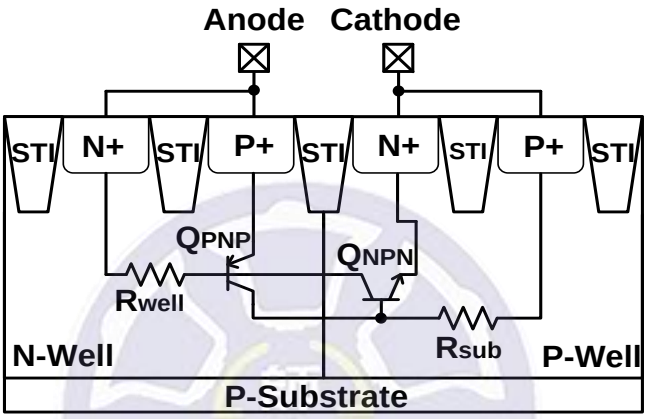


Fig. 3.4. Cross-sectional view of SCR.

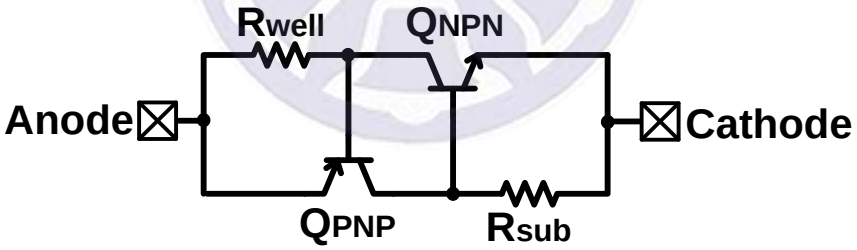


Fig. 3.5. Equivalent circuit of SCR.

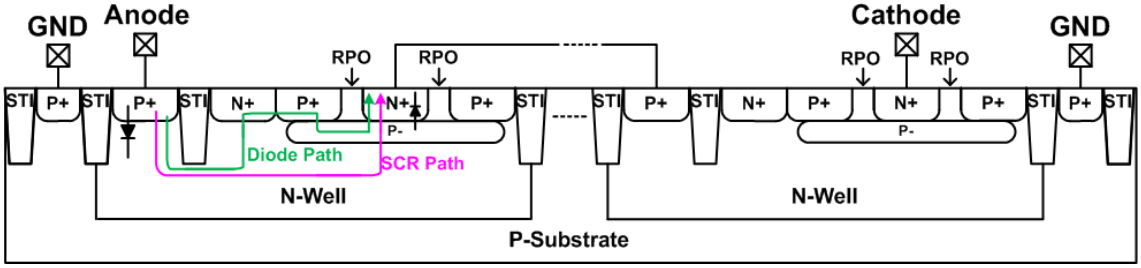


Fig. 3.6. Cross-sectional view of diode string with embedded silicon-controlled rectifier (DSESCR).

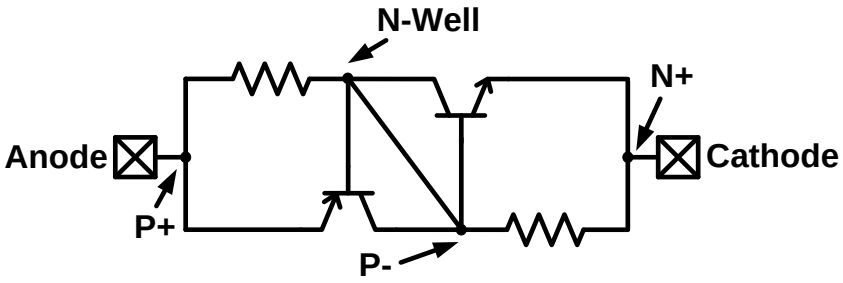


Fig. 3.7. Equivalent circuit of DSESCR.

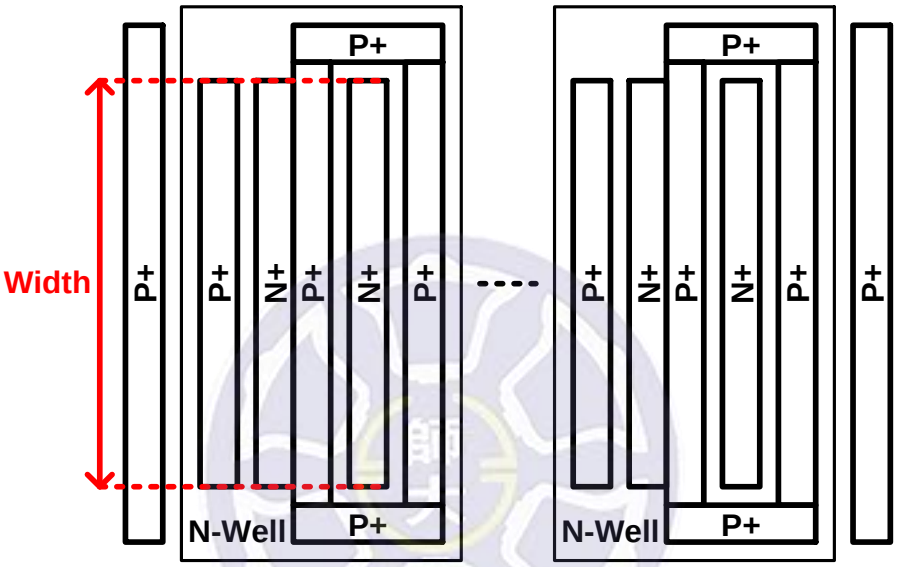


Fig. 3.8. Overhead view of DSESCR.

Table 3.2

Test device of DSESCR.

Test device	Width (um)	Diode counts
DSESCR_w20_d2	20	2
DSESCR_w20_d4		4
DSESCR_w20_d6		6
DSESCR_w60_d2	60	2
DSESCR_w60_d4		4
DSESCR_w60_d6		6
DSESCR_w100_d2	100	2
DSESCR_w100_d4		4
DSESCR_w100_d6		6

3.3 Measured Leakage Currents

To observe the leakage currents and the trigger phenomenon, the measured leakage currents of IDS and DSESCR are shown in Fig. 3.9. The leakage current was sweep from 0V to 4V operating voltage. Table 3.3 shows comparison of IDS and DSESCR leakage currents. The leakage current and layout area of the DSESCR can lower than the IDS. The design of the DSESCR has small layout area and leakage current.

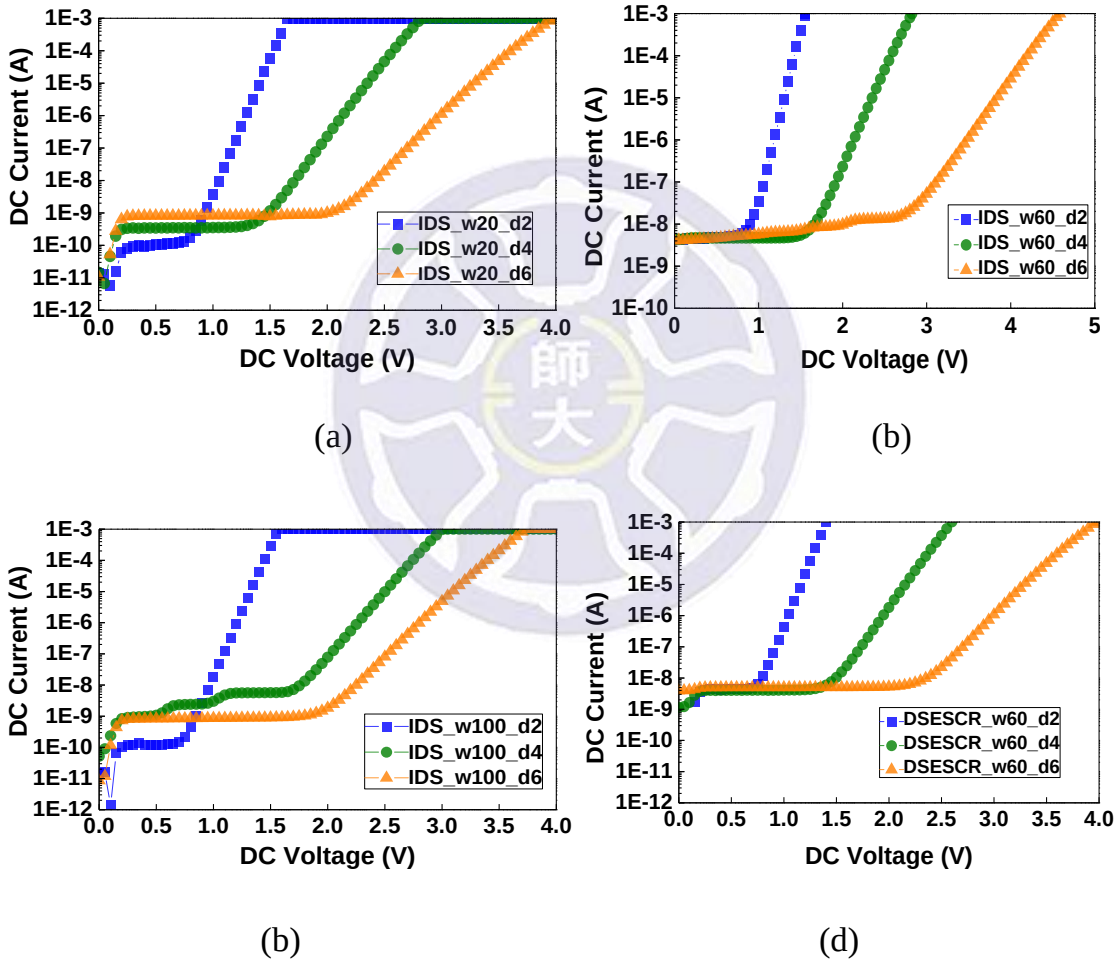


Fig. 3.9. Measured leakage currents of (a) 20um IDS with diode counts of 2, 4, and 6 diodes, (b) 60um IDS with diode counts of 2, 4, and 6 diodes, (c) 100um IDS with diode counts of 2, 4, and 6 diodes, (d) 60um DSESCR with diode counts of 2, 4, and 6 diodes.

Table 3.3
Comparison of IDS and DSESCR leakage current.

Test device	Width (um)	Diode counts	Layout area (um^2)	Leakage current (nA)
IDS	60	2	903	4.9 (at 0.6V)
		4	1809	4.7 (at 1.2V)
		6	2716	8.5 (at 1.8V)
DSESCR	60	2	563	4.4 (at 0.6V)
		4	1139	4.2 (at 1.2V)
		6	1715	5.1 (at 1.8V)

3.4 Experimental Results under Component-Level ESD Test

3.4.1 Measured TLP I-V Curves

The transmission-line-pulsing (TLP) system with 10-ns rise time and 100-ns pulse width is used to understand the turn-on behavior and the I-V characteristics in high-current regions of the ESD protection devices.

Each on-chip ESD protection device has been tested by TLP tester. The failure criterion is defined as leakage current shown between the test pads shifting over 30% from its original leakage current. In Fig. 3.13, the TLP-IV characteristics are measured.

The TLP I-V characteristics of IDS and DSESCR are shown in Fig. 3.13. In Fig. 3.13 (a)-Fig. 3.13 (c), TLP-IV characteristics of IDS are measured from anode to cathode under ESD stress. In Fig. 3.13 (d)-Fig. 3.13 (f), TLP-IV characteristics of DSESCR is measured from anode to cathode under ESD stress. The V_{t1} is defined voltage value of current 30mA.

Different diode counts can result in different trigger voltage. The V_h is equal to V_{t1}. The addition of dimension will cause lower R_{on} and higher $I_{t2.}$ Comparing with IDS, the DSESCR has the lower R_{on}. The R_{on} of DSESCR have some

smaller than IDS. The DSESCR dimension of 100 has higher I_{t2}. TLP-IV characteristics of all test circuits are measured from anode to cathode under ESD stress. All these TLP measurement results are also listed in Table 3.5.

Some leakage currents are higher and others are lower after TLP-IV characteristics are measured in DSESCR. The junction of the DSESCR was burn to short, so the leakage currents are higher. The metal of the DSESCR was burn to open, so the leakage currents are lower. The pulsed voltage injected into the DSESCR from anode to cathode. The formula is $P=V^2/R$. If R is smaller, the P will be bigger that metal is possibly burned to open. The parasitic resistance of metal (Rm) will become small due to the Rm is covered with via, as shown in Fig. 3.11 and Fig. 3.12. If the distance of anode and cathode to guard ring is longer, the parasitic resistance of metal (R1, R2, and R3) will increase, as shown in Fig. 3.10, Fig. 3.11, and Fig. 3.12. Thus, the 2R1 is bigger than the 2R2+Rm. The 2R2+Rm is bigger than the 2R3+2Rm. The power of 20um DSESCR with 4 and 6 diodes is higher than the power of 20um DSESCR with 2 diodes. Thus, the current of 20um DSESCR with 4 and 6 diodes is higher than the current of 20um DSESCR with 2 diodes. To prove the explanation, the current of 20um DSESCR with 4 and 6 diodes is higher than the current of 20um DSESCR with 2 diodes before original leakage current is shifting, as shown in Table 3.4.

The R2 and R3 of 20um DSESCR with 4 and 6 diodes is bigger than the Rm of 20um DSESCR with 4 and 6. Thus, the metal is possibly burned on the region of R2 and R3.

Table 3.4

The current of TLP-IV curve before the original leakage current shifting.

20um DSESCR	2 diodes	4 diodes	6 diodes
	1.38A	1.55A	1.58A

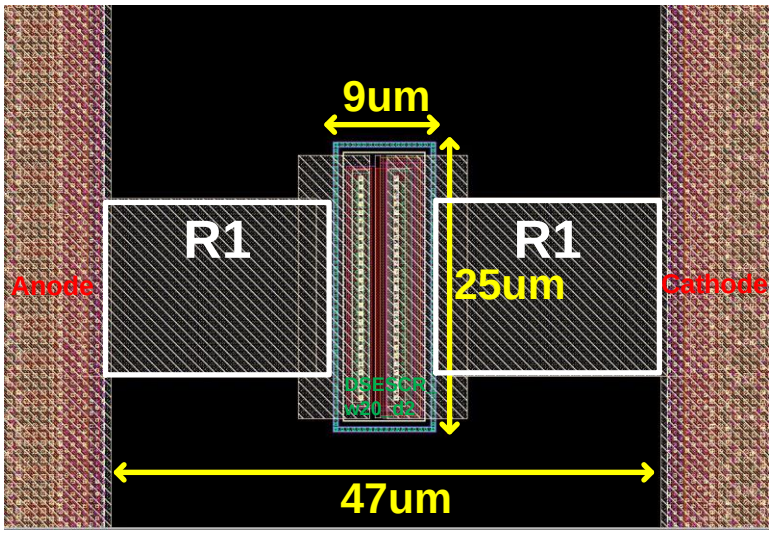


Fig. 3.10. The layout of the DSESCR_w20_d2.

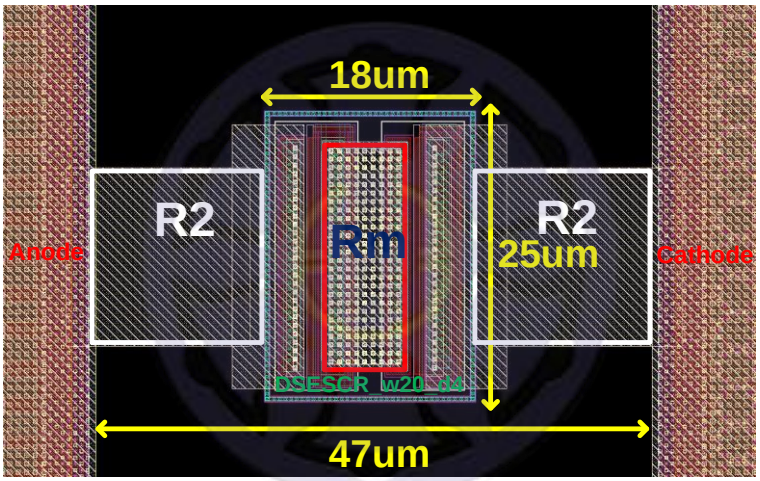


Fig. 3.11. The layout of the DSESCR_w20_d4.

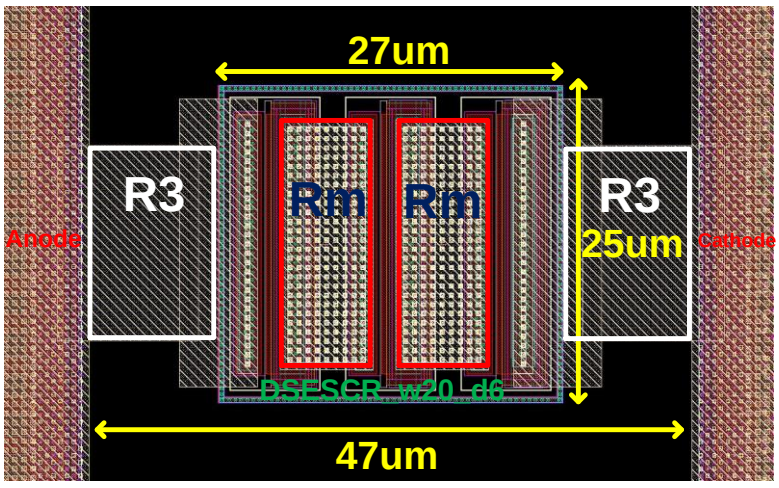


Fig. 3.12. The layout of the DSESCR_w20_d6.

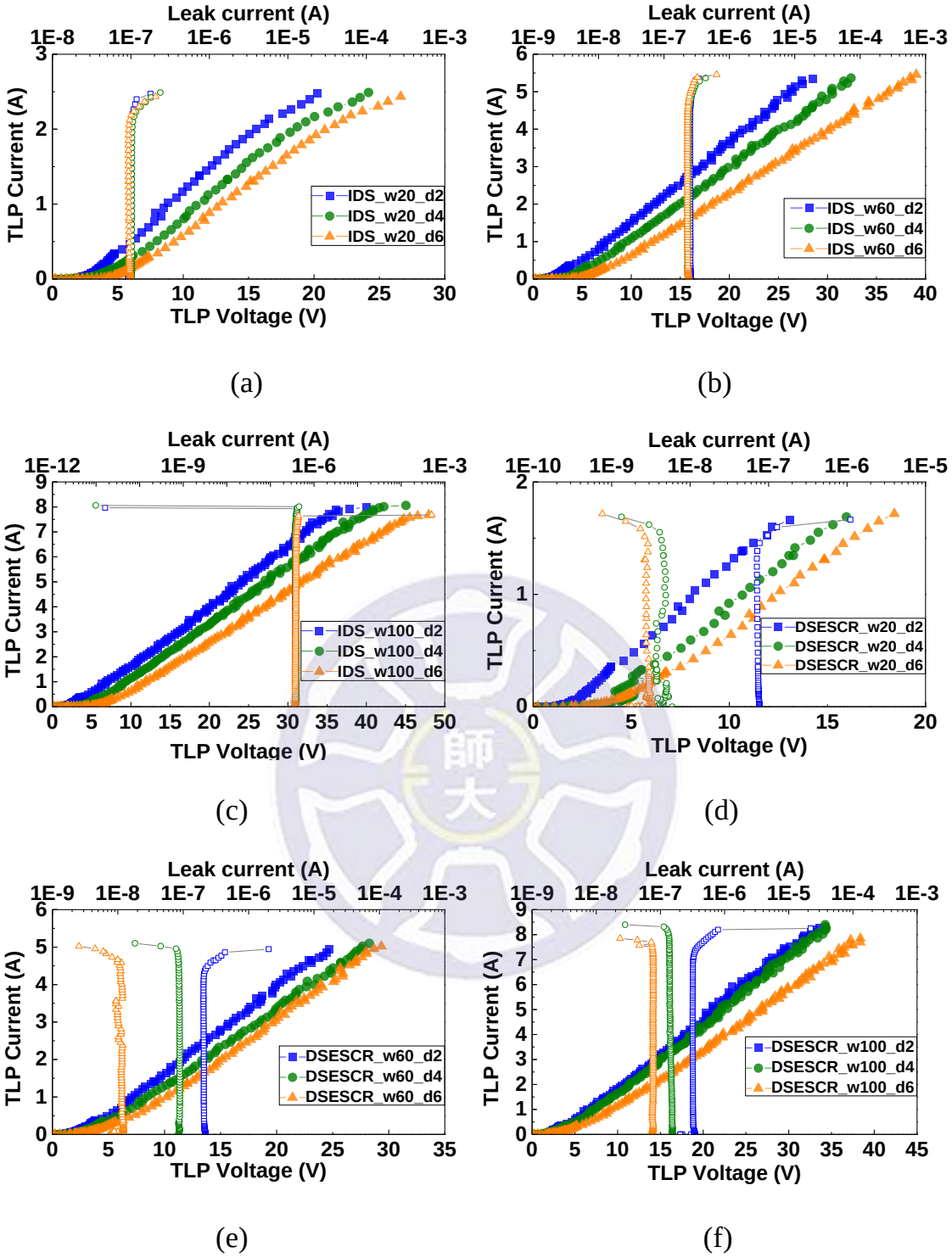


Fig. 3.13. Measured TLP-IV characteristics of (a) 20um IDS with 2, 4, and 6 diodes, (b) 60um IDS with 2, 4, and 6 diodes, (c) 100um IDS with 2, 4, and 6 diodes, (d) 20um DSESCR with 2, 4, and 6 diodes, (e) 60um DSESCR with 2, 4, and 6 diodes, (f) 100um DSESCR with 2, 4, and 6 diodes.

Table 3.5

Comparison of TLP measurement.

TLP (anode to cathode)				
Test device	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
IDS_w20_d2	2.3	2.3	2.4	6.4
IDS_w20_d4	3.2	3.2	2.4	7.2
IDS_w20_d6	4.5	4.5	2.4	7.9
IDS_w60_d2	1.6	1.6	5.3	5.1
IDS_w60_d4	3.2	3.2	5.3	5.6
IDS_w60_d6	4.4	4.4	5.4	6.2
IDS_w100_d2	1.6	1.6	7.9	4.4
IDS_w100_d4	3.3	3.3	8.0	4.6
IDS_w100_d6	5.0	5.0	7.6	5.1

TLP (anode to cathode)				
Test device	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)
DSESCR_w20_d2	1.7	1.7	1.6	6.4
DSESCR_w20_d4	3.8	3.8	1.6	6.7
DSESCR_w20_d6	3.7	3.7	1.6	8.1
DSESCR_w60_d2	1.5	1.5	4.9	4.6
DSESCR_w60_d4	2.1	2.1	5.0	5.1
DSESCR_w60_d6	2.6	2.6	5.0	5.5
DSESCR_w100_d2	2.0	2.0	8.2	3.6
DSESCR_w100_d4	1.7	1.7	8.3	3.7
DSESCR_w100_d6	2.7	2.7	7.8	4.4

3.4.2 Measured ESD Robustness

The human-body-model (HBM) ESD robustness of each circuit has been tested by the HBM tester. The failure criterion is defined as the I-V curves shown between the test pads shifting over 30% from its original curve after ESD stressed. All these HBM test results are also listed in Table 3.6.

The ESD robustness of human-body-mode in general commercial ICs must pass 2kV above. As shown in Table 3.6, ESD robustness of IDS, DSESCR all have passed the 2kV. In width 20um, the ESD robustness of DSESCR has lower than the ESD robustness of IDS. The others dimension almost have the same.

Table 3.6

Comparison of HBM ESD robustness.

Test device	HBM level (kV)	Test device	HBM level (kV)
IDS_w20_d2	4.5	DSESCR_w20_d2	3
IDS_w20_d4	6	DSESCR_w20_d4	3.75
IDS_w20_d6	6	DSESCR_w20_d6	3
IDS_w60_d2	>8	DSESCR_w60_d2	>8
IDS_w60_d4	>8	DSESCR_w60_d4	7.5
IDS_w60_d6	>8	DSESCR_w60_d6	>8
IDS_w100_d2	>8	DSESCR_w100_d2	7.25
IDS_w100_d4	>8	DSESCR_w100_d4	7.75
IDS_w100_d6	>8	DSESCR_w100_d6	7.75

3.4.3 Comparison and Discussion

The comparison among various diode string CMOS on-chip ESD protection have been summarized in Table 3.7. The layout area of DSESCR test device is lower than the layout area of prior devices. The I_{t2} of DSESCR is higher than the I_{t2} of IDS and the prior devices. The V_{t1} of DSESCR is lower than the V_{t1} of IDS and the prior devices. The proposed DSESCR can be a good on-chip ESD protection device.

Table 3.7

Comparison among the prior device, IDS, and DSESCR.

Test device		Diode counts	Width (um)	Layout area (um^2)	HBM level (kV)	TLP		
						I_{t2} (A)	V_{tr} (V)	R_{on} (A)
Reference [63]	D_P	2	100	1279	> 8	7.1	1.7	1.7
		4	100	2548	> 8	7.2	3.8	2.1
		6	100	3817	> 8	7.4	5.9	2.6
	D_N	2	100	2050	> 8	7.1	1.7	1.7
		4	100	3916	> 8	7.3	3.8	2.2
		6	100	5789	> 8	7.4	6	2.6
IDS		2	100	1390	>8	7.9	1.6	4.4
		4	100	2784	>8	8.0	3.3	4.6
		6	100	4177	>8	7.6	5.0	5.1
DSESCR		2	100	917	7.25	8.2	2.0	3.6
		4	100	1851	7.75	8.3	1.7	3.7
		6	100	2785	7.75	7.8	2.7	4.4

3.5 Experimental Results under System-Level ESD Test

According to the standard of IEC 61000-4-2, the ESD gun is used to evaluate the system-level ESD robustness. Using ESD gun test the IDS and DSESCR. Besides, the failure criterion is defined as leakage current shown between the test pads shifting over 30% from its original leakage current. Table 3.8 shows the system-level ESD robustness of IDS and DSESCR. The system-level ESD of improved diode string (IDS) does not increase by the size up that the p type guard ring of device structure possibly has been destroyed. The system-level ESD of stacked diode string with embedded SCR (DSESCR) can increase by the size up. Comparing IDS with DSESCR, DSESCR system-level ESD have a little higher than IDS.

Table 3.8

System-level ESD robustness of IDS and DSESCR.

Test device	System-level ESD robustness (kV)
IDS_w20_d2	0.9
IDS_w20_d4	0.8
IDS_w20_d6	0.8
IDS_w60_d2	1.1
IDS_w60_d4	1
IDS_w60_d6	1
IDS_w100_d2	1.1
IDS_w100_d4	1
IDS_w100_d6	1

Test device	System-level ESD robustness (kV)
DSESCR_w20_d2	0.7
DSESCR_w20_d4	0.8
DSESCR_w20_d6	0.7
DSESCR_w60_d2	1.2
DSESCR_w60_d4	1
DSESCR_w60_d6	1.2
DSESCR_w100_d2	1.5
DSESCR_w100_d4	1.5
DSESCR_w100_d6	1.3

3.5.1 Failure Analysis

The failure analysis (FA) has been finished to seek the failure location after the IDS test system-level ESD. The FA pictures of the IDS_w60_d2 after +1.2kV system-level ESD, the IDS_w60_d4 after +1.1kV system-level ESD, the IDS_w60_d6 after +1.1kV system-level ESD, the IDS_w100_d2 after +1.2kV system-level ESD, the IDS_w100_d4 after +1.1kV system-level ESD, the IDS_w100_d6 after +1.1kV system-level ESD are shown in Fig 3.14-Fig 3.20.

The layout and optical microscope (OM) picture of the IDS_w60_d2 is shown in Fig 3.14. The size, guard ring regions, and damaged regions of IDS_w60_d2 are shows in the picture and layout. After +1.2kV system-level ESD, the damaged regions are located on the P+ of guard ring and P+ of anode. As shown in Fig. 3.15, between P+ of the anode and guard ring exist parasitic resistances. When a higher energy inject into P+ of the anode, parasitic resistances are small, the P+ of the anode and guard ring possibility damage. Therefore, to improve the device of IDS_w60_d2, the spacing of the anode and guard ring can be increased that parasitic resistances can be increased. The system-level ESD robustness will be increased. In Fig 3.16-Fig 3.20, after system-level ESD, the damaged regions are also located on the P+ of guard ring. To improve the device of IDS, the space of guard ring can also be increased.

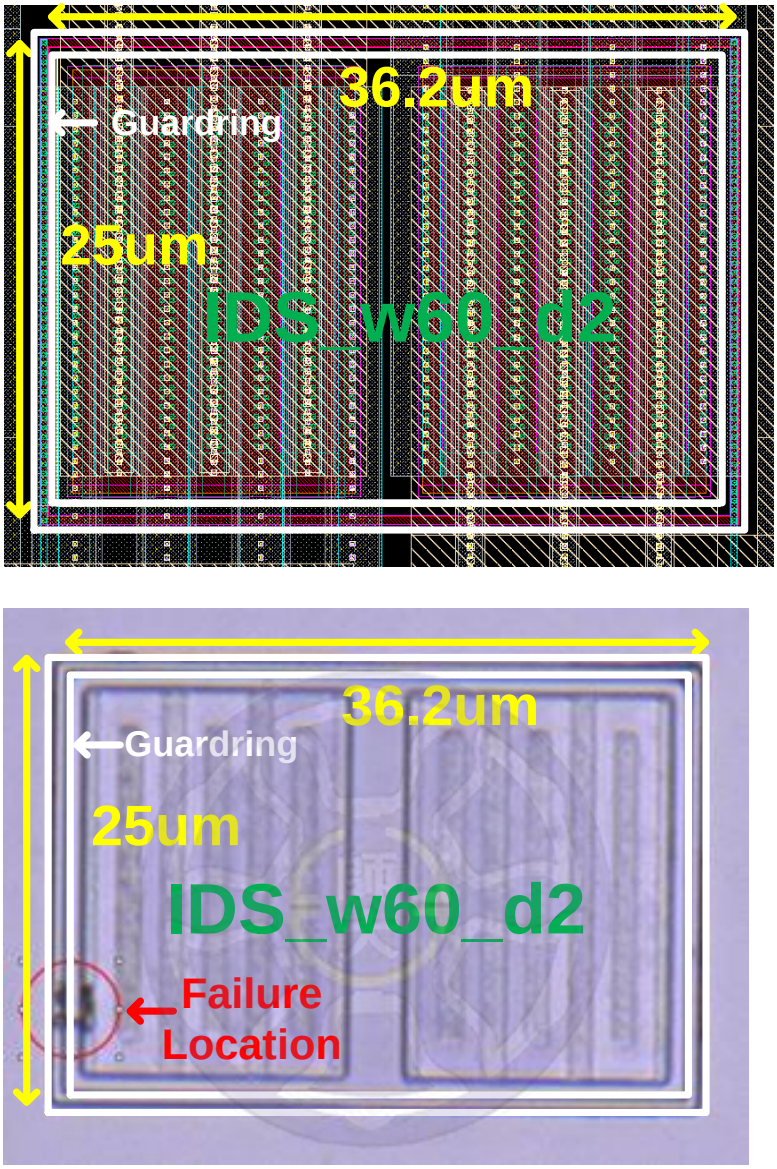


Fig. 3.14. The layout and OM picture of the IDS_w60_d2 after +1.2kV system-level ESD.

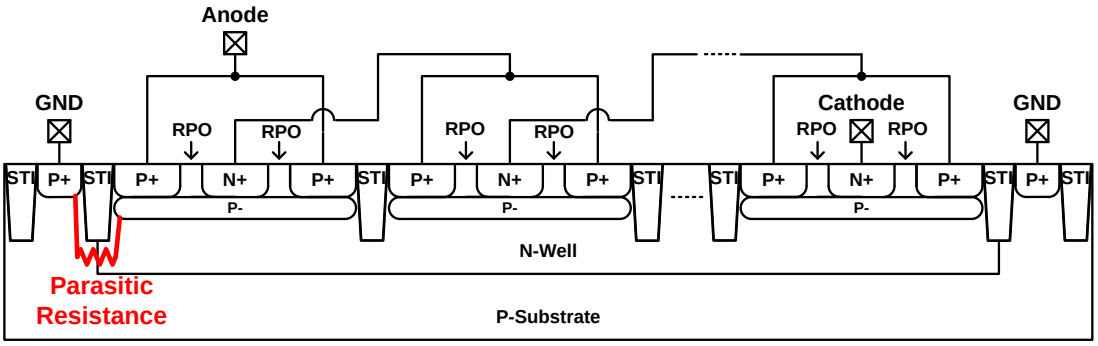


Fig. 3.15.Parasitic resistances in improved diode string (IDS).

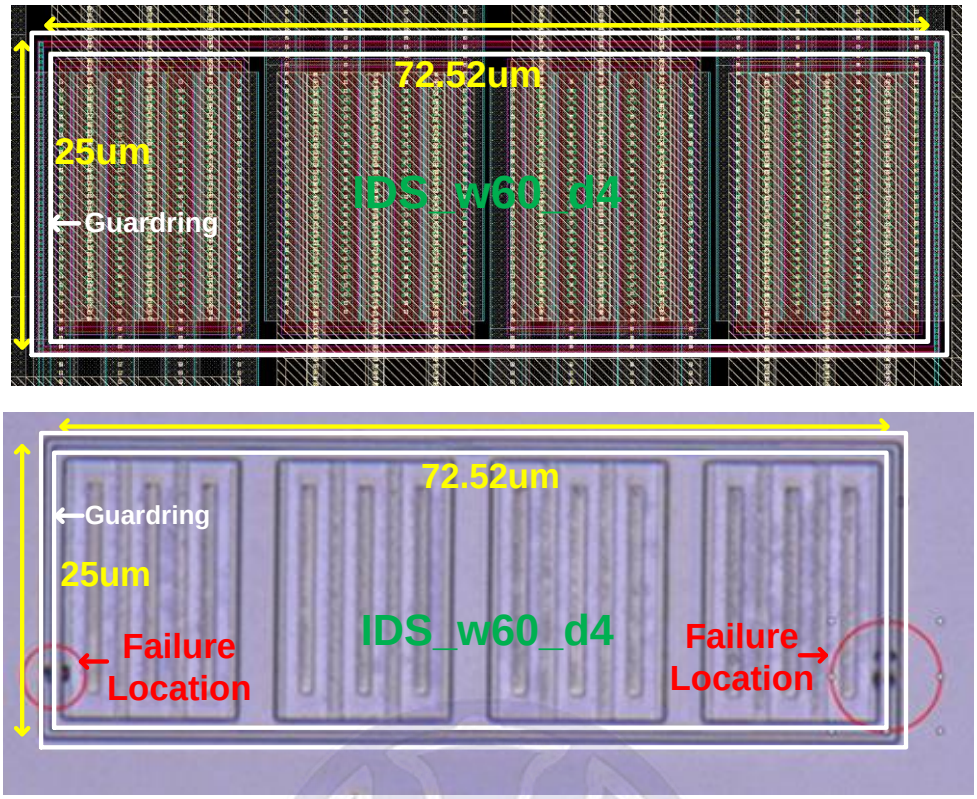


Fig. 3.16. The layout and OM picture of the IDS_w60_d4 after +1.1kV system-level ESD.

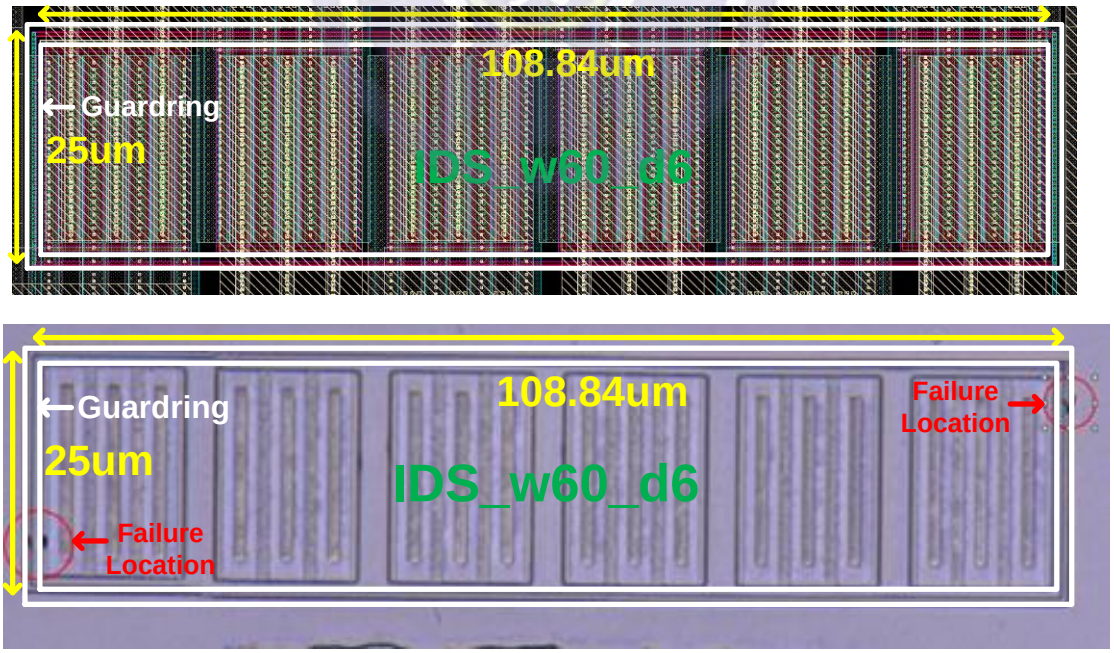


Fig. 3.17. The layout and OM picture of the IDS_w60_d6 after +1.1kV system-level ESD.

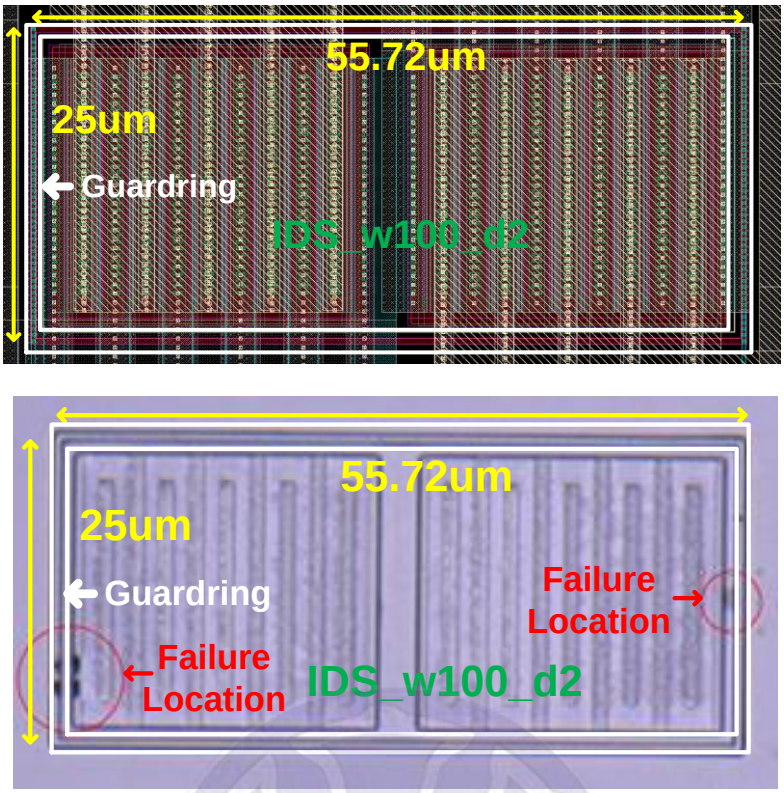


Fig. 3.18. The layout and OM picture of the IDS_w100_d2 after +1.2kV system-level ESD.

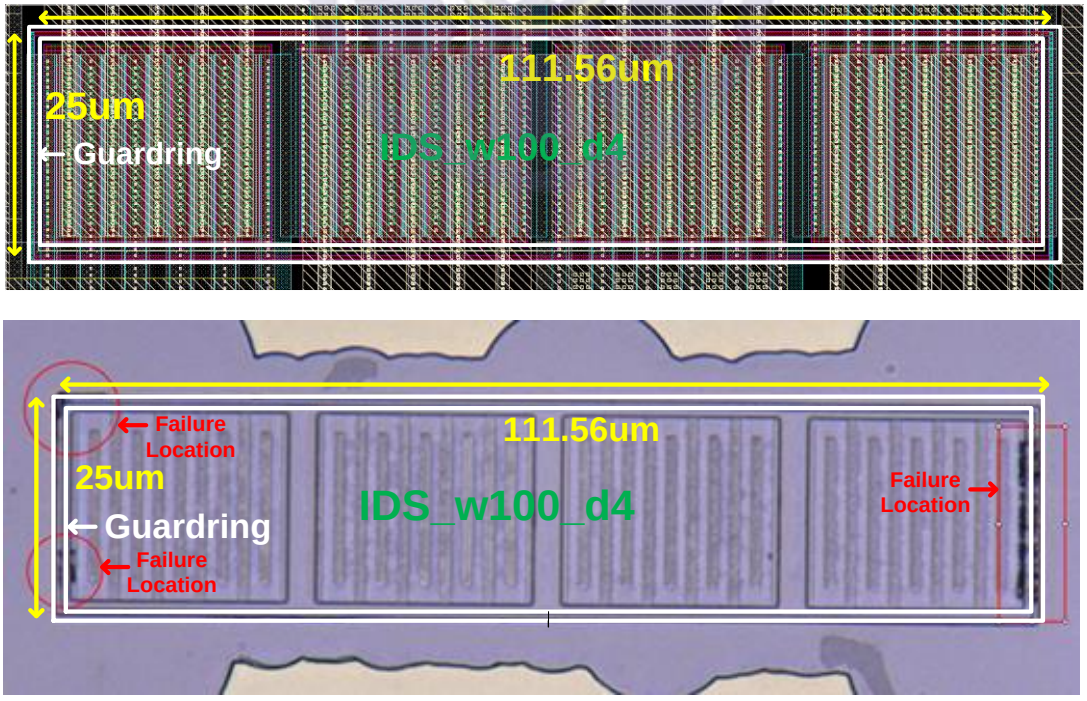


Fig. 3.19. The layout and OM picture of the IDS_w100_d4 after +1.1kV system-level ESD.

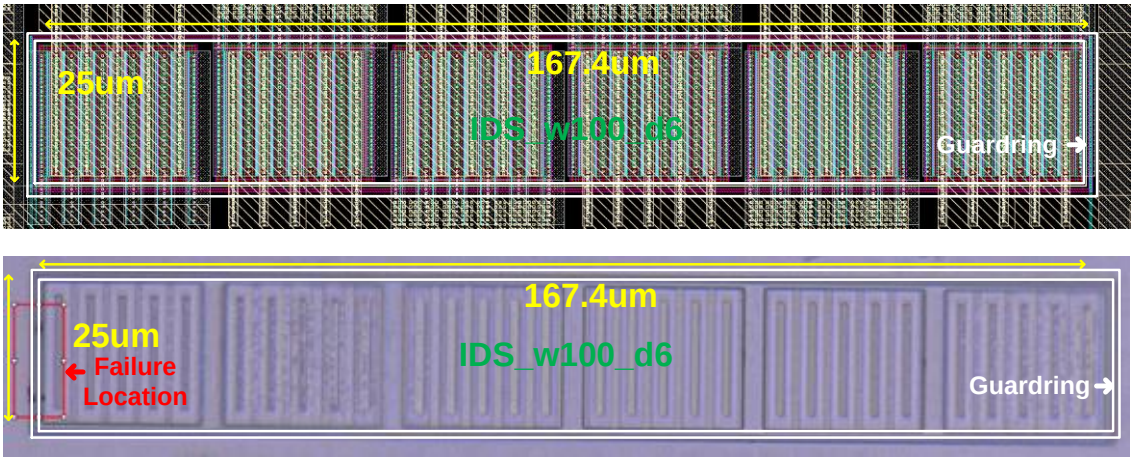


Fig. 3.20. The layout and OM picture of the IDS_w100_d6 after +1.1kV system-level ESD.

3.6 Comparison of measurement results

The HBM ESD robustness, current handling capability, and system-level ESD robustness of IDS and DSESCR integrate in Table 3.9. The HBM ESD robustness of IDS and DSESCR is 1.5 times as much as secondary breakdown current (I_{t2}) of IDS and DSESCR. Most of the system-level ESD robustness of DSESCR has better than IDS.

Table 3.9

Comparison of IDS and DSESCR.

Test device	Width	Diode counts	HBM level (kV)	TLP I_{t2} (A)	System-level ESD robustness (kV)
IDS	20	2	4.5	2.4	0.9
		4	6	2.4	0.8
		6	6	2.4	0.8
	60	2	>8	5.3	1.1
		4	>8	5.3	1
		6	>8	5.4	1
	100	2	>8	7.9	1.1
		4	>8	8.0	1
		6	>8	7.6	1
DSESCR	20	2	3	1.6	0.7
		4	3.75	1.6	0.8
		6	3	1.6	0.7
	60	2	>8	4.9	1.2
		4	7.5	5.0	1
		6	>8	5.0	1.2
	100	2	7.25	8.2	1.5
		4	7.75	8.3	1.5
		6	7.75	7.8	1.3

3.7 Summary

To understand and compare the traditional and novel device in the component-level and system-level ESD, the improved diode string (IDS) and stacked diode string with embedded SCR (DSESCR) are designed. The proposed stacked diode string with embedded SCR has been developed for on-chip ESD protection device. Verified in silicon chip, experimental results show that novel design device of DSESCR has the advantages of lower trigger voltage, lower layout area, higher ESD robustness, and lower leakage current. Besides, these ESD protection devices can be further used for system-level ESD to understand system-level ability. The system-level ESD robustness of improved diode string (IDS) does not increase by the size up because the guard ring of IDS has probably destroyed.

Finally, these experimental results can provide the design guideline for ESD protection in 0.18 um CMOS technology.

Chapter 4

Conclusions and Future Works

This Chapter summarizes the main results and contributions of this study. Future works of ESD protection design for internal circuits in CMOS process are also provided in the Chapter. In this study, the kinds of ESD protection devices have been developed in nanoscale BiCMOS and CMOS technology for component-level and system-level ESD protection design. Each of the test devices and circuits has been successfully verified in the test chip.

4.1 Conclusions

NBJT, diodes with power clamps, and GGNMOS with power clamps are studied under component-level and system-level ESD. TVS diode is used to improve the system-level ESD robustness.

Comparing novel DSESCR with TDS and IDS, DSESCR has the advantages of lower trigger voltage, lower layout area, higher currents, and lower leakage current. DSESCR can improve drawbacks of high clamp voltage and high leakage current of TDS and IDS. System-level ESD robustness of 100um DSESCR have higher than system-level ESD robustness of 100um IDS. The DSESCR recommend for ESD protection devices.

4.2 Future Works

On-chip ESD protection circuits for internal circuits are shown in Fig. 4.1. The designer can use ESD protection circuits of NBJT with R_{be}, diodes with power clamps, GGNMOS with power clamps, IDS, and DSESCR for internal circuits, such as low-noise amplifier (LNA) circuits, power amplifier (PA) circuits, and high speed circuits.

The designer can use two-stage system-level ESD protection to improve on-chip ESD protection circuits.

NBJT with R_{be}, diodes with power clamps, GGNMOS with power clamps, IDS, and DSESCR can also be further used for system-level and component-level ESD.

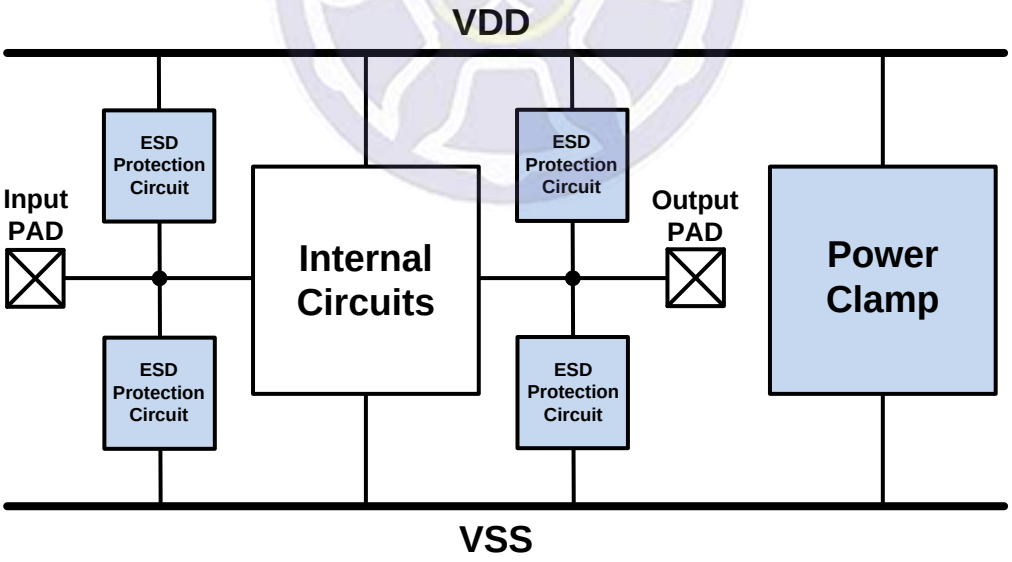


Fig. 4.1. On-chip ESD protection circuits for internal circuits.

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自　傳

研究生傅偉豪，生於桃園八德，與家人的感情非常和睦，主要興趣為ACGN及影集，來提供生活上的樂趣。

研究方面，在大學時期專題就為積體電路可靠度相關研究，也因此產生興趣，在研究所時期也是積體電路可靠度的相關研究，主要設計了多種靜電放電防護元件，並期望能讓使用者解決靜電放電的問題。

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