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24-GHz 低雜訊放大器之靜電放電防護設計

On-Chip ESD Protection Design for 24-GHz LNA

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24-GHz 低雜訊放大器之靜電放電防護設計

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摘　　要

本論文主旨為應用於射頻積體電路之全晶片靜電防護電路，本論文設計了兩種應用於高頻積體電路的靜電放電防護設計，並與先前論文所提出的傳統防護電路來做比較。所下線之晶片皆使用0.18μm CMOS製程。

傳統靜電放電箝制電路已被廣泛應用於靜電放電防護設計之中，然而其高佈局面積在先進製程中往往會是個麻煩，因此本篇論文利用矽控整流器低佈局面積與優秀靜電防護能力特性，來加以改善傳統電路，而矽控整流器的閂鎖效應與導通速度過慢問題，本論文也提出了解決方法；本論文提出使用內嵌入式矽控整流器二極體串來改良原先P型與N型二極體的靜電放電能力，透過量測結果比較，本論文提出的兩種靜電放電防護設計皆能在單一面積下提供最佳的靜電耐受度並擁有且較低損耗值。

為了驗證靜電防護電路應用於高頻電路的實際功用，本論文也設計了24GHz低雜訊放大器並搭配適當尺寸的防護電路，在量測結果中，本論文所提出的防護設計並不會影響高頻電路之響應。

關鍵字：靜電放電、矽控整流器、低雜訊放大器

On-Chip ESD Protection Design for 24-GHz LNA

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All ABSTRACT

This essay is to design an effective whole-chip ESD protection circuits for RF integrated circuit. In this essay, two types of ESD protection designs, which apply to RF integrated circuits have been proposed and compared with conventional ESD protections. All of circuits in this essay are fabricated in 0.18-μm CMOS process.

The conventional power-rail ESD clamp circuit has been used widely in ESD protection designs. However, the high layout area of conventional circuit is an issue in advanced process. Therefore, using silicon-controlled rectifier (SCR) with low layout area and excellent ESD protection ability improves the issue of the conventional power-rail ESD clamp circuit that is high layout area. Furthermore, solutions of the latch-up problem and slow-trigger-on speed of SCR have been proposed. In this essay, using the diode string with embedded SCR improves the issue of p-type and n-type diodes. Through the comparison of measurement results, two types of ESD protection designs can provide the best ESD robustness and the lowest loss at unit area.

In order to verify the practical function of ESD protection circuit on RF circuit, the low-noise amplifier (LNA) with the appropriate size of ESD protection circuit has been designed. In measurement results, proposed designs do not affect the RF performance.

Keywords: Electrostatic discharge, silicon-controlled rectifier, low-noise amplifier.

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在台師大電機研究所的碩士生涯中，首先要感謝我的恩師林群祐教授這兩年多來的細心教導，使學生能夠在靜電放電設計這博大精深的領域打好良好基礎，並且老師您也給予我最好的學習環境與資源，讓我能夠去CIC上課學習與參與研討會，吸取外界新資訊讓我收穫滿滿。除了專業知識的學習外，老師您積極的處事原則與嚴謹的研究態度，讓學生學習到如何高效率做好每件事並且繳出有水準的成果，十分感謝老師您對我的栽培，學生覺得非常充實與感動，並且準備好邁入人生的下一個階段。

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Chapter 1

Introduction

1.1 Motivation

In this era of globalization, the world is becoming more convenient through advances in technology. As the popularity of smartphones, making people more easily through the network to link each other's life. All kinds of electronic communication devices will be required for low power and faster operation speed. CMOS process has less cost and high efficiency among different process, so RFICs have been widely designed and fabricated in this process. However, there is still potential danger, which is electrostatic discharge (ESD) problem [1].

CMOS advanced technologies nowadays make the transistor scale down which let gate-oxide become thinner, but the gate-oxide punch through easily. A few volts of static electricity voltage will punch through the layer, making original MOSFET fail. Therefore, the internal circuit must equip ESD protection circuit to prevent ESD damage. The low-noise amplifier (LNA) is the front-end circuit of receiver structure, which is more likely to happen ESD events [2]. If LNA is attacked by ESD stress, the receiver will fail immediately. That is a horrible problem for communication applications. Hence, LNA must equip ESD protection circuit.

However, the parasitic effort of ESD protection circuit will influence RF performance [3]. Therefore, a good ESD protection design, which can provide strong ESD performance and less parasitic effort, will be a great challenge [4], [5].

1.2 Background of ESD

ESD events become a major issue of reliability, especially IC industries. Before every IC products shipment, they must pass safety certification. ESD specifications of industries are required to pass 2kV in human body model (HBM), 200V in machine model (MM), and 250V in charged device model (CDM) [6], [7]. In next paragraph, all of test methods will be introduced.

1.3 Testing Methods

Broadly speaking, ESD test standards in component level refer to three of test models, which are human-body-model (HBM), machine-model (MM) and charged-device-model (CDM). Using these test standards can help to understand ESD robustness of device.

When people touch ICs, the accumulated static electricity in human body will discharge into ICs. The discharge process may destroy ICs. In order to prevent these issues happen, the human body model (HBM) have been presented, as shown in Fig. 1.1. During the HBM test, the charges will charge the capacitor and then discharge into device under test (DUT) through 1.5 kΩ resistor.

Machine model (MM) is similar to HBM. As shown in Fig. 1.2, the equivalent circuit of MM has 200pF capacitor, but no resistor. During MM test, the charge of capacitor will discharge into DUT directly.

Charged device model (CDM) means a simulation model, which accumulates static electricity from IC internal and then the IC's pins touch the ground. The cumulative static electricity will be discharged from the internal to the ground, the discharge time which is about few nanoseconds is shorter than HBM and MM. As shown in Fig. 1.3,

the equivalent circuit of CDM has no resistor. In addition, the capacitance of model will change according to different position of IC or even the packaging. Therefore, the simulation of CDM is the most difficult in these models [8].

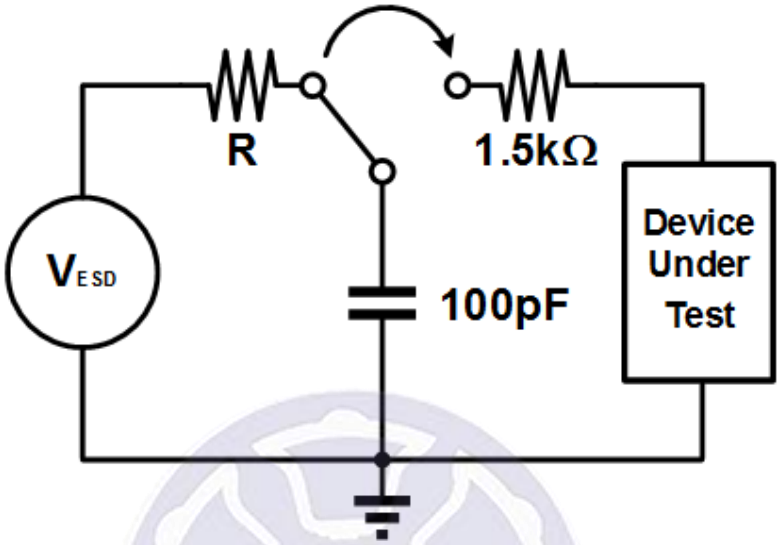


Fig. 1.1. Equivalent circuits of HBM.

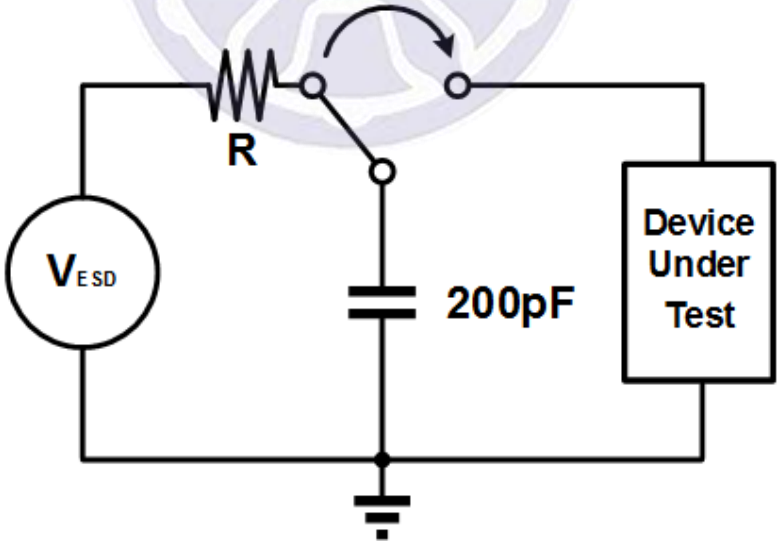


Fig. 1.2. Equivalent circuits of MM.

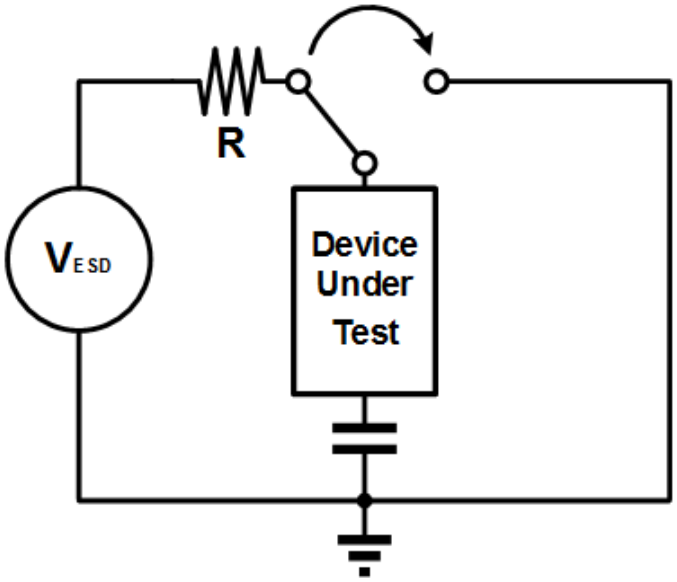


Fig. 1.3. Equivalent circuits of CDM.

1.4 Background of Whole-Chip ESD Protection Circuit

Nowadays, the advanced process has become nano level that can help increase the operating speed and frequency of transistor. However, the advanced process also bring the gate oxide of transistor to be thinner, making a few of static electricity punch through easily. ESD issues become more attention progressively, especially in radio-frequency integrated circuits (RFICs) [9], [10]. Thus, it is necessary to design an appropriate ESD protection circuit, avoiding high-frequency integrated circuit be attacked. Every IC should be equipped ESD protection circuit between input and output pads. Therefore, ESD protection device can provide a direct discharge path when the ESD events happened. Nevertheless, the ESD circuit also brings the load effect, causing a great deal of loss from the main circuit. The main reason of affecting high-frequency circuit characteristic is parasitic capacitance, as shown in Fig. 1.4. Therefore, the parasitic capacitance of ESD protection circuit is an important factor for high-frequency application. In next chapter, the solution of parasitic capacitance will be introduced.

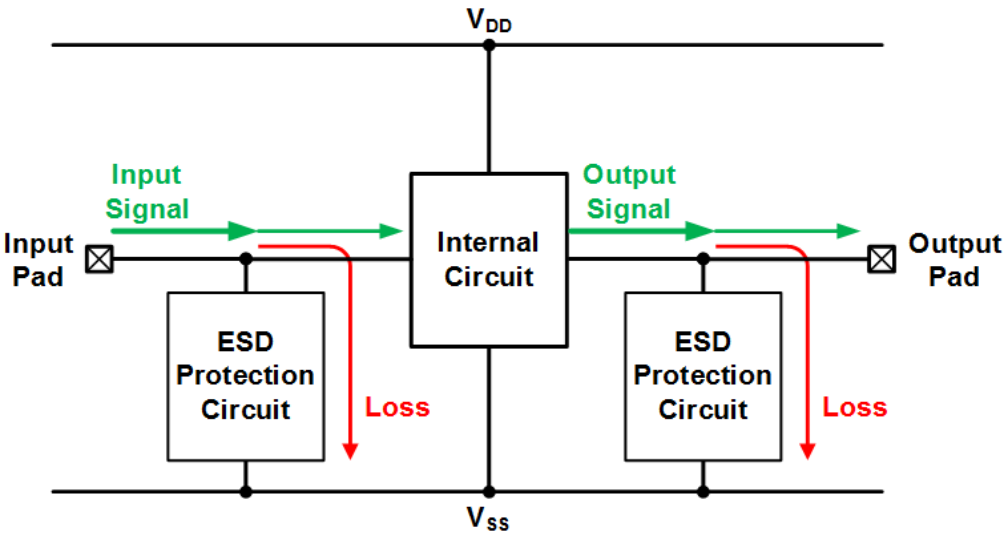


Fig. 1.4. Signal loss of ESD protection circuit.

In Fig. 1.5, this ESD protection circuit structure is used widely. To select the appropriate ESD protection device between I/O and V_{DD} /V_{SS} provides a discharge path to the power supply line. Moreover, the power-rail ESD clamp circuit between V_{DD} and V_{SS} uses to achieve the whole-chip ESD protection design. The ESD stress maybe positive or negative voltage on pad. Thus, designing ESD protection circuit should confirm the ESD discharge path. There are four paths about discharging ESD current at least. During the positive voltage appears on I/O pad and discharges ESD current from I/O to V_{SS}, which is called positive-to-V_{SS} (PS) mode. The other positive voltage discharge to V_{DD} is called positive-to-V_{DD} (PD) mode. During negative voltage discharge from I/O pad to V_{SS}, known as negative-to-V_{SS} (NS) mode. The last ESD discharge path is negative-to-V_{DD} (ND) mode, which means negative ESD current discharges from I/O pad to V_{DD}.

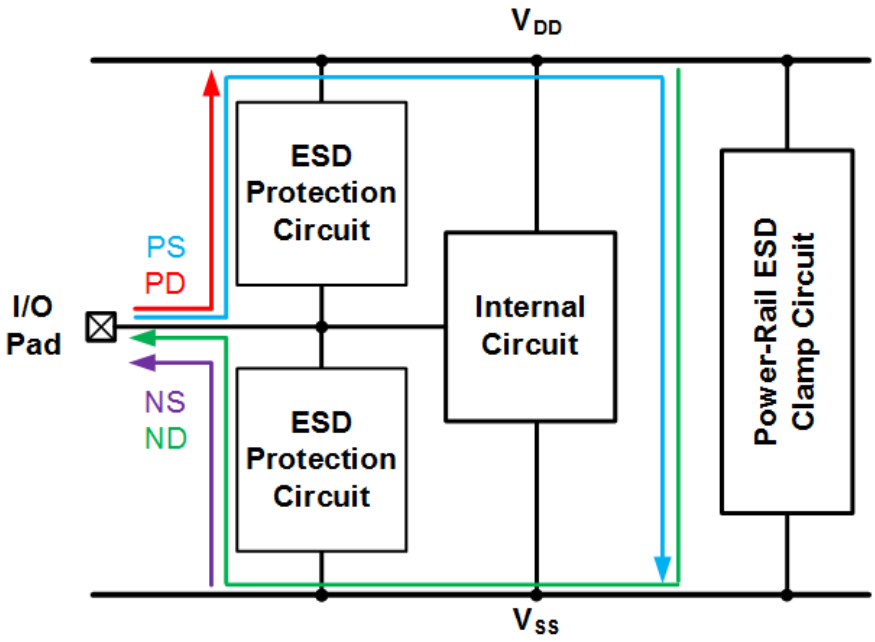


Fig. 1.5. Typical ESD protection circuit design.

Fig. 1.6 shows the ESD design window of ESD device design. When designing the ESD protection device must let the working area of device between the maximum supply voltage (V_{DD}) and the device breakdown voltage (V_{BD}). In the normal operation, the trigger voltage (V_{tri}) must be lower than the breakdown voltage; otherwise, the internal circuit will fail by ESD current before the protection device has turned on. The holding voltage (V_h) must be higher than the maximum supply voltage, otherwise, the protection device will produce a large number of leakage and it will cause the main circuit distortion. Additionally, the turn-on resistance (R_{on}) of the protection circuit will determine the power loss on ESD events. Finally, the ESD robustness of protection device can use the second breakdown current (I_{t2}) to determine the ESD protection device is good or not [11].

The second breakdown current means the component has reached the maximum current value of P-N junction limit. Once the current has exceeded, the component will produce a lot of leakage current and then burn. In the process, the leakage current makes an irreversible damage and loses the protection function. Thus, the component's

maximum ESD current equivalents approximately to I_{t2} when using HBM to test ESD component robustness. In the equation (1-1), the equivalent body resistance defines as 1500 ohms. The component resistance (R_{device}) almost is zero because the component has become conductive property when the component current value exceeds I_{t2}.

$$V_{ESD} \cong I_{t2} \times (1500 + R_{device}) \qquad (1\text{-}1)$$

In the ESD protection circuit, the component is used in the first breakdown area (1st breakdown regions) to discharge, the component has not broken yet. However, the limit of 1st breakdown regions still exists. The limit of 1st breakdown regions is second breakdown current. The component will burn due to the addition of voltage or current into second breakdown regions. Therefore, the equation shows the I_{t2} to multiply by 1.5 is the component 's ESD robustness value.

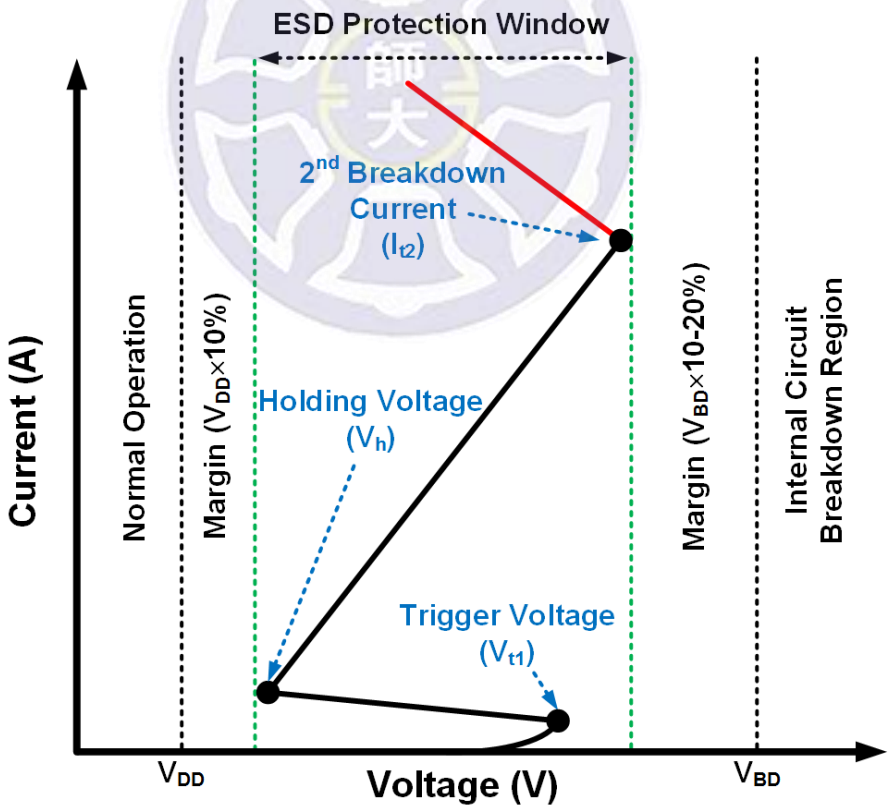


Fig. 1.6. ESD design window.

Many of ESD protection device has been presented now. For example, the forward-bias diode and silicon-controlled rectifier (SCR) are very great ESD protection components [12]-[14]. Fig. 1.7 and Fig. 1.8 shown application circuits. In next chapter, characteristic of ESD protection circuits will be introduced in detail.

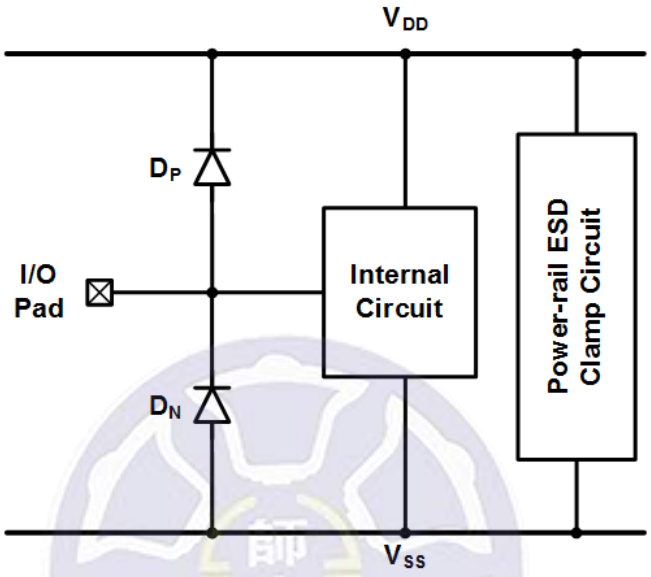


Fig. 1.7. ESD protection circuit with diodes.

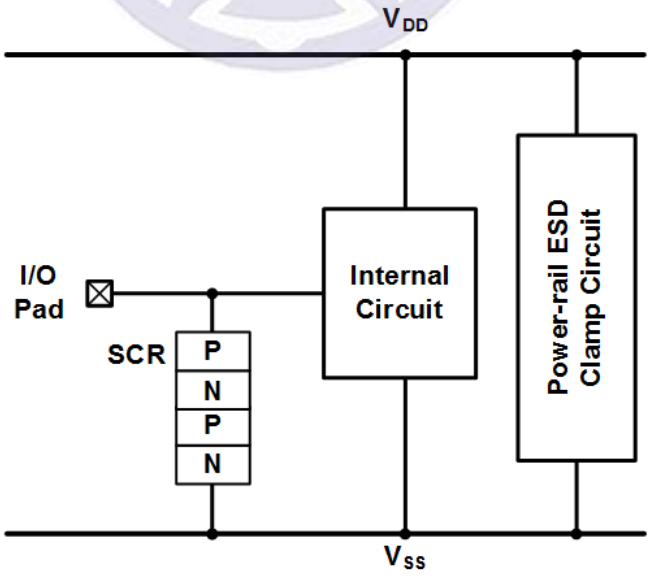


Fig. 1.8. ESD protection circuit with SCR.

1.5 Organization of This Dissertation

In Chapter 1, the motivation of designing ESD protection, the background and testing methods of whole-chip ESD protection circuit will be introduced.

In Chapter 2, all of ESD protection circuit have been fabricated in 0.18-μm CMOS process. In this study, the ESD protection circuit design will be introduced, including design steps and measurement results.

In Chapter 3, K-band low-noise amplifier design steps will be introduced. Design steps will be presented, including the theory, design, simulation and measurement.

In Chapter 4, summarizes all the research and future works on this topic.

Chapter 2

Whole-Chip ESD Protection Circuit Design

2.1 ESD Protection Component

2.1.1 Diode

In the forward-biased diodes have a good ESD performance, forward-biased diodes provide an ESD current discharge path. Furthermore, the diode also can use in trigger device, which is equipped with SCR, BJT and MOSFET. However, the frequency of RF operating speed rises gradually. The parasitic effect of the diode will affect internal circuit greatly. In order to overcome the parasitic effect problem adjust the number of diodes that can reduce the equivalent capacitance.

Common type of diodes are p-type and n-type. As shown in Fig. 2.1 and Fig. 2.2, two types of diodes including of p-type (P+/N-well) and n-type (N+/P-well) has been presented. Generally, the p-type diode connects I/O and V_{DD}, the n-type diode connects I/O and V_{SS} [15]. In this case, dual diodes or dual stacked diodes applied for I/O ESD protection device in common. However, the traditional dual diodes or dual stacked diodes is not suitable anymore in the advanced process. The leakage current of diode is a critical drawback at high temperature. For this reason, the modify structure of diode has been proposed that overcomes high leakage current. In next statement, a modify diode will be illustrated.

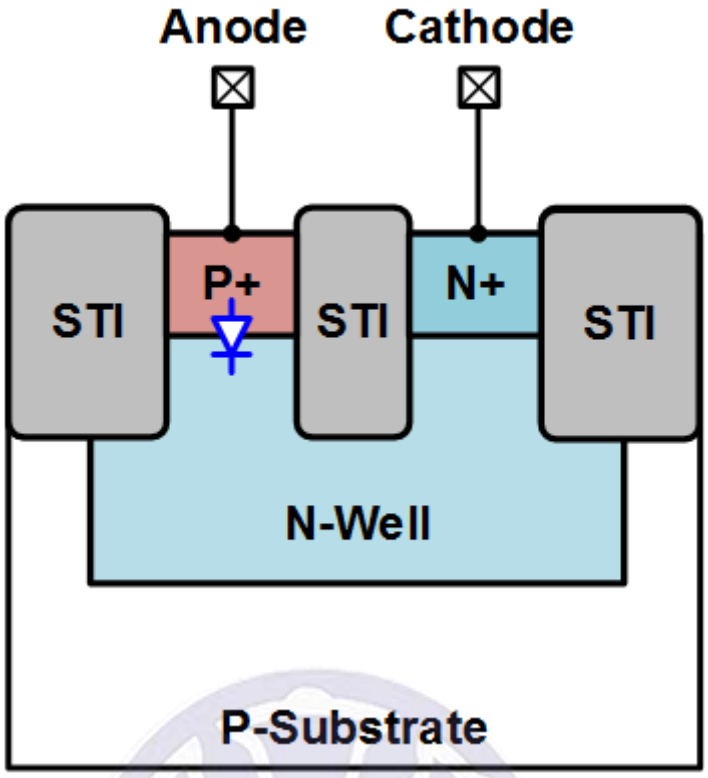


Fig. 2.1. Cross-sectional of p-type diode.

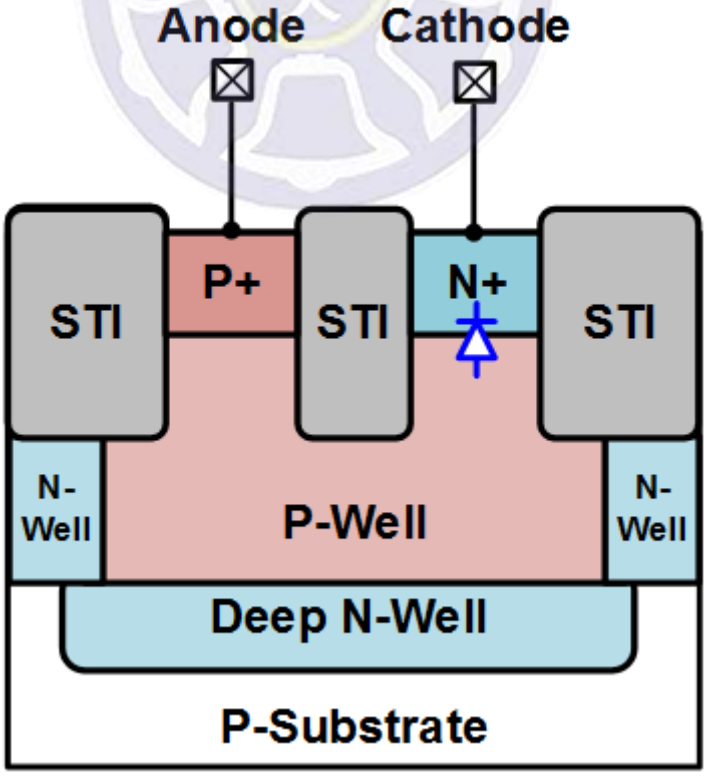
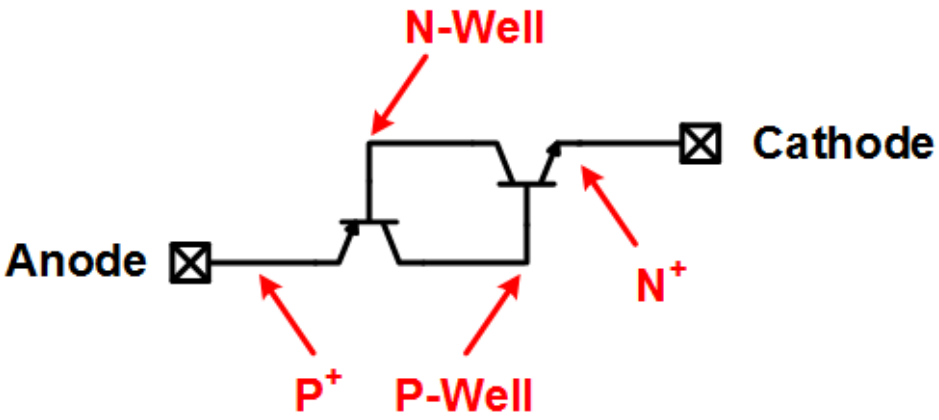


Fig. 2.2. Cross-sectional of n-type diode.

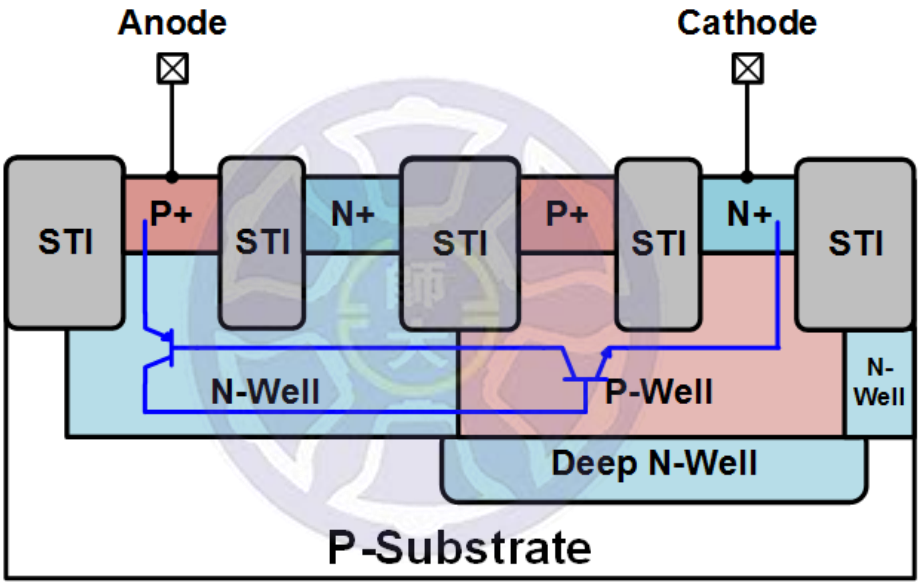
2.1.2 SCR

Silicon-controlled rectifier (SCR) is composed of the P-N-P-N four-layer semiconductor structure, as shown in Fig. 2.3. In Fig. 2.3 (a), SCR consists of PNP (P+/N-well/P-well) and NPN (N-well/P-well/N+) BJTs. SCR has an excellent ability [16], which can provide the highest electrostatic discharge performance on a unit area, as shown in Fig. 2.3 (b). However, SCR still has some issue need to overcome. One of problem is the latch-up that may lead serious distortion of circuit or the circuit burn. The four-layer structure of SCR will form two bipolar transistor and the bipolar transistor will form positive feedback until bipolar transistor has burned. Another problem is that SCR has higher trigger-on voltage than other ESD protection components. Thus, SCR has lower turn-on speed. If these problems of SCR has overcome, SCR can apply in lots of ESD protection circuit.

There are two solutions for improving latch-up problem. Operating SCR in low voltage environment and adding diodes in SCR prevent latch-up problem; choosing the former prevents the latch-up problem in this study. For overcoming high trigger-on voltage of SCR, adding a trigger-on device on SCR may be a good solution. As mentioned in the previous statement above, the diode is not only a great ESD protection component but also can be a trigger-on component. Using small-area diode makes improve SCR problems, which mean higher turn-on voltage and slower turn-on speed. Although this method may increase additional layout area, it can improve the turn-on speed of SCR effectively. In this essay, the SCR with the appropriate trigger-on component will be presented.



(a)



(b)

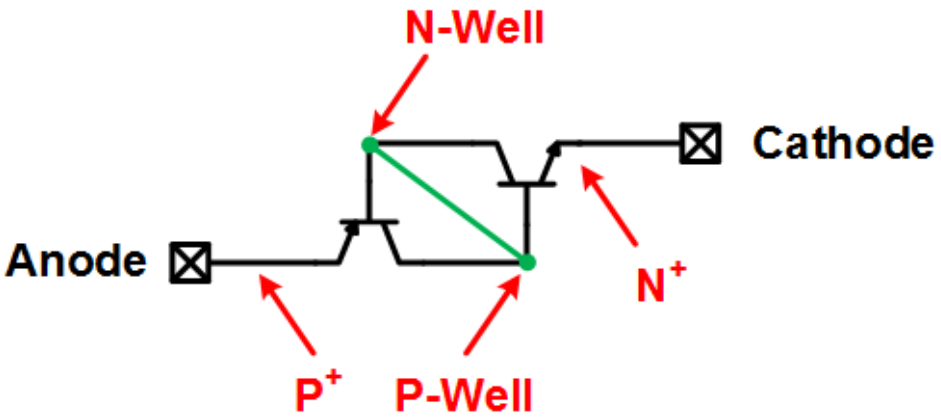
Fig. 2.3. (a) Equivalent circuit and (b) cross-sectional view of SCR.

2.1.3 DSSCR

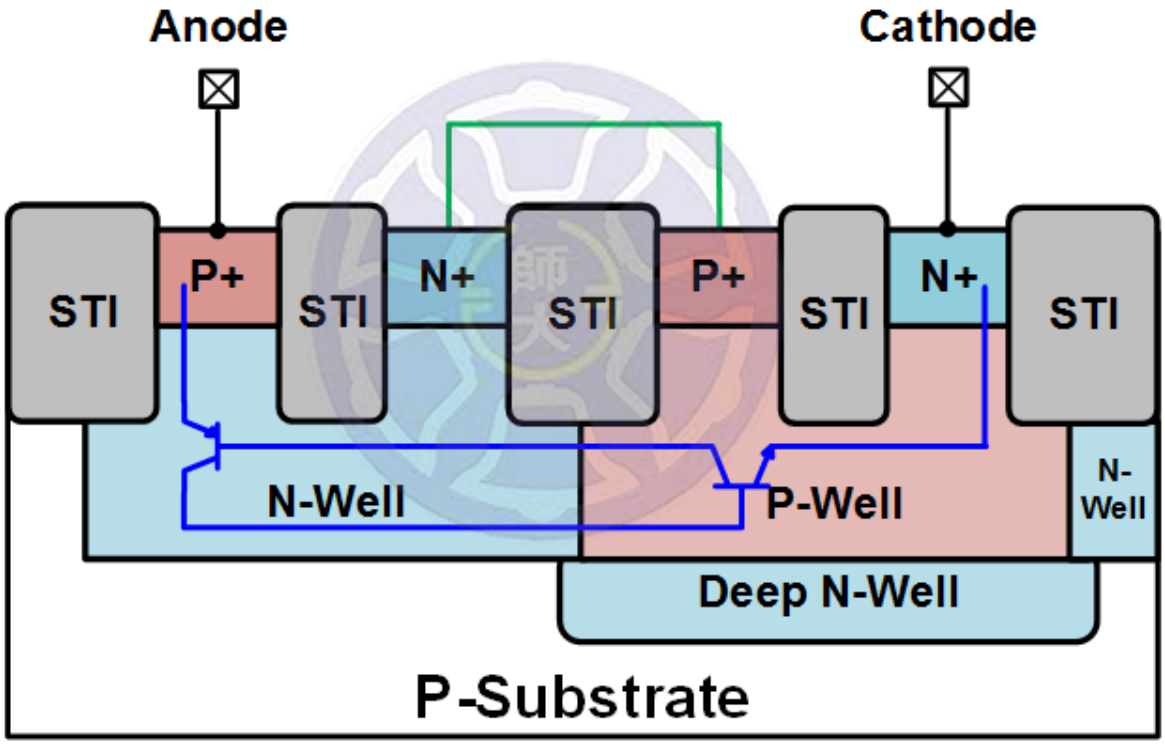
The large dimension of diode-string can provide a good ESD robustness, but it also accompanies large parasitic capacitance, which degrades the RF performance very much. Therefore, the parasitic capacitance of dual diodes is a key fault for high-frequency applications. The silicon-controlled rectifier (SCR) has been confirmed that it has low parasitic effects and high ESD robustness within less layout area. As a result, we propose a novel ESD protection device, which combines diode and SCR advantages [17].

The proposed diode string with embedded SCR presents in Fig. 2.4. Fig. 2.4 (a) shows the equivalent circuit and Fig. 2.4 (b) shows the device cross-sectional view. In Fig. 2.4 (a), DSSCR consists of a p-type diode, an n-type diode, PNP (P+/N-well/P-well) and NPN (N-well/P-well/N+) BJTs. In this structure, it forms diodes connect in series with the embedded SCR (P+/N-well/P-well/N+) that can be used to I/O-to-V_{DD} and V_{SS}-to-I/O, as shown in Fig. 2.4 (b). The deep N-well applies to divide the P-well from P-substrate. The number of diodes can adjust according to circuit needs.

When the ESD occurs, the diode strings will turn on and discharge the ESD current until the embedded SCR turn on. After that, the embedded SCR will take over the discharge. The diode is also a trigger circuit for SCR. Adjusting the number of diodes can alter the trigger voltage of SCR, so that it will remain off in the non-ESD event.



(a)



(b)

Fig. 2.4. (a) Equivalent circuit and (b) cross-sectional view of DSSCR.

2.2 Design of Power-Rail ESD Clamp

The MOS-based power-rail ESD clamp circuit is composed of an ESD detection circuit and a large size MOS which designs for discharging ESD current, as shown in Fig. 2.5. The large size MOS will be called M_{ESD} in this essay. The operated-principle of ESD detection circuit is using RC-inverter to detect ESD events [18]. Generally, the rise-time of V_{DD} power-on is about 1μS, but the rise time of ESD events is about 10ns. To adjust the time constant of ESD detection circuit at 0.1-1μS can differentiate between normal circuit operations and ESD events. In normal operation, the input terminal voltage of inverter can keep up with rising voltage of V_{DD}. Therefore, the output terminal of inverter keep at 0V and then M_{ESD} will close at the same time. When ESD events happened, the inverter will turn-on then the M_{ESD} will discharge ESD current.

Although the MOS-based power-rail ESD clamp is used widely before, it is not applicable anymore in advance process. The leakage current of M_{ESD} has become serious in nanoscale process and the problem of gate terminal. The gate of inverter also has leakage problem. Therefore, this work presents a SCR-based power-rail ESD clamp circuit, as shown in Fig. 2.6. The SCR-based power-rail ESD clamp circuit consists of a PNP (P+/N-well/P-well), NPN (N-well/P-well/N+) BJTs and a p-type diode, as shown in Fig. 2.7. In this structure of SCR-based power-rail ESD clamp, the width of SCR and diode all are 150μm. SCR-based power-rail ESD clamp cannot only reduce the layout area but also provide better ESD performance than traditional one [19], [20]. However, SCR have many of problems including latch-up and high trigger-on-voltage. In this work, SCR operates at low-voltage application that can prevent latch-up. SCR is designed two of trigger paths, which are trigger1 and trigger2, as shown in Fig. 2.6 and Fig. 2.7. Appropriate device can help to reduce trigger-on voltage of SCR through trigger paths. Furthermore, SCR parallels the p-type diode that can provide a discharge

path from the V_{SS} terminal. Thus, whole-chip ESD protection circuits can be perfect by adding diode.

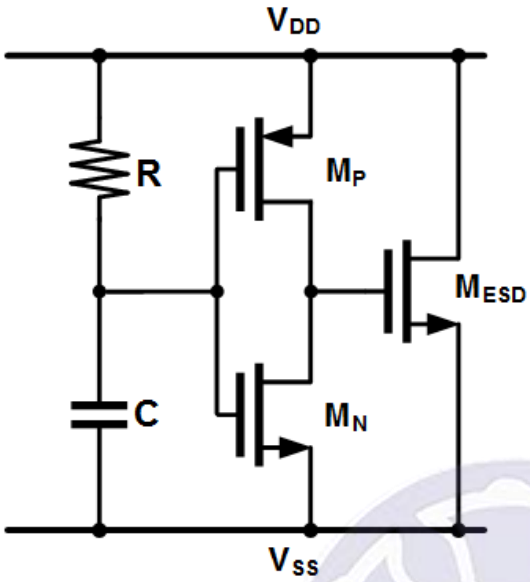


Fig. 2.5. MOS-based power-rail ESD clamp.

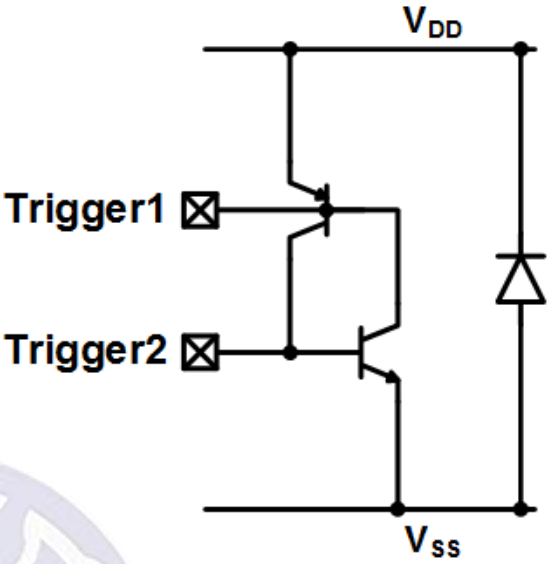


Fig. 2.6. SCR-based power-rail ESD clamp.

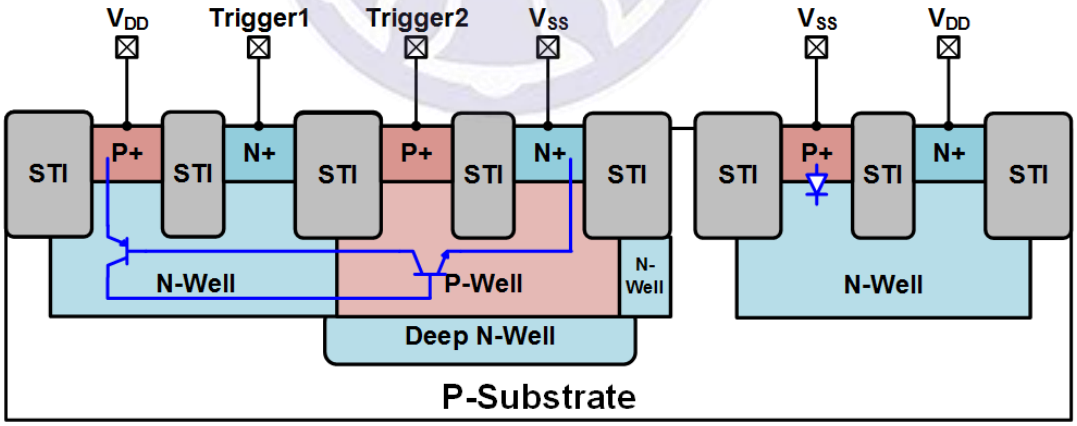


Fig. 2.7. Cross-sectional view of SCR-based power-rail ESD clamp.

2.3 Whole-Chip ESD Protection Circuit

In this work, all of circuits have been presented in a 0.18-μm CMOS. The design concept of whole-chip ESD protection circuit is using different ESD protection device and power-rail ESD clamp to achieve whole-chip ESD protection. Whole-chip ESD protection circuit designs contain prior arts and proposed designs [21]-[23]. All of circuit will be introduced as follows：

2.3.1 Prior Arts

1. Dual Diodes with MOS-Based Power-Rail ESD Clamp (DD_MOS)

In Fig. 2.8, it consists of dual diodes, which connects in series between I/O and V_{DD}/V_{SS} and MOS-based power-rail ESD clamp between V_{DD} and V_{SS}. This traditional ESD protection circuit can fulfill most of ESD robustness needs. When ESD events happened, the diode in series and MOS-based power-rail ESD clamp will provide ESD discharge paths, as shown in Fig. 2.8. Therefore, the internal circuit will not be attacked by ESD current. In normal operation, the ESD protection circuit will not turn on and then it will not affect internal circuit performance. In this work, dual diodes has been design three types of diode sizes. Fig. 2.9 is the layout top view of DD_MOS with different size.

Using ESD protection scheme needs to concern this problem, which is the parasitic capacitance of dual diodes avoids effecting internal performance too much. As a result, next statement will introduce an improving method.

2. Dual Stacked Diodes with MOS-Based Power-Rail ESD Clamp (DSD_MOS)

DSD_MOS is different from the number of diodes. As shown in Fig. 2.10, the purpose of dual stacked diodes is reducing the parasitic capacitance of diodes. In this scheme, the ESD protection circuit of diodes selects by four because it depends on an internal circuit that LNA does not need too much number of diodes in series. If the number of diodes is too much, the turn-on speed will be affected. Unless this ESD protection circuit applies to large swing signal circuit, the number of diodes will not add. In this scheme, DSD_MOS still provides four types of ESD discharging paths, as shown in Fig. 2.10. In this work, DSD_MOS has been design three types of diode sizes. Layout top view of DSD_MOS with different sizes, as shown in Fig. 2.11.

However, prior arts take too much layout area and bring too much loss. In advanced process, these drawbacks of prior arts will bring too much cost. Therefore, novel ESD protection circuit has proposed that uses SCR to replace the MOSFET in power-rail ESD clamp circuit. Next paragraph will introduce proposed designs in detail.

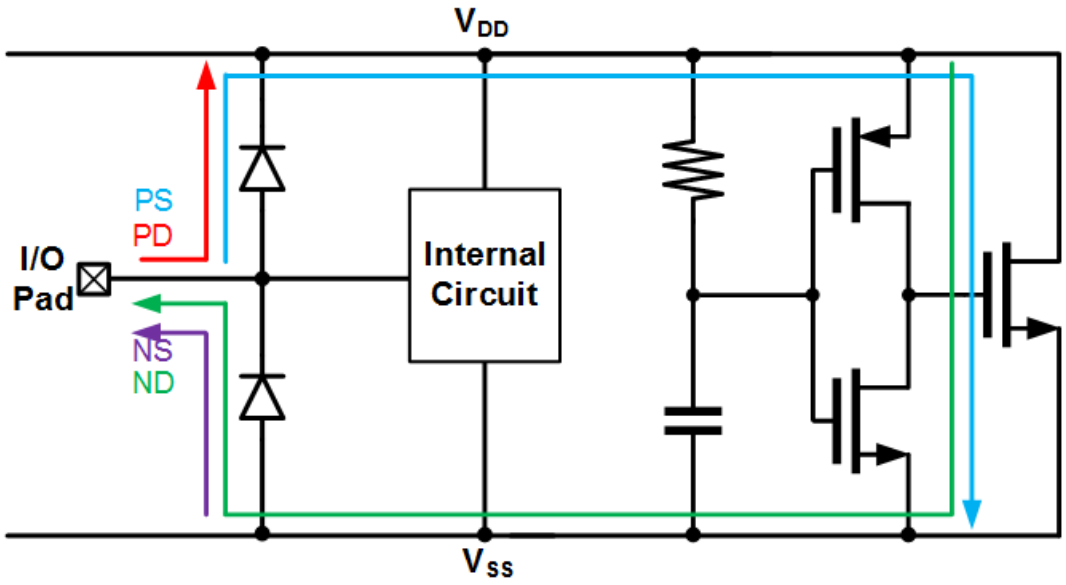
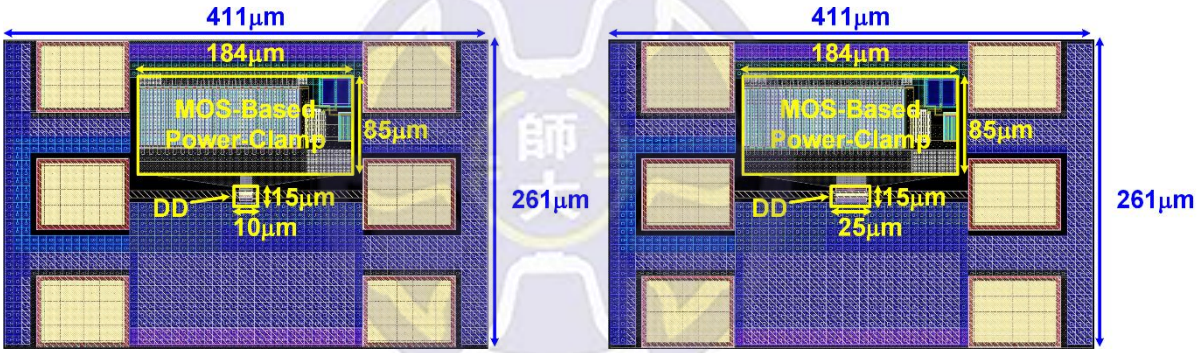
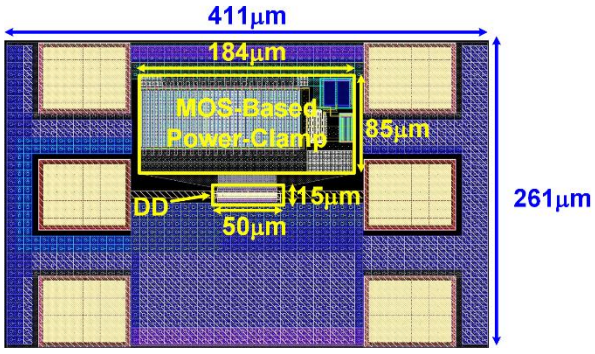


Fig. 2.8. Whole-chip ESD protection circuit of DD_MOS.



(a) (b)



(c)

Fig. 2.9. Layout top view of DD_MOS with (a) 10μm diode width, (b) 25μm diode width, and (c) 50μm diode width.

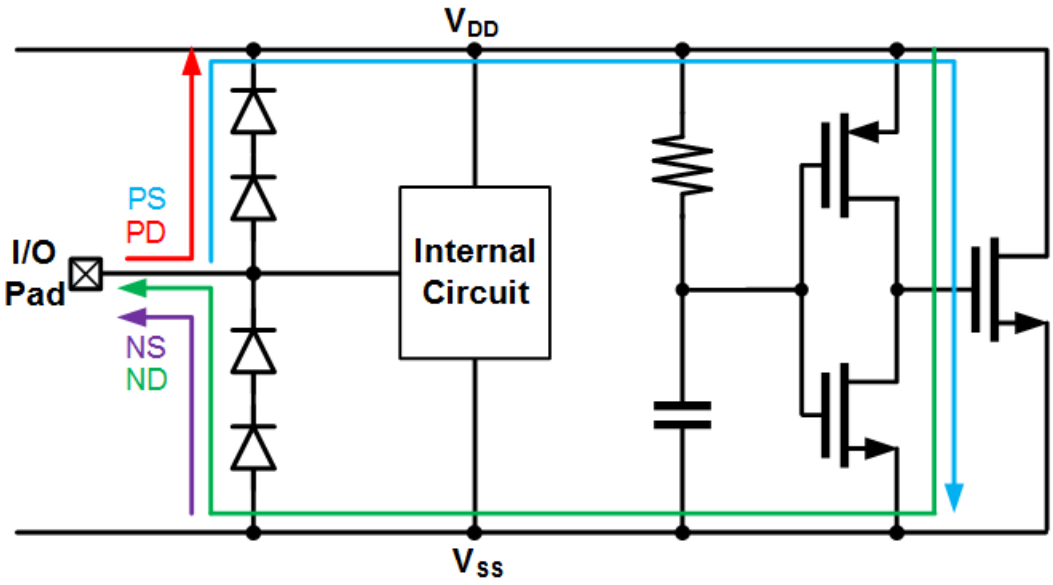
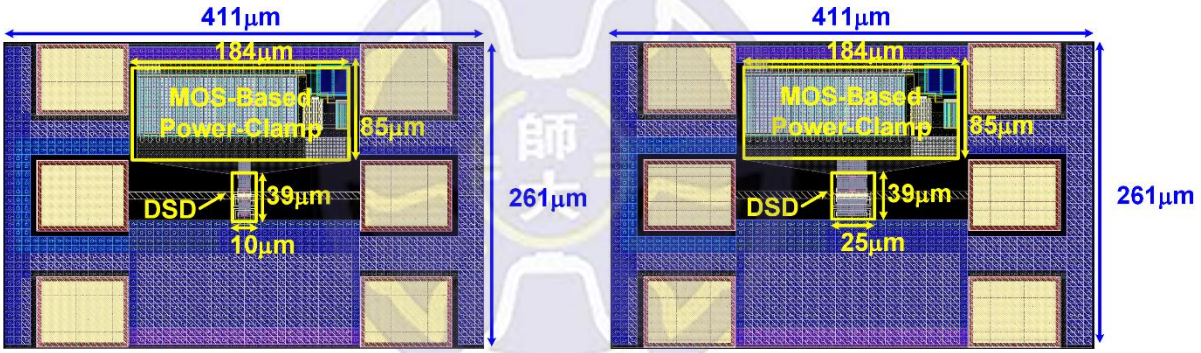
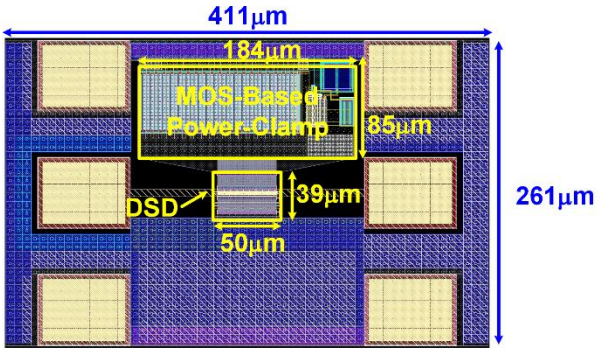


Fig. 2.10. Whole-chip ESD protection circuit of DSD_MOS.



(a) (b)



(c)

Fig. 2.11. Layout top view of DSD_MOS with (a) 10μm diode width, (b) 25μm diode width, and (c) 50μm diode width.

2.3.2 Proposed Designs

1. Dual Stacked Diodes with SCR-Based Power-Rail ESD Clamp (DSD_SCR)

This novel structure has presented in Fig. 2.12. It consists of dual stacked diodes and SCR-based power-rail ESD clamp. SCR needs to equip trigger-diode because of the high turn-on voltage. The trigger-diode selects a p-type diode whose area is smaller than other diodes. The trigger diode's function is that injects enough current into SCR. Under PS-mode and NS mode, the ESD current will discharge through trigger 1 and then the SCR will turn on, as shown in Fig. 2.12. Under PD-mode and ND mode, the ESD current will discharge through trigger 2, as shown in Fig. 2.12. Fig. 2.13 is the layout top view of DSD_SCR with different size.

After all, this scheme still has some room to improve. DSD can use the DSSCR to replace because DSSCR has better ESD performance than DSD. Therefore, next statement will be introduced the improving circuit.

2. DSSCR with SCR-Based Power-Rail ESD Clamp (DSSCR_SCR)

DSSCR has less parasitic effects and better ESD performance. Therefore, DSD has been replace to DSSCR. In Fig. 2.14, the novel design uses DSSCR and SCR-based power-rail ESD clamp. Under PS-mode, the diode series in DSSCR will discharge ESD current early until embedded SCR has been turn-on that will take over the most ESD current. So the main ESD discharge path is by embedded SCR provide. Therefore, ESD protection circuit of DSSCR_SCR has shown in Fig. 2.14. When the embedded SCR of DSSCR turns on, the ESD current will flow into trigger diode and then trigger the SCR-based power-rail ESD clamp. In this structure, it combines small layout area and low parasitic capacitance advantages. In next paragraph, all of measurement data will be introduced. In this work, ESD protection circuits have design with three types of sizes. Fig. 2.15 is the layout top view of DSSCR_SCR with different size.

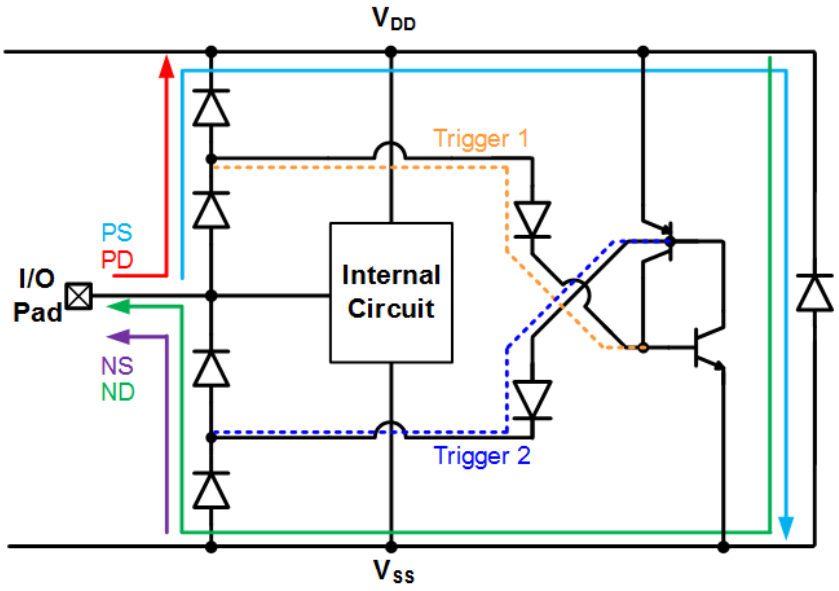
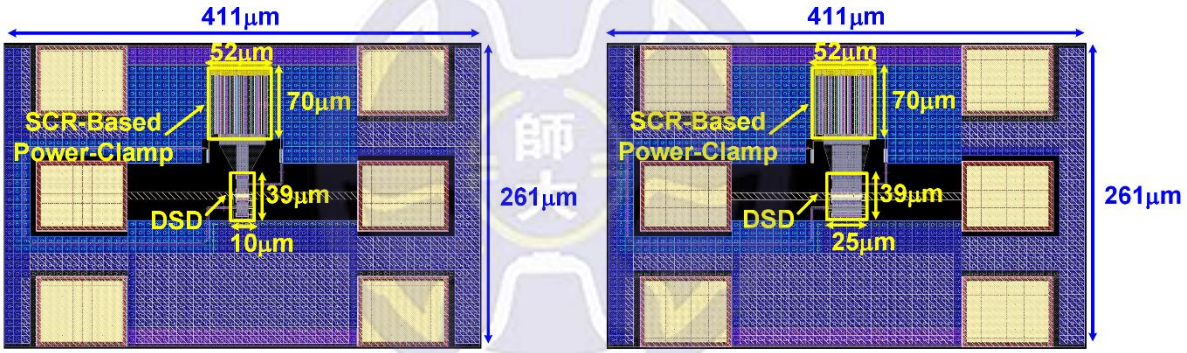
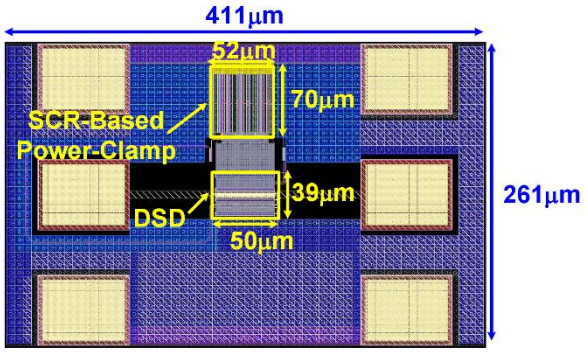


Fig. 2.12. Whole-chip ESD protection circuit of DSD_SCR.



(a) (b)



(c)

Fig. 2.13. Layout top view of DSD_SCR with (a) 10μm diode width, (b) 25μm diode width, and (c) 50μm diode width.

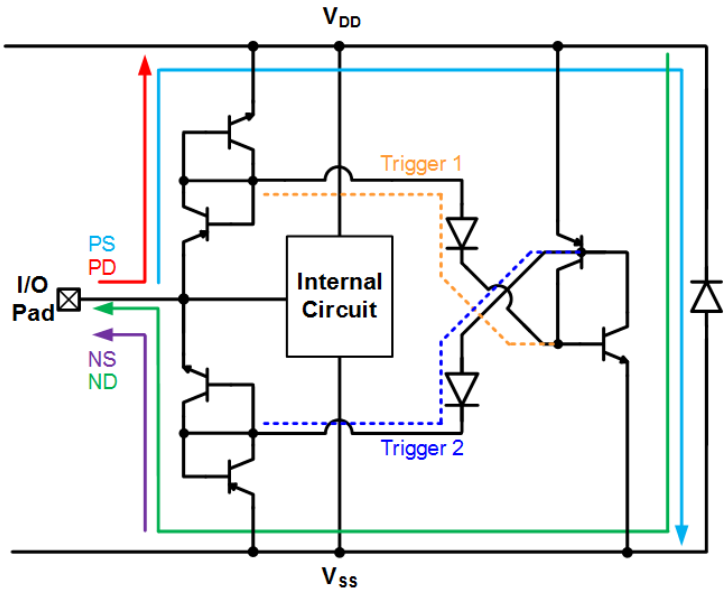
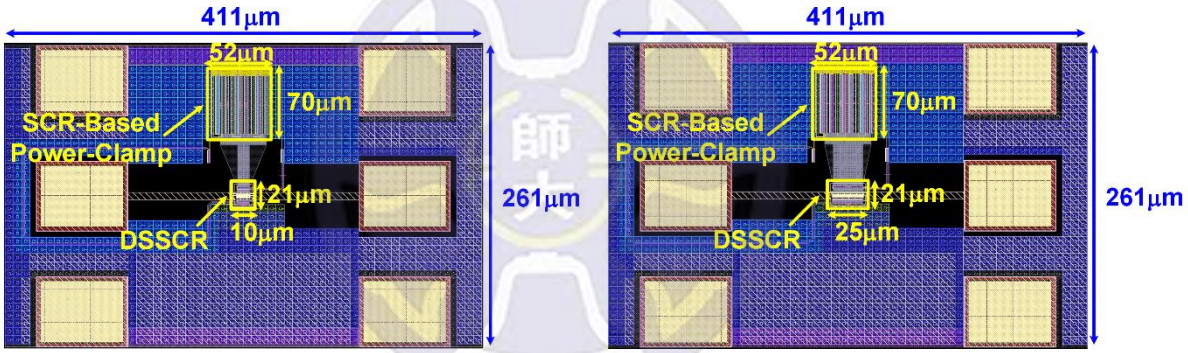
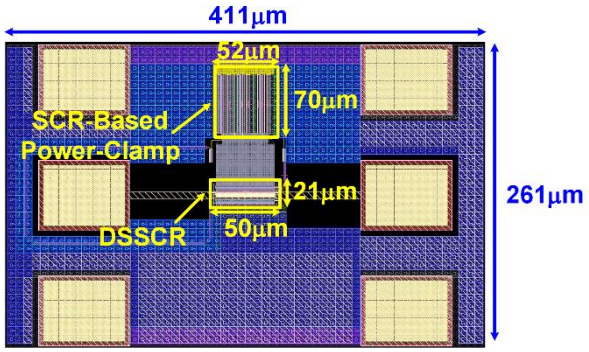


Fig. 2.14. Whole-chip ESD protection circuit of DSSCR_SCR.



(a) (b)



(c)

Fig. 2.15. Layout top view of DSSCR_SCR with (a) 10μm diode width, (b) 25μm diode width, and (c) 50μm diode width.

2.4 Experimental Results

Fig. 2.16 shows the chip photo of ESD protection circuit. All of circuit have been fabricated in a 0.18-μm CMOS process. Total area of ESD protection circuits is 3002 × 542 μm^2. There are fourteen ESD protection circuits, including four types of ESD protection with different sizes and de-embedding circuits. Next, measurement methods and results will be introduced in this section.

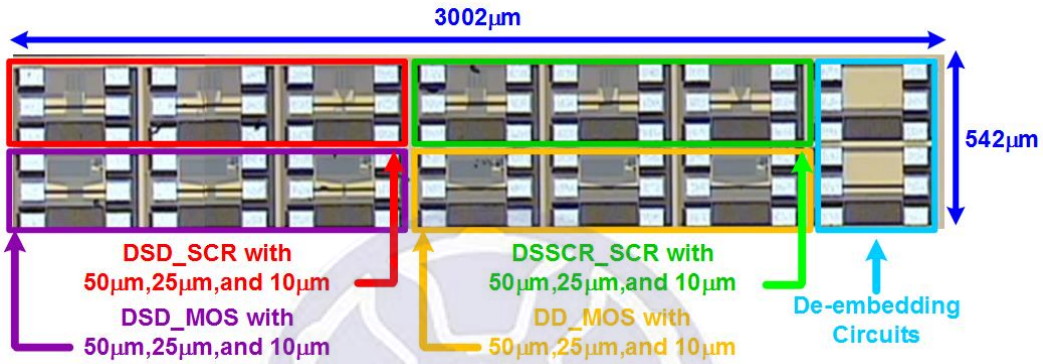


Fig. 2.16. Photograph of ESD protection circuits.

2.4.1 High-Frequency Performances

The high-frequency measurement of all ESD protection circuits is on-wafer measurement with 2-port GSG probes. For the sake of extracting the characteristics of ESD protection circuits, the de-embedding technique is used [24]-[26]. After that, the loss value of circuits can be learned. As shown in Fig. Fig. 2.17 (a) to Fig. 2.17 (c), loss of proposed designs are lower than traditional circuits. At 24 GHz, loss of DD_MOS with 50μm diode width is 3.99dB, DSD_MOS with 50μm diode width is 2.1dB, DSD_SCR with 50μm diode width is 1.05dB, and DSSSCR_SCR with 50μm diode width is 0.98dB. Next, the parasitic capacitance of circuit can be also known by de-embedding technique. Fig. 2.17 (d) to Fig. 2.17 (f) show capacitance values of ESD protection circuits. Hence, proposed designs can reduce loss effort of internal circuit with ESD protection circuit. Table 2.1 illustrates measurement results of circuit.

The dual diodes will have higher loss and capacitance than that of dual stacked diodes. According to the effect of series-structure, dual stacked diodes can reduce the capacitance significantly. In Fig. 2.17, the DD_MOS have worse loss and higher capacitance than those of other circuits.

Generally, the main reason of leading loss is the ESD protection circuits from V_{DD}-to-I/O and I/O-to-V_{SS}. The power-rail ESD clamp from V_{DD}-to-V_{SS} will not bring too much loss to internal circuit in the normal condition. For the sake of layout planning, the V_{DD} of each ESD protection circuits is floating in this work. The floating-V_{DD} results in the effect of power-rail ESD clamp. Therefore, the gate-oxide capacitance of MOS-based power-rail ESD clamp will affect the loss. In Fig. 2.17, the loss of DSD_MOS and DSD_SCR can know the effect of different power-rail ESD clamp circuits. SCR-based power-rail ESD clamp has less loss than that of MOS-based power-rail ESD clamp. There is a same situation in capacitance performance. For the sake of gate-oxide capacitance of MOS-based power-rail ESD clamp, the capacitance of DSD_MOS will be higher than that of DSD_SCR.

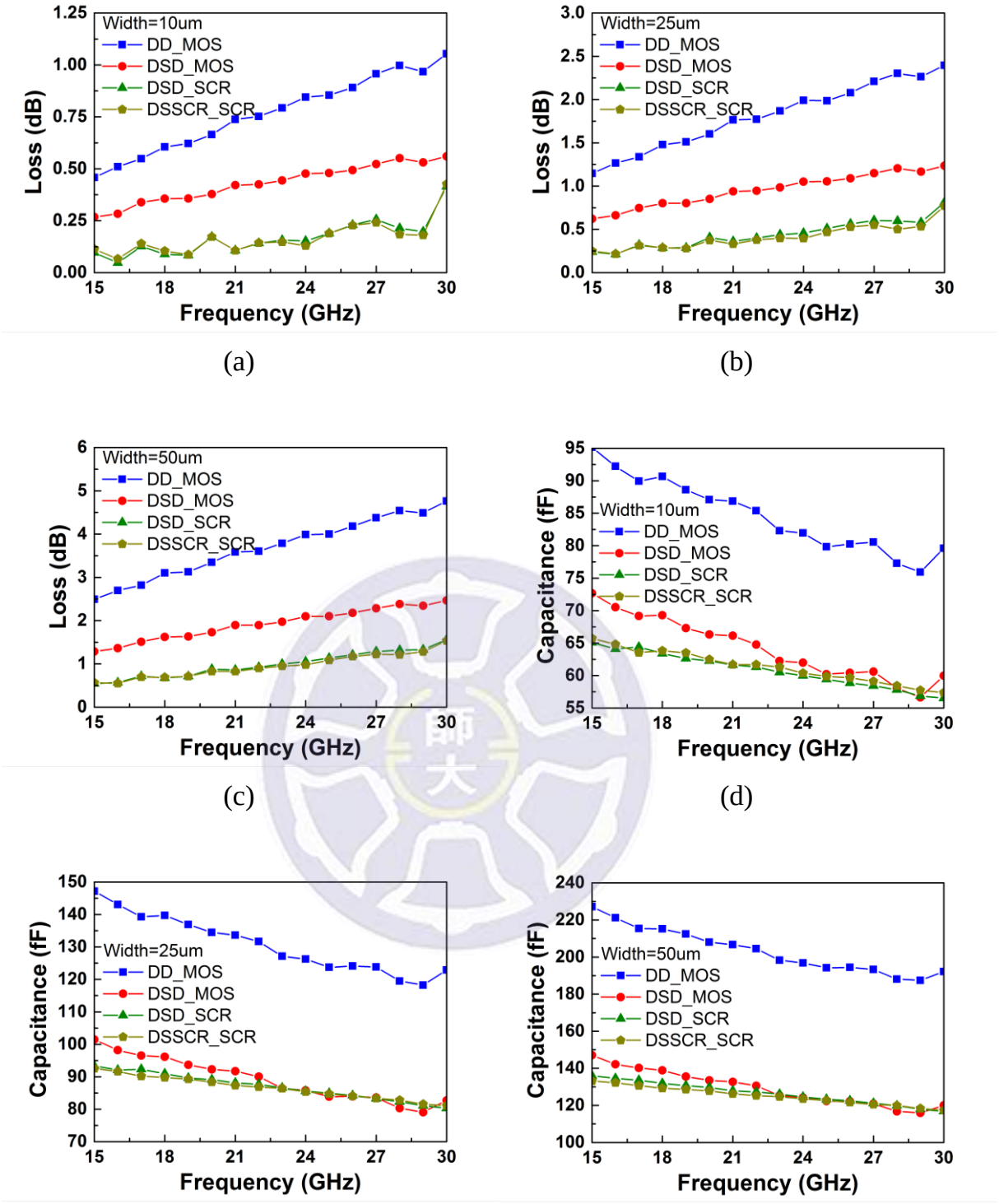


Fig. 2.17. Measured Loss of ESD protection circuit with (a) 10μm diode width, (b) 25μm diode width, and (c) 50μm diode width; measured capacitance of ESD protection circuit with (d) 10μm diode width, (e) 25μm diode width, and (f) 50μm diode width.

Table 2.1

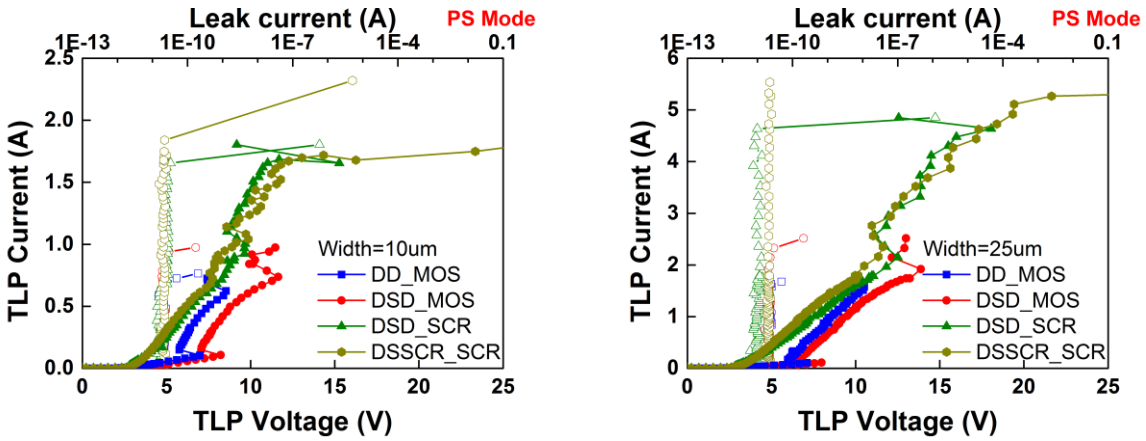
Measured loss and parasitic capacitance of ESD protection circuits.

Cell Name	**Diode Width (μm)**	**Loss (dB) at 24GHz**	**C (fF) at 24GHz**
DD_MOS	10	0.85	81.9
	25	1.99	126.2
	50	3.99	196.8
DSD_MOS	10	0.48	61.9
	25	1.05	85.7
	50	2.1	124.2
DSD_SCR	10	0.15	59.9
	25	0.46	85.5
	50	1.05	124.5
DSSCR_SCR	10	0.13	60.3
	25	0.4	85.3
	50	0.98	123.4

2.4.2 TLP I-V Curves

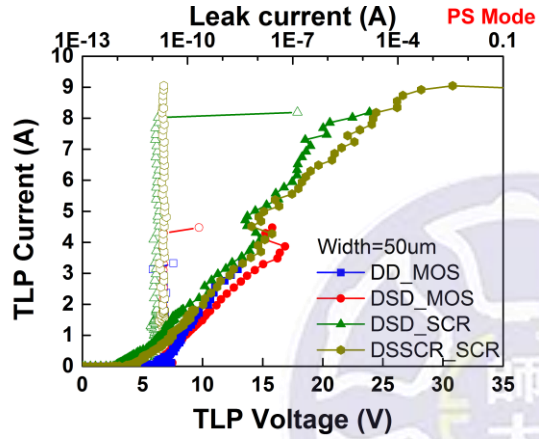
To measure the component's I-V characteristics uses the transmission-line-pulse (TLP) system without package. Fig. 2.18 (a) to Fig. 2.18 (c) are I-V curves of ESD protection circuits under PS mode and Fig. 2.18 (d) to Fig. 2.18 (f) are I-V curves of ESD protection circuits under NS mode. Under PS mode of measurement results, I_{t2} value of proposed designs are higher than traditional designs. Nevertheless, I_{t2} value of DSD_MOS is almost same as DSD_SCR and DSSCR_SCR under NS mode. Novel designs still have better ESD performance than conventional designs.

In this essay, the failure criterion is defined as the leakage current shifting over 30%.



(a)

(b)



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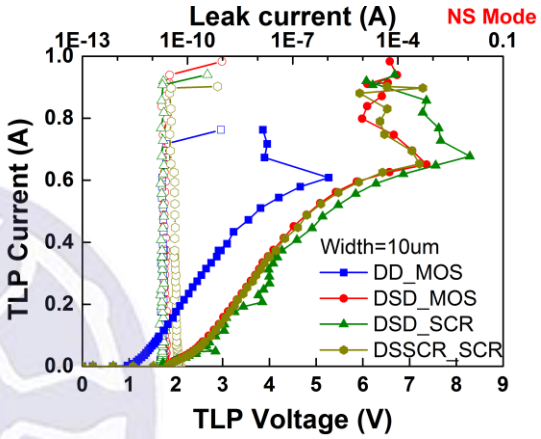

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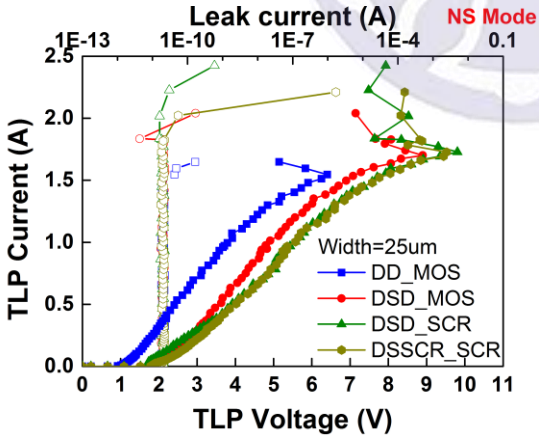
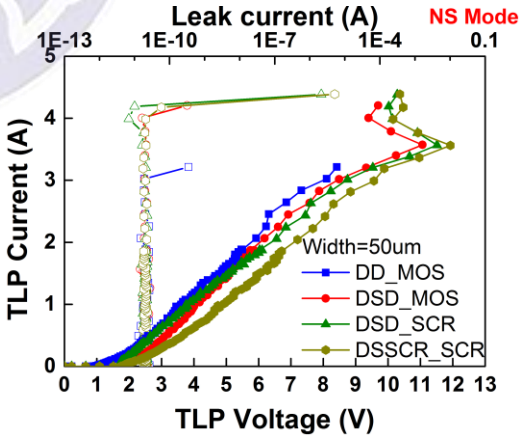


(e)



(f)

Fig. 2.18. Measured TLP I-V characteristic of ESD protection circuit with (a) 10μm diode width, (b) 25μm diode width, and (c) 50μm diode width under PS mode; Measured TLP I-V characteristic of ESD protection circuit with (d) 10μm diode width, (e) 25μm diode width, and (f) 50μm diode width under NS mode.

2.4.3 HBM Measurement Results

Using the ESD tester measures ESD robustness of ESD protection circuit after knowing the I_{t2} of circuit. In this essay, the failure criterion is defined as the leakage current shifting over 30%. The ESD robustness increases as width of diode increases. All measurement results show in table2.2. The layout area of proposed ESD protection circuit is also an outstanding advantage than conventional designs. At 50μm diode width, the layout area of DD_MOS is 0.0164mm^2, DSD_MOS is 0.0176mm^2, DSD_SCR is 0.0053mm^2, and DSSCR_SCR is 0.0044mm^2, respectively. Obviously, the layout area of novel design has reduced drastically.

Table 2.2

Measured TLP and HBM results of ESD protection circuits.

Cell Name	**Diode Width (μm)**	**Layout Area (mm^2)**	**I_{t2} (A)**		**HBM (kV)**	
			PS	**NS**	**PS**	**NS**
DD_MOS	10	0.0157	0.72	0.76	1	1
	25	0.016	1.75	1.64	2	2
	50	0.0164	3.9	3.42	5	5
DSD_MOS	10	0.016	0.97	0.98	1	1
	25	0.0166	2.5	1.83	3	3
	50	0.0176	4.29	4.2	5	6
DSD_SCR	10	0.0037	1.65	1.02	2	1
	25	0.0043	4.63	2.42	3	3
	50	0.0053	8.02	4.19	7	6
DSSCR_SCR	10	0.0035	1.83	1.01	2	1
	25	0.0039	5.5	2.02	3	3
	50	0.0044	8.3	4.17	8	6

2.4.4 CDM Measurement Results

CDM measurement results of ESD protection circuits are measured by using non-socketed CDM test. In non-socketed CDM test, the field-induced method has been used. CDM measurement results of positive and negative are illustrated in Table 2.3. All of CDM results pass the 400V that also pass the industry requires. In this essay, the maximum value of CDM measurement is ±1000V. In positive CDM measurement results, proposed designs are better than conventional designs. At 10μm diode width, the positive CDM of DD_MOS is 400V, DSD_MOS is 500V, DSD_SCR is 500V, and DSSCR_SCR is 600V, respectively. Besides the DD_MOS with 25μm diode width, others positive CDM results are >1000V. In negative CDM measurement results, prior arts are better than proposed designs. However, at 10μm diode width, the negative CDM of DD_MOS is -500V, DSD_MOS is -500V, DSD_SCR is -600V, and DSSCR_SCR is -700V, respectively. Proposed designs have high ESD robustness under positive CDM.

Table 2.3

Measured CDM results of ESD protection circuits.

Cell Name	**Diode Width (μm)**	**CDM (V)**	
		Positive	**Negative**
DD_MOS	10	400	-500
	25	900	<-1000
	50	>1000	<-1000
DSD_MOS	10	500	-500
	25	>1000	<-1000
	50	>1000	<-1000
DSD_SCR	10	500	-600
	25	>1000	-700
	50	>1000	-800
DSSCR_SCR	10	600	-700
	25	>1000	-700
	50	>1000	-700

2.4.5 Leakage

To measure the leakage of ESD protection circuit is at 25°C, 75^{0}C, 100^{0}C, and 125^{0}C, respectively. In this measurement results, the operating voltage is 0.8V, the diode width of ESD protection circuit is 25μm and the leakage path of ESD protection circuit is I/O-to-V_{SS}. Table 2.4 shows the leakage of ESD protection circuit at operating voltage. Proposed designs are better than conventional designs; DSSCR_SCR is the most outstanding ESD protection circuit, especially. At 125^{0}C, the leakage current of DD_MOS is 53nA, DSD_MOS is 117nA, DSD_SCR is 8nA, and DSSCR_SCR is 5.5nA, respectively. To sum up, the temperature influence of proposed designs is less than conventional designs

In this work, the V_{DD} of ESD protection circuits is floating. Therefore, there will be an additional leakage current from MOS-based power-rail ESD clamp. In table 2.4, the leakage current of each ESD protection circuit is all overestimated. Nevertheless, leakage currents of proposed designs are still better than those of prior art.

Table 2.4

Measured leakage current of ESD protection circuits.

Cell Name	**Leakage Current (nA) at 0.8V**			
	25^{0}C	**75^{0}C**	**100^{0}C**	**125^{0}C**
DD_MOS	0.012	2.4	11.8	53
DSD_MOS	0.022	5.3	27	117
DSD_SCR	0.014	0.673	2	8
DSSCR_SCR	0.013	0.214	1.14	5.5

2.4.6 Comparison

In this statement, a series of comparison considers a verity of parameters and measurement results. To analyze these comparisons learns each of ESD protection circuit performances.

Table 2.5 shows three types of equations, which consider HBM robustness, layout area, capacitance, loss. The first equation is HBM/layout area. HBM measurement results include PS mode and NS mode. The diode width of each circuits is 50μm as follows: Under PS mode, the HBM/layout area of DD_MOS is 305, DSD_MOS is 284, DSD_SCR is 1326, and DSSCR_SCR is 1827, respectively. Proposed designs, which are DSD_SCR and DSSCR_SCR, have higher HBM robustness at unit area, even though measurement results select NS mode. Next, comparing HBM robustness at unit capacitance uses HBM/capacitance in table 2.5. Under PS mode, HBM/capacitance of DD_MOS is 2.54, DSD_MOS is 4.02, DSD_SCR is 5.62, and DSSCR_SCR is 6.67 and, respectively. Proposed designs can provide better HBM robustness effectively at unit capacitance. Measurement results of NS mode are the same situation that proposed designs have better performance than prior arts. Last, the last equation is HBM/loss. Under PS mode, HBM/loss of DD_MOS is 1.25, DSD_MOS is 2.39, DSD_SCR is 6.67 and DSSCR_SCR is 8.16 and, respectively. Proposed designs, which select HBM/loss of NS mode, are better than prior arts.

In sum, proposed designs have greater performance than prior arts, as shown in table 2.5.

Table 2.5

Compared HBM robustness with different parameters.

Cell Name	Diode Width (μm)	HBM / Layout Area (kV/mm^2)		HBM / Capacitance (10^{-2}kV/fF)		HBM / Loss (kV/dB)	
		PS	NS	PS	NS	PS	NS
DD_MOS	10	63	63	1.22	1.22	1.18	1.18
	25	124	124	1.58	1.58	1.01	1.01
	50	305	305	2.54	2.54	1.25	1.25
DSD_MOS	10	62.4	62.4	1.62	1.62	2.08	2.08
	25	181	181	3.5	3.5	2.86	2.86
	50	284	341	4.02	4.83	2.39	2.86
DSD_SCR	10	538	269	3.39	1.67	13.33	6.67
	25	697	697	3.51	3.51	6.52	6.52
	50	1326	1136	5.62	4.82	6.67	5.71
DSSCR_SCR	10	565	283	2.92	1.46	15.4	7.69
	25	779	779	3.62	3.62	7.5	7.5
	50	1827	1370	6.67	5	8.16	6.12

Table 2.6 shows three types of equations, which consider CDM robustness, layout area, capacitance, and loss. There are two types of CDM measurement results, which are under positive and negative ESD stresses. The first equation is CDM/layout area that means CDM performance at unit area. Under positive CDM stresses, the CDM/layout of DD_MOS is over 60.6, DSD_MOS is over 55.9, DSD_SCR is over 182, and DSSCR_SCR is over 222, respectively. Proposed designs have higher CDM performance at unit area than prior arts whichever the type chosen. Next, the second equation is CDM/capacitance, which means CDM robustness at unit capacitance. Under positive CDM stresses, CDM/capacitance of DD_MOS is over 5.08, DSD_MOS is over 8.06, DSD_SCR is over 8.03, and DSSCR_SCR is over 8.33. Proposed designs can

provide better CDM performance at unit capacitance than prior arts. Last, the last equation is CDM/loss, which means CDM robustness at unit loss. Under positive CDM stresses, CDM/loss of DD_MOS is over 251, DSD_MOS is over 476, DSD_SCR is over 952, and DSSCR_SCR is over 1020. In brief, proposed designs have better CDM performance than prior arts through table 2.6.

As mentioned previously, proposed designs not only perform greater HBM/CDM robustness at area efficiency but also provide better HBM/CDM robustness at unit capacitance or loss.

Table 2.6

Compared CDM robustness with different parameters.

Cell Name	**Diode Width (μm)**	**CDM / Layout Area (kV/mm²)**		**CDM / Capacitance (V/fF)**		**CDM / Loss (V/dB)**	
		Positive	**Negative**	**Positive**	**Negative**	**Positive**	**Negative**
DD_MOS	10	25	-32	4.88	-6.11	471	-588
	25	55	<-62	7.13	<-7.92	452	<-503
	50	>61	<-61	>5.08	<5.08	>251	<-251
DSD_MOS	10	31	-31	8.08	-8.08	1041	-1041
	25	>60	<-60	>11.7	<-11.7	>952	<-952
	50	>57	<-57	>8.06	<-8.06	>476	<-476
DSD_SCR	10	134	-161	8.35	-10	3333	-4000
	25	>232	-162	>11.7	-8.18	>2173	-1521
	50	>189	-151	>8.03	-6.43	>952	-761
DSSCR_SCR	10	170	-198	8.76	-10.2	4615	-5384
	25	>260	-182	>12.1	-8.45	>2500	-1750
	50	>228	-160	>8.33	-5.83	>1020	-714

2.5 Summary

Proposed protection circuits have been demonstrated in silicon chip. Through a series of measurements, proposed designs, which are DSD_SCR and DSSCR_SCR, can provide better performance than prior arts. In high-frequency performance, proposed designs have low loss and low capacitance that will be helpful to RF circuit application. In HBM performance, proposed designs have higher HBM robustness than prior arts. In CDM performance, proposed designs also have higher CDM robustness under positive-level. In brief, proposed designs have greater ESD performance than prior arts. In leakage measurement results, proposed designs have low leakage current that will be helpful for reducing power consumption of circuits. In layout area, proposed designs occupies less area than prior arts significantly.

To sum up, proposed designs can achieve high ESD robustness, low loss, low parasitic capacitance, low layout area, and low leakage current at high temperature. It is very helpful for ESD protection designs, especially in the advanced process.

Chapter 3

24-GHz Low-Noise Amplifier

3.1 Introduction

A variety of consumer electronic products include automotive radar, automotive electronic and satellite communications all apply in K-band. Fig. 3.1 shows the transceiver system of architecture. In receive system, the low-noise amplifier is a key circuit of receiver system. LNA cannot only provide enough gain to amplify the RF signal, which is received from antenna but also reduce the noise of the whole system. LNA can improve the signal to noise ratio (SNR) of signal and then signal transfer to next stage correctly.

In this essay, the design step of 24-GHz LNA will be introduced in detail.

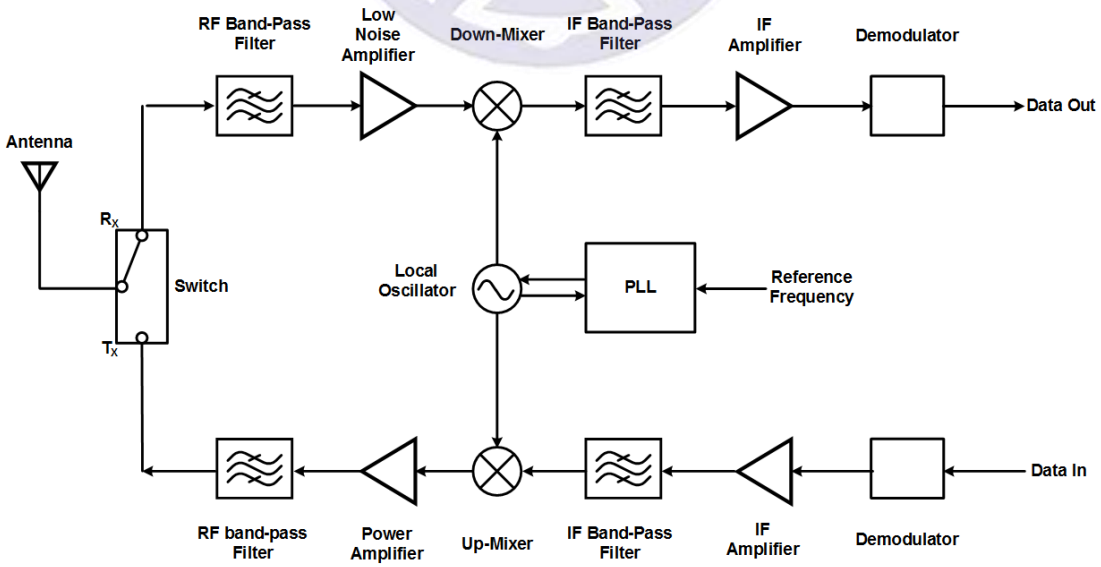


Fig. 3.1. Transceiver architecture.

3.2 Transistor Noise Sources

Generally, the transistor element noise can be classified into two categories: external noise and component internal thermal noise. The noise is a random signal, not cyclical. Even if the noise is known in the past, the exactly noise value still cannot be predicted. There are many types of noises, such as thermal noise, transistor gate noise and flicker noise. In this statement, different types of noises will be illustrated [27]-[29].

3.2.1 Thermal Noise

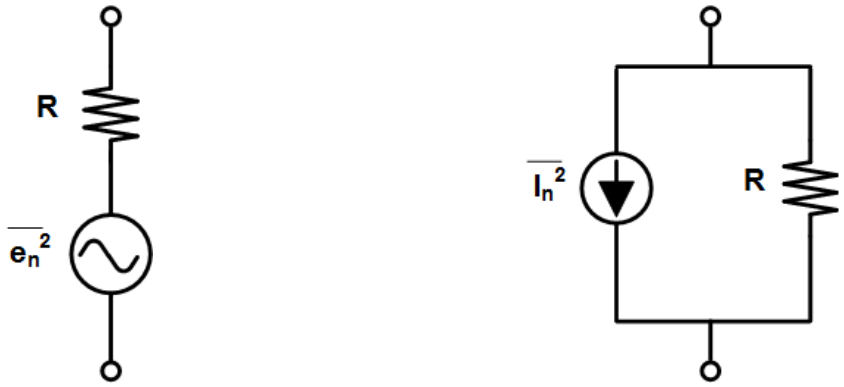
Thermal noise is also known as Johnson noise or Nyquist noise. The charge carrier in the conductor will form a varying current due to random thermal motion result in forming a random voltage. The thermal noise of resistor can be expressed by a series voltage source, as shown in Fig. 3.2 (a). The mean-square noise voltage can be expressed as

$$\overline{e_n{}^2} = 4kTR\Delta f \quad (3\text{-}1)$$

where k is the Bolzmann constant, and T is the absolute temperature, and the Δf is noise bandwidth. The mean-square noise voltage will be proportional to the absolute temperature.

The thermal noise of resistor can be represented by a parallel current source, as shown in Fig. 3.2 (b). The mean-square noise current can be expressed as

$$\overline{I_n{}^2} = \frac{\overline{e_n{}^2}}{R^2} = \frac{4kT\Delta f}{R} \quad (3\text{-}2)$$



(a) (b)

Fig. 3.2. Thermal noise model of (a) a voltage source (b) a current source.

When the transistor is operating in the saturation region, the channel electron will form a random current and voltage due to thermal excitation, which also called the channel thermal noise. This equivalent noise circuit shown in Fig. 3.3. The mean-square noise current can be expressed as

$$\overline{I_n^2} = 4kT\gamma g_m \quad (3\text{-}3)$$

Where γ is 2/3 in long channel transistor, and γ is over 1 in short channel transistor, and gm is transconductance of MOSFET.

According to the formula, the thermal noise can be expressed as

$$\overline{V_{n,out}^2} = 4kT\gamma g_m r_o^2 \quad (3\text{-}4)$$

where r_o is small signal impedance.

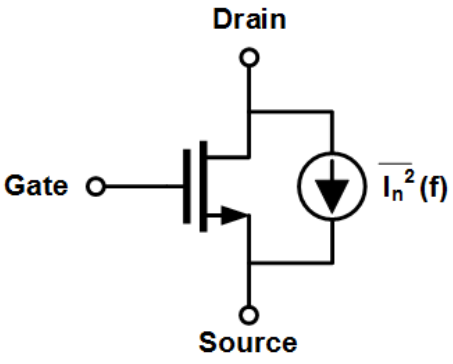


Fig. 3.3. Thermal noise model of transistor.

3.2.2 MOSFET Gate Resistance Noise

The transistor gate layout must use poly in CMOS process, result in transistors exist polysilicon resistance, as shown in Fig. 3.4. The resistance value is expressed as follows

$$R_g = \frac{R_g W}{3n^2 L} \quad (3\text{-}5)$$

where R_h is a poly resistance ,and n is the number of multi-finger and L is the channel length of transistor ,and W is the channel width of transistor.

The thermal noise can be expressed as

$$\overline{V_{n,out}}^2 = 4kT\frac{R_g}{3}(g_m r_o)^2 \quad (3\text{-}6)$$

According to the formula, using multiple fingers and short channel width of transistor can reduce the gate resistance noise.

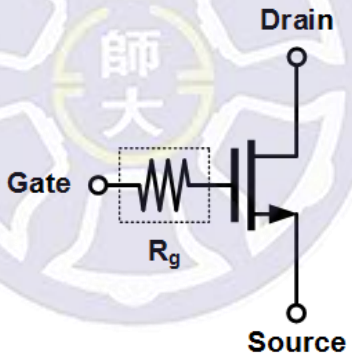


Fig. 3.4. Gate resistance of transistor.

3.2.3 Flicker Noise

There are many discontinuous junctions between the gate-oxide layer and the silicon substrate in the transistor and then that will produce redundant states. When the carrier moves in the interface, some carriers will be captured and generated randomly, resulting in flicker noise, as shown in Fig. 3.5. Flicker noise is also called 1/f noise. The flicker noise is affected by reciprocal frequency, which less effect on high-frequency performance.

The flicker noise can be expressed as

$$\overline{V_{n,out}}^2 = \frac{K}{C_{ox}WL}\frac{1}{f} \quad (3\text{-}7)$$

where K is the process parameter, and Cox is capacitance of gate oxide, and f is frequency.

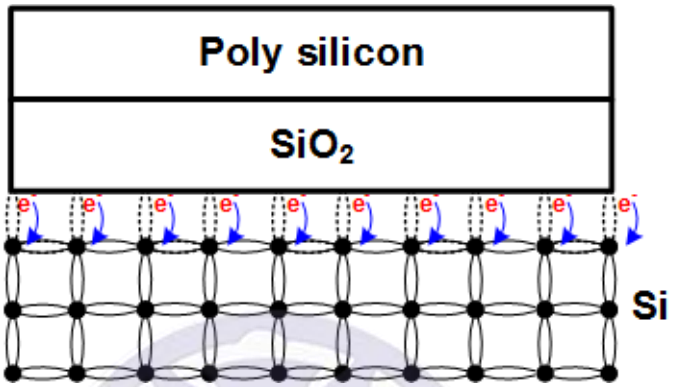


Fig. 3.5. Discontinuous bonding between oxide layer and silicon substrate.

3.3 Parameters of Designing Low-Noise Amplifier

3.3.1 Gain

In the microwave amplifier, the power of different locations will have different gain equation, as shown in Fig. 3.6. They can be classified into three categories:

1. Transducer Power Gain

The transducer power gain (G_T), which calculates the gain from the load to the source usually use in designing the normal RF amplifier. The equation shows as follows

$$G_T = \frac{P_L}{P_A} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \quad (3\text{-}8)$$

2. Available Power Gain

The available power gain (G_A), which calculates the gain from the network to the

source usually use in designing the low-noise amplifier.

$$G_A = \frac{P_{avo}}{P_A} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{|1-\Gamma_{out}|^2} \quad (3\text{-}9)$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{11}\Gamma_L} \quad (3\text{-}10)$$

3. Operating Power Gain

The operating power gain (G_P), which calculates the gain from the load to the source usually use in designing the power amplifier.

$$G_P = \frac{P_L}{P_{in}} = \frac{1}{|1-\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{11}\Gamma_L|^2} \quad (3\text{-}11)$$

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \quad (3\text{-}12)$$

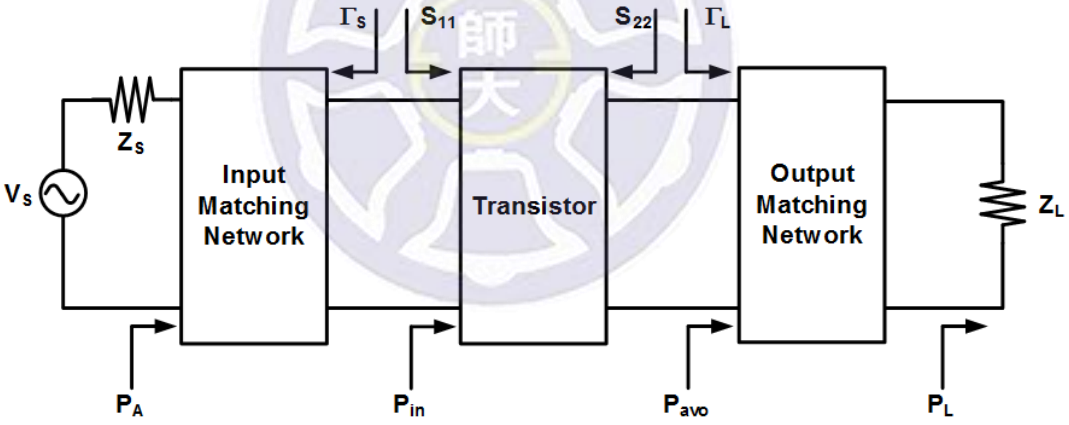


Fig. 3.6. Two-ports network of available power and actual power.

3.3.2 Stability

In designing the amplifier, using the stability factor (K) can determine the circuit whether stable or unstable. When the stability factor (K) >1, the amplifier is unconditionally stable; When the stability factor (K) <1, the amplifier is conditional stability and then we must use a stable circle to determine whether the amplifier is stable.

The flicker noise can be expressed as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (3\text{-}13)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (3\text{-}14)$$

3.3.3 Noise Figure

Noise Figure is defined as the signal noise rate (SNR) of input divided by the SNR of output. For example, the single-stage amplifier has shown in Fig. 3.7.

The noise figure can be expressed as

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{1}{G}\frac{N_{out}}{N_{in}} = \frac{N_a + GN_{in}}{GN_{in}} = 1 + \frac{N_a}{GN_{in}} \quad (3\text{-}15)$$

where S_{in} is input signal, and S_{out} is output signal, and N_{in} is input noise, and N_{out} is output noise, and G is gain, and N_a is the essence noise of circuit.

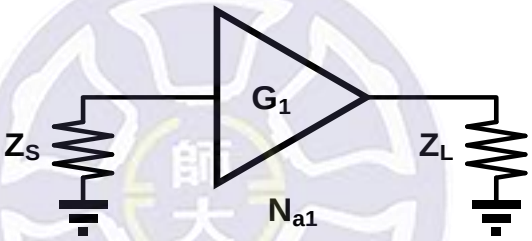


Fig. 3.7. Single-stage amplifier noise model.

Next, the two-stage amplifier has shown in Fig. 3.8. It can be learned that the two-stage circuit noise is the first-stage noise value plus the second-stage noise divided by the first-stage circuit gain.

$$NF = \frac{N_{a2} + G_2N_{a1} + G_1G_2N_{in}}{G_1G_2N_{in}} = 1 + \frac{N_{a1}}{G_1N_{in}} + \frac{N_{a2}}{G_1G_2N_{in}} = NF_1 + \frac{NF_2 - 1}{G_1} \quad (3\text{-}16)$$

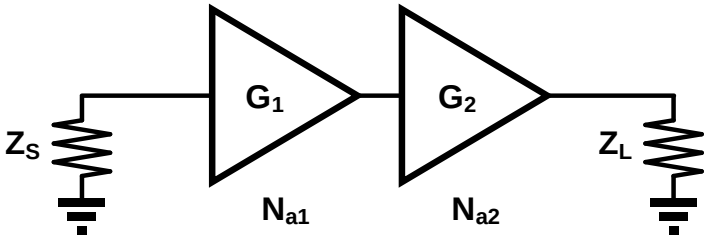


Fig. 3.8. Two-stage amplifier noise model.

Fig. 3.9 shows multistage amplifier circuit. According to the formula (3-16) can deduce the equation (3-17). It can be know that the key of system noise value is the first-stage amplifier noise. The noise of first-stage cannot be divided by subsequent circuit gain. In other words, the first-stage circuit must has low-noise and high gain, which can help reduce system noise

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdots + \frac{NF_N - 1}{G_1 G_2 \ldots G_{N-1}} \quad (3\text{-}17)$$

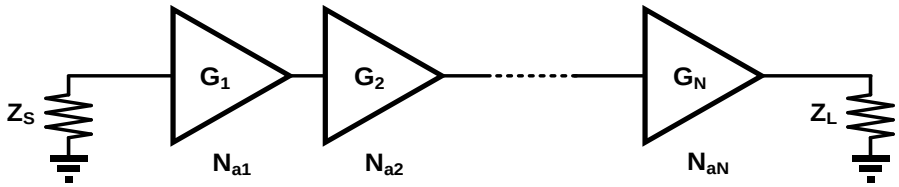


Fig. 3.9. Multistage amplifier noise model.

3.4 Circuit Design Steps

In generally, the architecture of amplifier usually uses the cascade structure or common source structure. Two of structures can raise the gain of circuit effectively. In this essay, choosing the two-stage common source structure to design the 24-GHz LNA [30]-[32]. In this statement, the design steps of 24GHz LNA will be introduced in detail.

3.4.1 Design of Transistor Bias

The first step of circuit design is choosing the bias of transistor. To choice the V_{gs} of transistor needs to consider the transconductance (g_m), the current of drain (I_D), the minimum noise (NF_{min}), and the maximum gain.

When V_{GS} is 0.8V, g_m has become saturation and I_D is gradually increasing, as shown in Fig. 3.10; the max gain has approached saturation and NF_{min} have risen gradually, as shown in Fig. 3.11. Therefore, considering the amplifier must have high

gain, suitable noise, and power consumption. The gate-bias has selected as 0.8V and the maximum voltage value of LNA is 1.2V that can decrease the power consumption.

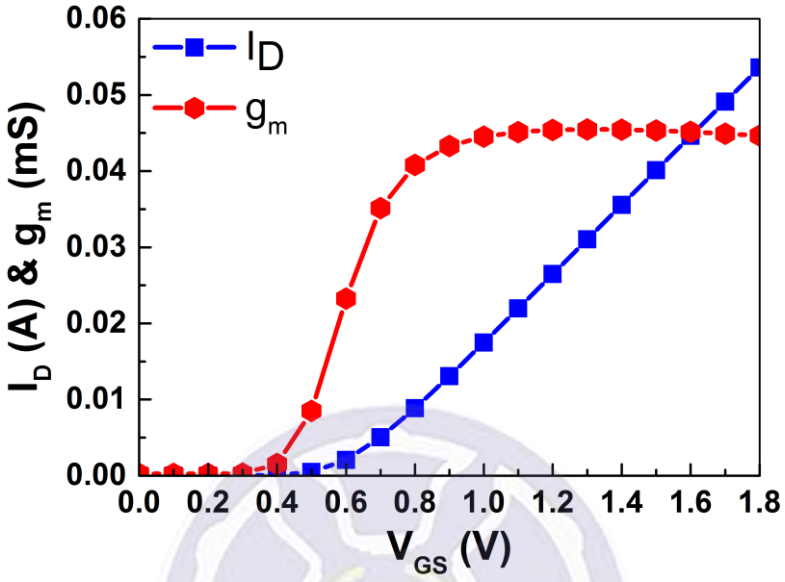


Fig. 3.10. Simulated I_D and g_m of the transistor with various gate-bias.

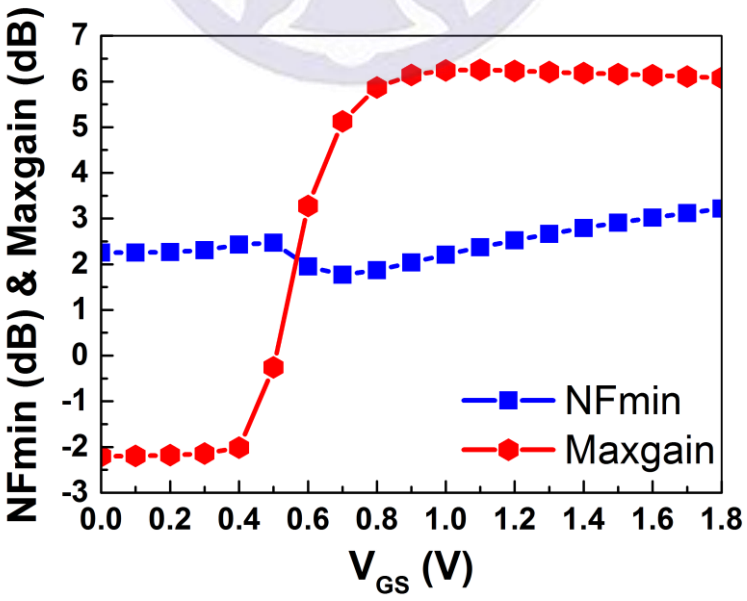


Fig. 3.11. Simulated NFmin and Max gain of the transistor with various gate-bias.

3.4.2 Design of Transistor Size

Next step is selecting the appropriate transistor size, the transistor can adjust the parameters for the channel length, channel width, number of finger. Designing above parameters needs to consider the maximum gain and minimum noise value. In generally, the channel length will choose the minimum value of the process in the circuit design. In this essay, all of circuit have been fabricated in a 0.18-μm CMOS process. Therefore, the channel length is 0.18μm.

Second step is selecting the channel width value. Using the Fig. 3.12 and Fig. 3.13 can choose suitable width value. The max gain will increase slowly as the width increase and then determine the width by the number of finger; The NFmin will increase with as the width increase and then determine the width by the number of finger. According to the Fig. 3.12 and Fig. 3.13, the width is 6μm and the number of finger is 10 that transistor will have high max gain and low NFmin. Therefore, the transistor size has been decided.

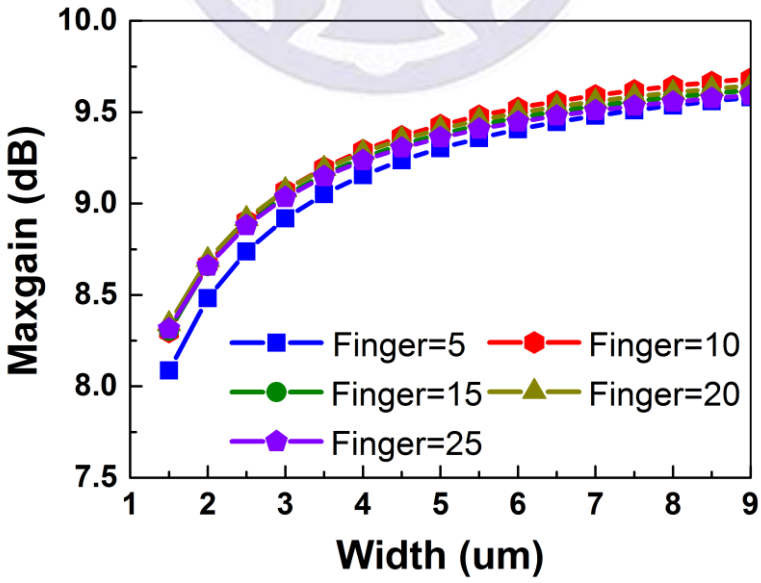


Fig. 3.12. Simulated Max gain of the transistor with various width and fingers.

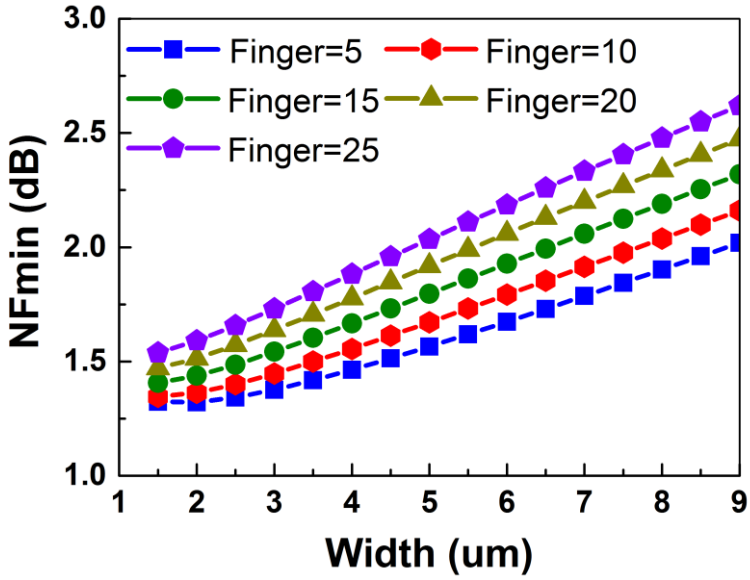


Fig. 3.13. Simulated NFmin of the transistor with various width and fingers.

3.4.3 Design of Source Degeneration Inductor

For the transistor operates at radio frequency, the position of the conjugate match point usually far away from NFmin point on Smith chart. Thus, the matching network matches in the high gain area, which is usually high noise area. In other words, the matching network matches in the low-noise area and the gain is often not high.

It is a difficult thing that achieves high gain and low noise at the same time. In order to solve this problem, the solution is adding an inductor at source, which is called source degradation inductor. It is very common in LNA designs [33], [34]. Although the source degradation inductor will affect the max gain, the position of the matching point on Smith chart will move to the NFmin point. Selecting the appropriate degradation inductor can achieve that the matching point approach the NFmin point without reducing too much transistor gain.

Fig. 3.14 shows the max gain under different inductor value. At 10dB of Max gain, there is a significant turning point. When the degradation-inductance increases, the

turning point will move to low frequency. In order to achieve high max gain, the source degeneration inductor will be selected between 60pH and 90pH in this study.

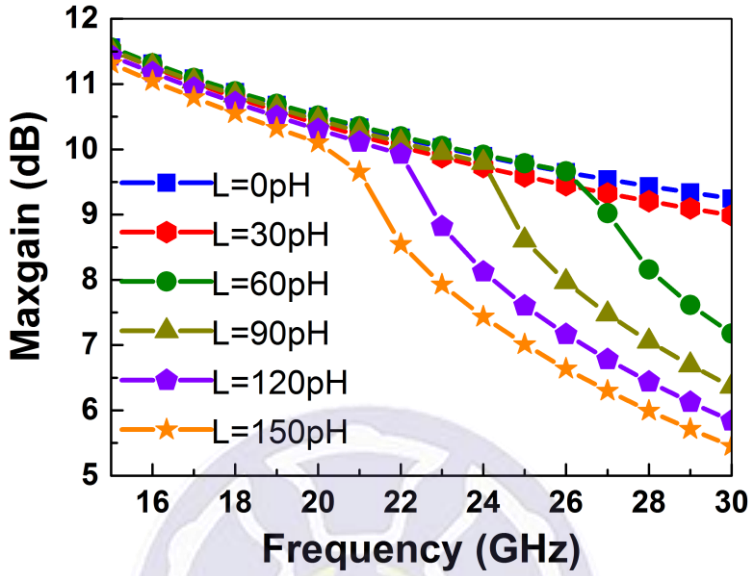


Fig. 3.14. Simulated Max gain of the transistor with various inductor values.

3.4.4 Design of Matching Network

After determining the bias condition, the size of transistor, and the source degeneration inductor, starting to decide the architecture of matching network. Designing the circuit needs to consider stage-to-stage matching including the conjugate match, power match, and noise match as shown in Fig. 3.15. The matching network design will be introduced in this statement.

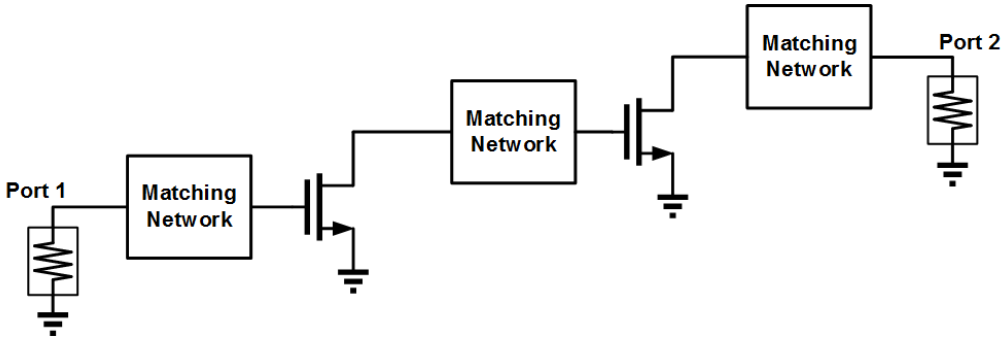


Fig. 3.15. Matching network design.

1. Input-Stage Matching Network

Fig. 3.16 is the input matching circuit. In order to make the amplifier get the lowest noise value, the input-stage needs to make noise match, which is the impedance from the 50Ω to match the NFmin impedance point. Adding the source degradation inductor can let matching point move to the NFmin point closely. The C_1 is the parasitic capacitance of ESD protection circuit. Through a parallel inductor and series inductor, letting the input impedance matches to the NFmin point as shown in Fig. 3.17.

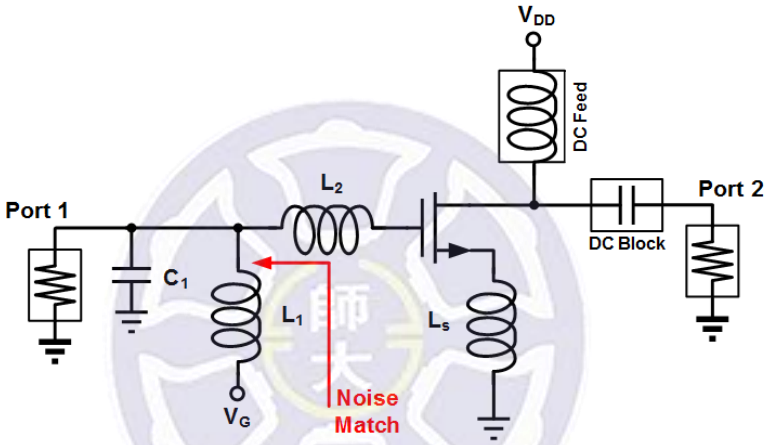


Fig. 3.16. Input-stage matching circuit design.

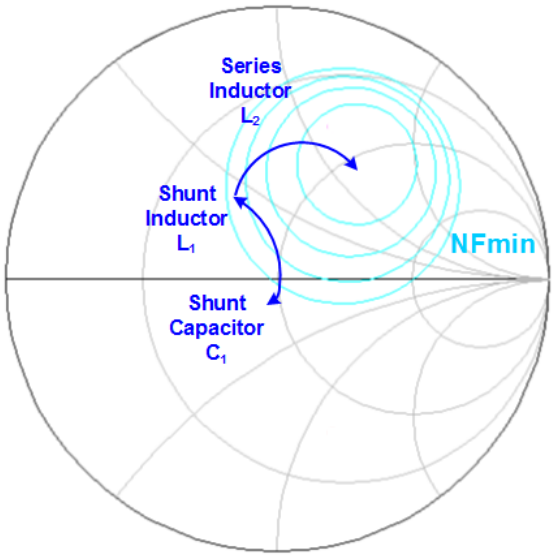


Fig. 3.17. Trace of impedance in input matching network.

2. Stage-to-Stage Matching Network

The stage-to-stage matching network uses the conjugate match between first stage and second stage, as shown in Fig. 3.18. At first, finding out the output return loss (S_{22}) of first stage and the input return loss (S_{11}) of second stage. Next, the stage-to-stage matching is conjugate matching. Fig. 3.19 shows the trace of conjugate matching. Using a parallel inductor matches the conjugate matching that let circuit has the max gain.

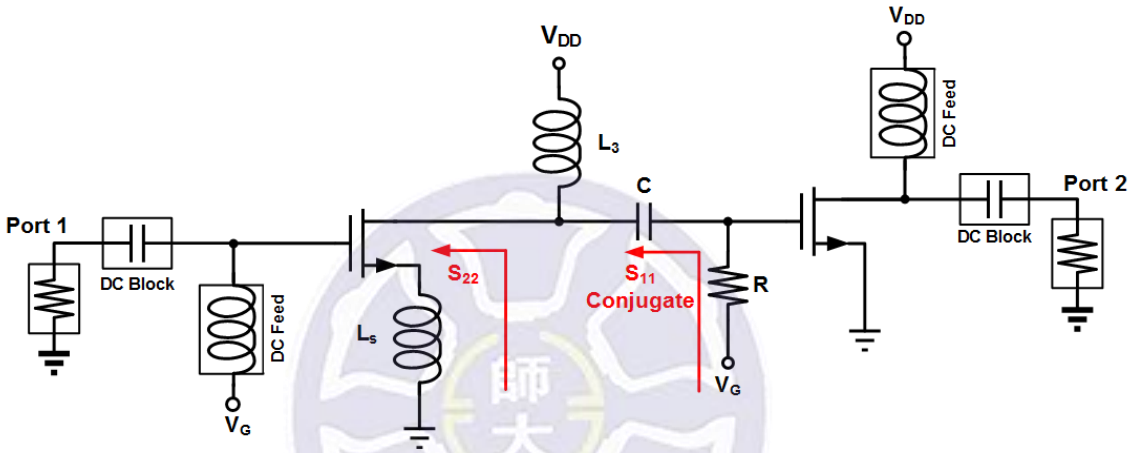


Fig. 3.18. Stage-to-stage matching circuit design.

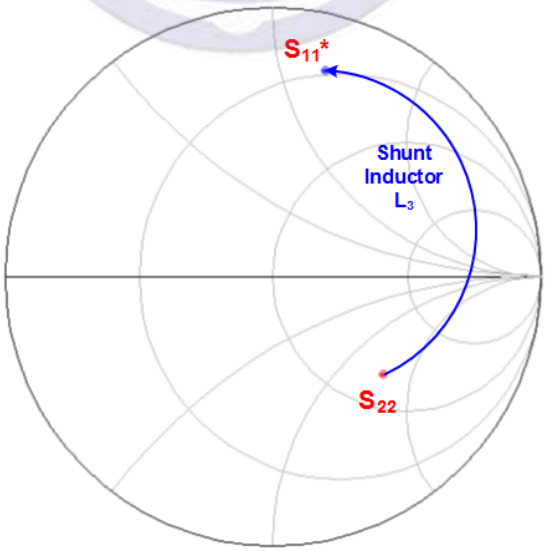


Fig. 3.19. Trace of impedance in stage-to-stage matching network.

3. Output-Stage Matching Network

In order to do the output impedance matching, it must to find out the output return loss (S_{22}) of second stage. Output-stage matching network uses the conjugate match between 50Ω of output and the S_{22} of second stage, as shown in Fig. 3.20. Fig. 3.21 shows the trace of conjugate matching. Using a series inductor and a parallel inductor match the conjugate matching that will let circuit has max gain.

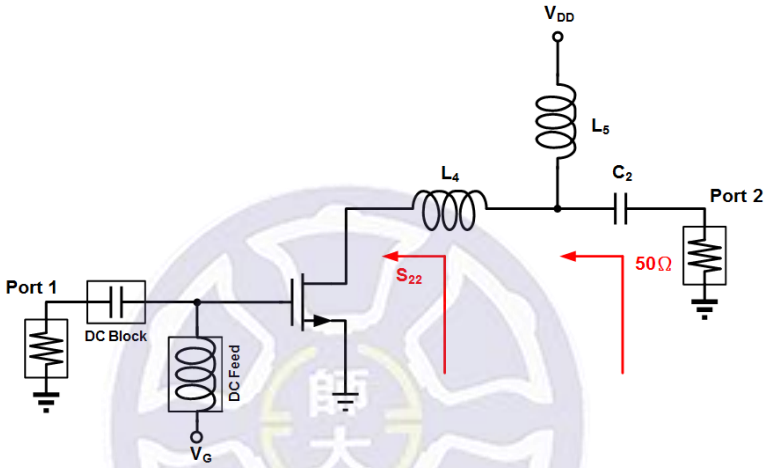


Fig. 3.20. Output-stage matching circuit design.

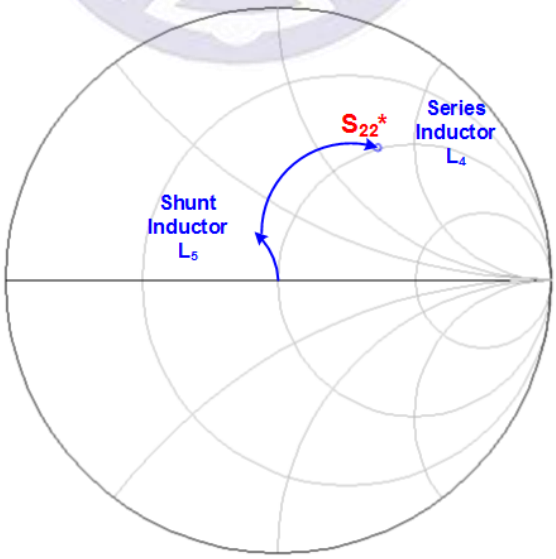


Fig. 3.21. Trace of impedance in output-stage matching network.

3.4.5 Design of Bypass Circuit

In the transistor bias design, the gate-bias (V_G) will through the large resistance (R_1) to the gate of transistor. The drain of transistor needs to equip the bypass circuit, which can protect the circuit performance and avoid low-frequency oscillation. The bypass circuit uses the two-stage circuit, as shown in Fig. 3.22. The first stage uses the C_1, which can achieve the AC-short. The second stage uses C_2 and R_1, which make low-frequency signal attenuation.

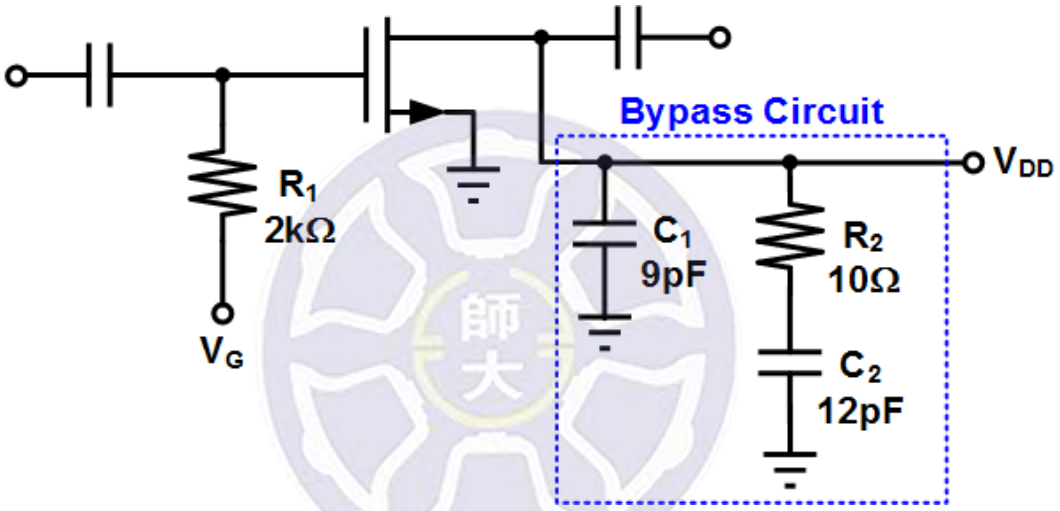


Fig. 3.22. Design of bypass circuit.

3.5 LNA Simulation Results

3.5.1 LNA

The circuit simulation uses the advanced design system (ADS) and the electromagnetic simulation uses the SONNET. The circuit architecture uses the two-stage, which is the two-stage common-source amplifier, as shown in Fig. 3.23. Moreover, the maximum voltage value of LNA is 1.2V, the bias voltage is 0.8V, and the power consumption of circuit is 13.69mW, respectively. Using the same bypass circuit can reduce the layout area. Moreover, using C_1, which represents the capacitor of ESD protection circuits, simulates the influence on LNA. According the effect of C_1, adjusting the component of matching network makes LNA have better RF performance.

Simulation results have shown in Fig. 3.24 to Fig. 3.26. S_{11} is -20.99dB, S_{21} is 14.51dB, S_{22} is -20.55dB, noise is 5.361dB, and K is 1.799, respectively. Fig 3.27 shows the layout top view of 24-GHz LNA.

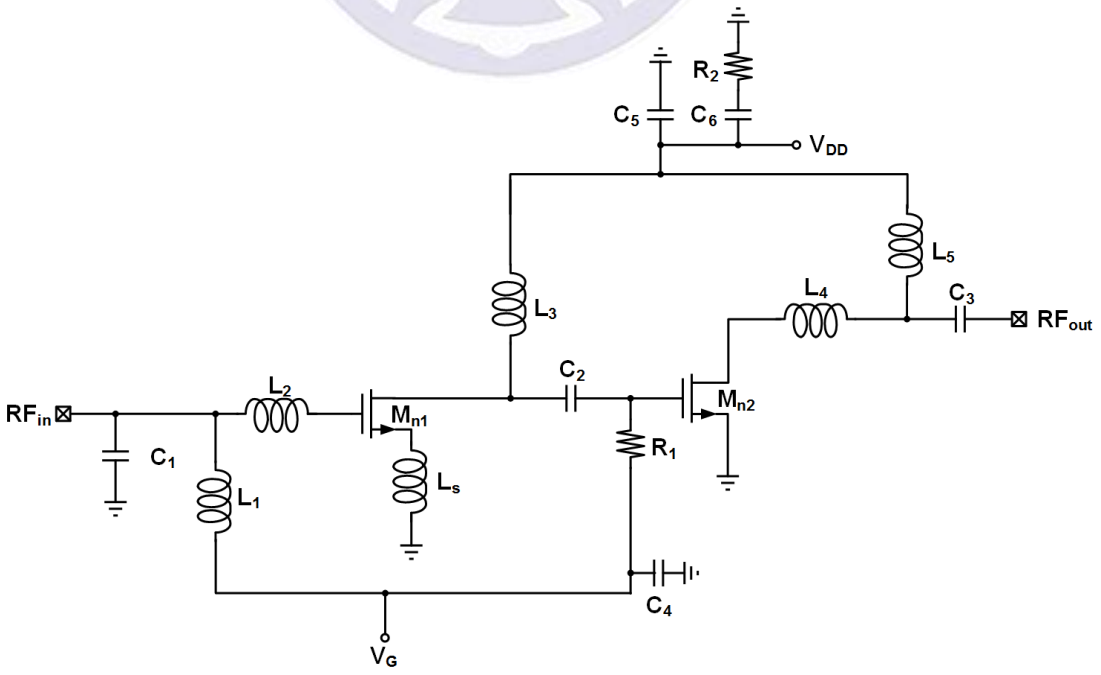


Fig. 3.23. 24-GHz LNA circuit architecture.

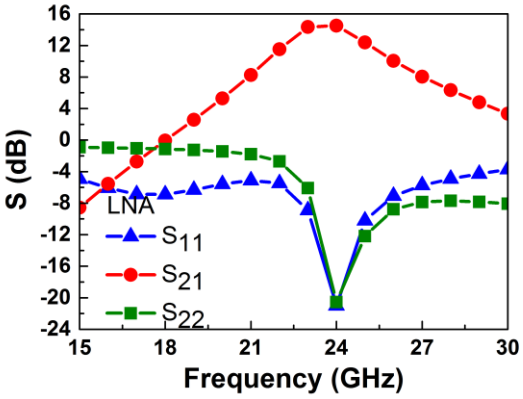


Fig. 3.24. Simulated S-parameters of LNA.

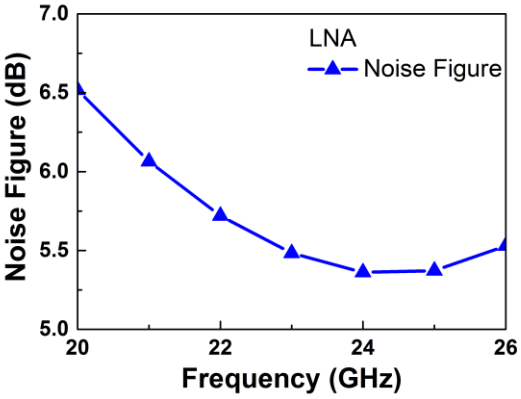


Fig. 3.25. Simulated noise figure of LNA.

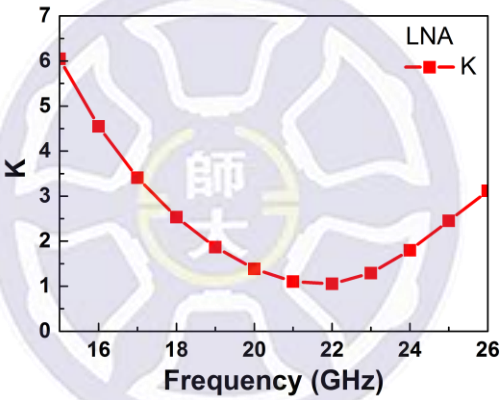


Fig. 3.26. Simulated stability of LNA.

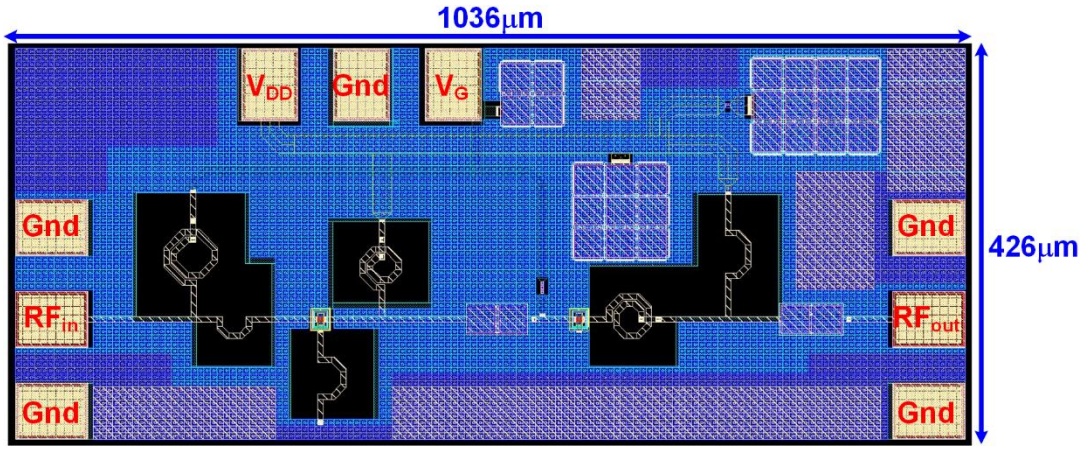


Fig. 3.27. Layout top view of 24-GHz LNA.

3.5.2 LNA with ESD Protection Circuit

In order to investigate the effect of ESD protection circuit on LNA whether to effect the LNA performance. In this work, using the ideal capacitor replaces the ESD protection circuit. The estimation of ESD protection circuit capacitance uses the ADS simulation and the measurement results previously. After ensuring parasitic capacitance of ESD protection circuit, using this capacitance value to equip LNA. Simulation results of LNA with ESD protection circuits and layout top view have been shown in Fig. 3.28 to Fig. 3.43. At last, the diode width of ESD protection circuit selects 10μm that can bring least the parasitic effect to LNA.

All of simulation results still maintains great RF performance. S_{11} is less than -20dB, S_{21} is about 14.5dB, S_{22} is less than -15dB, noise is about 5.5dB, and K is over 1, respectively. As a whole, it makes no difference to effect of ESD protection circuits on LNA performance. The layout area of LNA with ESD protection circuit is 1076μm × 426μm. On the other hand, the area of proposed designs is much lower than prior arts, especially in the power clamp. The area of MOS-based power-clamp is 184μm × 85μm and SCR-based power-clamp is 70μm × 52μm. That is a considerable difference. Therefore, proposed designs can improve area efficiency of ESD protection designs.

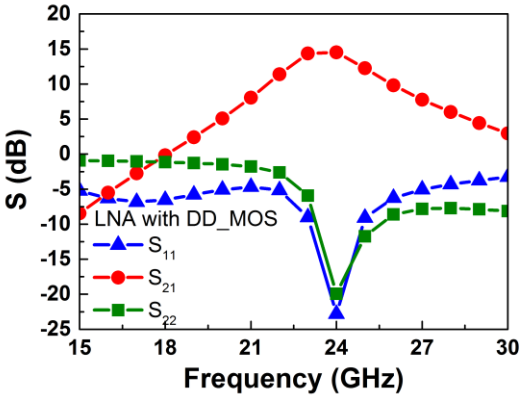


Fig. 3.28. Simulated S-parameters of LNA with DD_MOS.

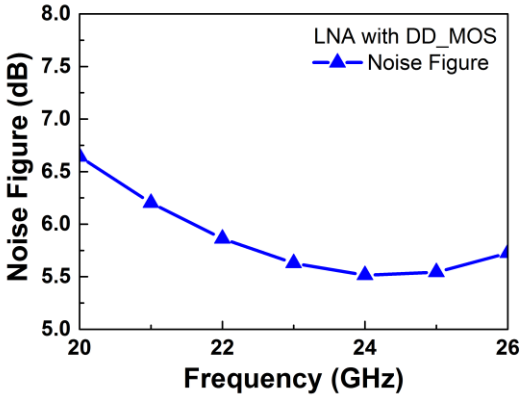


Fig. 3.29. Simulated noise figure of LNA with DD_MOS.

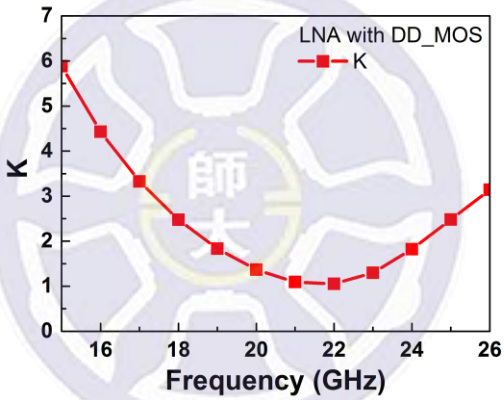


Fig. 3.30. Simulated stability of LNA with DD_MOS.

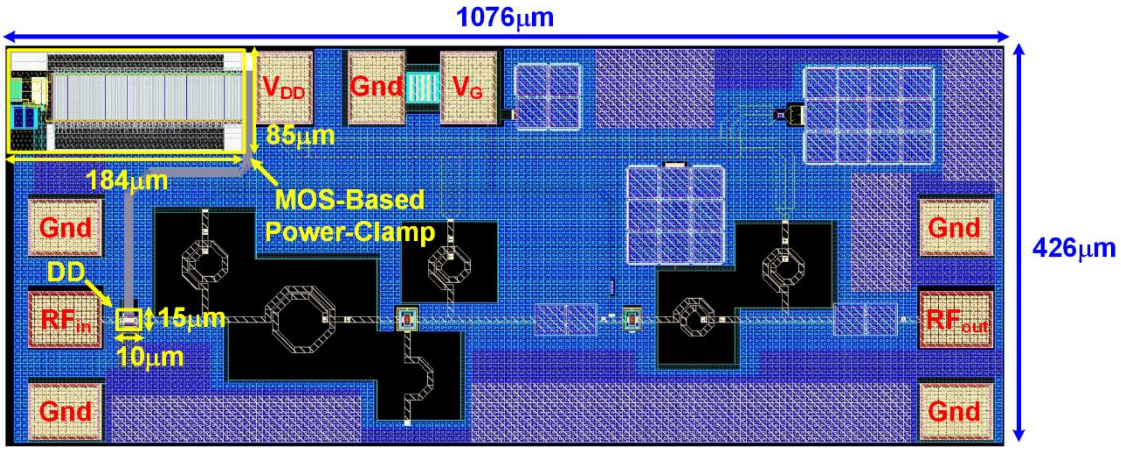


Fig. 3.31. Layout top view of LNA with DD_MOS.

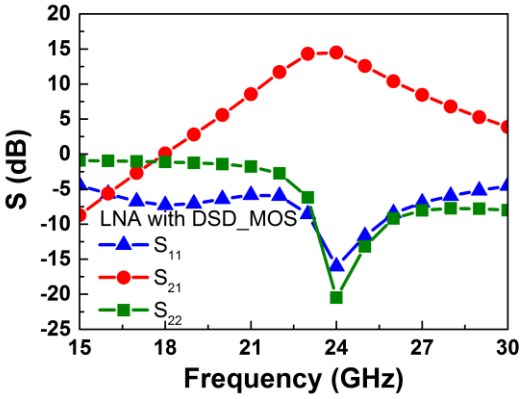


Fig. 3.32. Simulated S-parameters of LNA with DSD_MOS.

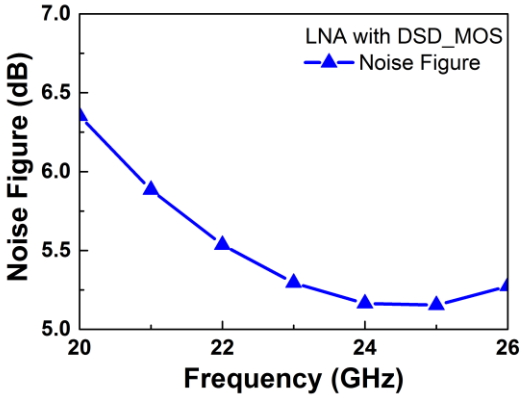


Fig. 3.33. Simulated noise figure of LNA with DSD_MOS.

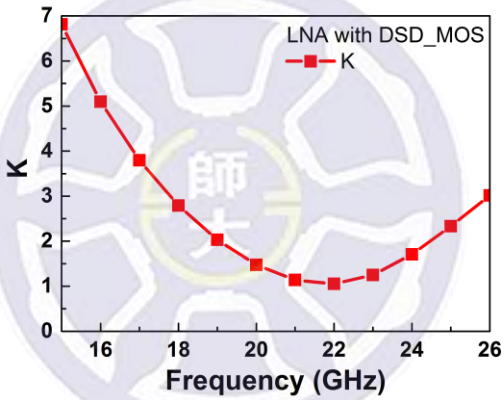


Fig. 3.34. Simulated stability of LNA with DSD_MOS.

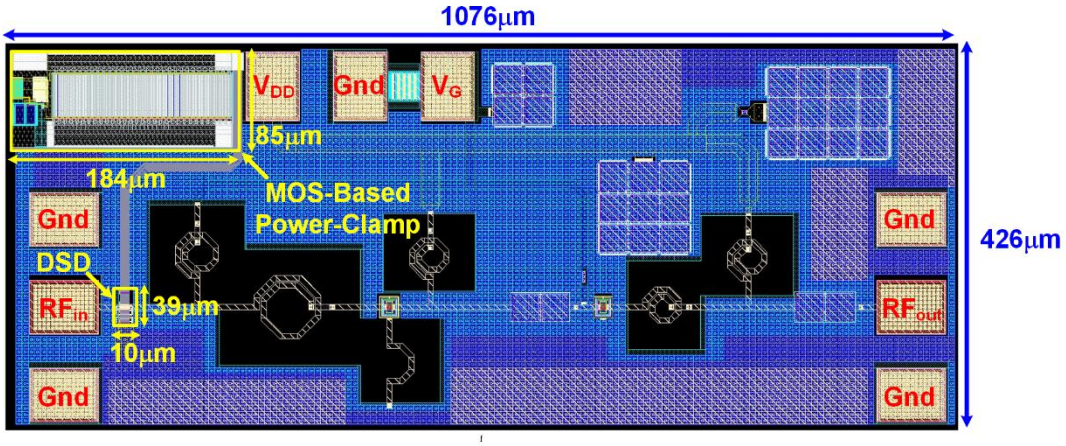


Fig. 3.35. Layout top view of LNA with DSD_MOS.

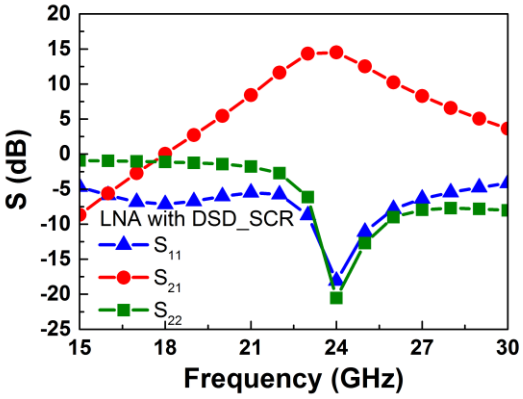


Fig. 3.36. Simulated S-parameters of LNA with DSD_SCR.

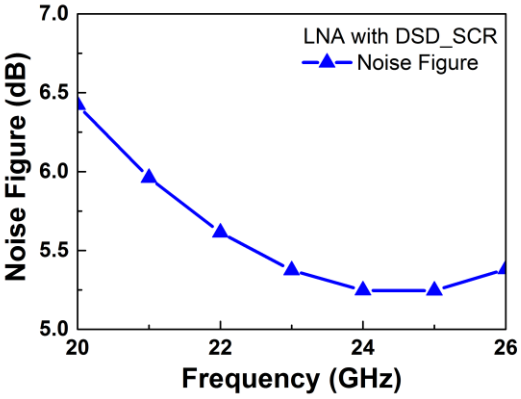


Fig. 3.37. Simulated noise figure of LNA with DSD_SCR.

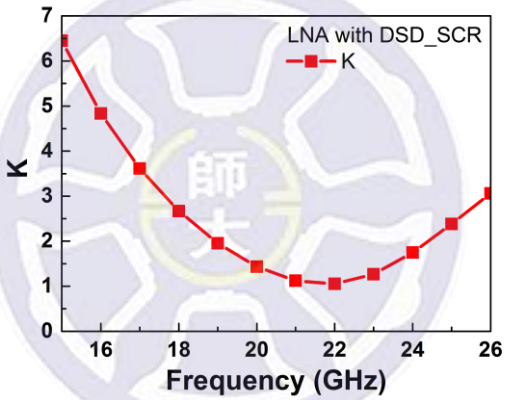


Fig. 3.38. Simulated stability of LNA with DSD_SCR.

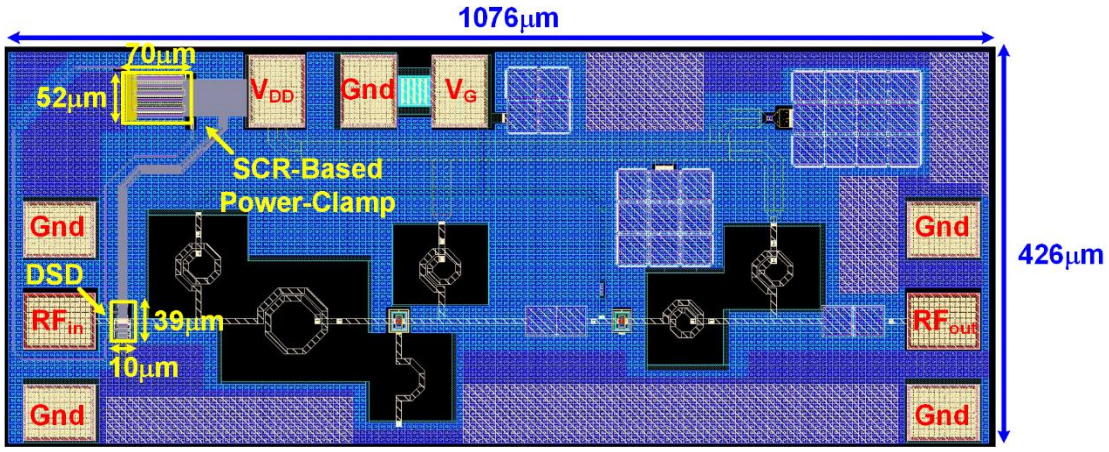


Fig. 3.39. Layout top view of LNA with DSD_SCR.

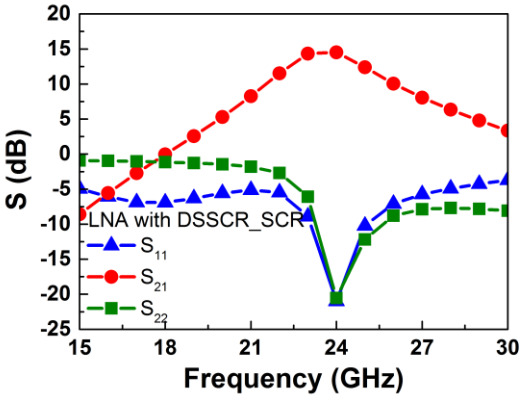


Fig. 3.40. Simulated S-parameters of LNA with DSSCR_SCR.

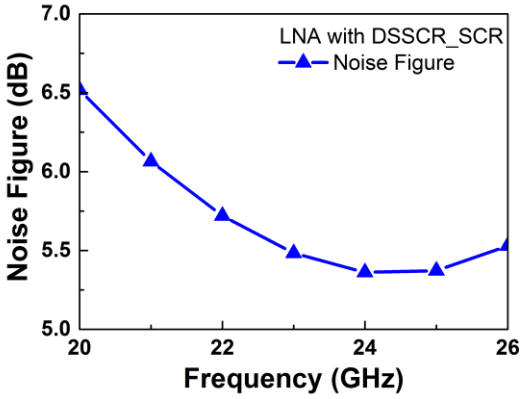


Fig. 3.41. Simulated noise figure of LNA with DSSCR_SCR.

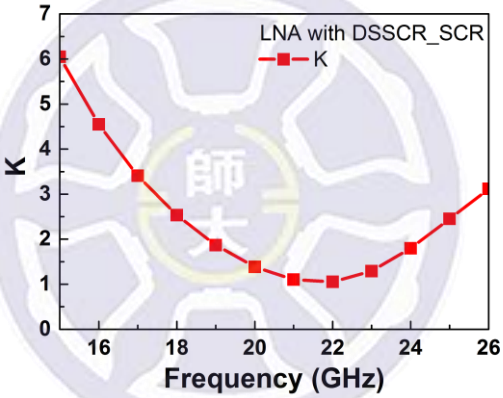


Fig. 3.42. Simulated stability of LNA with DSSCR_SCR.

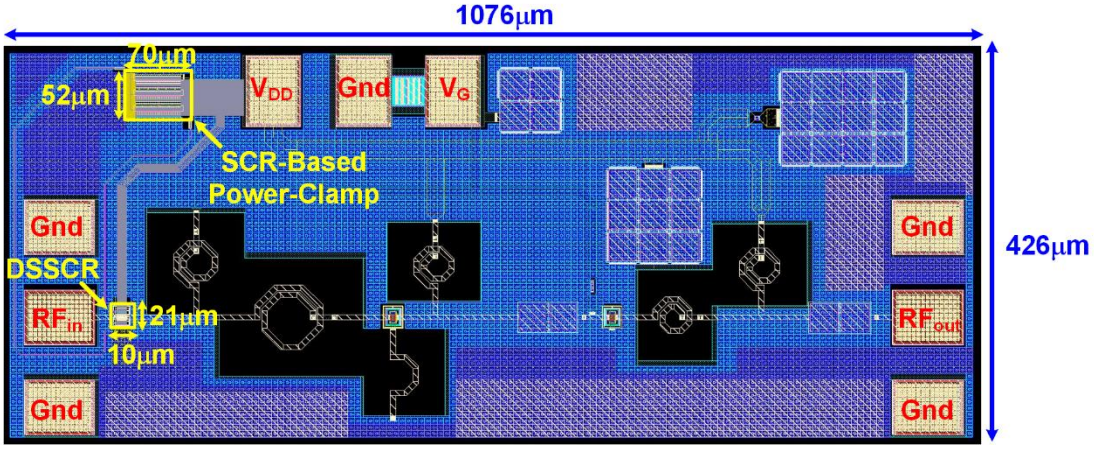


Fig. 3.43. Layout top view of LNA with DSSCR_SCR.

3.6 LNA Measurement Results

The high-frequency measurement of all LNA circuits is on-wafer measurement with 2-port GSG probes. S-parameters of all LNA circuits are measured by using vector network analyzer. Noise figures of all LNA circuits are measured by using noise analyzer. In measurement-steps, the power-supply voltage (V_{DD}) is 1.2V and the gate-bias (V_G) is 0.8V. ESD robustness of all LNA circuits are measured by using ESD tester. In this statement, the failure criterion is defined as the RF performance failure.

3.6.1 LNA

Fig. 3.44 is the photograph of 24-GHz LNA. Fig. 3.45 and Fig. 3.46 are measurement results of S-parameters and noise figure. At 24-GHz, S_{11} is -19.11dB, S_{21} is 9.87, the S_{22} is -13.88dB, the noise figure is 5.95dB, respectively. Next, ESD robustness of LNA is measured by using the HBM tester. After 0.5kV HBM stress, S-parameters of LNA have been failed, as shown in Fig. 3.47. Therefore, the HBM robustness of LNA is 0kV.

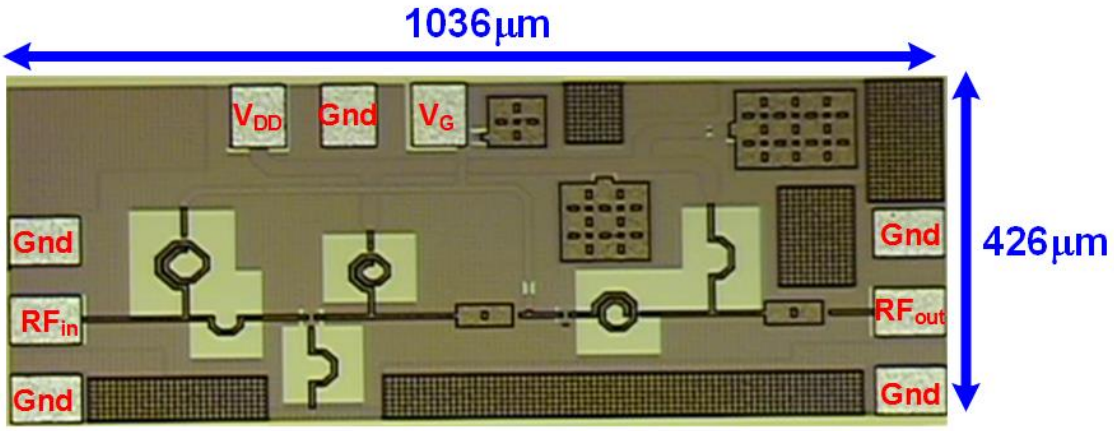


Fig. 3.44. Photograph of 24GHz LNA.

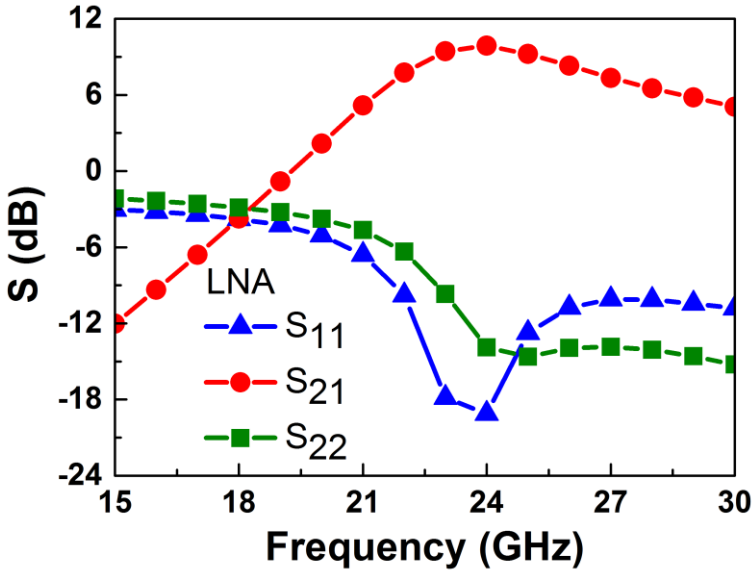


Fig. 3.45. Measured S-parameters of LNA.

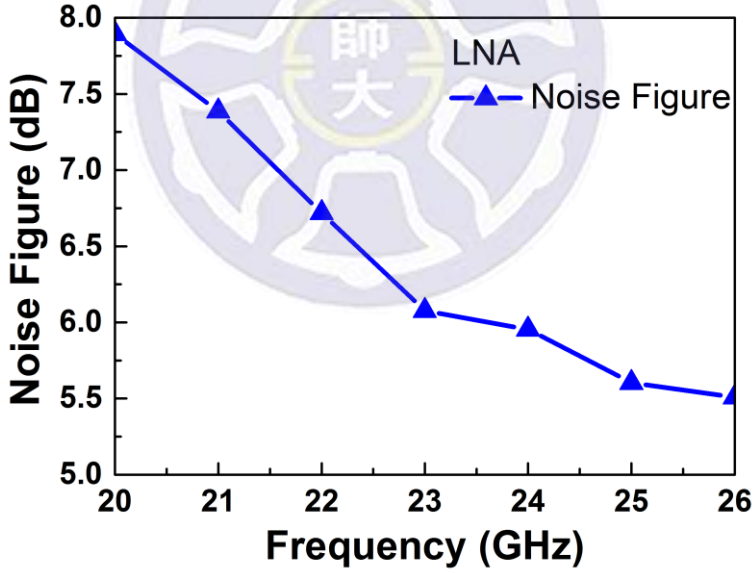


Fig. 3.46. Measured noise figure of LNA.

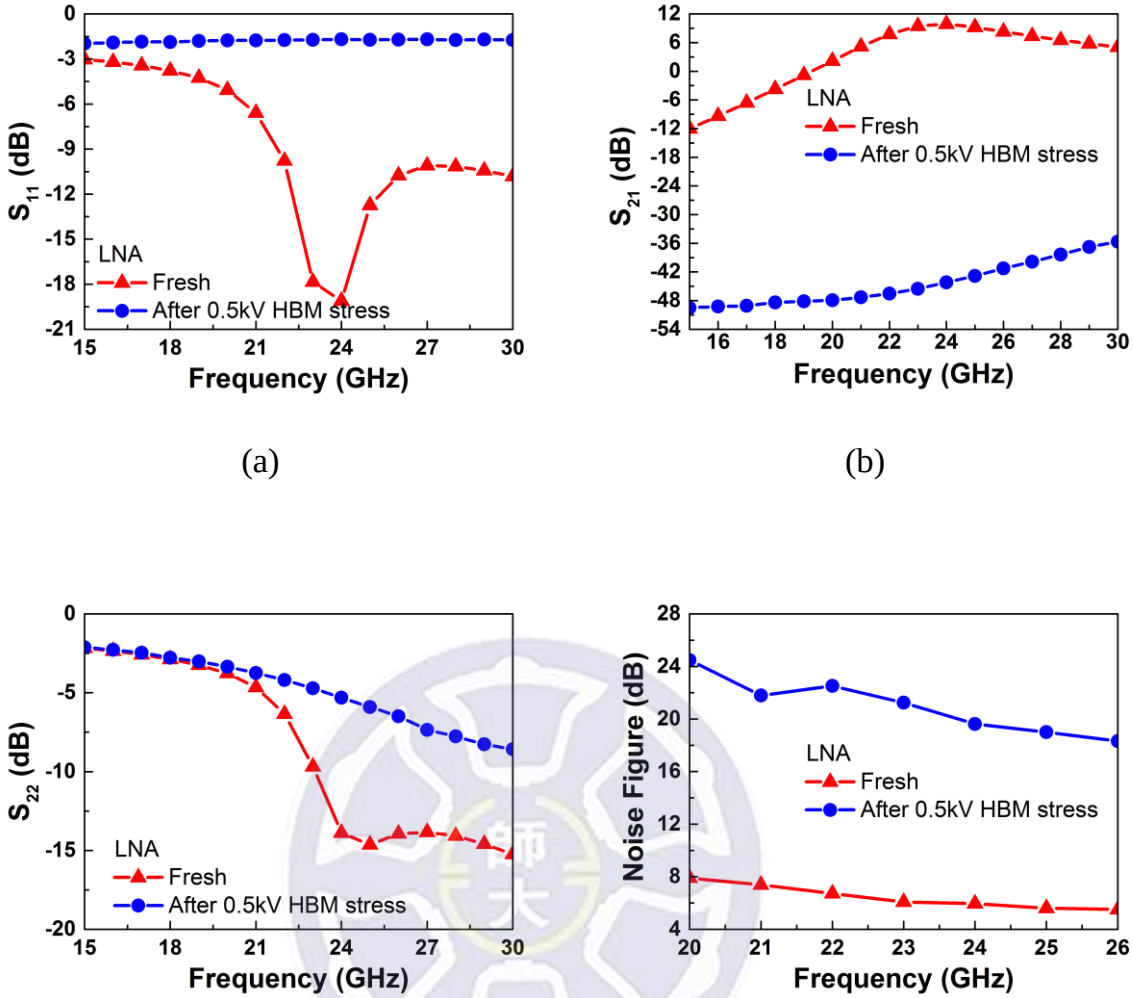


Fig. 3.47. Measured (a) S_{11}, (b) S_{21}, (c) S_{22}, and (d) noise figure, of the LNA after HBM stress.

3.6.2 LNA with ESD Protection Circuit

Fig. 3.48 to Fig. 3.51 show photographs of LNA with ESD protection circuits, respectively.

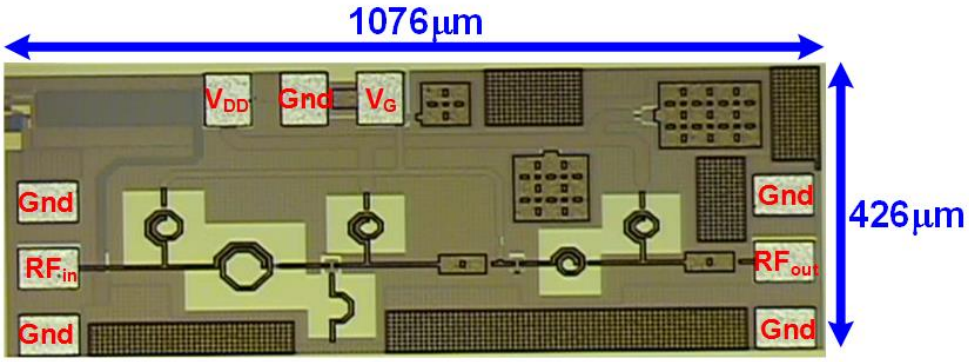


Fig. 3.48. Photograph of LNA with DD_MOS.

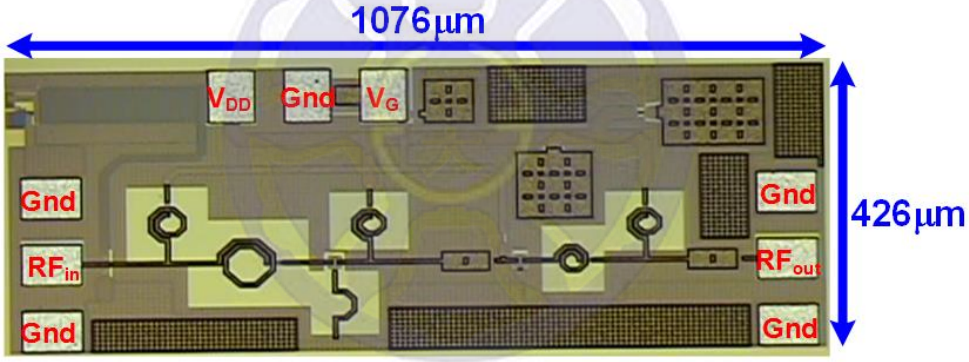


Fig. 3.49. Photograph of LNA with DSD_MOS.

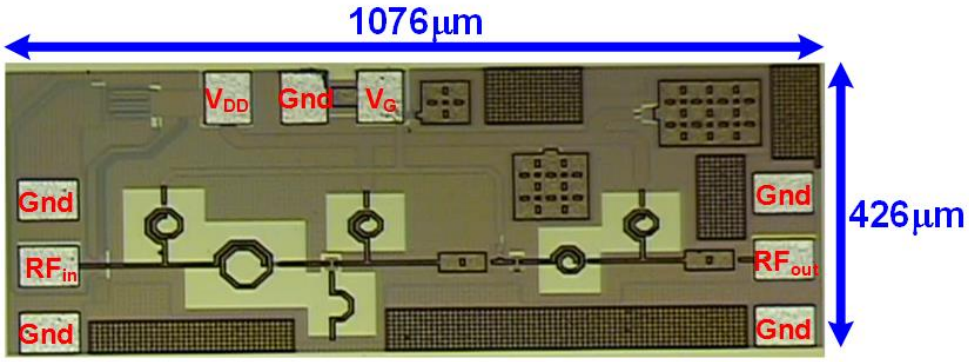


Fig. 3.50. Photograph of LNA with DSD_SCR.

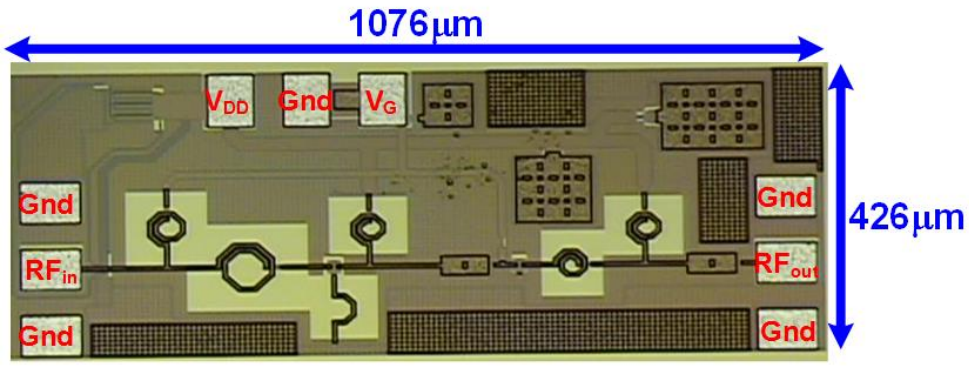
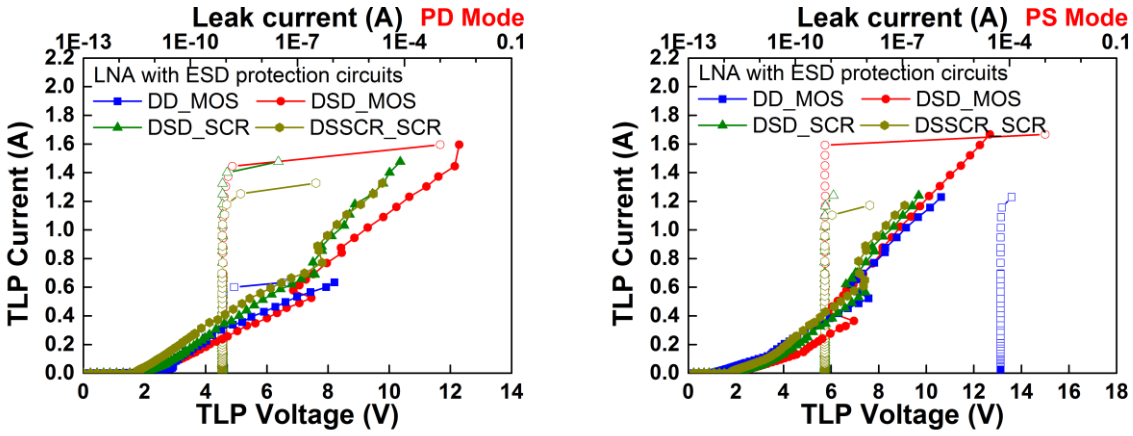


Fig. 3.51. Photograph of LNA with DSSCR_SCR.

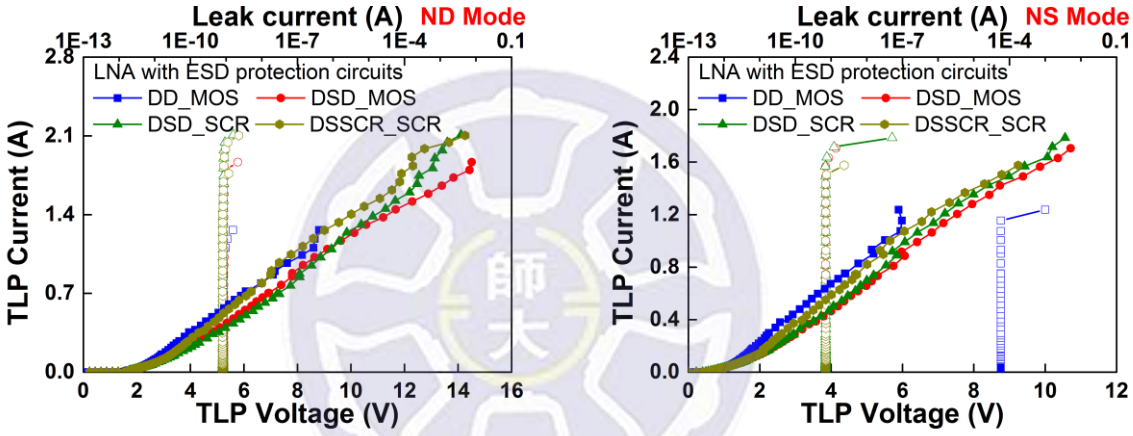
1. TLP I-V Curves

Measuring the I-V characteristics of all LNA circuits uses the transmission-line-pulse (TLP) system without package. Fig. 3.52 shows the TLP I-V characteristic of LNA under four types of modes. After measuring characteristics of all LNA circuits, the HBM robustness of LNA with ESD protection circuits can be predicted.

In this measurement results, the failure criterion is defined as the leakage current shifting over 30%. There are unique phenomena, which are the leakage of DD_MOS under PS mode and NS mode. The leakage current of DD_MOS is much higher than other ESD protection circuits, because the dual diodes of DD_MOS has been turned-on. During the TLP measurement steps, the positive/negative voltage is 0.8/-0.8 that can explain why dual diodes has been turned-on.



(a) (b)



(c) (d)

Fig. 3.52. Measured TLP I-V characteristic of LNA under (a) PD mode, (b) PS mode, (c) ND mode, and (d) NS mode.

The TLP I-V characteristic of ESD protection circuits under V_{DD}-to-V_{SS} mode has shown in Fig. 3.53. During the TLP measurement steps, proposed designs makes V_G of LNA be half-operating voltage. In order to prevent LNA turning-on, the operating voltage selects 0.4V. LNA with proposed designs not only can be triggered early but also have higher I_{t2} as shown in Fig. 3.53. I_{t2} of proposed designs is about 8A and that of prior arts is 5.2A. Proposed designs have more excellent ESD performances than those of prior arts. The purpose of high I_{t2} is necessary because the power-rail ESD

clamp cannot be failed before ESD protection device broken. If the ESD specification becomes increase in the future, the high ESD performance of proposed designs still can be applied. Therefore, proposed designs have more possibilities, which mean different applications in ESD protection design, than those of prior arts.

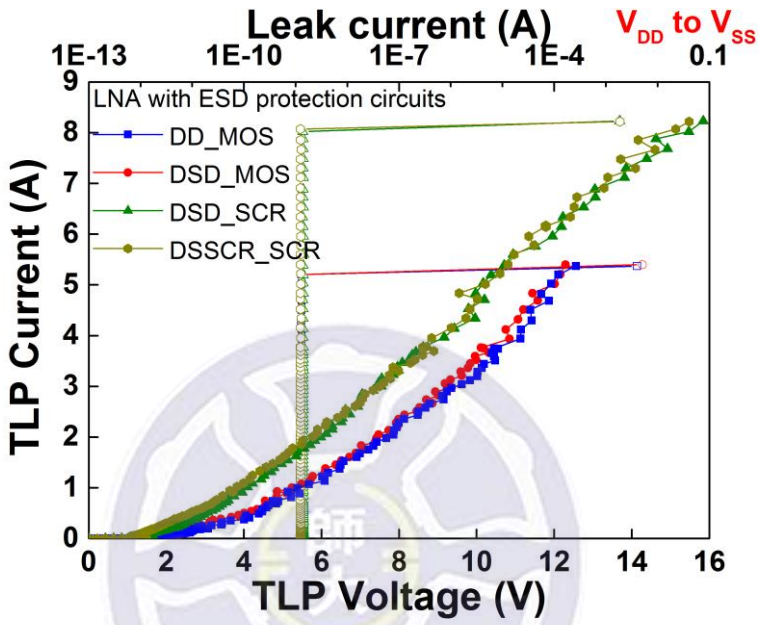


Fig. 3.53. Measured TLP I-V characteristic of LNA with ESD protection circuits under V_{DD}-to-V_{SS} mode.

2. High-Frequency Performance

Fig. 3.54 to Fig. 3.57 are measurement S-parameters of LNA with ESD protection circuits. All of S_{11} is less than -15dB, S_{21} is about 10dB, S_{22} is less than -13dB, respectively. Comparing with original S-parameters of LNA is not affected too much. Every S-parameters of LNA with ESD protection circuits still have good RF performance. That is to say, ESD protection circuits all can use in LNA successfully.

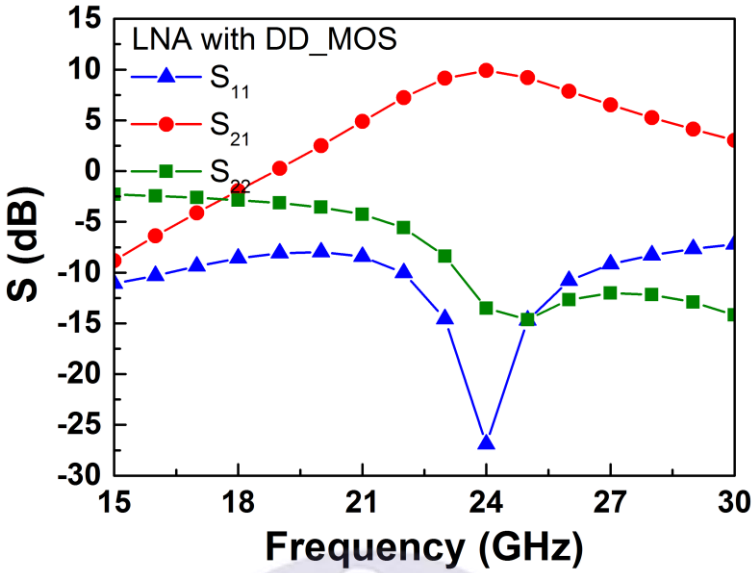


Fig. 3.54. Measured S-parameters of LNA with DD_MOS.

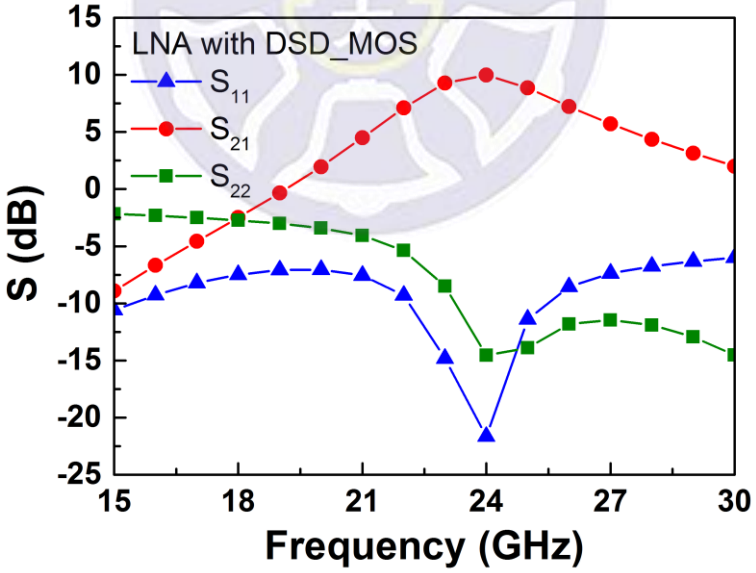


Fig. 3.55. Measured S-parameters of LNA with DSD_MOS.

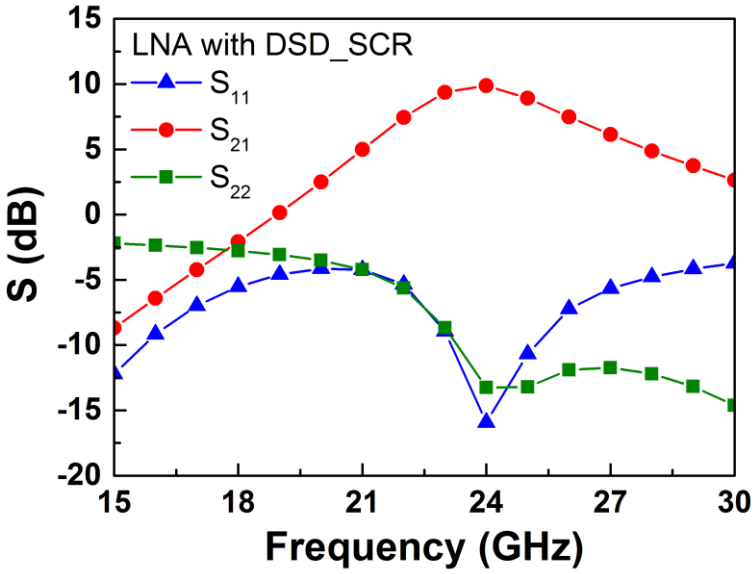


Fig. 3.56. Measured S-parameters of LNA with DSD_SCR.

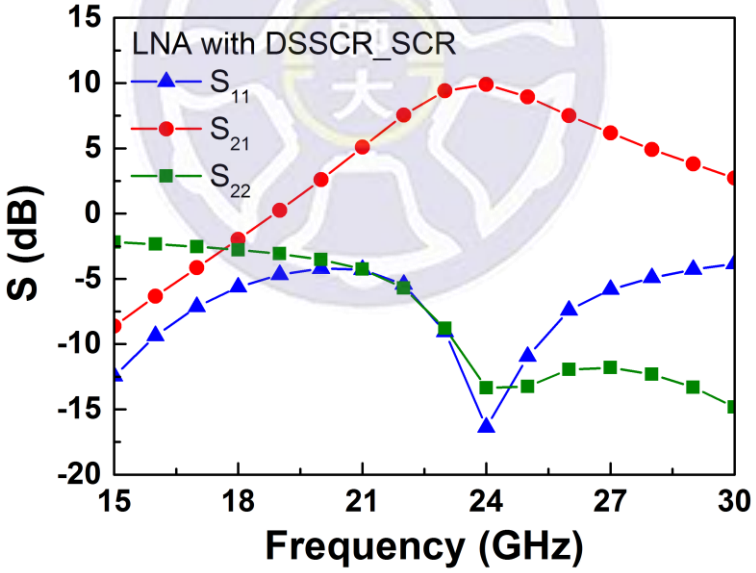


Fig. 3.57. Measured S-parameters of LNA with DSSCR_SCR.

Fig. 3.58 is the measurement results of the LNA with DD_MOS after HBM stress. The HBM measurement range is 0kV to 3kV and the measurement step is 0.5kV. After 2.5kV HBM stress, the RF performance of LNA with DD_MOS has failed. Therefore, HBM robustness of LNA with DD_MOS is 2kV.

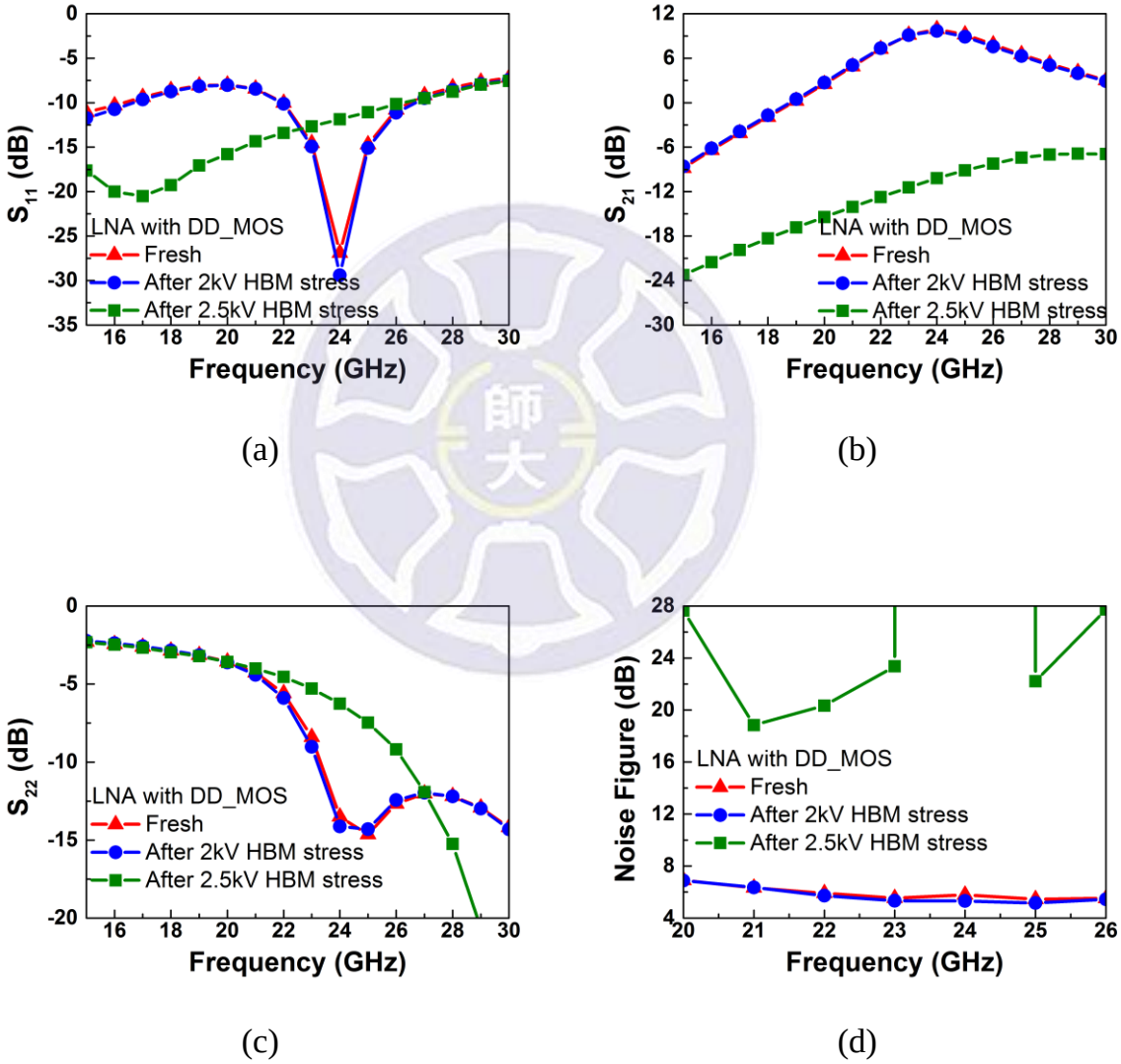


Fig. 3.58. Measured (a) S_{11}, (b) S_{21}, (c) S_{22}, and (d) noise figure, of LNA with DD_MOS after HBM stress.

Fig. 3.59 is measurement results of the LNA with DSD_MOS after HBM stress. After 2.5kV HBM stress, the RF performance of LNA with DSD_MOS has failed. Therefore, the HBM robustness of LNA with DSD_MOS is 2kV.

As mentioned above, prior arts, which are DD_MOS and DSD_MOS, can only bear 2kV HBM robustness.

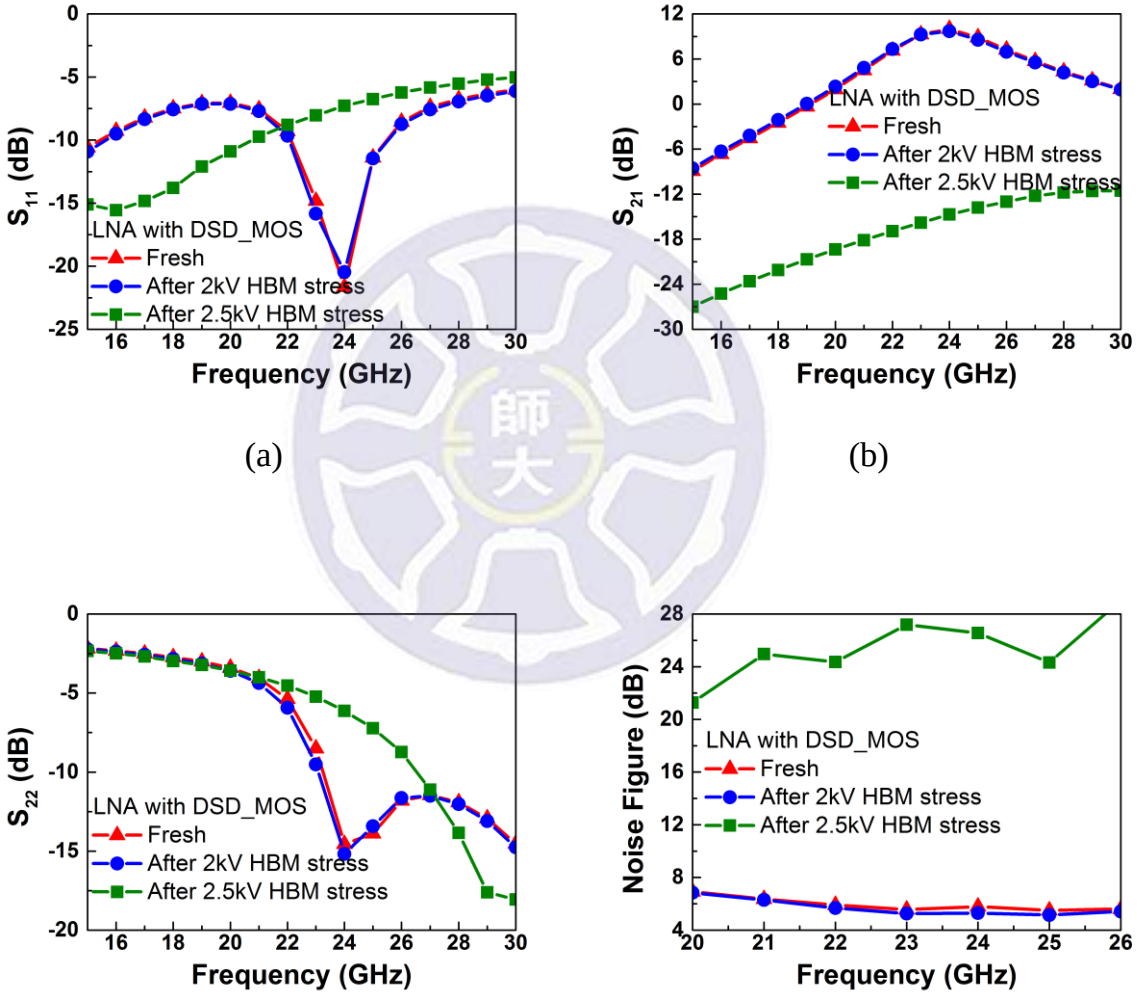


Fig. 3.59. Measured (a) S_{11}, (b) S_{21}, (c) S_{22}, and (d) noise figure, of LNA with DSD_MOS after HBM stress.

Fig. 3.60 is measurement results of the LNA with DSD_SCR after HBM stress. After 3kV HBM stress, the RF performance of LNA with DSD_SCR has failed. In other words, the HBM robustness of LNA with DSD_SCR is 2.5kV.

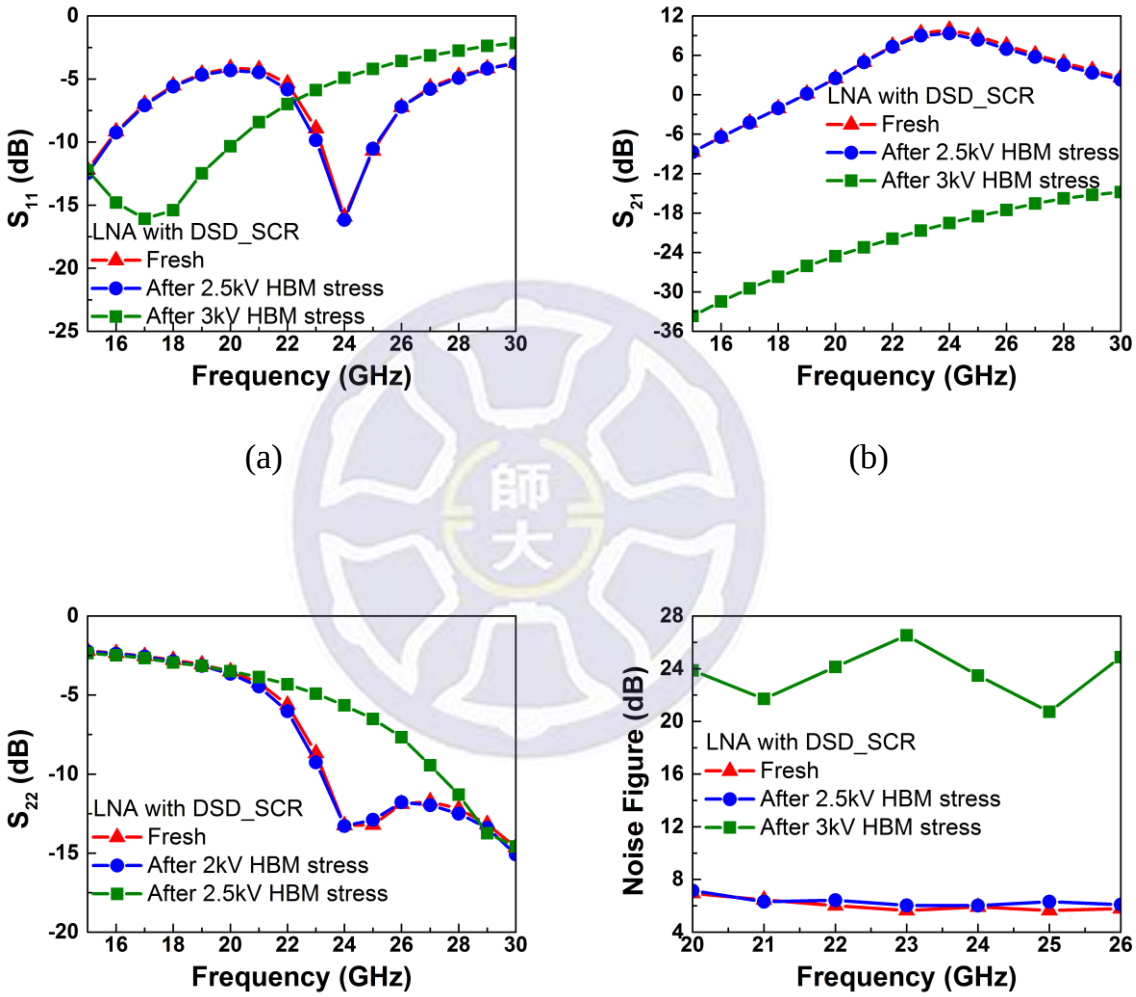


Fig. 3.60. Measured (a) S_{11}, (b) S_{21}, (c) S_{22}, and (d) noise figure, of LNA with DSD_SCR after HBM stress.

Fig. 3.61 is measurement results of the LNA with DSSCR_SCR after HBM stress. After 3kV HBM stress, the RF performance of LNA with DSSCR_SCR has failed. According to above-mentioned measurement results, LNA with proposed designs, which are DSD_SCR and DSSCR_SCR, can bear 2.5kV HBM robustness.

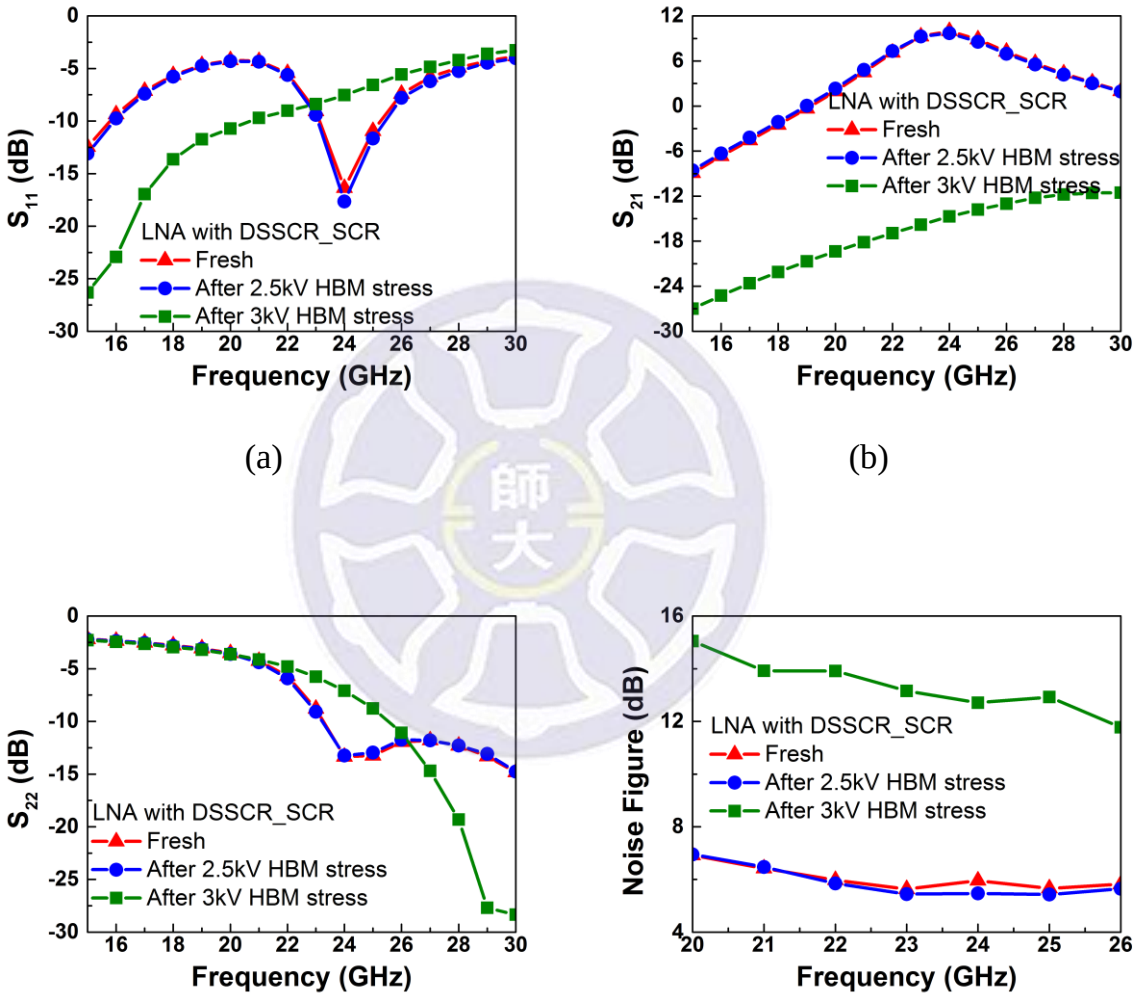


Fig. 3.61. Measured (a) S_{11}, (b) S_{21}, (c) S_{22}, and (d) noise figure, of LNA with DSSCR_SCR after HBM stress.

Table 3.1 shows comparisons of LNA with ESD protection circuits. After LNA equipped with ESD protection circuits, RF performances of LNA with ESD protection circuits do not change. That means ESD protection circuits will not lead degeneration to LNA. Using references compares with this works. The amazing advantage of proposed designs is that ESD protection circuits occupy less layout area. The ESD protection area of LNA with DSD_SCR is 3718μm^2, LNA with DSSCR_SCR is 3538 μm^2. Proposed designs can reduce the layout area significantly without reducing the ESD performance. Table 3.1 also shows the HBM robustness of LNA with ESD protection circuits. LNA with DD_MOS is 2kV, LNA with DSD_MOS is 2kV, LNA with DSD_SCR is 2.5kV, and LNA with DSSCR_SCR is 2.5kV, respectively. The ESD performance of proposed designs is better than prior arts.

Table 3.1

Comparison among ESD protection circuits.

Cell Name		Freq.	Tech.	Gain (dB)	Noise Figure (dB)	V_{DD} (V)	P_{dc} (mW)	ESD Protection Area (μm^2)	HBM (kV)
This work	LNA	24 GHz	CMOS 0.18-μm	9.8	5.9	1.2	20.4	N/A	0
	LNA with DD_MOS				5.8			15790	2
	LNA with DSD_MOS				5.8			16030	2
	LNA with DSD_SCR				5.9			3718	2.5
	LNA with DSSCR_SCR				5.9			3538	2.5
Reference [35]			CMOS 0.13-μm	10	6.8	1.2	41	16800	2
Reference [36]			CMOS 0.13-μm	14	5	1.5	48	8398	2.5
Reference [37]			SiGe 0.35-μm	12	3.1	3.3	18	11900	2

3.7 Discussion and Summary

3.7.1 Debug

In measurement results of LNA, the S-parameters and noise figure are inconsistent with simulation results. Therefore, using re-simulation finds the unconsidered factor of LNA. After re-simulation and verification, the inconsistent reason of S-parameters and noise figure has found, as shown in Fig. 3.62. The effect of pad and part of signal line have not added to the simulation, as shown in Fig. 3.63. After re-simulation, re-simulations of S-parameters and noise figure have shown in Fig. 3.64. S-parameters and noise figure of re-simulation are coincident with measurement results closely. As long as EM simulation of circuit is more completive, the simulation will meet real measurement results closely.

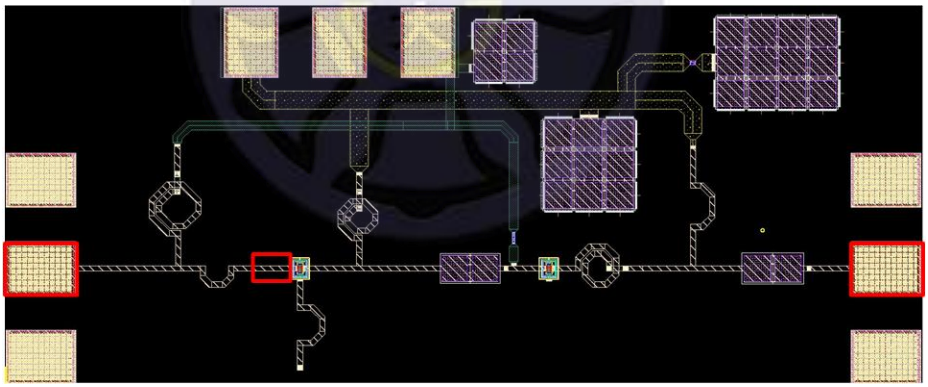
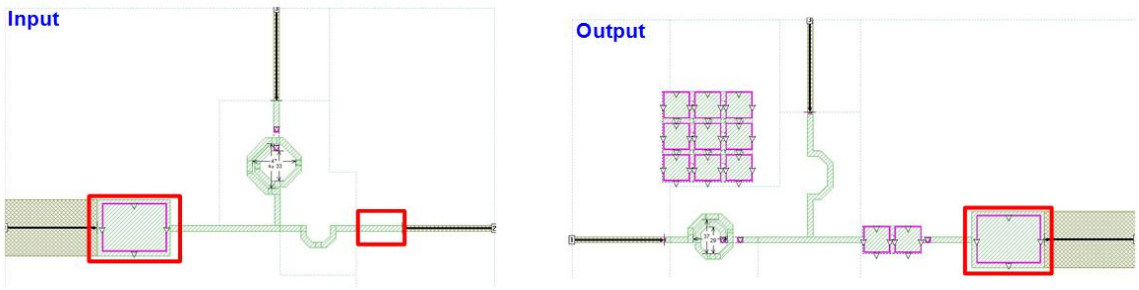


Fig. 3.62. Area of EM has not consider before.



(a) (b)

Fig. 3.63. EM simulations of (a) input, and (b) output.

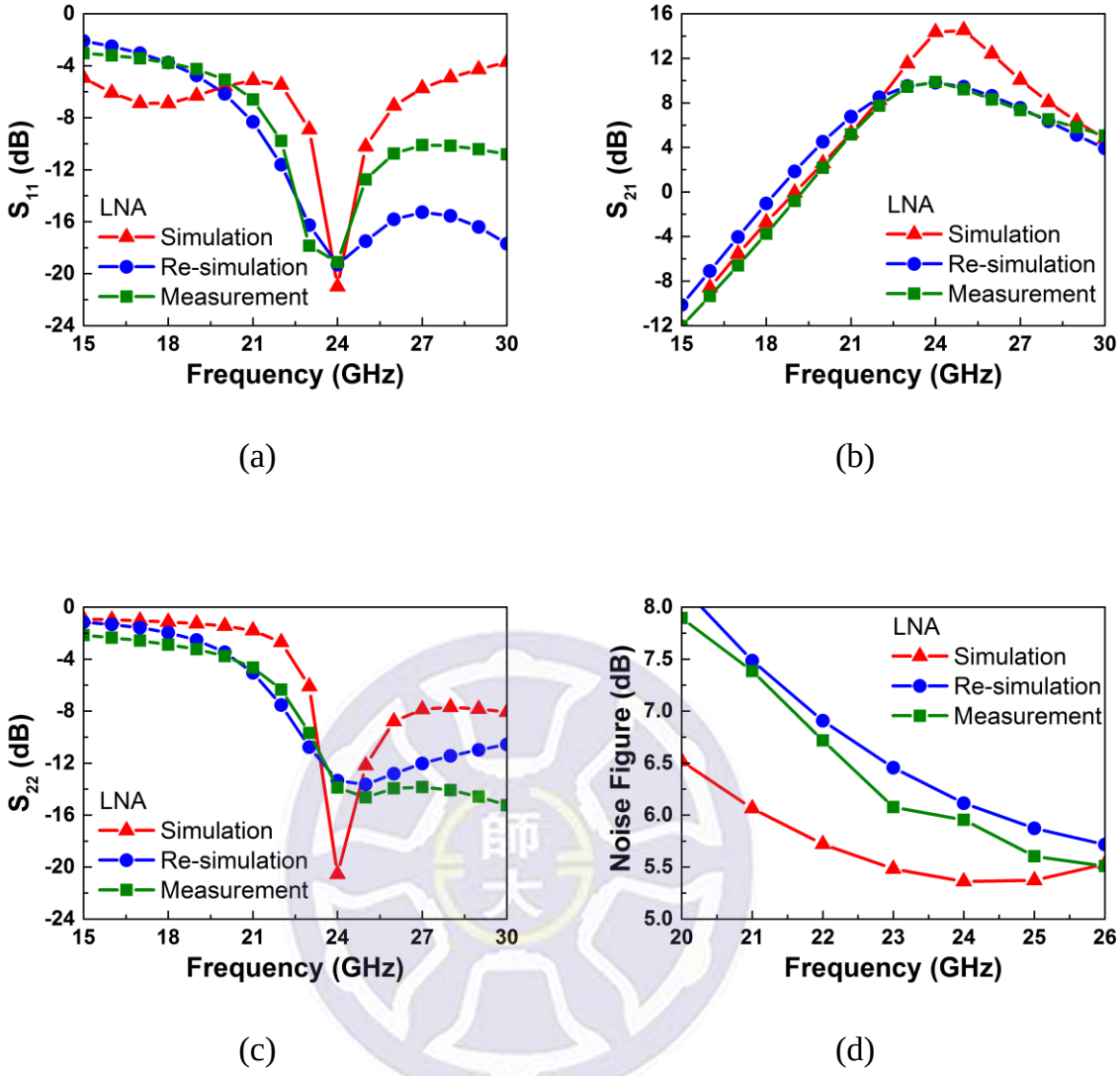


Fig. 3.64. Compared (a) S_{11}, (b) S_{21}, (c) S_{22}, and (d) noise figure, of LNA.

3.7.2 Summary

In this study, the 24-GHz LNA composes of two common-source design. At 24GHz, S_{21} of LNA is 9.87dB, S_{11} is -19.11dB, S_{22} is -13.88dB, noise figure is 5.95dB. After HBM stress, ESD robustness of LNA with prior arts, which are DD_MOS and DSD_MOS, are all 2kV. On the other hand, ESD robustness of LNA with prior arts proposed designs, which are DSD_SCR and DSSCR_SCR, are all 2.5kV.

The most amazing advantage of proposed designs is that DSD_SCR and

DSSCR_SCR can provide enough HBM robustness by occupying less layout area. The ESD protection area of LNA with DSD_SCR is 3718μm^2 and that of LNA with DSSCR_SCR is 3538 μm^2. In contrast to LNA with prior arts, providing 2kV HBM robustness occupies larger layout area. Proposed designs really can reduce the layout area significantly without reducing the ESD performance.

To sum up, proposed designs not only reduce the layout area but also provide the highest ESD performance at unit area without reducing the RF performance of internal circuit.

Chapter 4

Conclusion and Future Works

In this chapter, measurement results and contributions of this study will be summarized. Future work of DSSCR and SCR-base power-rail ESD clamp will also provide.

4.1 Conclusion

In Chapter 2, drawbacks of conventional designs have been introduced. Therefore, two of proposed designs, which are DSD_SCR and DSSCR_SCR have been proposed. The following measurement results select 50μm diode width: DSD_SCR and DSSCR_SCR have better ESD robustness, which are 7kV and 8kV HBM than conventional designs. In high-frequency performance, DSD_SCR and DSSCR_SCR have less loss, which are 1.05dB and 0.98dB than conventional designs. In positive CDM measurement results, the CDM robustness of ESD protection circuits are all >1000V. In leakage current results, at 125^0C, DD_MOS is 53nA, DSD_MOS is 117nA, DSD_SCR is 8nA, and DSSCR_SCR is 5.5nA, respectively. In this Chapter, all devices have been fabricated in a 0.18-μm CMOS process.

In Chapter 3, important parameters and design steps of designing 24-GHz LNA have been introduced in detail. After measuring, the parameters of LNA as follows: At 24GHz, S_{21} is 9.87dB, S_{11} is -19.11dB, S_{22} is -13.88dB, noise figure is 5.95dB. However, the LNA cannot bear 0.5kV HBM stress. Therefore, this chapter also presents ESD protection circuits applying in LNA. After LNA equip with DSSCR_SCR, LNA with

DSSCR_SCR can bear 2.5kV HBM stress without degrading the RF performance. It is better than LNA with prior arts.

4.2 Future Works

In this study, proposed designs can improve the ESD robustness of internal circuit. Furthermore, proposed designs can overcome many drawbacks including degrading RF performance, occupying too much layout area, and bringing too much leakage current. Diode strings with embedded silicon-controlled rectifier (DSSCR) with SCR-based power-rail ESD clamp can provide great ESD performance and less parasitic effect. DSSCR_SCR can be used in high-frequency applications. Eventually, for the sake of latch-up, SCR can equip diodes in series that can increase the holding voltage of SCR, as shown in Fig. 4.1. In order to avoid unnecessary leakage, adjusting the number of diodes from diode string1/diode string2 can adjust voltage of V_{DD}-to-I/O and I/O-to-V_{SS} that can prevent internal circuit turning-on.

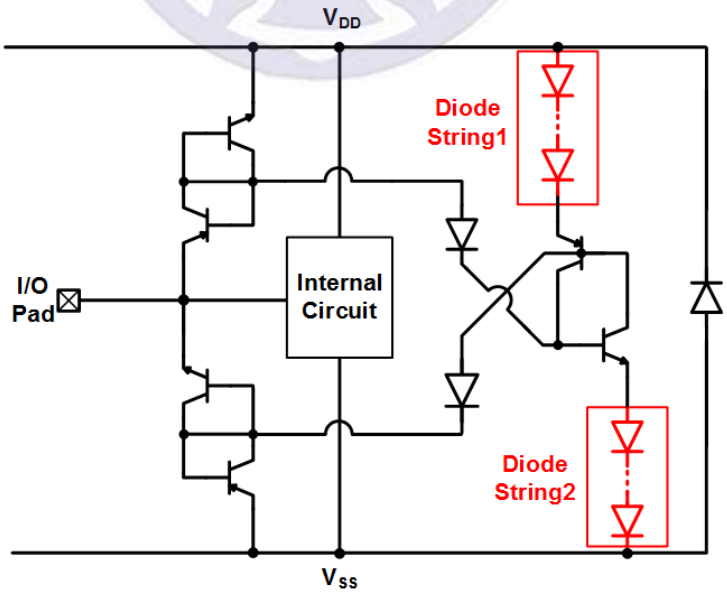
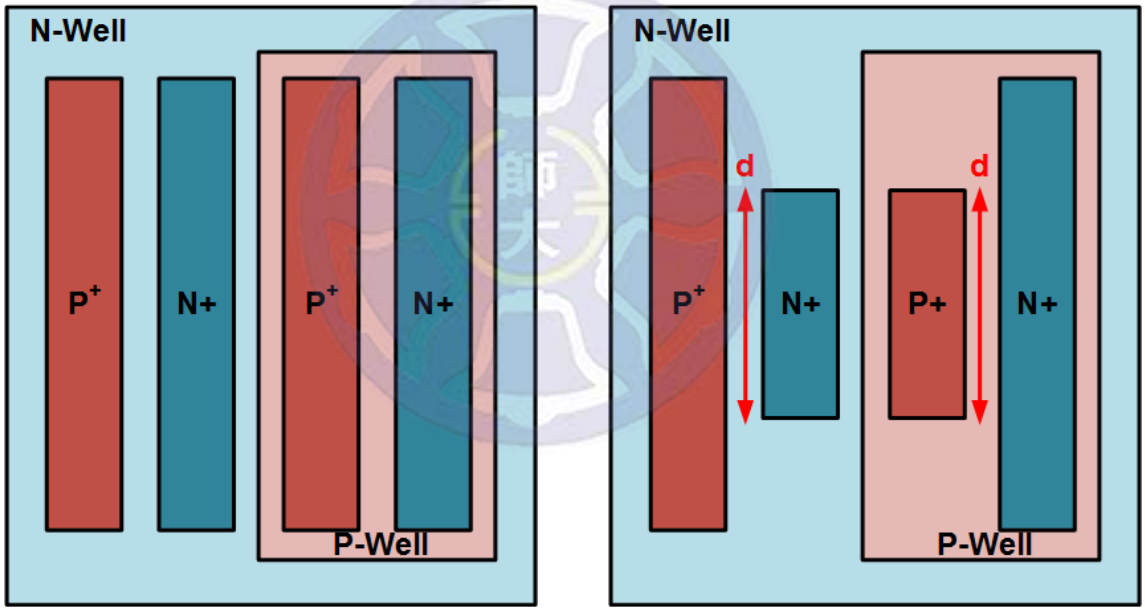


Fig. 4.1. Improved method of proposed design.

Proposed design, which is DSSCR_SCR, has not meet expectation. In TLP-measurement results, the I-V curve of DSSCR_SCR is like that of DSD_SCR. That means the embedded SCR of DSSCR has not been triggered. DSSCR still uses the dual stacked diodes to discharge ESD current. The reason of this phenomenon is the layout planning. In Fig. 4.2 (a), the width of P^+ and N^+ is all the same that will not let embedded SCR trigger quickly. In order to trigger SCR successfully, adjusting the width of N^+ and P^+ lets the SCR be triggered quickly that also can reduce the turn-on resistance of DSSCR, as shown in Fig. 4.2 (b). Therefore, using this improved method can let DSSCR_SCR meet our expectation.



(a) (b)

Fig. 4.2. (a) Original layout top view and (b) improved layout top view of diode string with embedded SCR.

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Publication List

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