國立臺灣師範大學電機工程學系

碩士論文

指導教授：林群祐 博士

極低寄生電容之靜電放電防護設計

ESD Protection Design with Ultra-Low Parasitic Capacitance

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摘　　要

本篇論文研究主軸為極低寄生電容之全晶片靜電放電防護設計，採用 0.18-μm 之 CMOS 以及 SiGe BiCMOS 製程，並實際搭配所設計的靜電放電防護元件應用至不同頻段的低雜訊放大器。

在 CMOS 製程設計堆疊式二極體內嵌入式矽控整流器，該元件有小的佈局面積、低寄生電容、以及高耐受度。將堆疊式二極體內嵌入式矽控整流器應用至操作在 24-GHz 的低雜訊放大器，並驗證全晶片靜電放電防護設計。使用 BiCMOS 製程設計垂直式 NPN 元件，降低元件的觸發電壓，並將垂直式 NPN 元件加在 2.4-GHz 低雜訊放大器上模擬電路特性。

關鍵字：靜電放電、低雜訊放大器、堆疊式二極體內嵌入式矽控整流器、垂直式 NPN。

ESD Protection Design with Ultra-Low Parasitic Capacitance

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ABSTRACT

The main thesis of this dissertation is a whole-chip electrostatic discharge (ESD) protection design with ultra-low parasitic, and the ESD devices are applied to radio-frequency integrated circuit (RFIC). The ESD devices are attached to low-noise amplifier (LNA) at 2.4-GHz and 24-GHz in 0.18-μm SiGe BiCMOS and CMOS technologies, respectively.

The stacked diodes with embedded silicon-controlled rectifier (SDeSCR) is designed in 0.18-μm CMOS technology, which has advantages of small layout area, low parasitic capacitance, and strong ESD robustness. In addition, the SDeSCR devices are applied to the 24-GHz LNA, and the function of the LNA with SDeSCR devices is verified. The VNPN device is fabricated in 0.18-μm SiGe BiCMOS technology. The proposed design effectively reduces the trigger voltage of the VNPN device. The characteristics of 2.4-GHz LNA with VNPN devices are simulated.

Keywords: Electrostatic discharge (ESD), low-noise amplifier (LNA), stacked diodes with embedded silicon-controlled rectifier (SDeSCR), vertical NPN (VNPN).

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在國立臺灣師範大學電機工程研究所求學生涯中，有幸認識到不少師長以及同學們，一開始尋找指導教授時，還很害怕找不到適合的指導教授，畢竟在大學的求學階段表現尚可。首先，要感謝我的指導老師林群祐教授，這兩年半來，受到老師的多方面指導，不僅研究要求嚴謹，也提供許多資源給學生使用，像是到國家晶片中心上課和參與國內外研討會。每一次的研究內容與老師討論，老師都會參與討論並適時的給予學生建議，也放手讓學生去做研究，雖然不是每一次的實驗都能獲得預期的結果，但老師還是鼓勵學生從失敗中學習並成長，使得學生現今有著豐碩的研究成果。老師採取的管理方式是讓學生學會自我管理，在既有的時間內自行規畫研究進度，讓學生能夠高效率的做好每一件事情。除了研究上之外，未來的人生方向也能夠與老師討論，老師也會提供意見給與學生參考，使得學生在人生的十字路口中，能夠做一個較佳的選擇並朝未來邁進。

感謝國家晶片中心提供學生良好的資源及環境，讓學生能夠晶片下線與量測，另外也要感謝國立交通大學電子工程學系的柯明道教授以及國立臺北科技大學電子工程學系的劉俊傑教授作為我的口試委員，學生的碩士學位考試能夠邀請到兩位 IEEE fellow 給予論文修改上的意見，使得學生碩士論文更加完整。除此之外，柯明道教授及其研究群也提供學生進行晶片驗證的良好環境，讓學生能夠使用儀器量測數據以利分析。

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黃國倫 謹誌於師大

中華民國一零七年六月

Contents

Table Captions

Figure Captions

Chapter 1

Introduction

1.1 Motivation

Since the development of integrated circuits (ICs), electrostatic discharge (ESD) is always an important reliability issue [1]-[4]. Currently, with the rapid development of CMOS technologies, ESD protection is more important than past. ESD may cause a large current (several amperes) in a short time (nanoseconds), and it often results in damages in IC products and increases defect rate. Many papers have concerned about the ESD issues in CMOS technologies.

CMOS technologies are widely used in the radio-frequency integrated circuits (RFICs) because of the low cost, and the CMOS technologies have been used to implement low-noise amplifier (LNA). The LNA is the input terminal of the RF transceiver [5], which is the most vulnerable to outside interference, such as ESD. When ESD events occur, they may change the original characteristics of the LNA, such as gain decrease and noise figure (NF) increase. In this work, using dual diodes (DD), dual stacked diodes (DSD), and stacked diodes with embedded silicon-controlled rectifier (SDeSCR) be the ESD protection devices. The ESD devices with MOS-based power-rail ESD clamp circuit and SCR-based power-rail ESD clamp circuit form a whole-chip ESD protection circuits.

Using SiGe BiCMOS technology leads to good performances, including low noise, low power consumption, high drive, and high speed [6], and using the vertical NPN (VNPN) devices be an ESD protection devices.

If an ESD stress to the IC, it makes the IC lose its original characteristics, and this is irreversible. Thus, the ESD protection design must be equipped to the IC products. To improve the ESD robustness, adding effective on-chip ESD protection device is a good way to prevent IC from ESD damages. This thesis presents innovative ESD device design, and the ESD devices are applied to the LNA to achieve whole-chip ESD protection design. In addition, the advantages and disadvantages of proposed ESD devices are also compared with the conventional ESD protection devices.

1.2 Background of ESD

Electrostatic discharge (ESD) is an inevitable problem. With the progress of technology, the problems of ESD is more and more serious. Every kind of product must pass the safety test before it is shipped. Different tests have different industry standards. The approaches of common test have human-body model (HBM), machine model (MM), charged-device model (CDM). These test methods have different standards in component-level ESD test. The other is system-level ESD test that uses ESD gun to test the products.

1.3 Standard of Component-Level ESD Test

A general ESD protection window is shown in Fig. 1.1 [7], where the protection device should turn-on in the specified region defined by the supply voltage (V_{DD}) and the internal circuit breakdown voltage (V_{BD}). If the holding voltage (V_h) is lower than V_{DD}, there will be latch-up issues [8]. If the trigger voltage (V_{t1}) is higher than V_{BD}, the circuit cannot be protected from ESD damage [9]. The designers must make sure that the ESD protection device conforms to the ESD protection window.

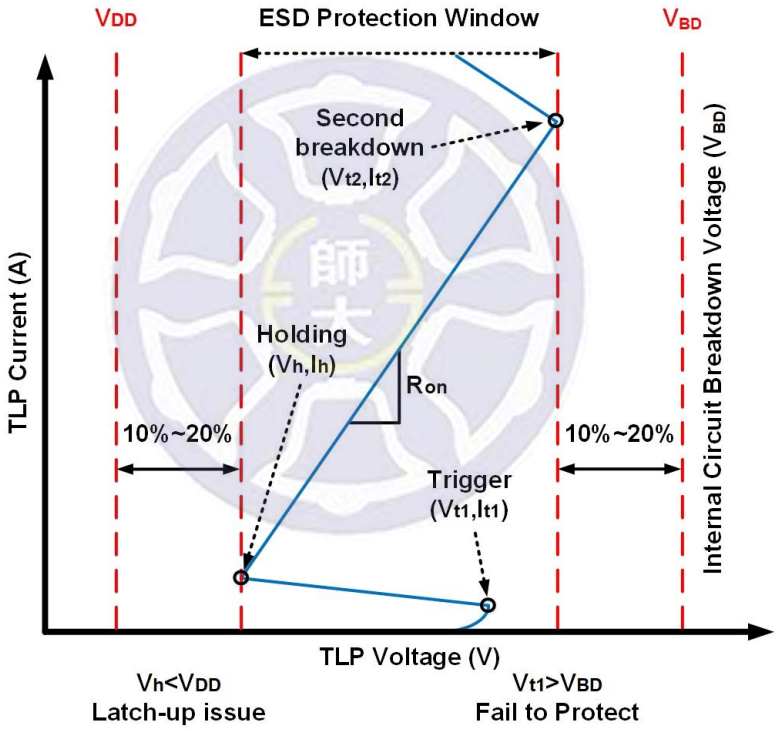


Fig. 1.1. ESD protection window.

In component-level, using transmission-line-pulsing (TLP) system observes the I-V characteristics of the ESD devices [10], [11]. Besides, using ESD simulator tests the HBM ESD robustness [12], [13], and the result is an important indicator of the IC reliability. The common tests have HBM, MM, and CDM, and its equivalent circuits are shown in Fig. 1.2. The equivalent capacitance and resistance of the HBM are 100pF and 1.5kΩ, respectively. The equivalent capacitance and resistance of the MM are 200pF and 0Ω, respectively. The ICs accumulate charge during the fabrication process. Charged ICs touch other objects can cause self-discharge situation, so this situation may make the ICs defeat. The above phenomenon is called CDM. Table 1.1 shows the standards of the HBM and MM ESD level according to industry council on ESD target levels [14]. Table 1.2 shows the standards of the CDM ESD level according to industry council on ESD target levels [15]. The white paper 1 explains that the MM test is no needed, and JEDEC documents provide sufficient evidence to prove that and stop using the test model [16], [17]. Because the HBM and CDM test are sufficient to test the ESD robustness of the IC in component-level ESD.

The study of this work is based on wafer level, so the HBM ESD event is the primary concern, and the CDM test item is not tested in this work.

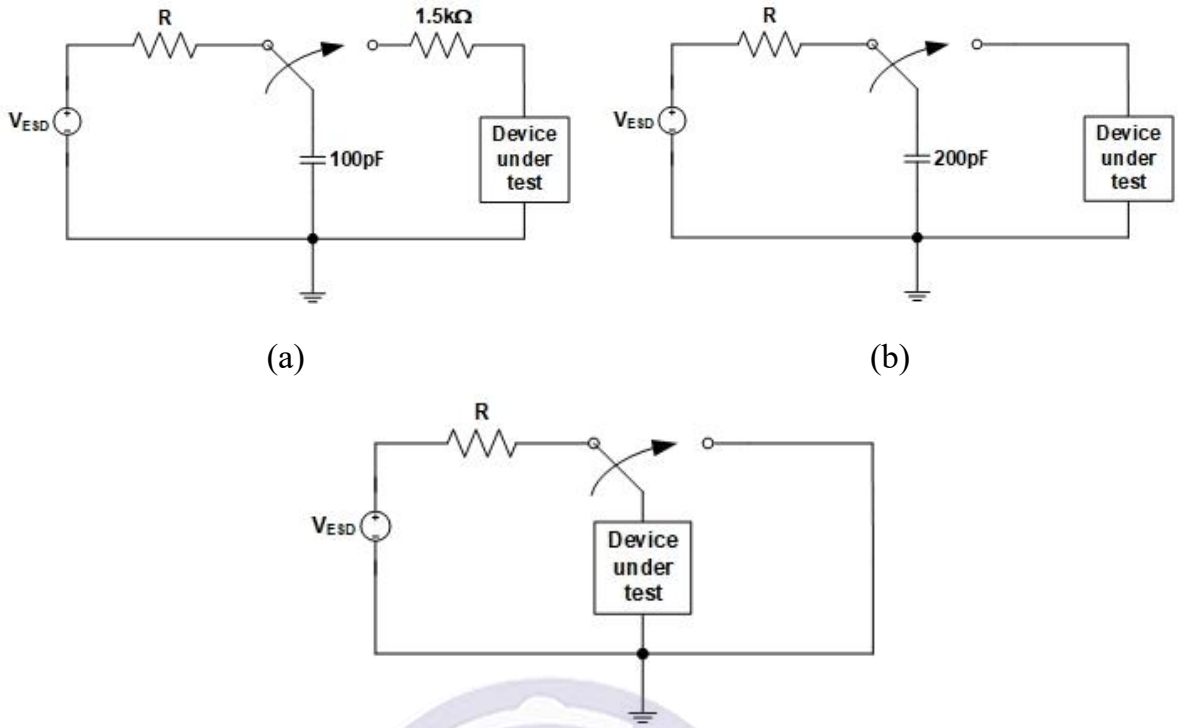


Fig. 1.2. The equivalent circuit of (a) human-body model (HBM), (b) machine model (MM), and (c) charged-device model (CDM).

Table 1.1

Standards of HBM ESD level.

HBM ESD Level	**Impact on Manufacturing Environment**
100V to < 500V	Detailed ESD control method are required.
500V	Basic ESD control methods allows safe manufacturing with proven margin.
1kV	
2kV	

Table 1.2

Standards of CDM ESD level.

CDM ESD Level	ESD Control Requirements
$V_{CDM} \leq 125V$	◆ Basic ESD control methods with grounding of metallic machine parts and control of insulators. ◆ Process specific measures to reduce the charging of the device or to avoid a hard discharge. ◆ Charging/discharging measurements at each process step.
$125V \leq V_{CDM} \leq 250V$	◆ Basic ESD control methods with grounding of metallic machine parts and control of insulators. ◆ Process specific measures to reduce the charging of the device or to avoid a hard discharge.
$V_{CDM} \geq 250V$	◆ Basic ESD control methods with grounding of metallic machine parts and control of insulators.

1.4 Background of Whole-Chip ESD Protection for RF Circuits

Nowadays, with the rapid development of CMOS technologies, the problem caused by ESD is more and more important. The ESD problem is inevitable in the fabrication process of the chips. To avoid these problems, adding a whole-chip ESD protection circuit to the IC prevents the IC from ESD damage during the fabrication process. The input and output of the circuits are most vulnerable to ESD events. The ESD events cause circuit original characteristics change, and this is an irreversible phenomenon. The input and output of the RF transceiver architecture are a low-noise amplifier (LNA) and a power amplifier (PA), respectively, as shown Fig. 1.3 [18]. The ESD events will bring the impact of the RF circuits such as gain decrease, noise figure (NF) increase. Therefore, both circuits need a whole-chip ESD protection circuit to protect and prevent the ESD events.

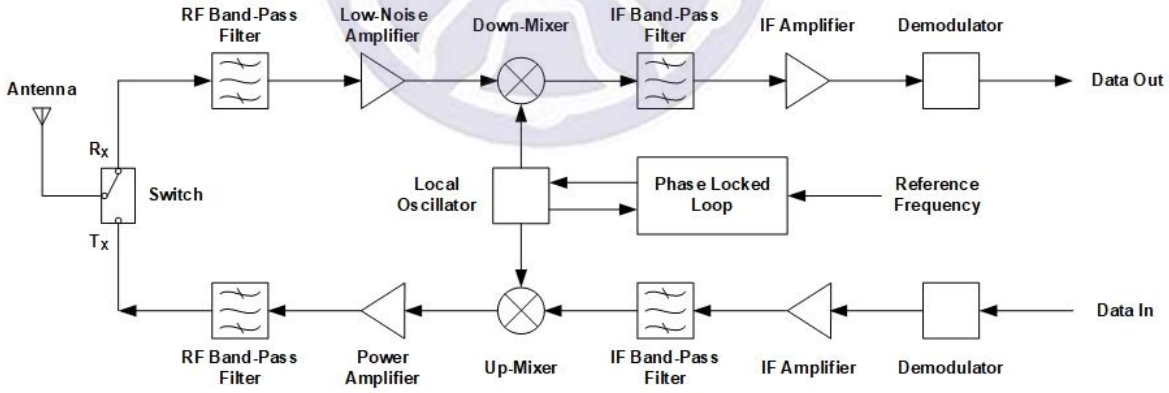


Fig. 1.3. RF transceiver architecture.

The ESD protection devices are used in high-frequency circuit design. However, the ESD devices cause the signal loss [19], [20], as shown in Fig. 1.4, so the high-frequency circuit will be affected by the parasitic effect of the ESD devices. The ESD devices and matching network of the high-frequency circuits must be co-designed. The ESD device be a part of the matching network, and adding the resistor, inductor, and capacitor components adjust the impedance matching point. The ESD devices are applied to the high-frequency circuit and simulate the effect of the ESD devices on the circuit.

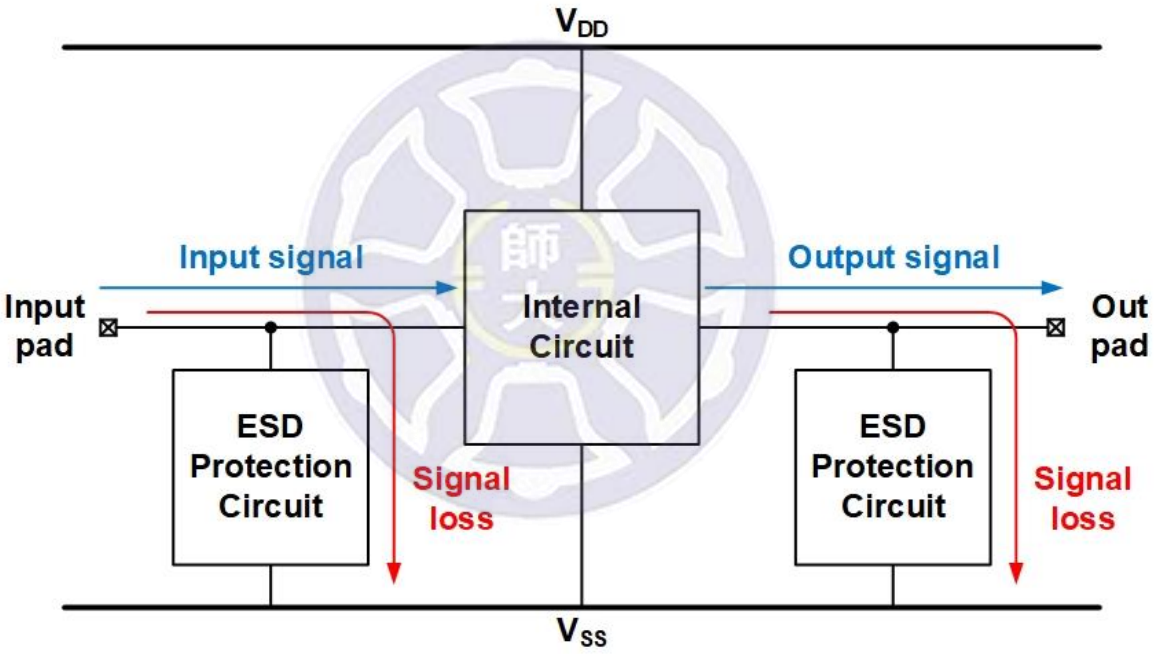


Fig. 1.4. Signal loss of ESD protection circuit at input and output pads.

The ESD protection devices are located at the I/O pad to V_{DD} and the I/O pad to V_{SS}, respectively. This purpose prevents the ESD currents flowing into the internal circuit. In addition, the power-rail ESD clamp circuit is located between V_{DD} and V_{SS} to prevent the ESD currents flowing into the internal circuit. As shown in Fig. 1.5, the conventional whole-chip ESD protection design has six ESD paths [21]. For positive

voltage at I/O pad with grounded V_{SS}, the ESD currents flow from I/O pad to V_{SS}, which is named PS mode. For negative voltage at I/O pad with grounded V_{SS}, the ESD currents flow from V_{SS} to I/O pad, which is named NS mode. For positive voltage at I/O pad with grounded V_{DD}, the ESD currents flow from I/O pad to V_{DD}, which is named PD mode. For negative voltage at I/O pad with grounded V_{DD}, the ESD currents flow from V_{DD} to I/O pad, which is named ND mode. For positive voltage at V_{DD} with grounded V_{SS}, the ESD currents flow from V_{DD} to V_{SS}, which is named PDS mode. For negative voltage at V_{SS} with grounded V_{DD}, the ESD currents flow from V_{SS} to V_{DD}, which is named NDS mode.

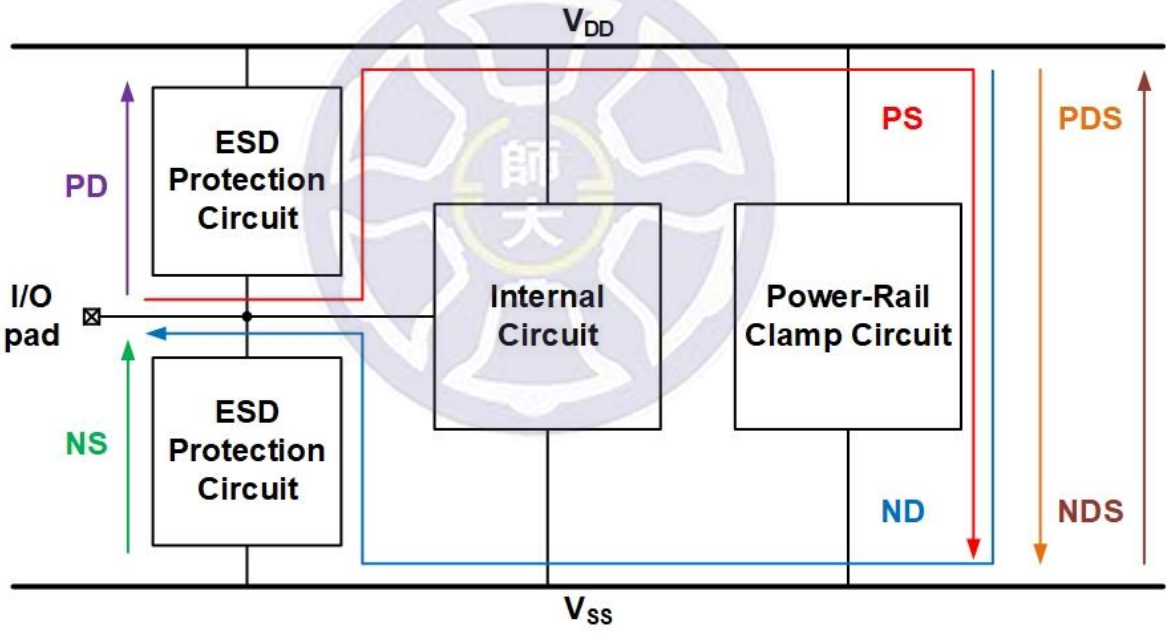


Fig. 1.5. The conventional whole-chip ESD protection design.

1.5 Organization of This Thesis

In this thesis, the motivation, background, and the standard of the ESD test have been introduced. The background of a whole-chip ESD protection for radio-frequency circuits will be introduced in chapter 1. Chapter 2 discusses the traditional ESD devices and proposed different types stacked diodes with embedded silicon-controlled rectifier (SDeSCR), and the ESD devices collocate the MOS-based or SCR-based power-rail ESD clamp circuit. The 24-GHz LNA with traditional devices and SDeSCR devices are discussed in chapter 3. Chapter 4 discusses the 2.4-GHz LNA with vertical NPN (VNPN) devices in 0.18-μm silicon-germanium (SiGe) BiCMOS technology. Chapter 5 summarizes all the key points of thesis and derives the future work.

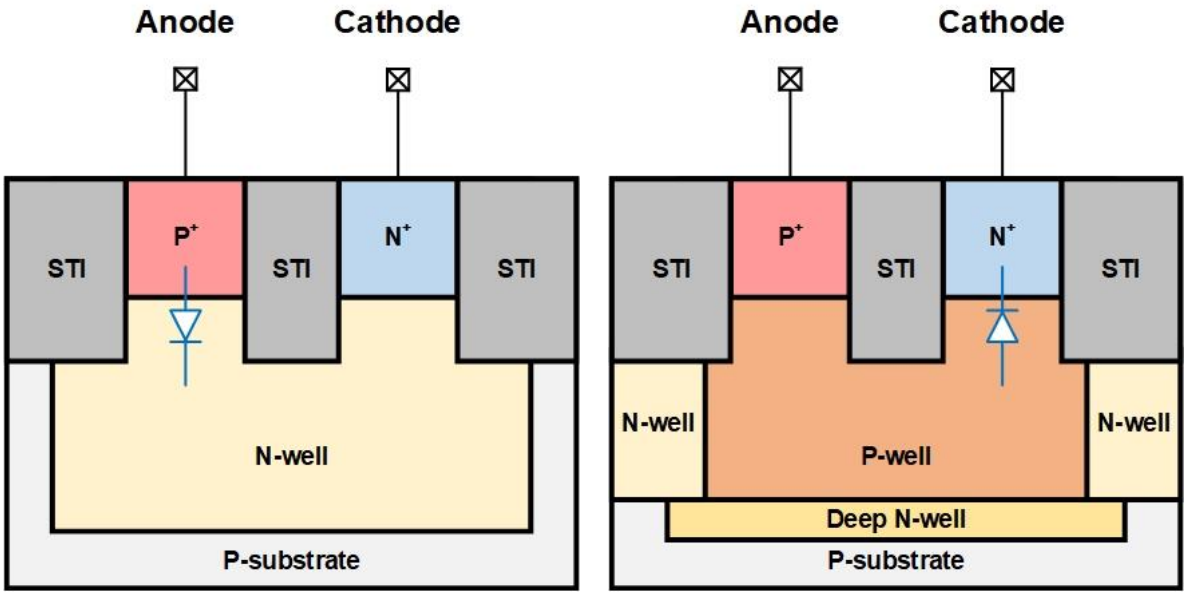
Chapter 2

Design of Whole-Chip ESD Protection Circuit in CMOS Technology

2.1 Structure of ESD Devices

2.1.1 Diode

Diode is a common component, and it is not only applied widely to different circuits, but also be used as ESD devices. The diode forward breakdown voltage is about 0.7V, and the reverse breakdown voltage is about 10V or even more. In different structures and processes have different differences. The p-type diode consists of P^+, N-well, N^+, and P-substrate, and the shallow trench isolation (STI) isolates P^+ and N^+, from thee anode to cathode forms a forward diode, as shown in Fig. 2.1(a). The n-type diode consists of P^+, P-well, N-well, deep N-well, N^+, and P-substrate. STI isolates P^+ and N^+, and the deep N-well isolates P-well and P-substrate. A forward diode are formed from the anode to cathode, as shown in Fig. 2.1(b).



(a) (b)

Fig. 2.1. The cross-sectional view of (a) p-type and (b) n-type diodes.

In whole-chip ESD protection design, the diode is located between I/O pad and V_{DD} or V_{SS}, which is named dual diodes (DD), as shown in Fig. 2.2 [21]. DD architecture is typical design. The diode is equivalent to the capacitor, and the parasitic capacitance of DD between I/O pad and ground is the sum of the two diodes.

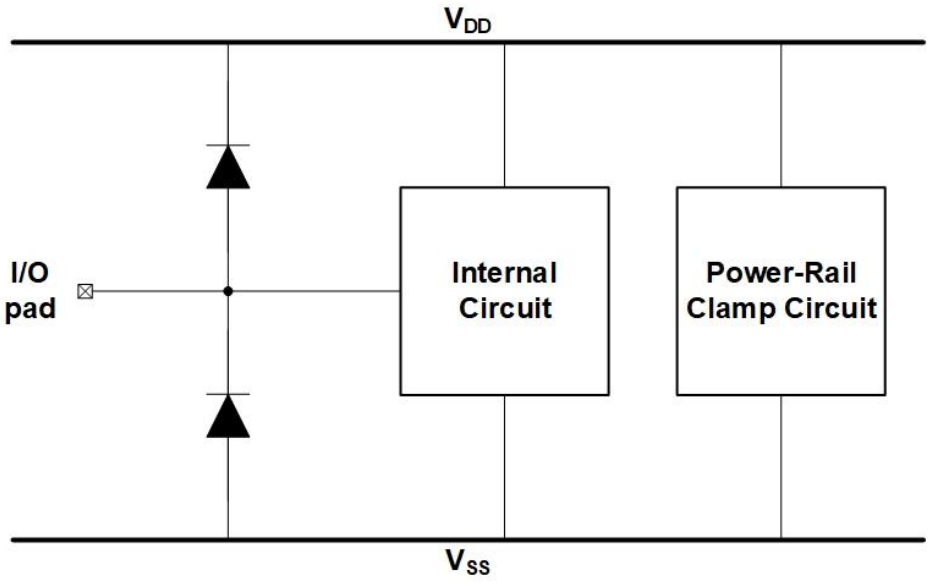


Fig. 2.2. Whole-chip ESD protection with dual diodes.

The other whole-chip ESD protection design uses stacked diodes. The stacked diodes are connected between I/O pad and V_{DD} and between V_{SS} to I/O pad, which is named dual stacked diodes (DSD), as shown in Fig. 2.3 [22], [23]. The parasitic capacitance of DSD architecture is half of DD architecture, which is the same as the parasitic capacitance of a diode. The ESD robustness of DSD architecture is higher than DD architecture, but trigger voltage of DSD architecture also increases. Therefore, the stacked diodes must consider operating voltage and choose the appropriate for number of stacks, or components in the normal operating voltage will produce unnecessary leakage current to result power consumption increases.

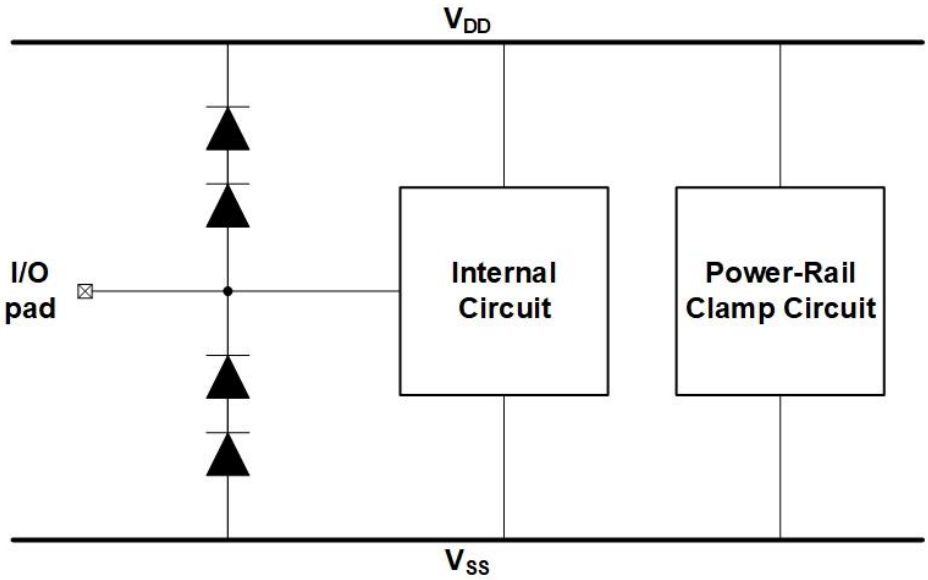
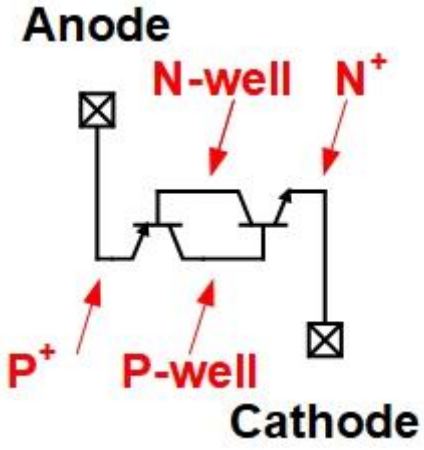


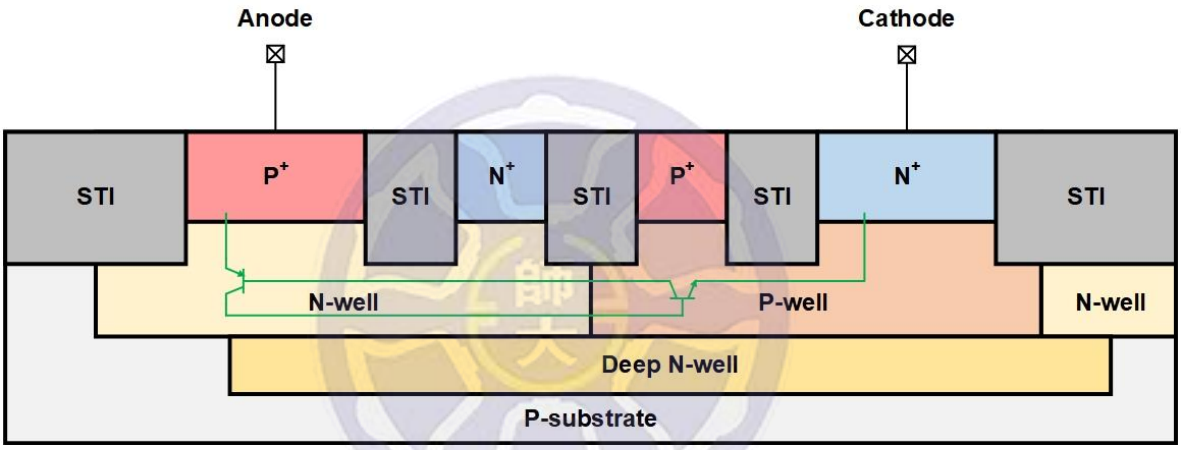
Fig. 2.3. Whole-chip ESD protection with dual stacked diodes.

2.1.2 Silicon-Controlled Rectifier

The silicon-controlled rectifier (SCR) device has advantages of low loss, low parasitic capacitance, low clamping voltage, and small layout area [24]-[27]. The SCR has features of low holding voltage and high trigger voltage. As shown in Fig. 2.4, the SCR consists of P^+, N-well, deep N-well, P-well, N^+, and P-substrate. The latch-up is a serious issue for SCR, which causes the current to gradually increase until the device burns because of the positive feedback mechanism. The other problem is that the breakdown voltage of N-well to P-well junction is related to the trigger voltage of the SCR. The ESD currents flow from the anode to cathode through P^+, N-well, P-well, and N^+. The N-well and the P-well form a reverse diode resulting in the breakdown voltage of the SCR increase. Therefore, the drawback of repairing SCR is the main purpose.



(a)



(b)

Fig. 2.4. (a) The equivalent circuit and (b) the cross-sectional view of SCR.

2.1.3 Stacked Diode with Embedded Silicon-Controlled Rectifier

In order to mend the shortcomings of the SCR, the stacked diode with embedded SCR (SDeSCR) device has been presented [28]. The base of PNP and NPN bipolar junction transistor (BJT) are connected together to decrease the trigger voltage of the SCR. The equivalent circuit of the SDeSCR device is shown in Fig. 2.5. The top view and cross-sectional view of type I and type II SDeSCR devices are shown in Fig. 2.6 and Fig. 2.7. The deep N-well is located between P-well and P-substrate, which isolates the electrical potential of the P-well and P-substrate. As shown in Fig. 2.8, if the deep N-well is not implanted in the SCR, the diode is formed from the anode to N-well, and the N-well, P-well, and P-substrate have the same potential. Therefore, the path from the anode to the cathode is not the originally designed p-n-p-n junction. In Fig. 2.6(a), reducing the base size decreases the turn-on resistance of the SDeSCR device and improves the ESD robustness. If the base size is too large, the resistance will increase proportionally, so that the parasitic SCR is not easy to be triggered. Fig. 2.6(b) shows the type II SDeSCR device, the positions of P^+ and N-well as well as N^+ and P-well are swapped. The distance of the anode to the cathode is shortened to reduce the trigger voltage of the SDeSCR device. The size of type I and type II SDeSCR devices are based on that the ratio of SCR width (W_{SCR}) to base width (W_{base}) is 10 to 1 and 20 to 1. In type I and type II SDeSCR devices, W_{SCR} and W_{base} are equal W_1 and W_2.

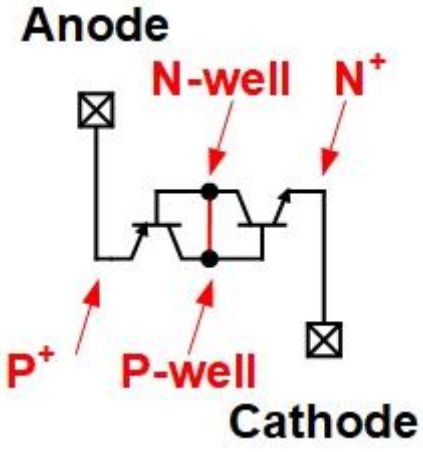
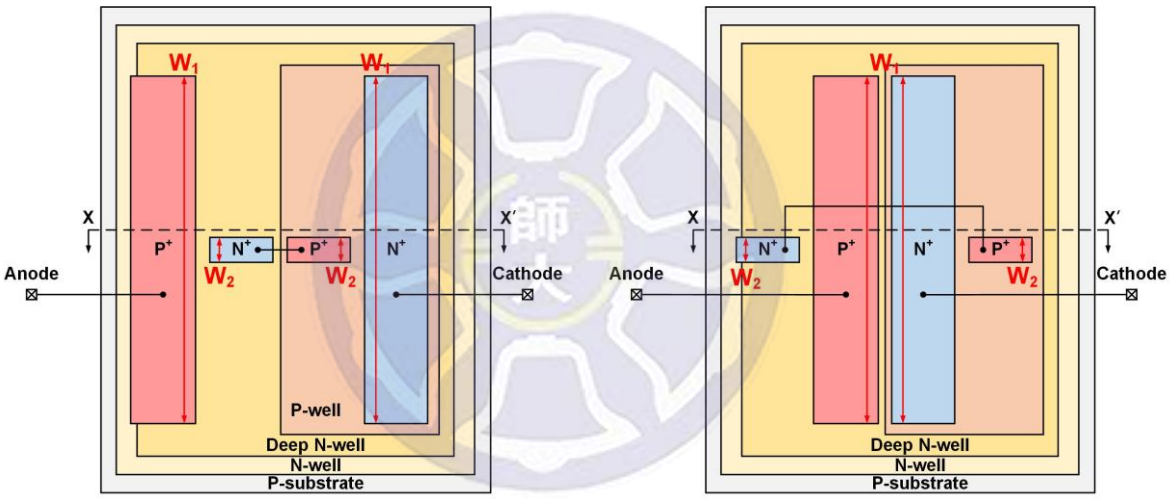
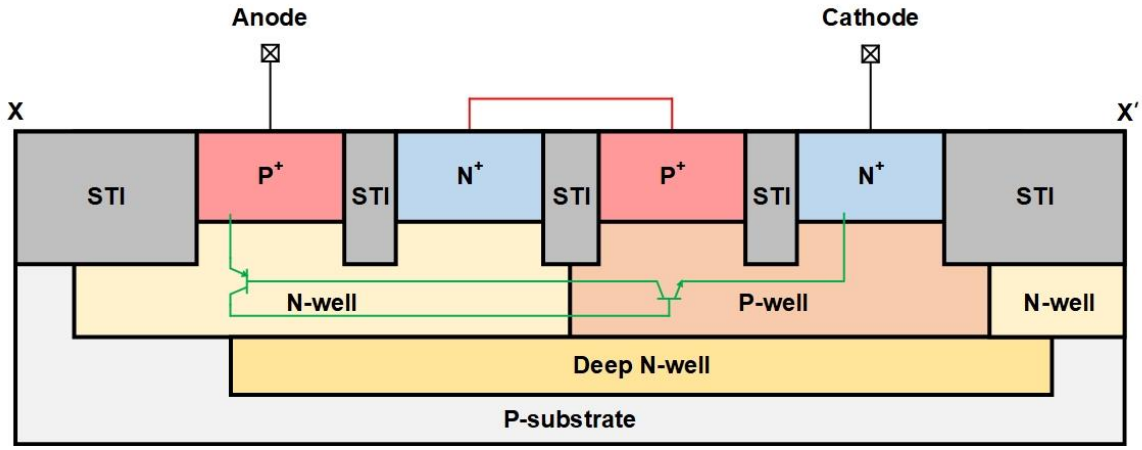


Fig. 2.5. The equivalent circuit of SDeSCR device.

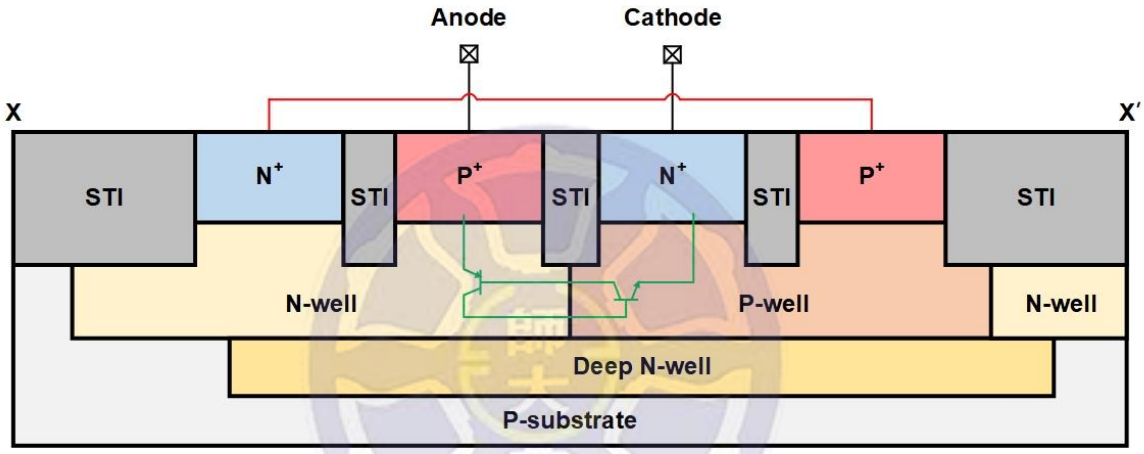


(a) (b)

Fig. 2.6. The top view of (a) type I and (b) type II SDeSCR devices.



(a)



(b)

Fig. 2.7. The cross-sectional view of (a) type I and (b) type II SDeSCR devices.

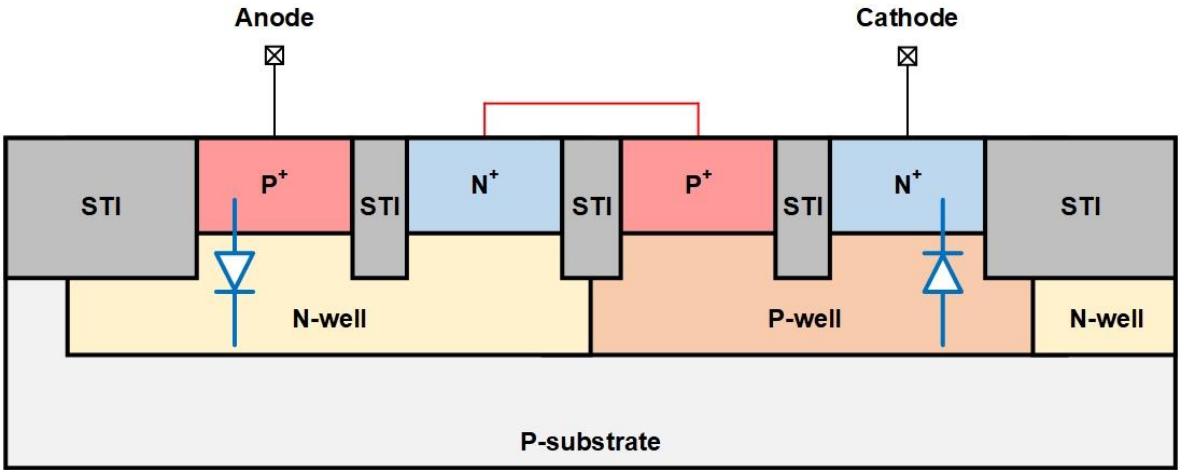
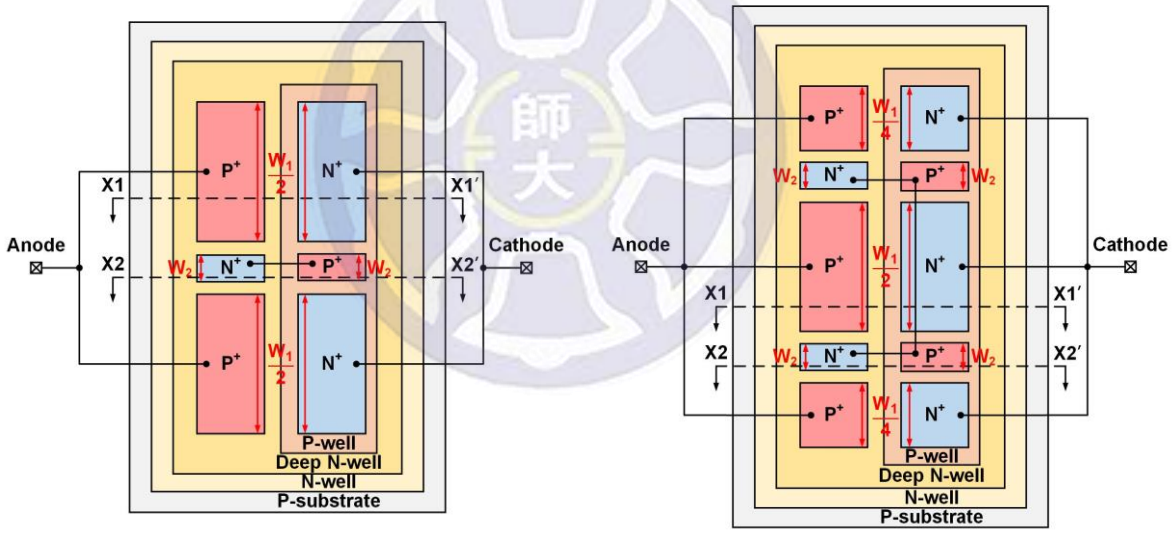


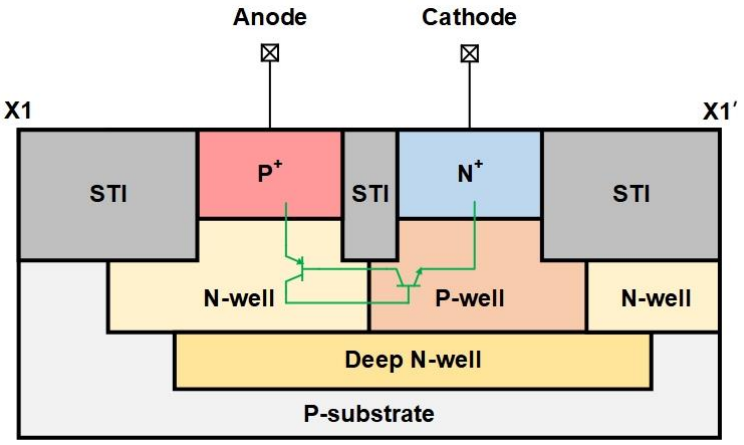
Fig. 2.8. The cross-sectional view of SDeSCR devices without deep N-well.

Further design in Fig. 2.9, the cross-sectional of type III and type IV SDeSCR devices is shown in Fig. 2.10, these designs combine the above advantages. In Fig. 2.9(a), P^+ of the anode and N^+ of the anode are divided into two segmentations. Another N^+ and P^+ are inserted into P^+ of the anode and N^+ of the cathode, respectively. Both designs shorten the distance of the anode to cathode and insert N^+ and P^+ into P^+ of the anode and N^+ of the cathode to make the SDeSCR devices more uniform conduction. The W_{SCR} and W_{base} are $2\times\frac{W_1}{2}$ and W_2. In Fig. 2.9(b), P^+ of the anode and N^+ of the anode are divided into three segmentations, and the W_{SCR} is the sum of the $\frac{W_1}{2}$ and $2\times\frac{W_1}{4}$, and the W_{base} is the sum of the $2\times W_2$.

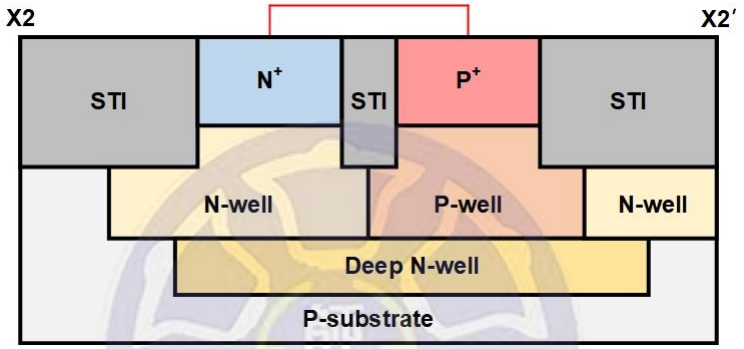


(a) (b)

Fig. 2.9. The top view of (a) type III and (b) type IV SDeSCR devices.



(a)



(b)

Fig. 2.10. The cross-sectional view of type III and type IV SDeSCR devices: (a) from X1 to X1' and (b) from X2 to X2'.

2.2 Design of Power-Rail ESD Clamp Circuit

2.2.1 MOS-Based Power-Rail ESD Clamp Circuit

The MOS-based power-rail ESD clamp circuit consist of resistor, capacitor, inverter, and large size NMOS and connects between V_{DD} and V_{SS}, as shown in Fig. 2.11. When ESD hits V_{DD}, the capacitor is not yet charged. V_A is low and V_B is high, so M_{big} will be turned on and discharge the ESD currents. In normal operation, the capacitor charges with the RC time constant. The V_A is high, and the V_B is low, so M_{big} will be turned on

and discharge the ESD currents. This architecture has two drawbacks. One is that the V_A potential rises with the RC time constant. The ESD pulse is not yet over, the V_A potential may change from low to high, and the V_B potential change from high to low, so M_{big} turn off. Therefore, the M_{big} cannot discharge the ESD currents, in which case internal circuit may be suffered ESD damage. The ESD robustness improves as the size of M_{big} increases, but the leakage current increases accordingly. The ESD events happen in dozens to hundreds of nanoseconds, and the power supply turns on at the milliseconds. In design, the RC time constant is designed at the microseconds. Therefore, the resistance and capacitance use 10kΩ and 10pF, respectively.

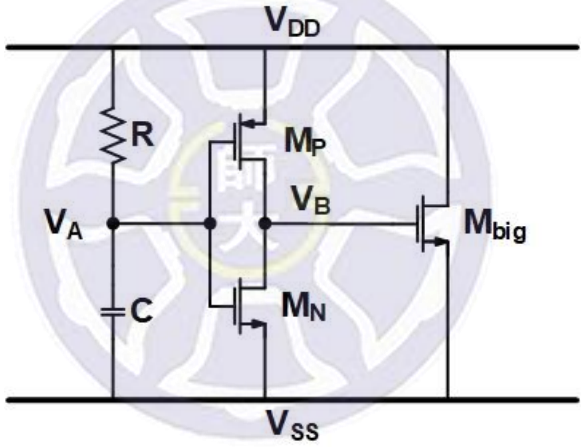


Fig. 2.11. MOS-based power-rail ESD clamp circuit.

2.2.2 SCR-Based Power-Rail ESD Clamp Circuit

The SCR-based power-rail ESD clamp circuit is connected between V_{DD} and V_{SS}, and a forward diode is connected between V_{SS} and V_{DD}. The SCR-based power-rail ESD clamp circuit has a lower leakage current and a smaller layout area than MOS-based power-rail ESD clamp circuit [29]. In SCR-based power-rail ESD clamp circuit, base of NPN BJT and base of PNP BJT connect trigger diodes. The diode between V_{SS} and V_{DD} (D_{SD}) is designed to discharge the ESD currents from V_{SS} to V_{DD}, as shown in Fig. 2.12.

As a result, using SCR as a power-rail ESD clamp circuit is more practical than MOS-based power-rail ESD clamp circuit. In next section, it will introduce the design of ESD device combined with power-rail ESD clamp circuit.

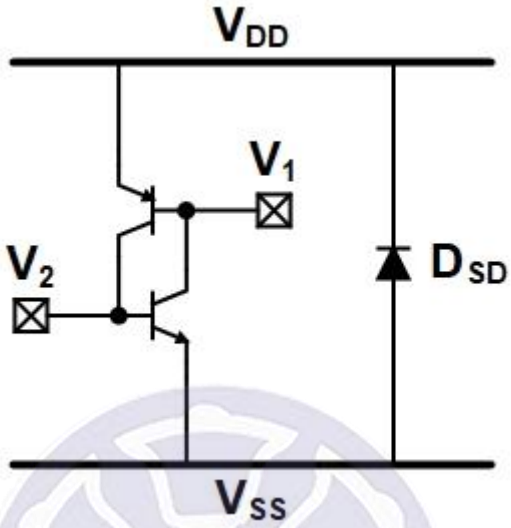


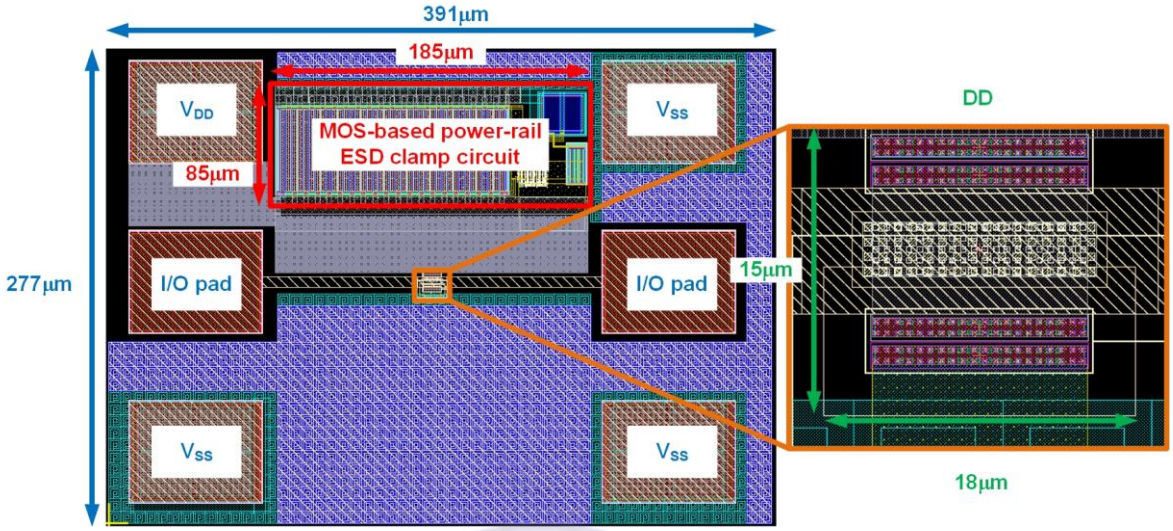
Fig. 2.12. SCR-based power-rail ESD clamp circuit.

2.3 Whole-Chip ESD Protection Design

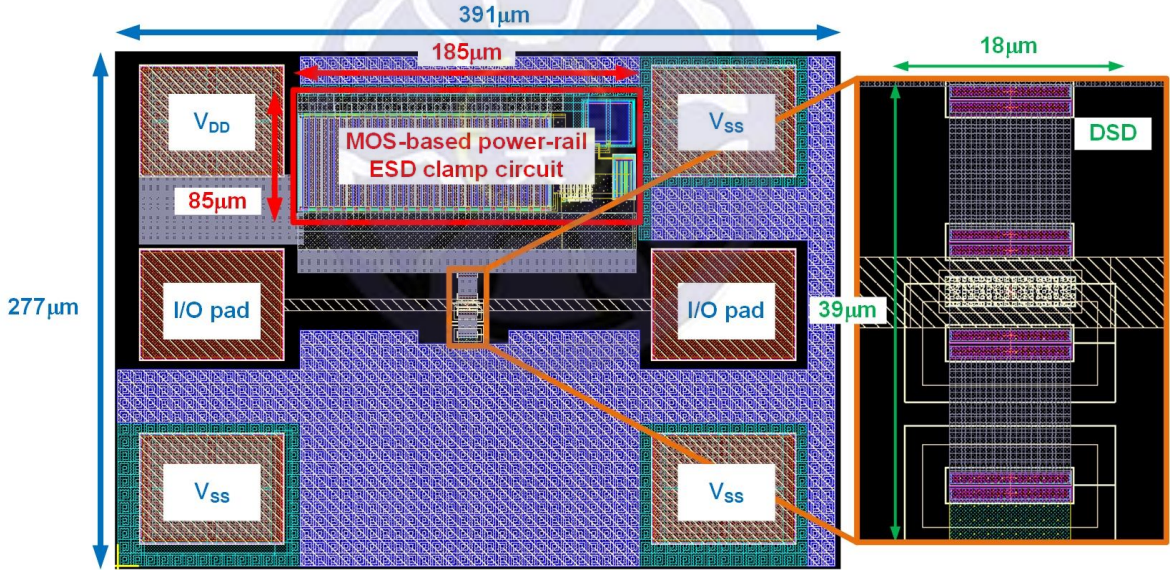
2.3.1 DD and DSD Devices with MOS-Based Power-Rail ESD Clamp Circuit

After the ESD devices operating principle are explained, the DD device is attached to I/O pad of internal circuit, and the MOS-based power-rail ESD clamp circuit is connected between V_{DD} and V_{SS}. The DD device with MOS-based power-rail ESD clamp circuit is named DD_MOS [30], [31]. The DSD device is attached to I/O pad of internal circuit, and MOS-based power-rail ESD clamp circuit is connected between V_{DD} and V_{SS}. The DSD device with MOS-based power-rail ESD clamp circuit is named DSD_MOS. The layout top view of DD_MOS and DSD_MOS is shown in Fig. 2.13(a) and 2.13(b), respectively. The layout area of DD device, DSD device, and MOS-based

power-rail ESD clamp circuit are 270 μm^2, 702 μm^2, and 15725 μm^2.



(a)



(b)

Fig. 2.13. The layout top view of (a) DD_MOS and (b) DSD_MOS.

2.3.2 DSD Device with SCR-Based Power-Rail ESD Clamp Circuit

The DSD device is attached to I/O pad of internal circuit, and the SCR-based power-rail ESD clamp circuit is connected between V_{DD} and V_{SS}. The DSD device with SCR-based power-rail ESD clamp circuit is named DSD_SCR, as shown in Fig. 2.14 [27]. Besides, two trigger diodes (D_{t1} and D_{t2}) are connected between DSD device and SCR-based power-rail ESD clamp circuit. The functions of the trigger diodes also include to decrease the leakage current from V_{DD} to V_{SS} because the trigger path has six diodes from V_{DD} to V_{SS}. The six diodes include (1) emitter/base junction of PNP in SCR between V_{DD} and V_{SS}, (2) D_{t2}, (3) base/emitter junction of NPN in SDeSCR device between V_{SS} and I/O pad, (4) emitter/base junction of PNP in SDeSCR device between I/O pad and V_{DD}, (5) D_{t1}, and (6) base/emitter junction of NPN in SCR between V_{DD} and V_{SS}. The layout top view of DSD_SCR is shown in Fig. 2.15, and the layout area of DSD device and SCR-based power-rail ESD clamp circuit is 702 μm^2 and 3640 μm^2.

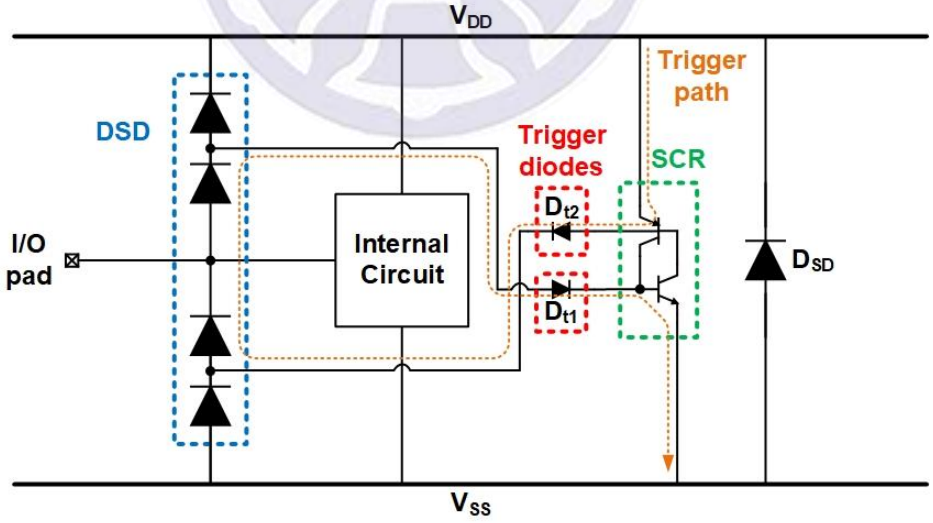


Fig. 2.14. Whole-chip ESD protection of DSD_SCR.

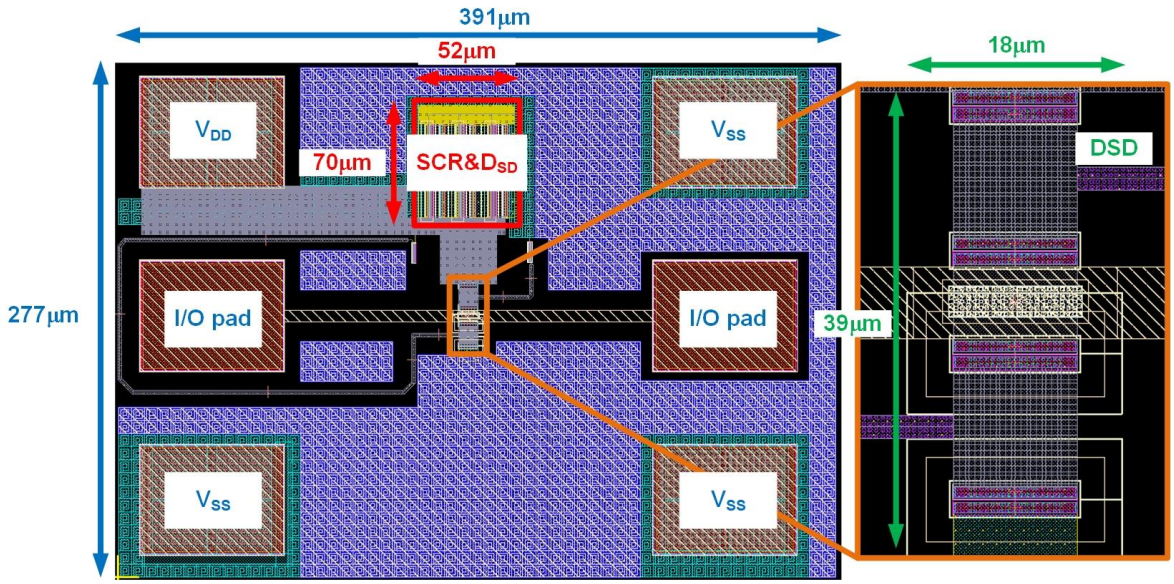


Fig. 2.15. The layout top view of DSD_SCR.

2.3.3 SDeSCR Devices with SCR-Based Power-Rail ESD Clamp Circuit

The proposed SDeSCR device is attached to I/O pad of internal circuit, and the SCR-based power-rail ESD clamp circuit is connected between V_{DD} and V_{SS}. Combing the SDeSCR device and SCR-based power-rail ESD clamp circuit is named SDeSCR_SCR, as shown in Fig. 2.16. The D_{t1} and D_{t2} are connected between SDeSCR devices and SCR-based power-rail ESD clamp circuit. The trigger diodes trigger the SCR between V_{DD} and V_{SS} and decrease the trigger voltage of the SCR. As shown in Fig. 2.17, if deep N-well is not implanted in SCR, a SDeSCR device is formed two diodes. In normal operation, the leakage current will be larger because the bias voltage is 0.8V at I/O pad, as shown in Fig. 2.18. The ESD paths will be different from the originally designed paths. For positive voltage at I/O pad with grounded V_{SS}, the ESD currents flow from I/O pad to V_{SS} through a diode formed by SDeSCR device. For positive voltage at I/O pad with grounded V_{DD}, the ESD currents flow from I/O pad to V_{DD} through two diodes: (1) a diode formed by SDeSCR device and (2) D_{SD}. For negative voltage at I/O pad with grounded V_{SS}, the ESD currents flow from V_{SS} to I/O

pad through a diode formed by SDeSCR device. For negative voltage at I/O pad with grounded V_{DD}, the ESD currents flow from V_{DD} to I/O pad through three diodes: (1) a diode formed by SCR, (2) D_{t2}, and (3) a diode formed by SDeSCR device. Although SDeSCR_SCR without deep N-well still has the ability to discharge the ESD currents, the proposed design is to mend the shortcomings of diode. The diode has high turn-on resistance and high parasitic capacitance. Therefore, the deep N-well for SCR is very important. The layout top view of different types SDeSCR_SCRs is shown in Fig. 2.19 and Fig. 2.20. The minimum size of type I, type II, type III, and type IV SDeSCR devices layout area is 414 μm^2, 396 μm^2, 380 μm^2, and 420 μm^2, respectively, and the SCR-based power-rail ESD clamp circuit between V_{DD} and V_{SS} is 3640 μm^2.

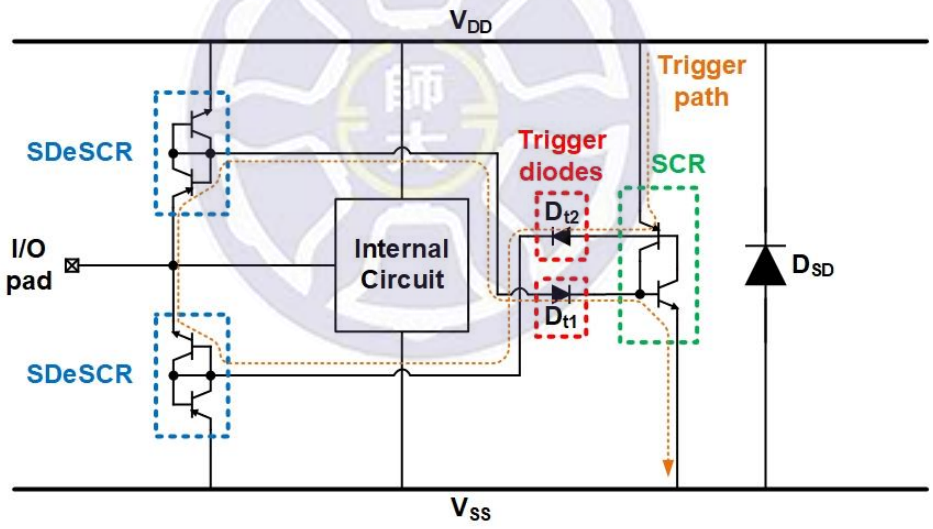


Fig. 2.16. Whole-chip ESD protection of SDeSCR_SCR.

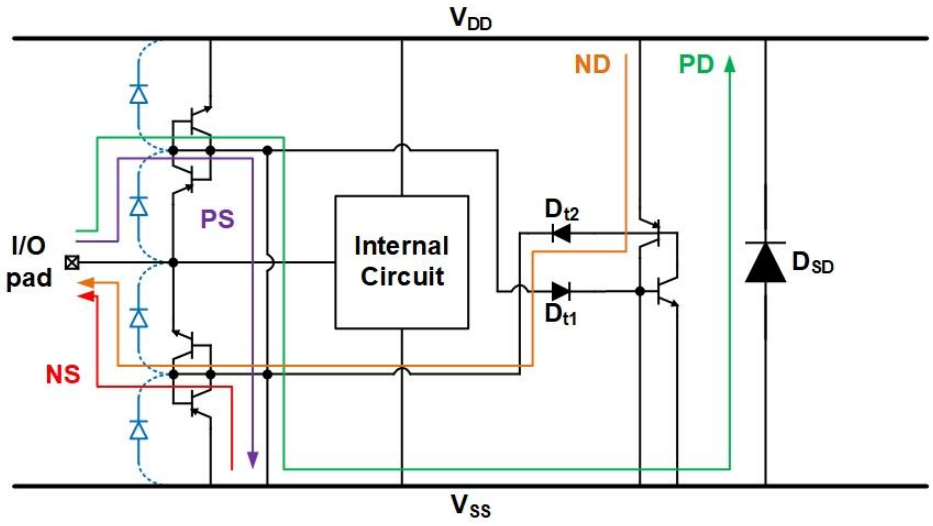


Fig. 2.17. The ESD paths of SDeSCR_SCR without deep N-well.

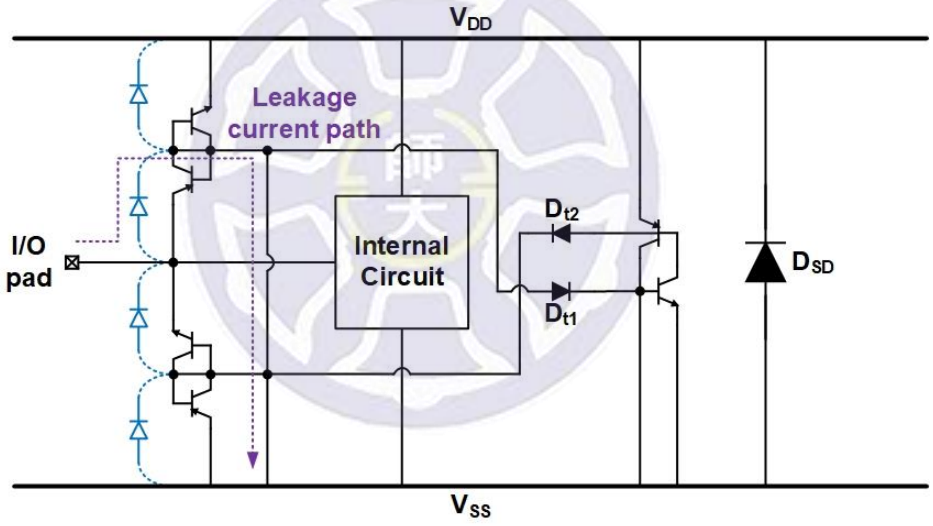
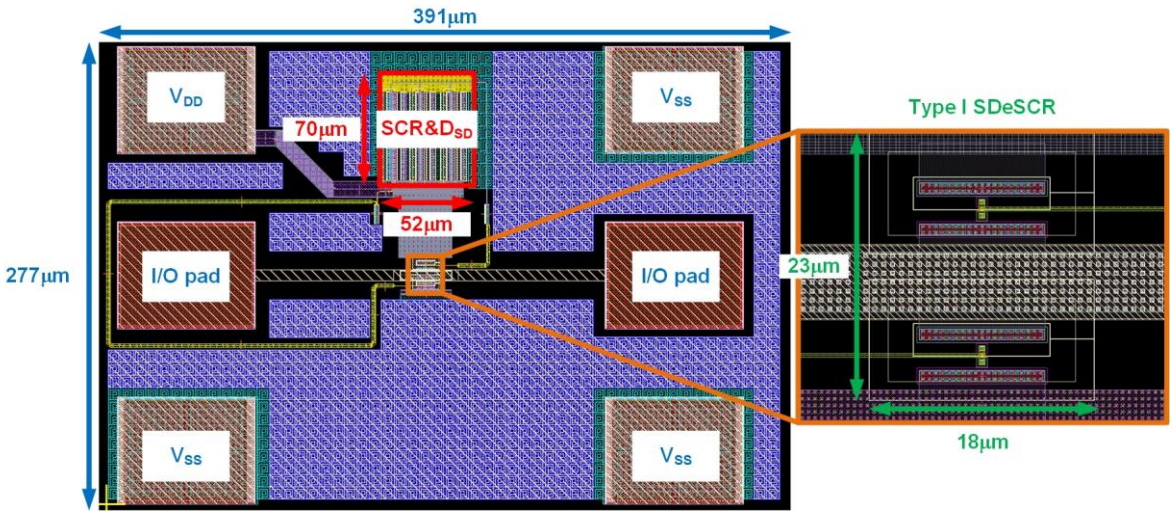
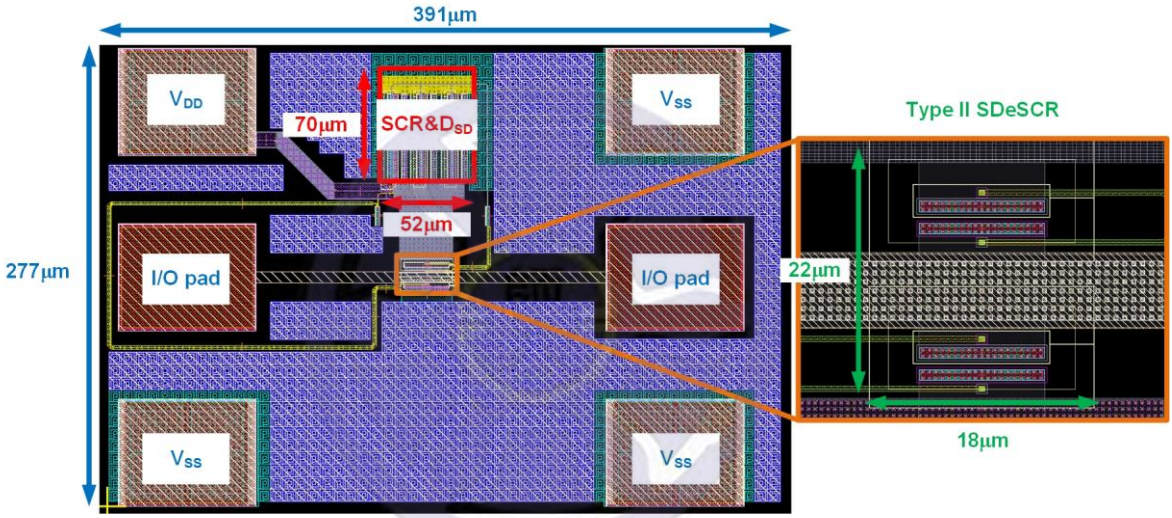


Fig. 2.18. The leakage current path of SDeSCR_SCR without deep N-well in normal operation.

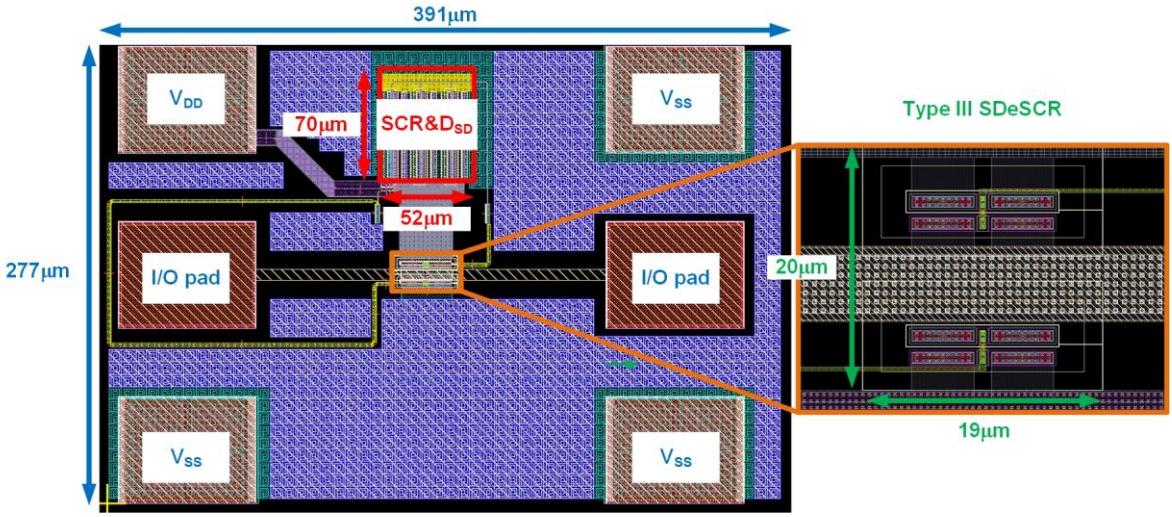


(a)

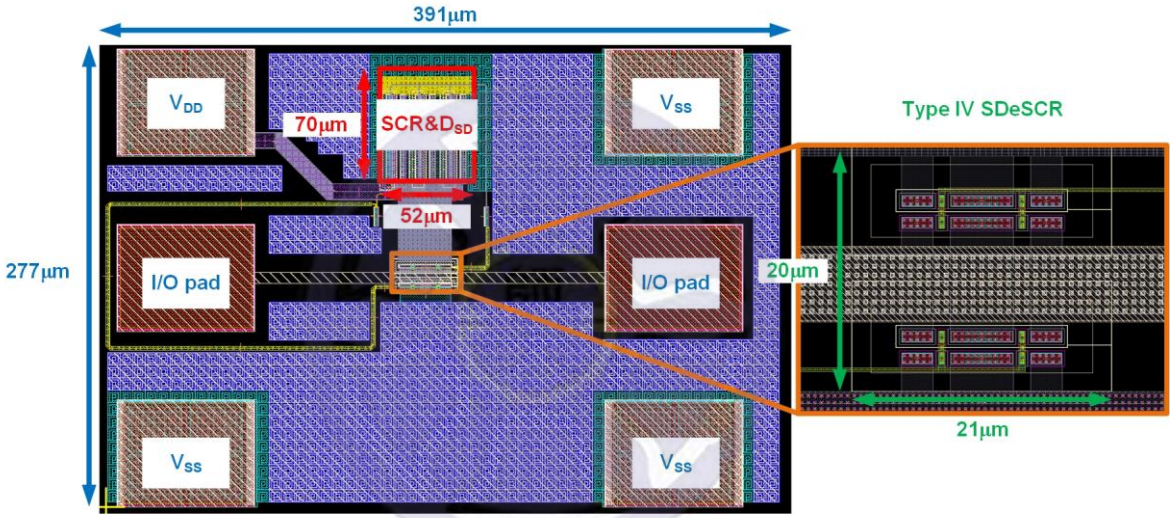


(b)

Fig. 2.19. The layout top view of (a) type I and (b) type II SDeSCR_SCRs.



(a)



(b)

Fig. 2.20. The layout top view of (a) type III and (b) type IV SDeSCR_SCRs.

2.4 Verification of Test Devices

2.4.1 Parameters of Test Devices

The sizes of test devices are shown in Table 2.1, the traditional devices include DD_MOS, DSD_MOS, and DSD_SCR, and the diode width is 10 μm. The proposed four types SDeSCR devices are designed different layout styles. The W_{SCR} has 10 μm and 25 μm sizes, and the ratio of W_{SCR} to W_{base} is 10 to 1 and 20 to 1. The SDeSCR

devices follow that the ratio of W_{SCR} to W_{base} is 10 to 1 and 20 to 1 expect type IV SDeSCR device. In type IV SDeSCR devices, the ratio of W_{SCR} to W_{base} of 20 to 1 cannot be achieved because the layout is limited to 0.18-μm CMOS process.

Table 2.1

The sizes of traditional devices and SDeSCR_SCRs.

Test devices		Diode width (μm)	
DD_MOS		10	
DSD_MOS		10	
DSD_SCR		10	
Test devices		W_{SCR} (μm)	W_{base} (μm)
SDeSCR_SCR	Type I	10	0.5
			1
		25	1.25
			2.5
	Type II	10	0.5
			1
		25	1.25
			2.5
	Type III	10	0.5
			1
		25	1.25
			2.5
	Type IV	10	1
		25	1.25
			2.5

2.4.2 The Equipment of ESD Test and High-Frequency Measurement

The pictures of TLP system and HBM tester are shown in Fig. 2.21. The TLP system is used to measure the I-V curves of the ESD devices, and the pulse width and pulse rise time are setting 100 ns and 10 ns, respectively. In addition, the ESD stress is divided

into positive or negative voltage. Using HBM tester tests ESD devices and gradually increase the ESD stresses to observe ESD robustness of devices. In high-frequency measurement, all the ground pads are connected together, and both the signal pads are also connected together. One of ground pads is separated and be a power pad, and the parasitic effects of power-rail ESD clamp circuit are not considered, as shown in Fig. 2.22 [32]. The chip photo of traditional devices and SDeSCR_SCRs is shown in Fig. 2.23. The information on the photo clearly shows the sizes and layout location of the test devices, and the layout area of the test devices is about 2.038 mm^2.

(a) (b)

Fig. 2.21. The pictures of (a) TLP system (b) HBM tester.

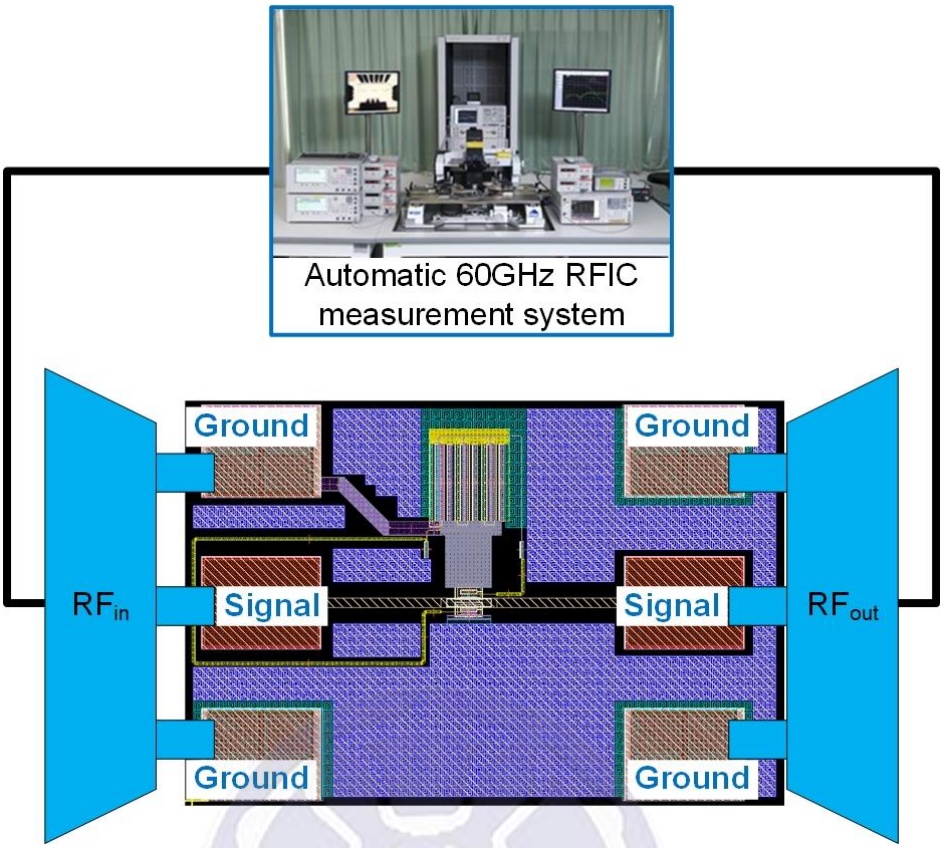


Fig. 2.22. The test devices in high-frequency measurement.

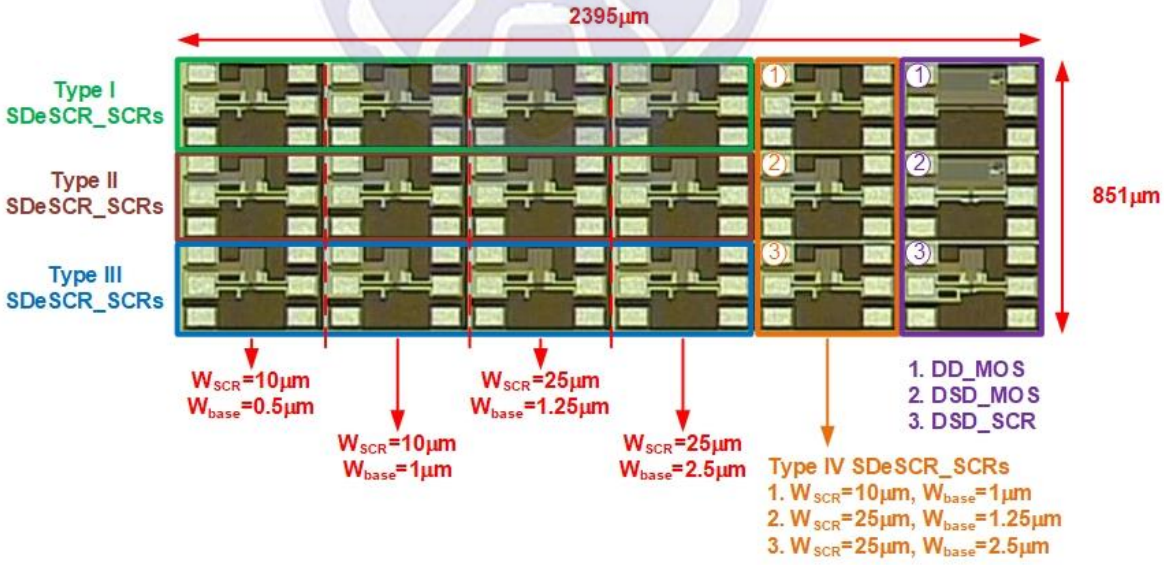


Fig. 2.23. Chip photo of traditional devices and SDeSCR_SCRs.

2.4.3 TLP I-V Curves of ESD Devices

In order to determine whether the ESD devices damaged or not, observing leakage current of devices is a way. When leakage current suddenly increases, it represents devices short. When leakage current suddenly decreases from large to small, it represents metal lines open. From the leakage current offset more than 30% to determine the test devices burned, according to the measurement results, the failures are all because of devices short.

Measured TLP I-V curves are shown in Fig. 2.25 to Fig. 2.28. In traditional devices, DD_MOS and DSD_MOS have snapback phenomenon at TLP voltage of over 6 V because the parasitic NPN BJT of M_{big} is triggered, as shown in Fig. 2.24(a) and (d). Besides, Fig. 2.25 to Fig. 2.28 show the SDeSCR_SCRs at different modes. In SDeSCR devices, the failure current of type III and type IV is slightly less than type I and type II because the base area (W_{base}) of type I and type II SDeSCR devices is twice that of type III and type IV SDeSCR devices. Therefore, the failure current and base area of the SDeSCR devices have a close relationship, and the failure current is inversely proportional to base area of SDeSCR devices [32]. In order to compare the clamping voltage of the test devices at the same discharging current, the clamping voltage (V_{clamp}) is defined at TLP current of 0.6A. Each SDeSCR_SCRs have snapback phenomenon because the parasitic SCR is triggered. The TLP characteristic at different modes are summarized in Table 2.2 to Table 2.5.

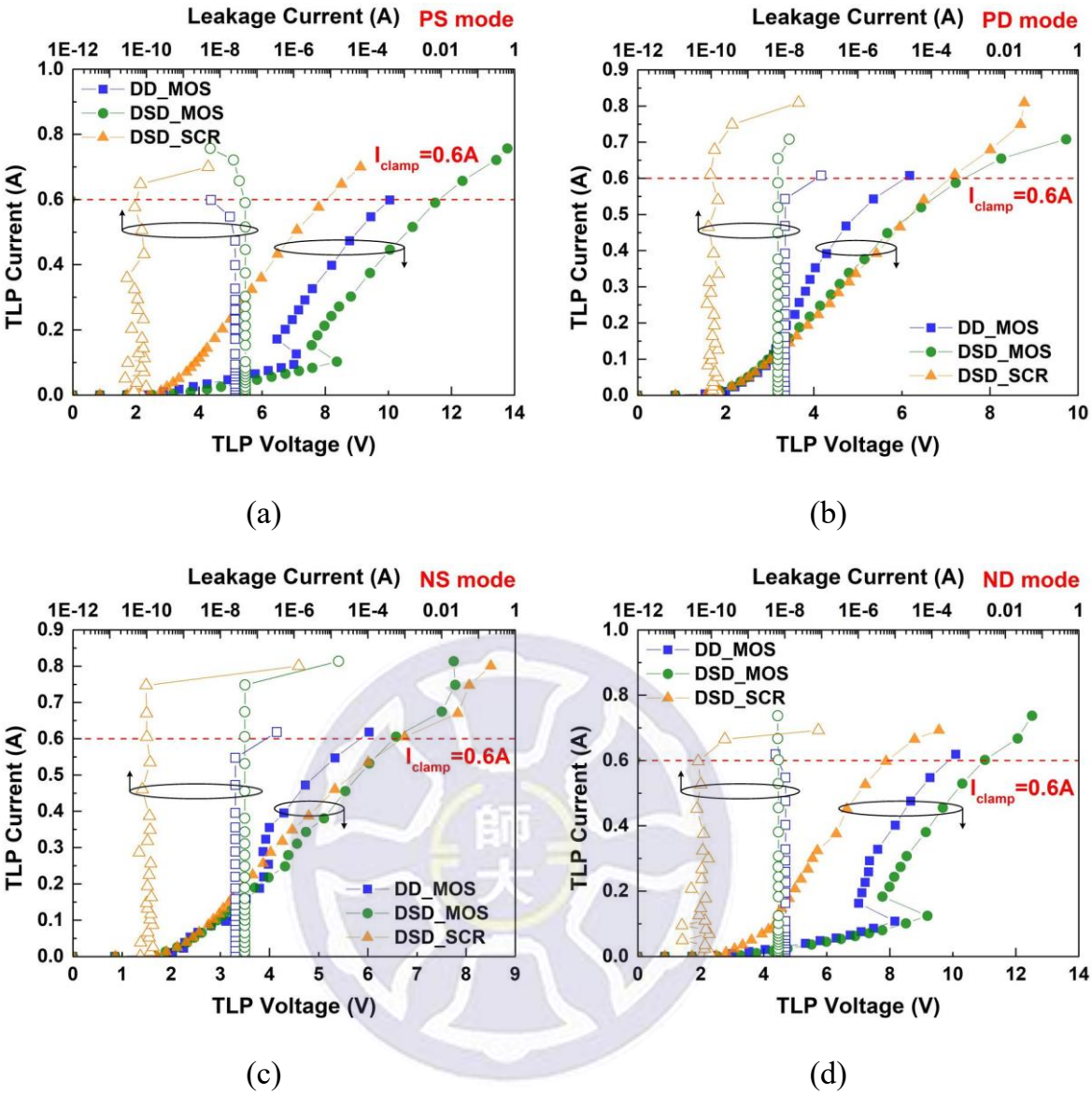


Fig. 2.24. Measured TLP I-V curves of traditional devices at (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

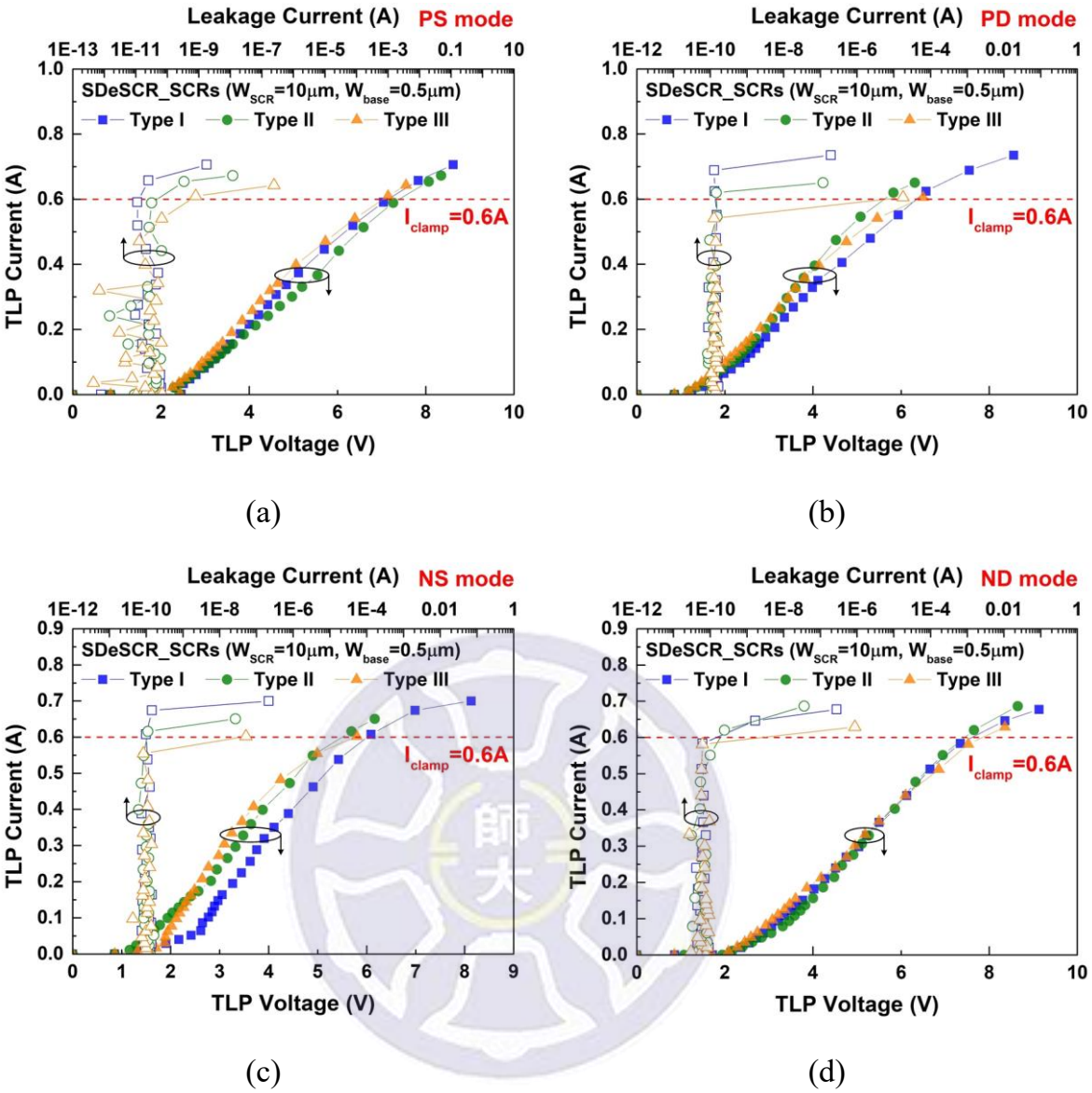


Fig. 2.25. Measured TLP I-V curves of SDeSCR_SCRs (W_{SCR} =10 μm, W_{base}=0.5 μm) at (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

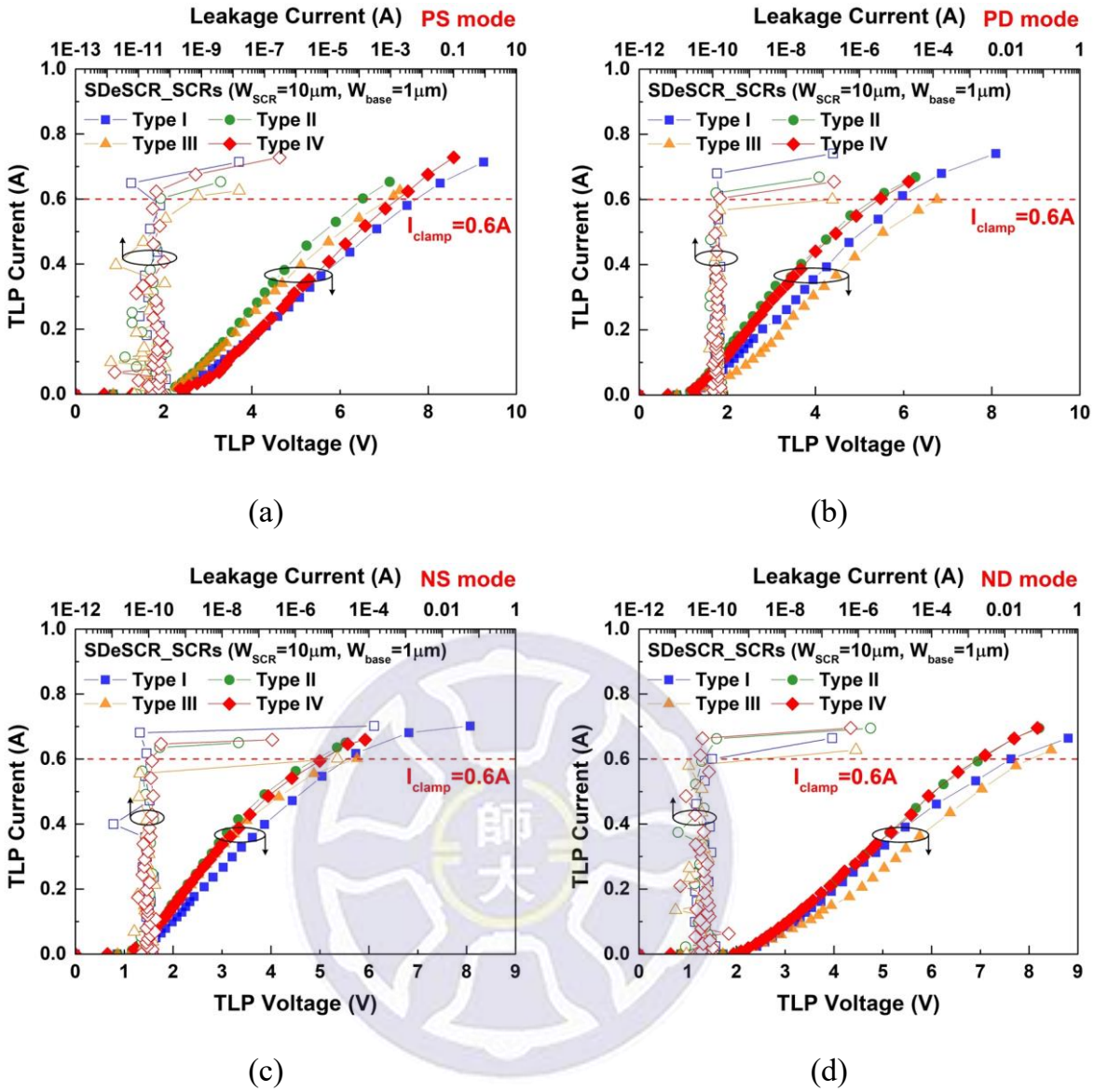


Fig. 2.26. Measured TLP I-V curves of SDeSCR_SCRs (W_{SCR} =10 μm, W_{base}=1 μm) at (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

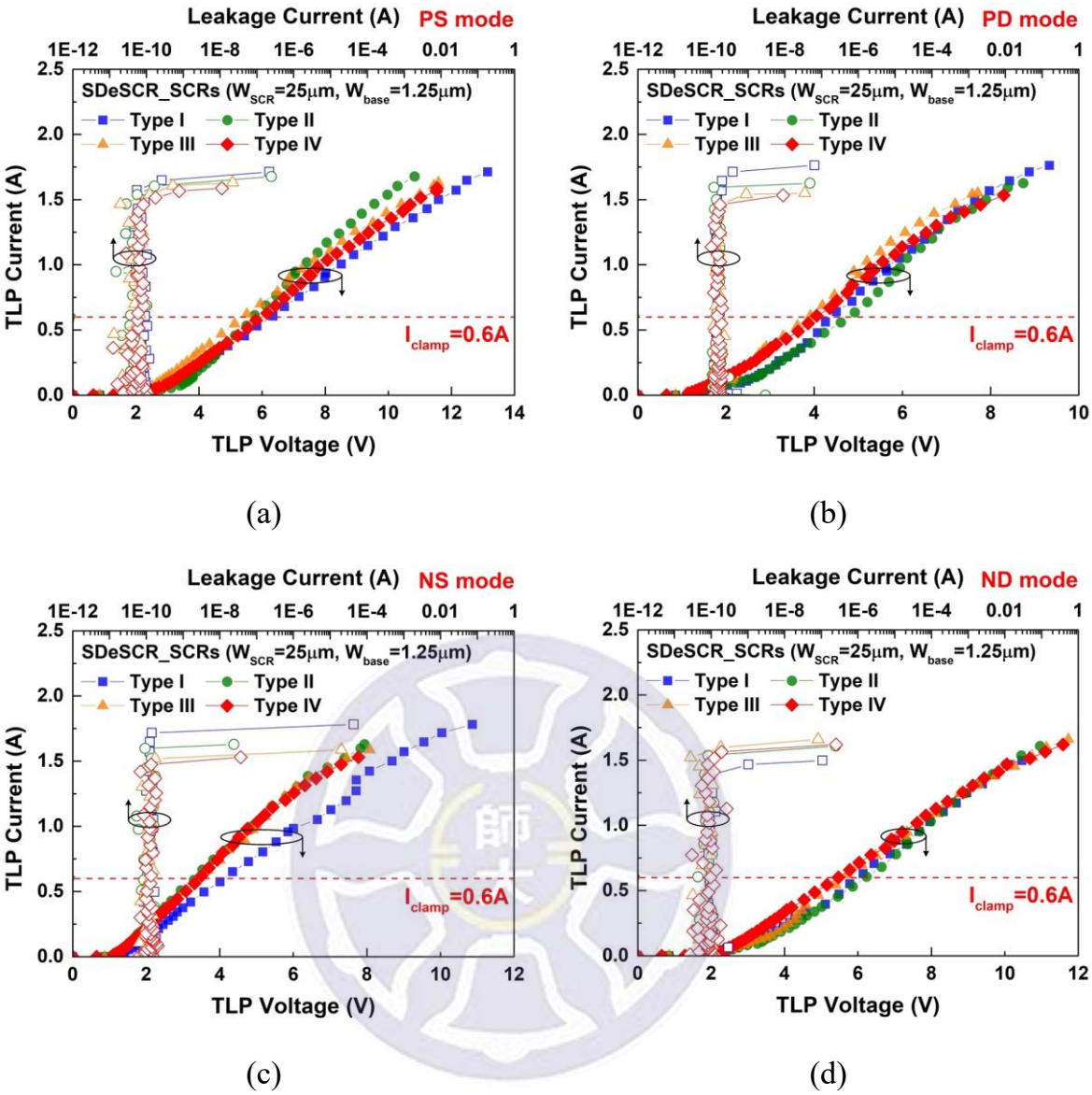


Fig. 2.27. Measured TLP I-V curves of SDeSCR_SCRs (W_{SCR} =25 μm, W_{base}=1.25 μm) at (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

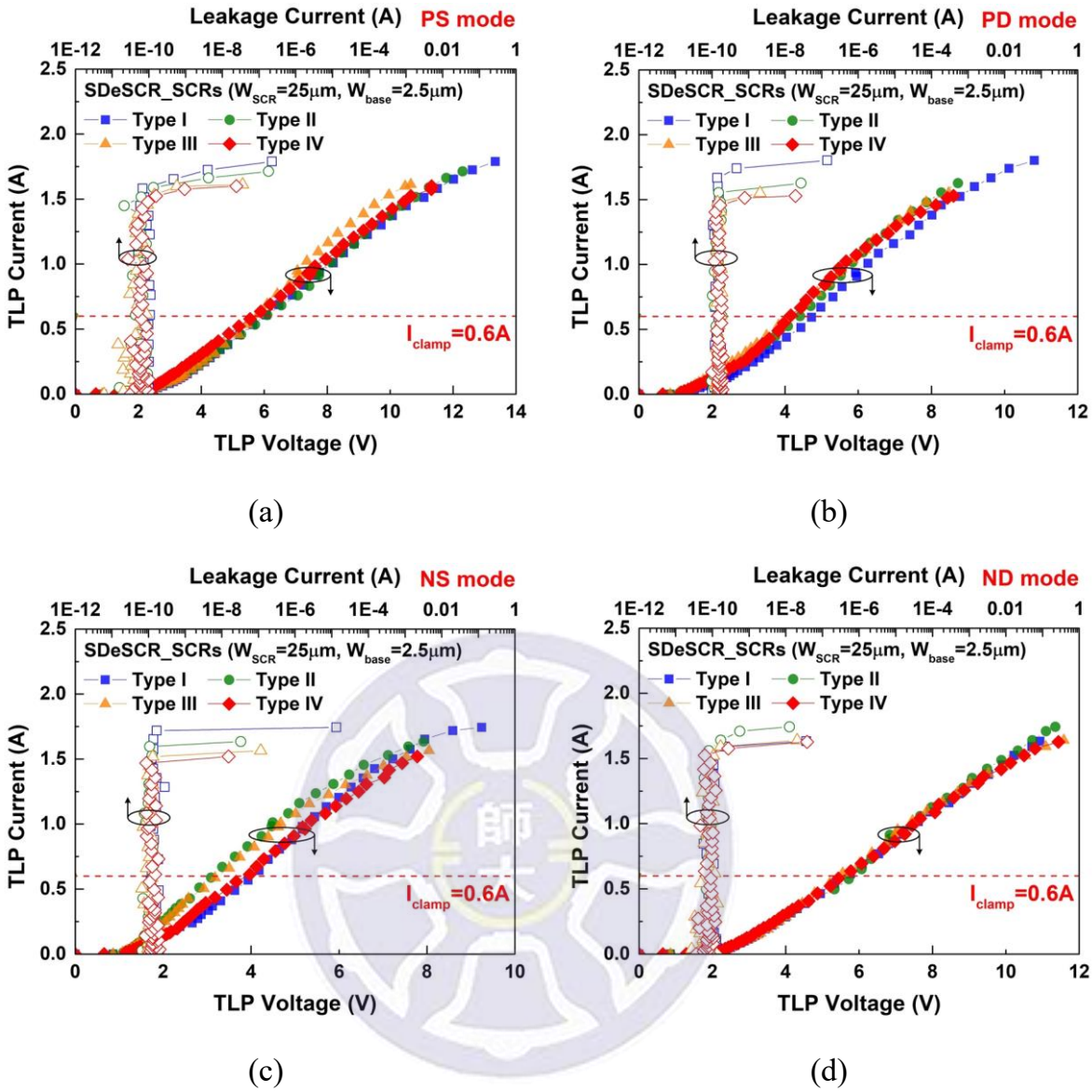


Fig. 2.28. Measured TLP I-V curves of SDeSCR_SCRs (W_{SCR}=25 μm, W_{base}=2.5 μm) at (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

Table 2.2

Measured TLP characteristic of traditional devices and SDeSCR_SCRs at PS mode.

Test devices at PS mode		Diode width (μm)		V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{clamp} @0.6A (V)
DD_MOS		10		1.89	1.89	0.57	13.68	>9.65
DSD_MOS		10		2.69	2.69	0.74	14.76	11.48
DSD_SCR		10		2.44	2.44	0.67	9.37	7.94
Test devices at PS mode		W_{SCR} (μm)	W_{base} (μm)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{clamp} @0.6A (V)
SDeSCR_SCR	Type I	10	0.5	2.5	2.25	0.69	8.67	7.04
			1	2.52	2.28	0.66	9.44	7.67
		25	1.25	2.43	2.14	1.66	6.34	6.34
			2.5	2.43	2.16	1.65	5.91	6.93
	Type II	10	0.5	2.43	2.16	0.64	9.13	7.43
			1	2.43	2.14	0.63	7.76	6.52
		25	1.25	2.4	2.16	1.64	5.17	5.72
			2.5	2.4	2.1	1.65	5.83	5.93
	Type III	10	0.5	2.44	2.15	0.61	7.58	7.01
			1	2.44	2.15	0.61	7.62	7.03
		25	1.25	2.39	2.07	1.61	5.64	5.41
			2.5	2.38	2.1	1.6	5.08	5.75
	Type IV	10	1	2.48	2.26	0.68	8.18	7.02
		25	1.25	2.42	2.12	1.57	5.82	5.94
			2.5	2.43	2.08	1.58	5.64	5.67

Table 2.3

Measured TLP characteristic of traditional devices and SDeSCR_SCRs at PD mode.

Test devices at PD mode		Diode width (μm)		V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{clamp} @0.6A (V)
DD_MOS		10		1.21	1.21	0.59	8.03	>5.94
DSD_MOS		10		1.72	1.72	0.7	10.76	7.48
DSD_SCR		10		1.56	1.56	0.75	9.56	7.04
Test devices at PD mode		W_{SCR} (μm)	W_{base} (μm)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{clamp} @0.6A (V)
SDeSCR_SCR	Type I	10	0.5	1.51	1.25	0.71	9.51	6.38
			1	1.5	1.24	0.71	8.87	5.82
		25	1.25	1.29	1.14	1.73	4.56	4.4
			2.5	1.29	1.19	1.77	5.24	4.72
	Type II	10	0.5	1.29	1.13	0.6	6.96	5.63
			1	1.5	1.15	0.62	7.23	5.37
		25	1.25	1.28	1.1	1.61	4.65	4.8
			2.5	1.29	1.18	1.61	4.69	4.41
	Type III	10	0.5	1.29	1.13	0.59	8.3	>6.19
			1	1.29	1.16	0.57	8.9	>6.34
		25	1.25	1.28	1.06	1.54	4.09	3.84
			2.5	1.29	1.06	1.53	4.65	4.15
	Type IV	10	1	1.51	1.18	0.62	6.75	5.48
		25	1.25	1.29	1.07	1.48	4.56	4.1
			2.5	1.29	1.07	1.51	5.25	4.15

Table 2.4

Measured TLP characteristic of traditional devices and SDeSCR_SCRs at NS mode.

Test devices at NS mode		Diode width (μm)		V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{clamp} @0.6A (V)
DD_MOS		10		1.22	1.22	0.6	7.64	5.79
DSD_MOS		10		1.69	1.69	0.7	9.77	6.42
DSD_SCR		10		1.82	1.82	0.76	8.38	6.58
Test devices at NS mode		W_{SCR} (μm)	W_{base} (μm)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{clamp} @0.6A (V)
SDeSCR_SCR	Type I	10	0.5	1.5	1.32	0.69	9.15	5.9
			1	1.5	1.24	0.68	8.3	5.44
		25	1.25	1.32	1.15	1.73	5.28	4.09
			2.5	1.49	1.15	1.73	4.54	3.93
	Type II	10	0.5	1.28	1.16	0.63	7.61	5.51
			1	1.51	1.16	0.64	6.71	4.88
		25	1.25	1.29	1.05	1.61	4.34	3.3
			2.5	1.3	1.06	1.61	4.18	3.09
	Type III	10	0.5	1.29	1.19	0.56	7.62	>5.53
			1	1.29	1.2	0.57	6.78	>5.16
		25	1.25	1.29	1.05	1.55	4.16	3.42
			2.5	1.29	1.05	1.55	4.14	3.29
	Type IV	10	1	1.51	1.17	0.65	6.28	5
		25	1.25	1.29	1.05	1.51	4.17	3.42
			2.5	1.29	1.07	1.5	4.27	3.86

Table 2.5

Measured TLP characteristic of traditional devices and SDeSCR_SCRs at ND mode.

Test devices at ND mode		Diode width (μm)		V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{clamp} @0.6A (V)
DD_MOS		10		2.06	2.06	0.64	13.17	9.82
DSD_MOS		10		2.93	2.93	0.69	14.57	11.02
DSD_SCR		10		2.5	2.5	0.67	9.47	7.88
Test devices at ND mode		W_{SCR} (μm)	W_{base} (μm)	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	V_{clamp} @0.6A (V)
SDeSCR_SCR	Type I	10	0.5	2.31	2.14	0.6	9.18	7.57
			1	2.32	2.17	0.65	9.63	7.63
		25	1.25	2.31	2.06	1.45	5.58	5.95
			2.5	2.31	2.06	1.62	5.47	5.65
	Type II	10	0.5	2.32	2.1	0.67	9.43	7.5
			1	2.31	2.08	0.68	8.74	6.95
		25	1.25	2.29	2.04	1.6	5.5	6.24
			2.5	2.3	2.02	1.73	5.42	5.86
	Type III	10	0.5	2.31	2.08	0.61	9.4	7.78
			1	2.31	2.11	0.61	9.42	7.94
		25	1.25	2.24	2.02	1.65	5.73	5.63
			2.5	2.3	2.02	1.63	5.62	5.43
	Type IV	10	1	2.32	2.1	0.68	8.2	6.94
		25	1.25	2.31	2.02	1.58	5.71	5.47
			2.5	2.31	2.03	1.59	5.43	5.63

2.4.4 Analysis TLP I-V Curves of ESD Devices

The ESD paths pass only through the ESD devices of input terminal at PD mode and NS mode to compare different types SDeSCR devices, as shown in Fig. 2.29 and Fig. 2.30. The trigger voltage of the small size SDeSCR devices slight increases about from 1.3 V to 1.5 V. The large size SDeSCR devices have a lower turn-on resistance, and the holding voltage of the SDeSCR devices is almost the same. The SDeSCR devices of the same W_{SCR} and different W_{base} have roughly the same turn-on resistance, and the I_{t2} also increases as size of W_{SCR} increases. The traditional devices and SDeSCR_SCRs are compared at different modes, as shown in Fig. 2.31. The DSD_SCR has a smaller turn-on resistance than DD_MOS and DSD_MOS, but it is still larger than type III and type IV SDeSCR devices.

The layout area includes ESD device and power-rail ESD clamp circuit. SDeSCR_SCRs have the different turn-on resistance in different layout styles. The proposed different types SDeSCR_SCRs also improves the R_{on}. In most cases, the R_{on} of type III and type IV SDeSCR_SCRs is smaller than type I and type II SDeSCR_SCRs because type III and type IV SDeSCR_SCRs insert the base into collect and emitter to make the SDeSCR devices more uniform conduction. The turn-on resistance of the test devices at different modes are summarized in Table 2.6.

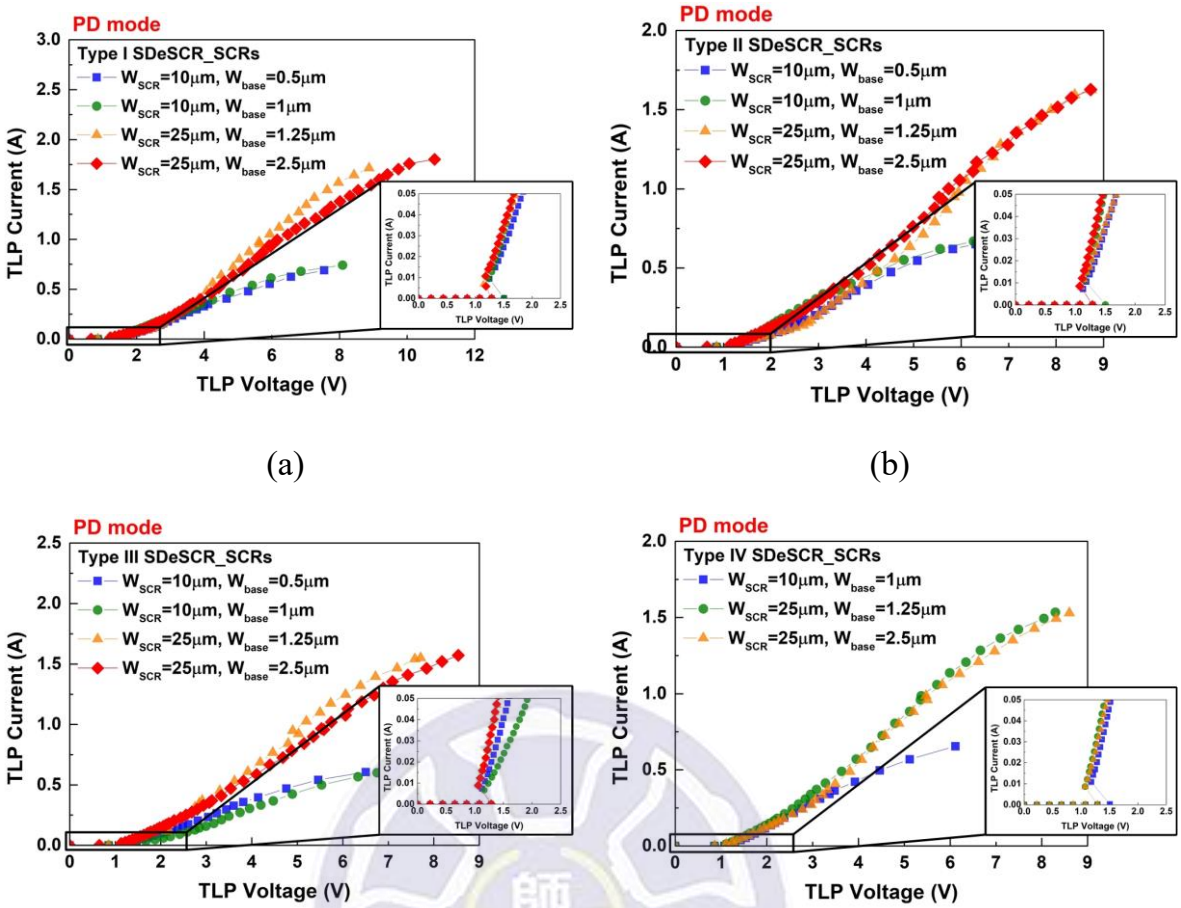


Fig. 2.29. Measured TLP I-V curves of (a) type I, (b) type II, (c) type III, and (d) type IV, SDeSCR_SCRs at PD mode.

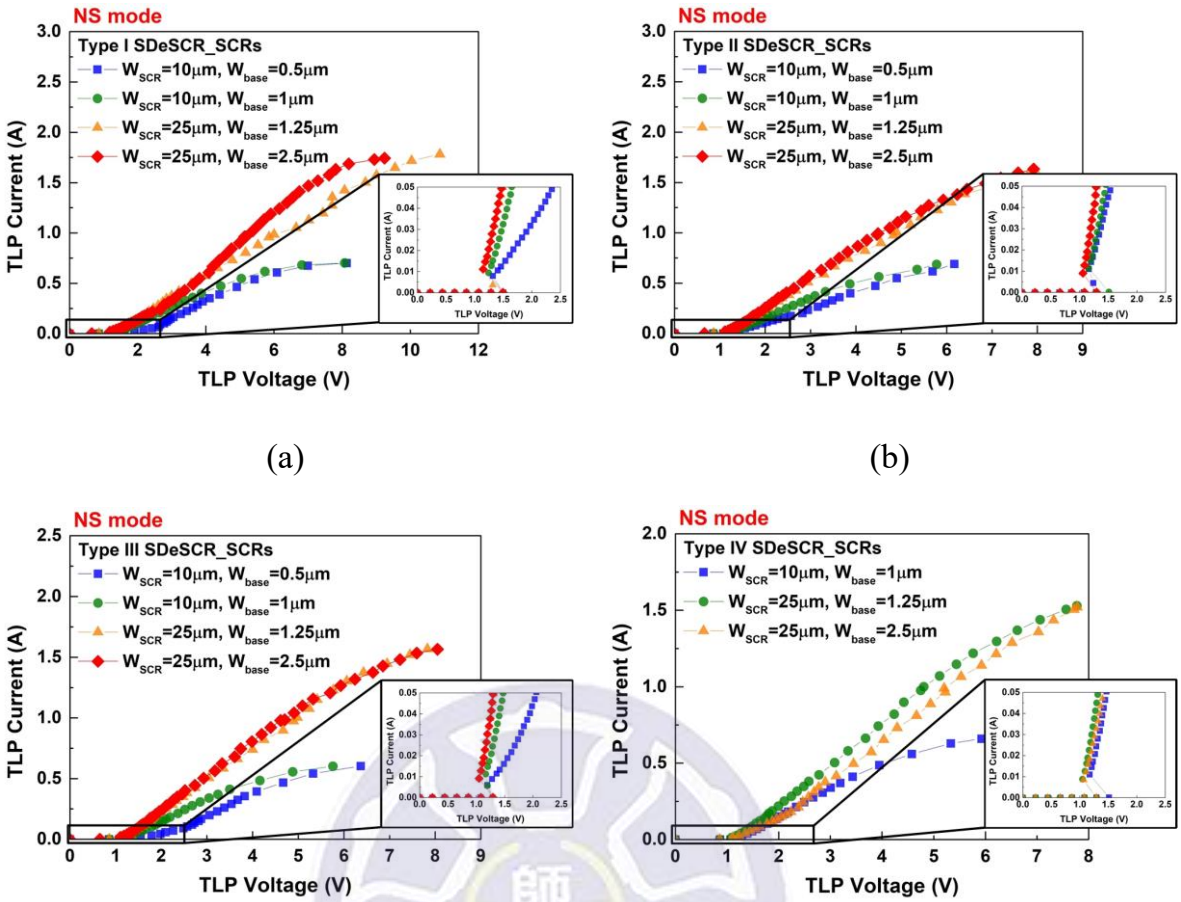


Fig. 2.30. Measured TLP I-V curves of (a) type I, (b) type II, (c) type III, and (d) type IV, SDeSCR_SCRs at NS mode.

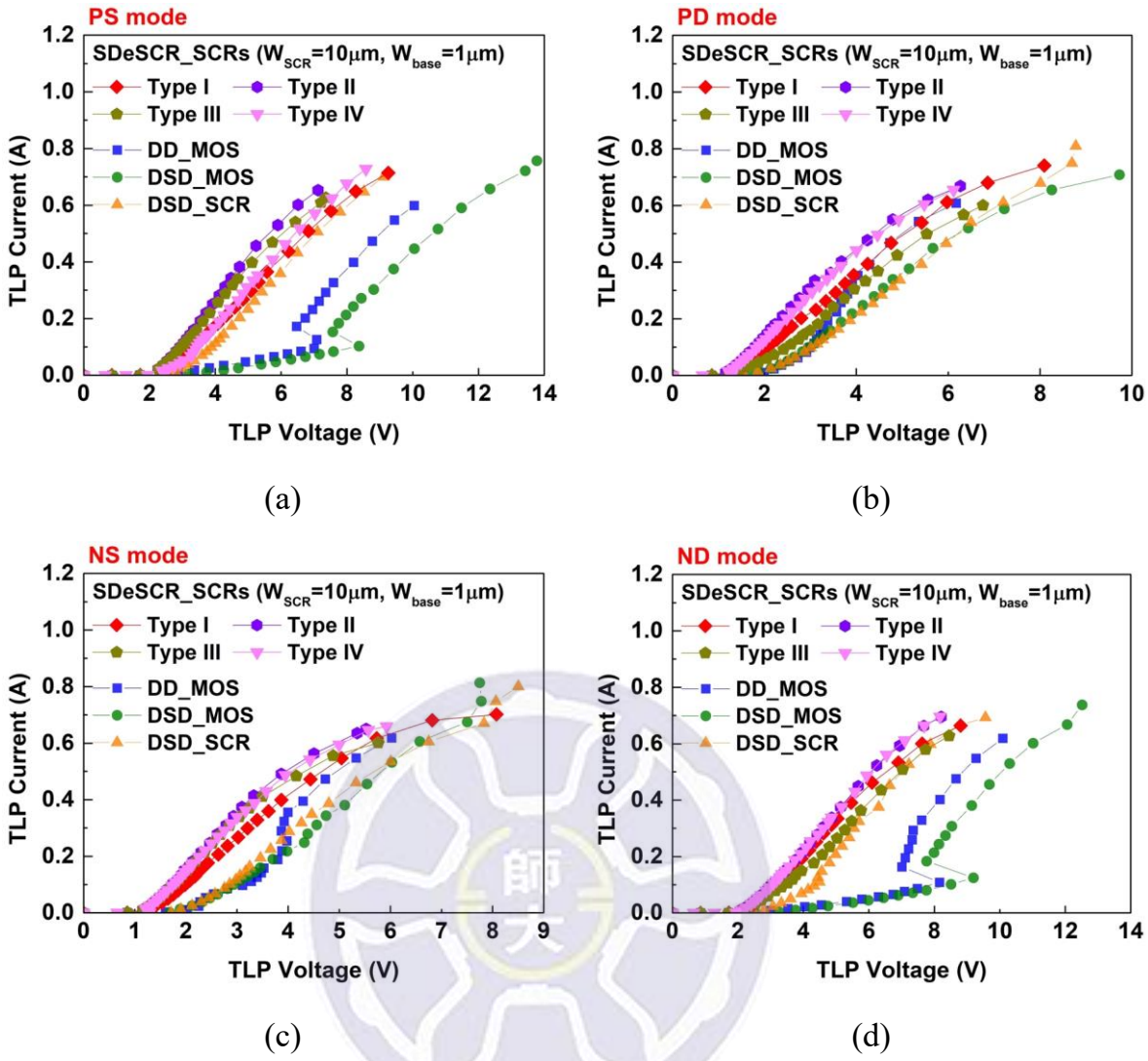


Fig. 2.31. Comparison among TLP I-V curves of traditional devices and SDeSCR_SCRs at (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

Table 2.6

Measured R_{on} of traditional devices and SDeSCR_SCRs.

Test devices		Diode width (μm)		R_{on} (Ω)			
				PS	PD	NS	ND
DD_MOS		10		13.68	8.03	7.64	13.17
DSD_MOS		10		14.76	10.76	9.77	14.57
DSD_SCR		10		9.37	9.56	8.38	9.47
Test devices		W_{SCR} (μm)	W_{base} (μm)	R_{on} (Ω)			
				PS	PD	NS	ND
SDeSCR_SCR	Type I	10	0.5	8.67	9.51	9.15	9.18
			1	9.44	8.87	8.3	9.63
		25	1.25	6.43	4.56	5.28	5.58
			2.5	5.91	5.24	4.54	5.47
	Type II	10	0.5	9.13	6.96	7.61	9.43
			1	7.76	7.23	6.71	8.74
		25	1.25	5.17	4.65	4.34	5.5
			2.5	5.83	4.69	4.18	5.42
	Type III	10	0.5	7.58	8.3	7.62	9.4
			1	7.62	8.9	6.78	9.42
		25	1.25	5.64	4.09	4.16	5.73
			2.5	5.08	4.65	4.14	5.62
	Type IV	10	1	8.18	6.75	6.28	8.2
		25	1.25	5.82	4.56	4.17	5.71
			2.5	5.64	5.52	4.27	5.43

2.4.5 HBM Robustness

Table 2.7 shows the HBM level of the test devices at different modes, and the interval of the HBM level is set to 300 V for per step. The DD_MOS, DSD_MOS, and DSD_SCR can bear at least 0.9 kV, 1.2 kV, and 1.2 kV of HBM level, respectively. The SDeSCR device have 10 μm and 25 μm sizes that can bear 1.2 kV and 3 kV of the HBM level, respectively.

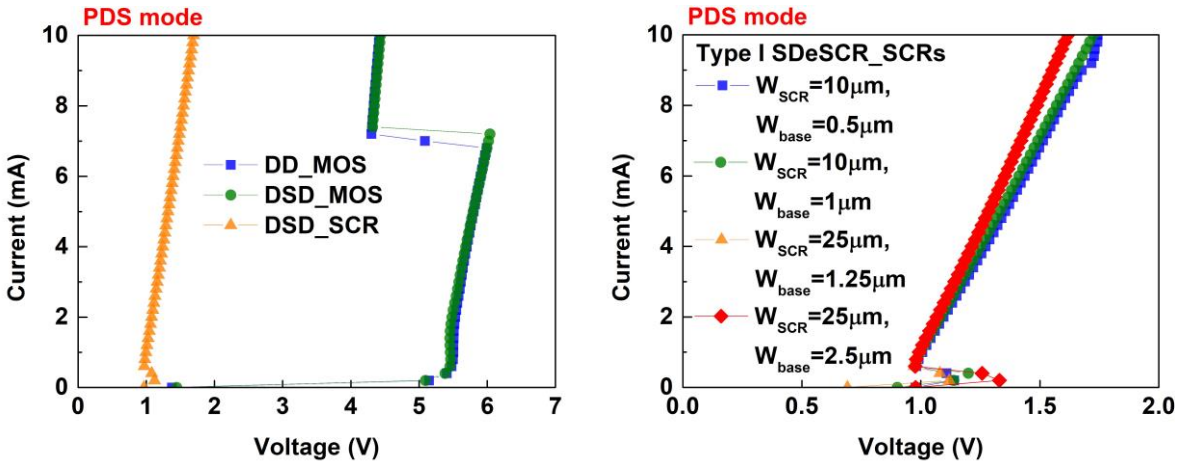
Table 2.7

Measured HBM robustness of traditional devices and SDeSCR_SCRs.

Test devices		Diode width (μm)		HBM level (kV)			
				PS	PD	NS	ND
DD_MOS		10		1.2	0.9	1.2	1.2
DSD_MOS		10		1.5	1.2	1.5	1.5
DSD_SCR		10		1.5	1.5	1.5	1.2
Test devices		W_{SCR} (μm)	W_{base} (μm)	HBM level (kV)			
				PS	PD	NS	ND
SDeSCR_SCR	Type I	10	0.5	1.2	1.2	1.2	1.2
			1	1.2	1.2	1.2	1.2
		25	1.25	3.3	3.3	3.3	3
			2.5	3.3	3.3	3.3	3.3
	Type II	10	0.5	1.2	1.2	1.5	1.2
			1	1.2	1.2	1.5	1.2
		25	1.25	3	3.3	3.3	3.3
			2.5	3.3	3.3	3.3	3.3
	Type III	10	0.5	1.2	1.2	1.5	1.2
			1	1.2	1.2	1.5	1.2
		25	1.25	3	3	3.3	3
			2.5	3	3	3.3	3
	Type IV	10	1	1.2	1.2	1.2	1.5
		25	1.25	3	3	3	3
			2.5	3	3	3	3

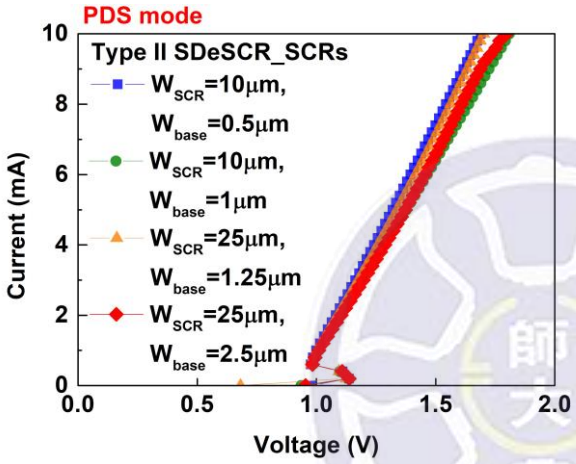
2.4.6 DC I-V Curves

To ensure that the test devices do not have latch-up issues in normal operation, the dc I-V curves are measured. The difference between dc I-V curve and TLP I-V curve is that TLP I-V curve is used to predict the ESD robustness of the test device. The bias voltage of V_{DD} and V_{SS} are 1.2 V and 0 V. The voltage difference from V_{DD} to V_{SS} is 1.2 V at PDS mode. This mode may have latch-up issues. Measured dc I-V curves of test devices are shown in Fig. 2.32. In traditional devices, DD_MOS and DSD_MOS have snapback phenomenon at dc voltage of about 6 V because the parasitic NPN BJT of M_{big} is triggered. In addition, the SCR-based power-rail ESD clamp circuit also have snapback phenomenon. Different types and sizes of SDeSCR_SCRs have slightly different results. The holding voltage of SDeSCR_SCRs at PDS mode is lower than V_{DD} (1.2 V), which causes latch-up issues. In order to solve the latch-up issues, several diodes can be connected to the SCR-based power-rail ESD clamp circuit in series to increase its holding voltage, as shown in Fig. 2.33. The dc I-V characteristics of traditional devices and SDeSCR_SCRs are summarized in Table 2.8.

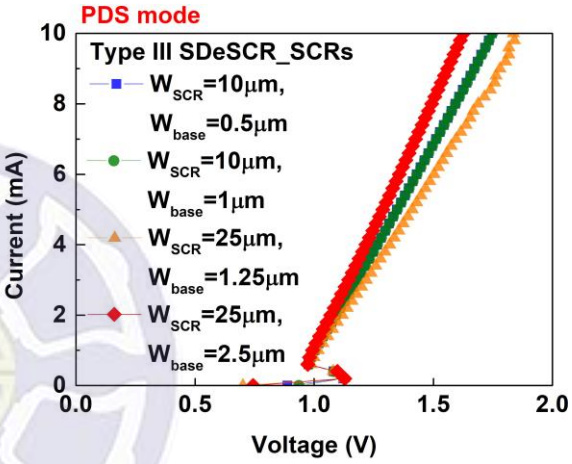


(a)

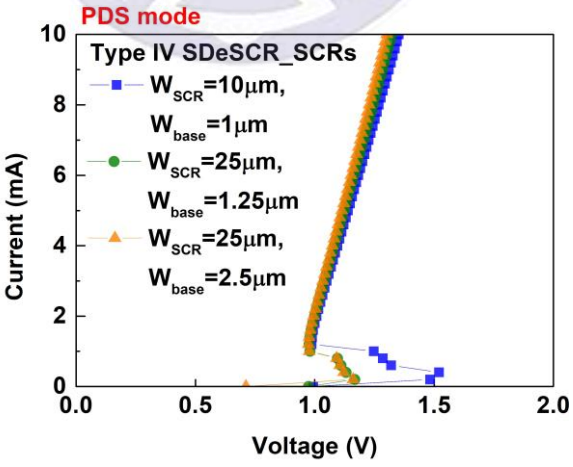
(b)



(c)



(d)



(e)

Fig. 2.32. Measured dc I-V curves of (a) traditional devices, (b) type I, (c) type II, (d) type III, and (e) type IV, SDeSCR_SCRs at PDS mode.

Table 2.8

Measured dc I-V characteristics of traditional devices and SDeSCR_SCRs at PDS mode.

Test devices		Diode width (μm)		V_h (V) at PDS mode
DD_MOS		10		4.3
DSD_MOS		10		4.32
DSD_SCR		10		0.97
Test devices		W_{SCR} (μm)	W_{base} (μm)	V_h (V) at PDS mode
SDeSCR_SCR	Type I	10	0.5	0.98
			1	0.98
		25	1.25	0.97
			2.5	0.98
	Type II	10	0.5	0.98
			1	0.98
		25	1.25	0.98
			2.5	0.98
	Type III	10	0.5	0.98
			1	0.98
		25	1.25	0.99
			2.5	0.97
	Type IV	10	1	0.99
		25	1.25	0.98
			2.5	0.97

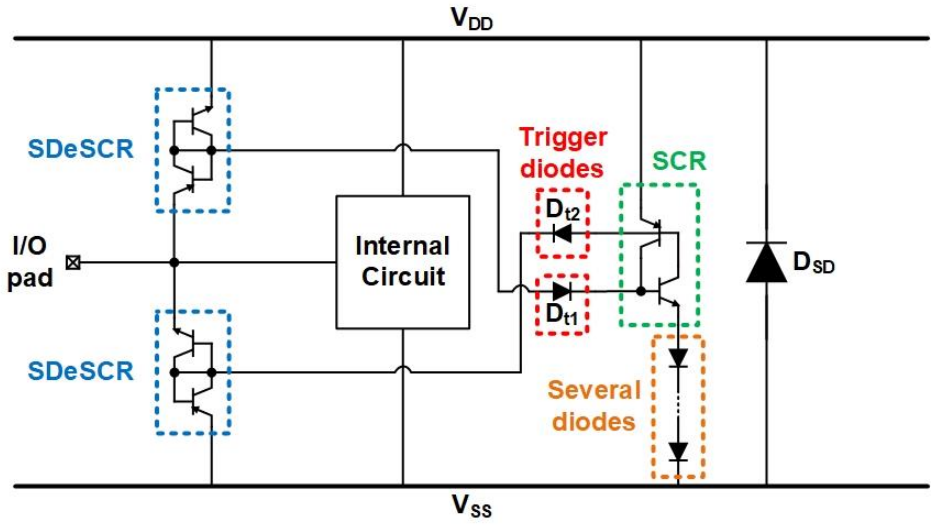
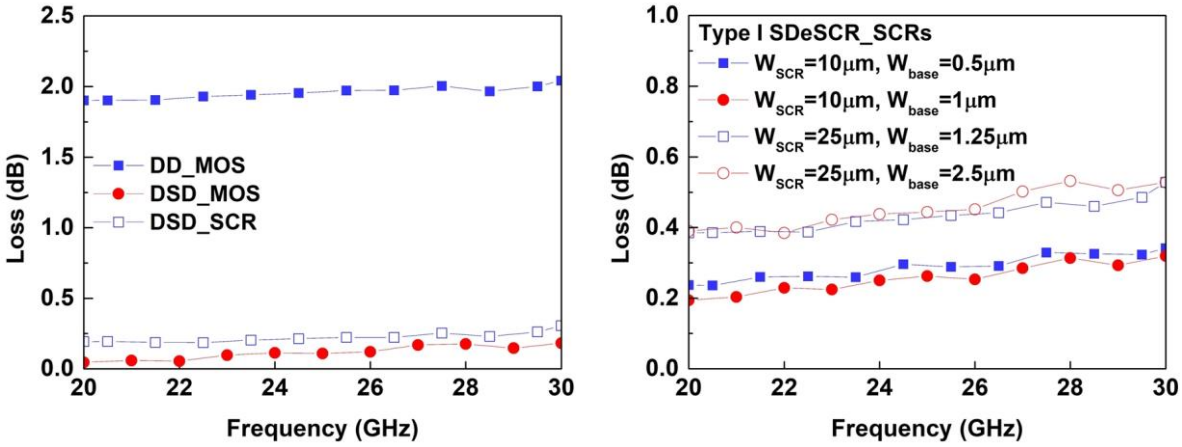


Fig. 2.33. Several diodes can be connected SCR-based power-rail ESD clamp circuit in series.

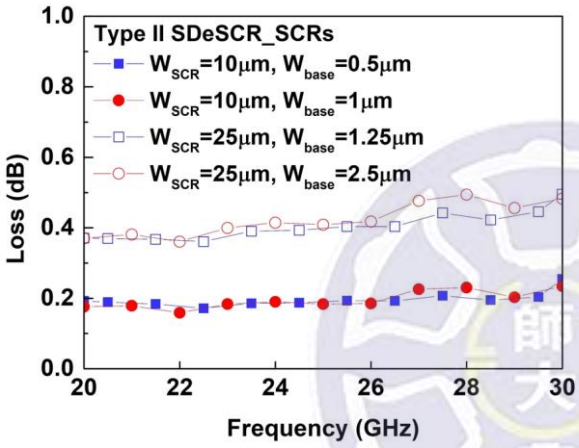
2.4.7 The High-Frequency Characteristics

Using the RFIC measurement system measures the s-parameter of the ESD devices, as shown in Fig. 2.34. To remove pads and metal lines other than ESD devices, the de-embedding technique is used [34], [35]. The loss of DD_MOS, DSD_MOS, and DSD_SCR at 24-GHz is 1.97 dB, 0.11 dB, and 0.23 dB. It can be observed that the loss of DD_MOS is larger than DSD_MOS and DSD_SCR. At the same W_{SCR}, the loss of SDeSCR_SCRs is almost the same. The W_{base} does not affect the loss of SDeSCR_SCRs, so the measurement results are similar. The loss of SDeSCR_SCRs increases as size increases. As shown in Fig. 2.35, the parasitic capacitance of DD_MOS, DSD_MOS, and DSD_SCR at 24-GHz is 46.23 fF, 30.79 fF, and 29.31 fF. The SDeSCR_SCRs have approximate parasitic capacitance and increase with W_{SCR}. The ESD devices with larger parasitic capacitance have a greater impact on the RF circuit. Measured loss and parasitic capacitance of traditional devices and SDeSCR_SCRs are summarized in Table 2.9.

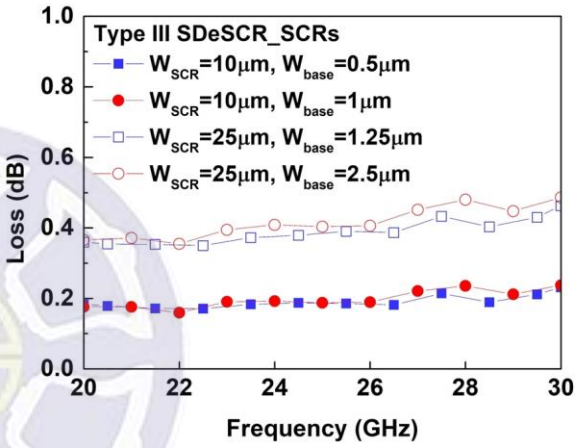


(a)

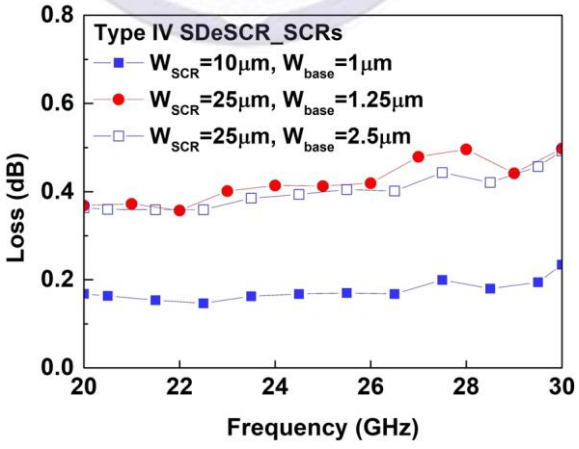
(b)



(c)

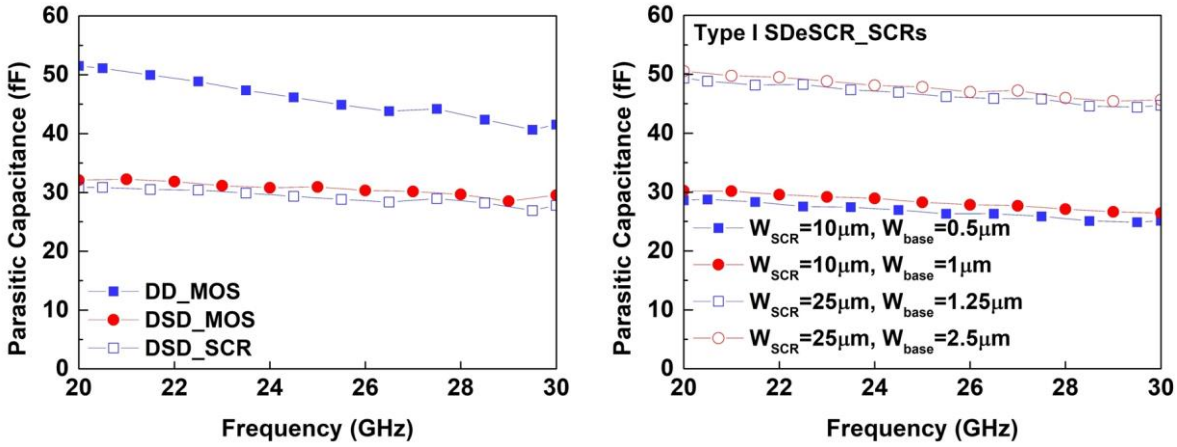


(d)



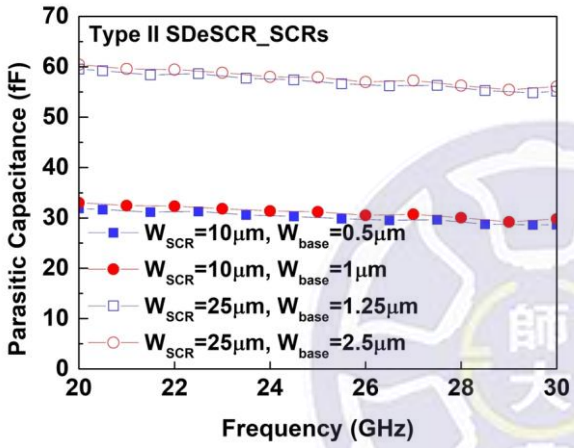
(e)

Fig. 2.34. Measured loss of (a) traditional devices, (b) type I, (c) type II, (d) type III, and (e) type IV, SDeSCR_SCRs.

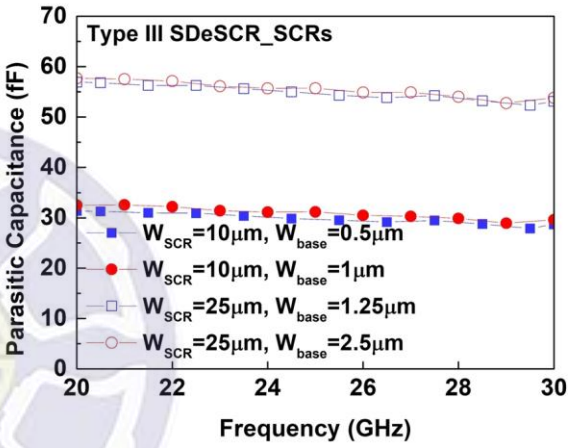


(a)

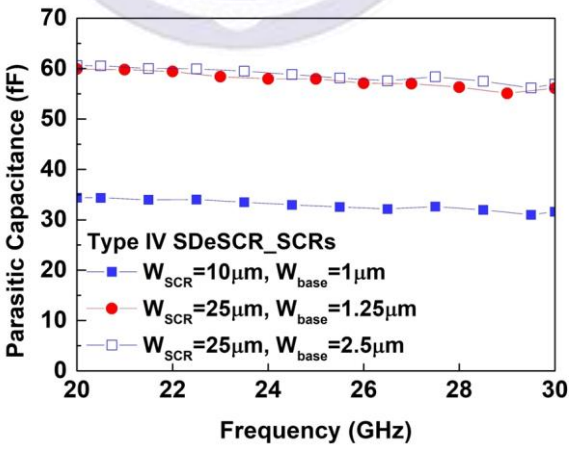
(b)



(c)



(d)



(e)

Fig. 2.35. Measured parasitic capacitance of (a) traditional devices, (b) type I, (c) type II, (d) type III, and (e) type IV, SDeSCR_SCRs.

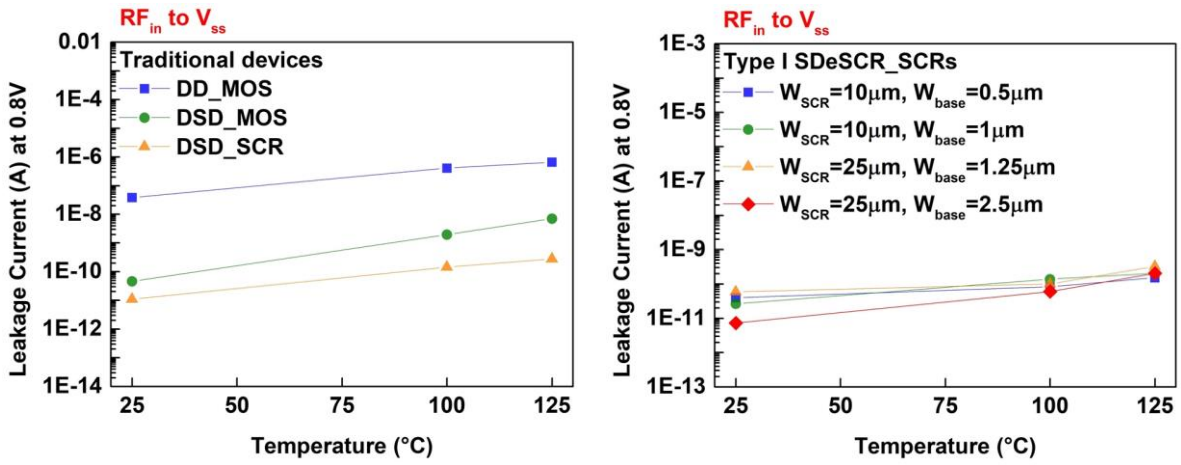
Table 2.9

Measured loss and parasitic capacitance of traditional devices and SDeSCR_SCRs.

Test devices		Diode width (μm)		Loss (dB) at 24-GHz	Parasitic capacitance (fF) at 24-GHz
DD_MOS		10		1.97	46.23
DSD_MOS		10		0.11	30.79
DSD_SCR		10		0.23	29.31
Test devices		W_{SCR} (μm)	W_{base} (μm)	Loss (dB) at 24-GHz	Parasitic capacitance (fF) at 24-GHz
SDeSCR_SCR	Type I	10	0.5	0.28	27.38
			1	0.25	28.94
		25	1.25	0.43	46.85
			2.5	0.44	48.11
	Type II	10	0.5	0.21	30.19
			1	0.19	31.38
		25	1.25	0.41	57.18
			2.5	0.41	58.01
	Type III	10	0.5	0.20	29.96
			1	0.19	31.13
		25	1.25	0.40	54.91
			2.5	0.41	55.69
	Type IV	10	1	0.18	32.97
		25	1.25	0.41	57.98
			2.5	0.41	58.6

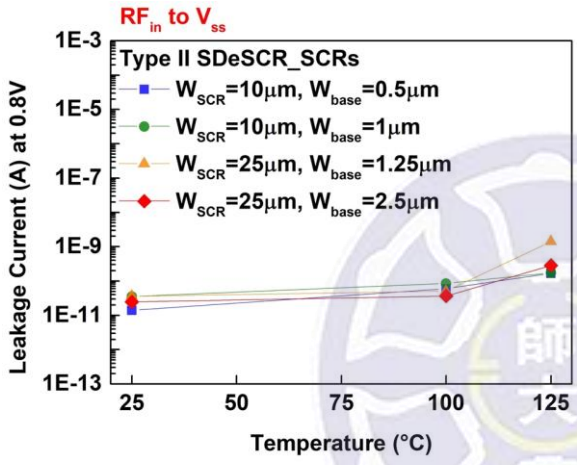
2.4.8 Leakage Current of ESD Devices at Different Temperatures

The leakage current of the ESD devices is measured at 25˚C, 100˚C, and 125˚C. The bias voltage is 0.8V, and the light source is turned off during measurement. The leakage current of SDeSCR_SCRs is lower than DD_MOS and DSD_MOS at 100˚C and 125˚C. The leakage current of the ESD devices increases as temperature increases, as shown in Fig. 2.36. Measured results are summarized in Table 2.10.

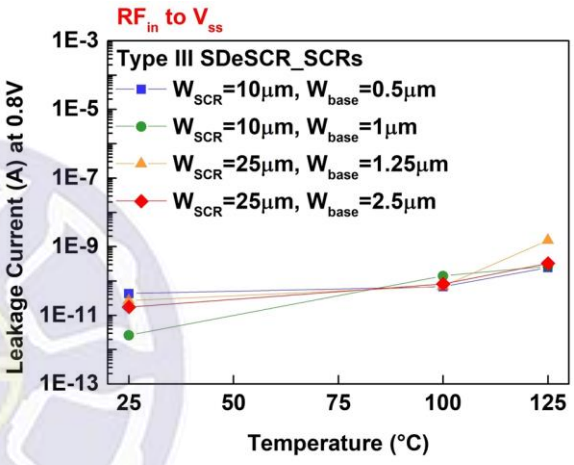


(a)

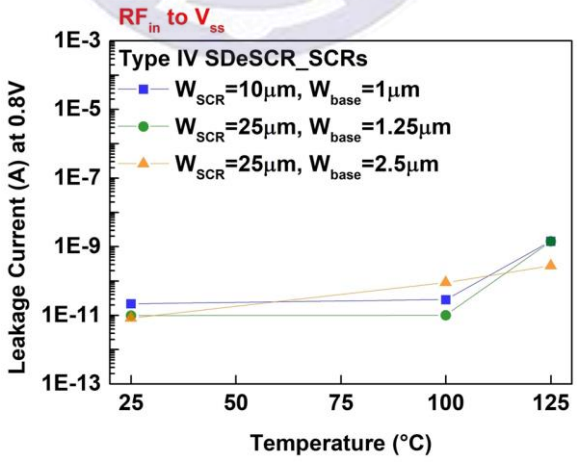
(b)



(c)



(d)



(e)

Fig. 2.36. Measured leakage current of (a) traditional devices, (b) type I, (c) type II, (d) type III, and (e) type IV, SDeSCR_SCRs.

Table 2.10

Measured leakage current of traditional devices and SDeSCR_SCRs.

Test devices		Diode width (μm)		Leakage current (nA) at 0.8V		
				25˚C	100˚C	125˚C
DD_MOS		10		38.32	396.4	648
DSD_MOS		10		0.045	1.941	6.911
DSD_SCR		10		0.011	0.142	0.272
Test devices		W_{SCR} (μm)	W_{base} (μm)	Leakage current (nA) at 0.8V		
				25˚C	100˚C	125˚C
SDeSCR_SCR	Type I	10	0.5	0.039	0.082	0.152
			1	0.026	0.137	0.206
		25	1.25	0.058	0.1	0.32
			2.5	0.007	0.06	0.205
	Type II	10	0.5	0.014	0.059	0.166
			1	0.035	0.083	0.173
		25	1.25	0.036	0.049	1.384
			2.5	0.025	0.036	0.286
	Type III	10	0.5	0.042	0.068	0.242
			1	0.003	0.139	0.267
		25	1.25	0.026	0.069	1.52
			2.5	0.018	0.082	0.324
	Type IV	10	1	0.022	0.028	1.423
		25	1.25	0.01	0.01	1.418
			2.5	0.008	0.09	0.273

2.4.9 Comparison

The turn-on resistance, HBM level, and parasitic capacitance of test devices are already summarized in Table 2.6, Table 2.7, and Table 2.9, respectively. Table 2.11 shows the layout area of DD, DSD, and SDeSCR devices, and the figure of merit (FOM) is defined to compare the performance of test devices. In application, the parasitic effect of the ESD devices must be as small as possible, otherwise it will greatly affect the characteristics of the circuit. Besides, the clamping voltage and turn-on resistance of ESD devices are proportional. The lower clamping voltage represents a smaller power consumption of the ESD devices.

The larger the value of the FOM, the better. Proposed SDeSCR_SCRs have better performance than traditional devices. The type III and type IV SDeSCR_SCRs have the advantages of low clamping voltage, low trigger voltage, and small layout area. Selecting the large size SDeSCR_SCRs will be better than the small size.

$$\text{FOM}=\frac{\text{HBM level}}{\text{parasitic capacitance}\times\text{layout area}\times V_{clamp}}\left(\frac{\text{kV}}{\text{fF}\times 10^{-6}\mu\text{m}^2\times\text{V}}\right) \quad (2\text{-}1)$$

Table 2.11

The layout area and FOM of test devices.

Test devices		Diode width (μm)		Layout area (μm^2)	FOM			
					PS	PD	NS	ND
DD_MOS		10		270	<10	<12.1	16.6	9.8
DSD_MOS		10		702	6.1	7.4	10.8	6.3
DSD_SCR		10		702	9.2	10.4	11.1	7.4
Test devices		W_{SCR} (μm)	W_{base} (μm)	Layout area (μm^2)	FOM			
					PS	PD	NS	ND
SDeSCR_SCR	Type I	10	0.5	414	15	17.8	19.3	15
			1	414	13.1	18.5	19.8	14.1
		25	1.25	759	14.6	21.1	22.7	14.2
			2.5	759	13	19.2	23	16
	Type II	10	0.5	396	13.5	17.8	22.8	13.4
			1	396	14.8	18	24.7	13.9
		25	1.25	726	12.6	16.6	24.1	12.7
			2.5	726	13.2	17.8	25.4	13.4
	Type III	10	0.5	380	15	<17	<23.8	13.6
			1	380	14.4	<16	<24.6	12.8
		25	1.25	700	14.4	20.3	25.1	13.9
			2.5	700	13.4	18.5	25.7	14.1
	Type IV	10	1	420	12.3	15.8	17.3	15.6
		25	1.25	720	12.1	17.5	21	13.1
			2.5	720	12.5	17.1	18.4	12.6

2.5 Summary

The traditional ESD devices and the proposed different types SDeSCR_SCRs have been fabricated in 0.18-μm CMOS technology. The TLP I-V curves, dc I-V curves, HBM robustness, leakage current, loss, and parasitic capacitance of test devices are measured. The proposed different types SDeSCR_SCRs have the lower clamping voltage and turn-on resistance than traditional devices at the same size. In the case where W_{SCR} is 10 μm and 25 μm, SDeSCR_SCRs provide at least 1 kV and 3 kV HBM ESD level. Although the SDeSCR_SCRs have almost the same HBM robustness as traditional devices, the layout area of SDeSCR_SCRs have only a quarter of DD_MOS and DSD_MOS. From the defined FOM values, it can be demonstrated that SDeSCR_SCRs have better performance that traditional devices.

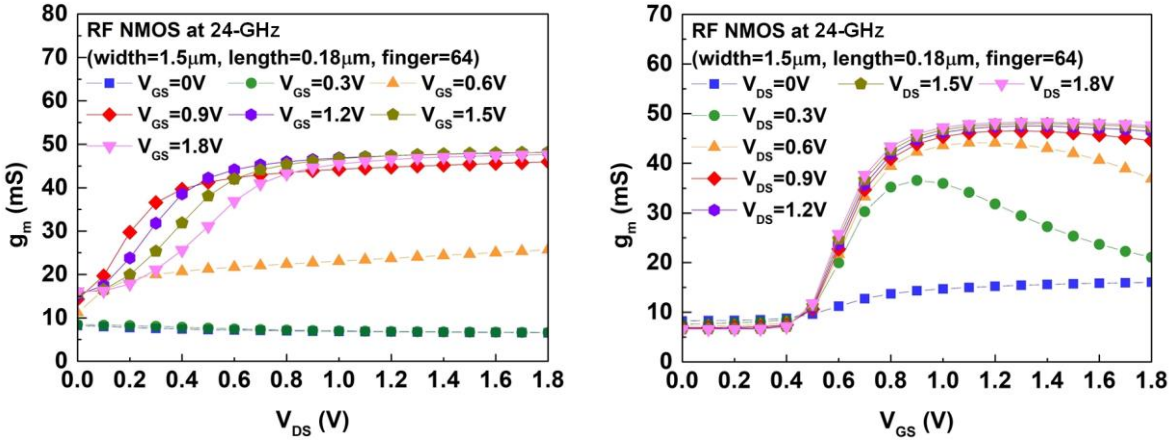
Chapter 3

Application of ESD Devices to 24-GHz Low-Noise Amplifier in CMOS Technology

3.1 24-GHz Low-Noise Amplifier

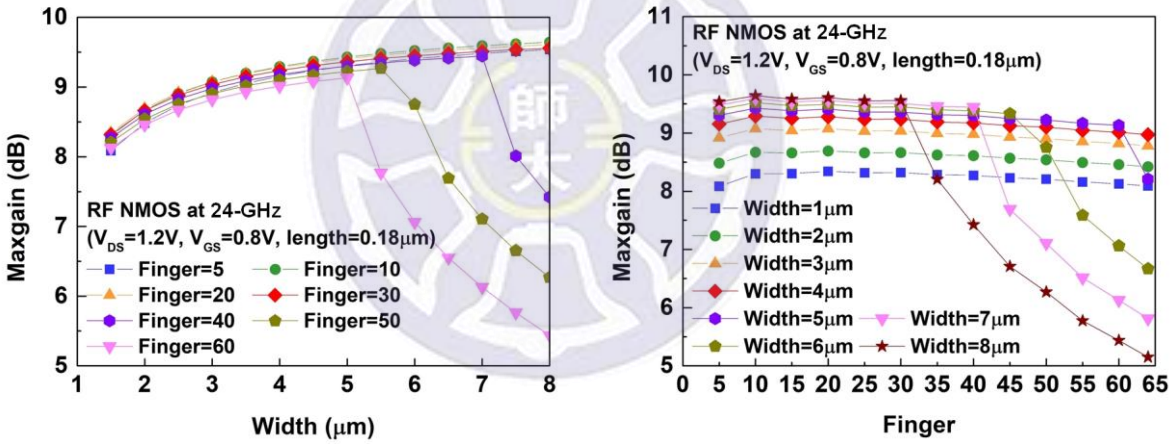
3.1.1 Design Steps of 24-GHz Low-Noise Amplifier

In 24-GHz LNA design steps, the circuit specifications are set, such as gain and noise figure (NF). The appropriate transistor size is selected for the circuit. First, the V_{DS} and V_{GS} are swept from 0 V to 1.8 V, and the V_{DS} and V_{GS} are selected as 1.2 V and 0.8 V, as shown in Fig. 3.1. Second, selecting the bias voltage decides the transistor size to obtain maximum gain and minimum noise figure. The width size and finger number of transistor are swept from 1.5 μm to 8 μm and from 2 to 64, respectively. The width size and finger number of transistor are selected as 6 μm and 10, as shown in Fig. 3.2 and Fig. 3.3. Third, the inductor connects between the source of transistor and ground to determine the cutoff frequency, which is source degeneration inductor (L_S). The L_S is swept from 0 pH to 150 pH to obtain maximum gain, and the value of L_S is selected between 60 pH and 90 pH, as shown in Fig. 3.4. Following the above steps, a single transistor can obtain maximum performance. In order to increase gain of circuit, two-stage structure is used. The matching network of the LNA will be introduced in next.



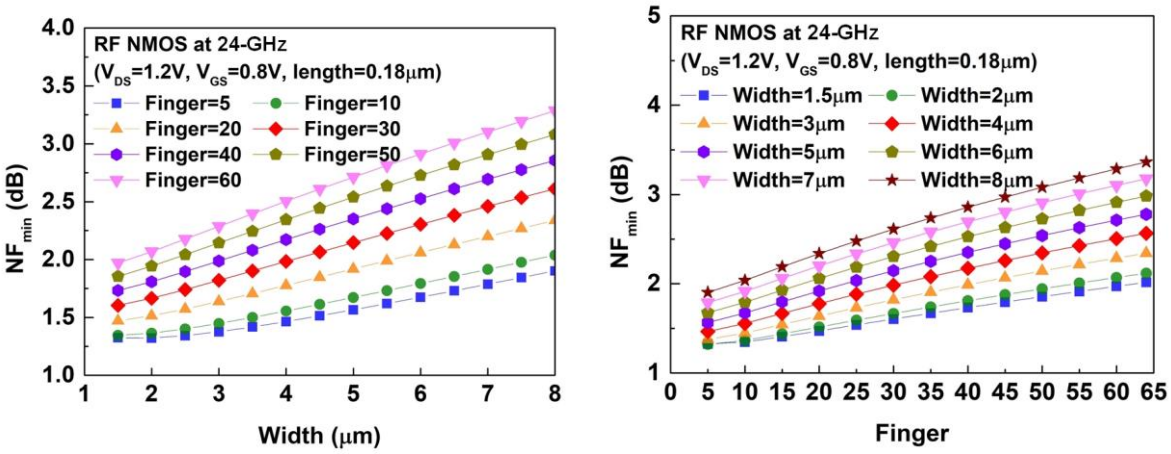
(a) (b)

Fig. 3.1. Simulated g_m of RF NMOS (width=1.5 μm, length=0.18 μm, finger=64) with various (a) V_{DS} and (b) V_{GS} at 24-GHz.



(a) (b)

Fig. 3.2. Simulated Max gain of RF NMOS (V_{DS}=1.2 V, V_{GS}=0.8 V, length=0.18 μm) with various (a) width and (b) finger at 24-GHz.



(a) (b)

Fig. 3.3. Simulated NF_{min} of RF NMOS (V_{DS}=1.2 V, V_{GS}=0.8 V, length=0.18 μm) with various (a) width and (b) finger at 24-GHz.

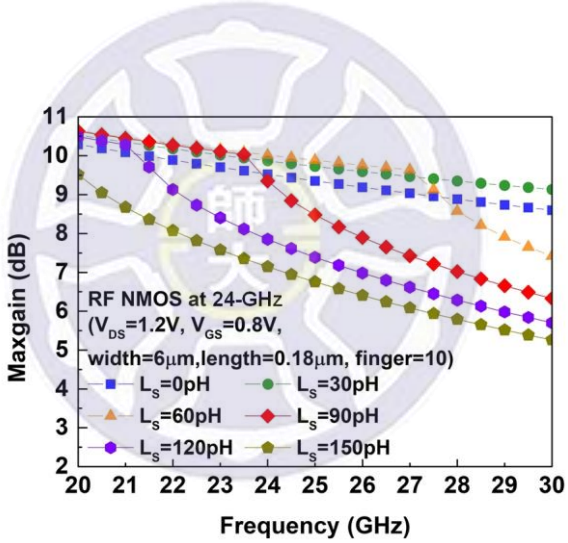


Fig. 3.4. Simulated Max gain of RF NMOS (V_{DS}=1.2V, V_{GS}=0.8 V, width=6 μm, length=0.18 μm, finger=10) with various L_S at 24-GHz.

3.1.2 Structure of 24-GHz Low-Noise Amplifier

As shown in Fig. 3.5, the architecture of a 24-GHz LNA is composed of two stage and common source topology [36], [37]. The input matching network, output matching network, and inter-stage matching network are labeled by the green, blue, and red lines, respectively. The input matching network that is conjugate match is composed of L_{in} and

L_G, and V_G via L_{in} that is RF choke give bias to avoid RF signal loss to ground. The bias voltage V_G and V_{DD} are designed 0.8 V and 1.2 V, respectively, and the power dissipation of the LNA is 57.8 mW. Since the input impedance is designed 50 Ω, the source of M_{N1} adds an inductor to reduce noise figure degradation, and the value of inductor L_S can adjust the cutoff frequency. In order to allow the previous stage of the signal deliver to the next stage, adding the inter-stage matching network that compose of L_o and C_o is necessary. Another component R_o has the same function as the inductor, which is designed 2 kΩ. The output matching network is composed of L_{out1}, L_{out2}, and C_{out}, and the V_{DD} via L_{out2} that is RF choke give bias to avoid RF signal loss. The simulation results and the layout top view of the LNA without ESD protection are shown in Fig. 3.6 and Fig. 3.7.

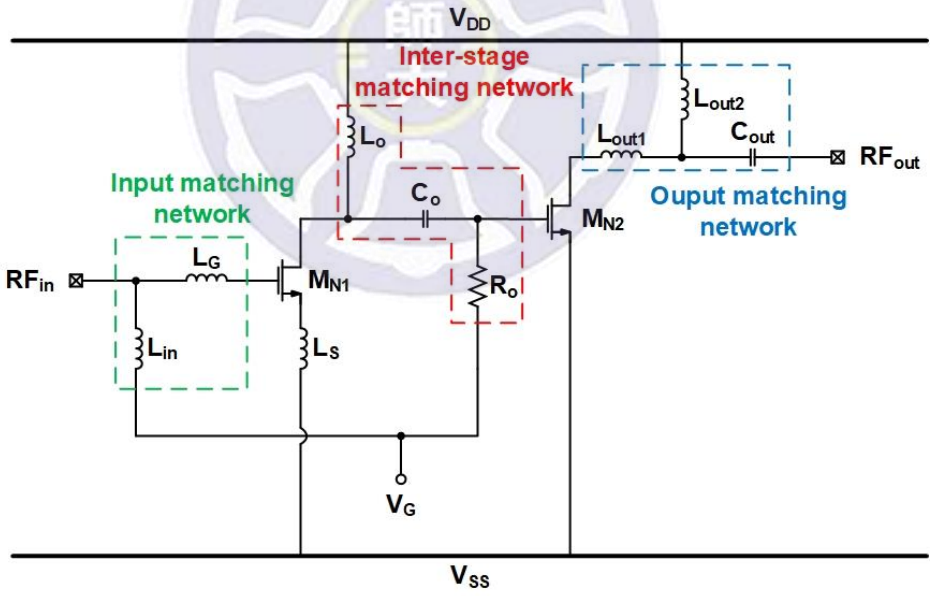
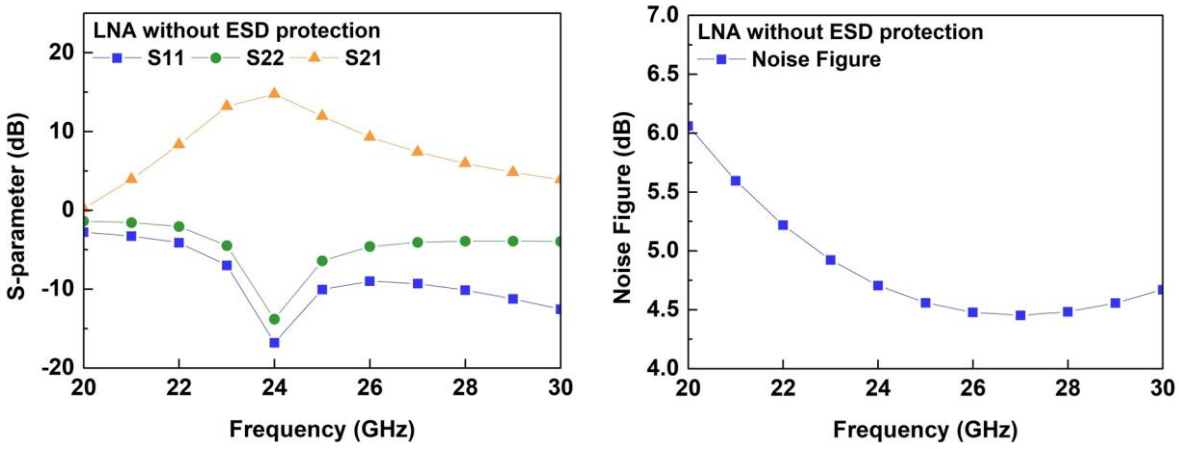
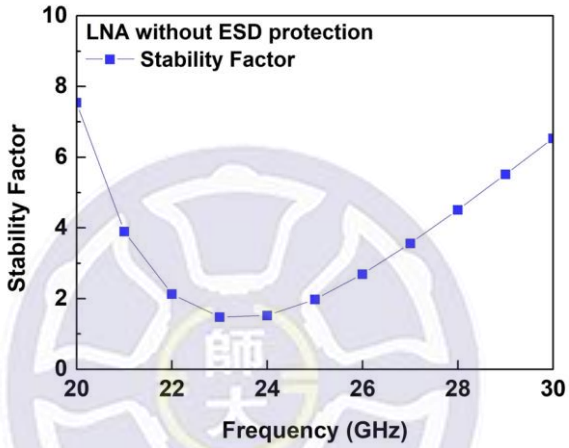


Fig. 3.5. The architecture of 24-GHz LNA.



(a) (b)



(c)

Fig. 3.6. Simulated (a) s-parameters, (b) noise figure, and (c) stability factor, of 24-GHz LNA without ESD protection.

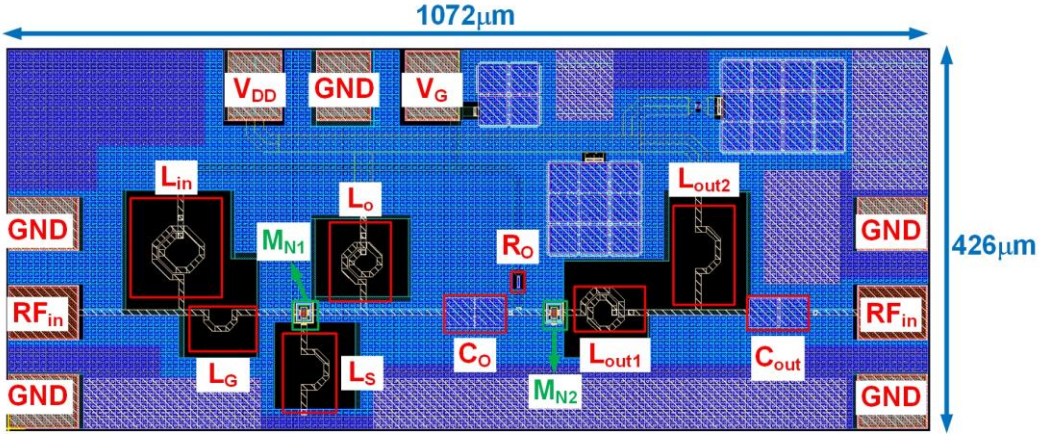


Fig. 3.7. The layout top view of 24-GHz LNA without ESD protection.

3.1.3 24-GHz Low-Noise Amplifier with ESD Protection

The simulation results of the LNA with DD_MOS, DSD_MOS, and DSD_SCR are shown in Fig. 3.9, Fig. 3.12, Fig. 3.15, respectively. The simulation results of the LNA with type III (W_{SCR}=10 μm, W_{base}=0.5 μm) SDeSCR_SCR and type IV (W_{SCR}=10 μm, W_{base}=1 μm) SDeSCR_SCR are shown in Fig. 3.18 and Fig. 3.20, respectively. The MOS-based and SCR-based power-rail ESD clamp circuit are used in LNAs. In LNA with ESD protection devices, the S11 and S22 are less than -15 dB, and S21 is about 15 dB. The noise figure is between 4.5 dB and 5.5 dB, and stability factor is more than 1. The parasitic capacitances of type III and type IV SDeSCR_SCRs are almost the same, so the characteristics of LNAs are similar. Besides, the layout top view of the LNA with DD_MOS, DSD_MOS, DSD_SCR, type III SDeSCR_SCR, and type IV SDeSCR_SCR is shown in Fig. 3.10, Fig. 3.13, Fig. 3.16, Fig. 3.19, and Fig. 3.21, respectively. The layout top view includes matching network and ESD protection circuit. The layout area of LNAs is 0.457 μm^2.

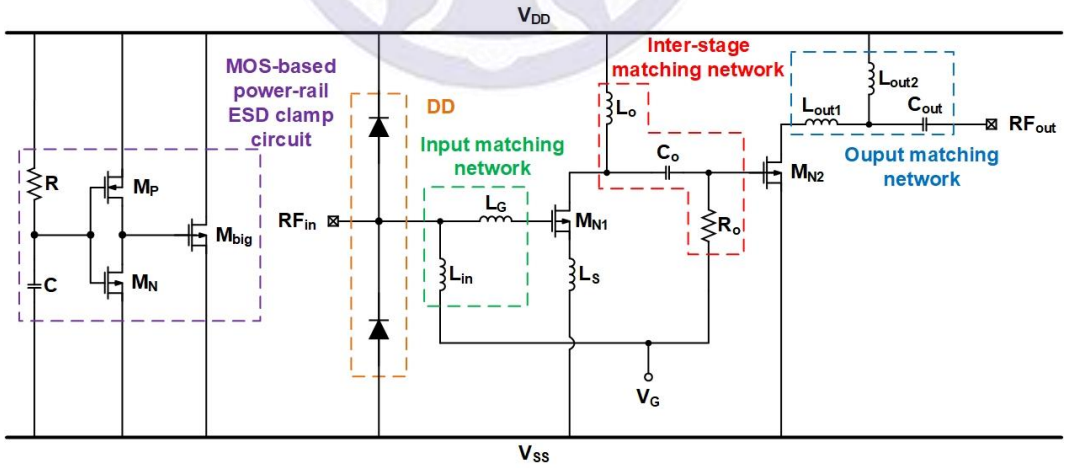
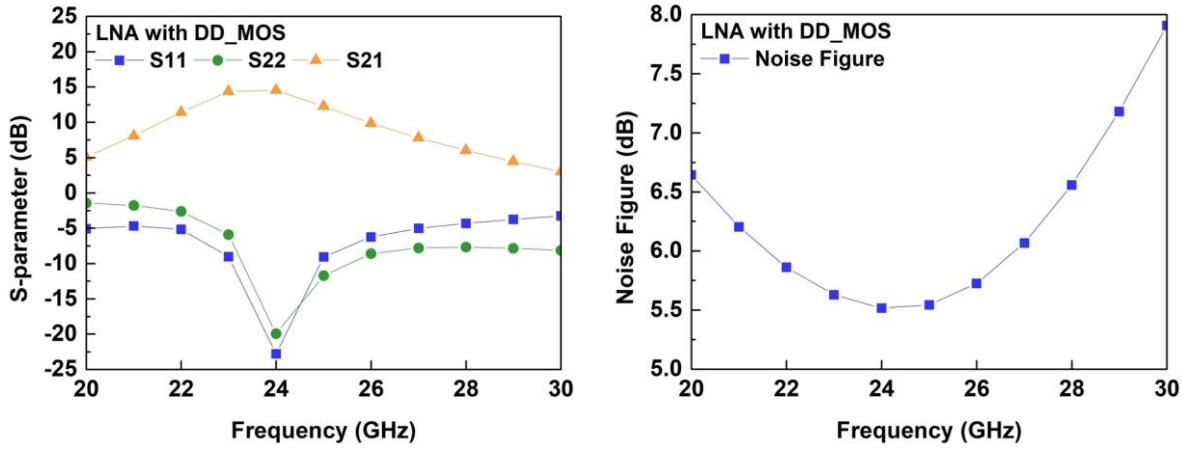
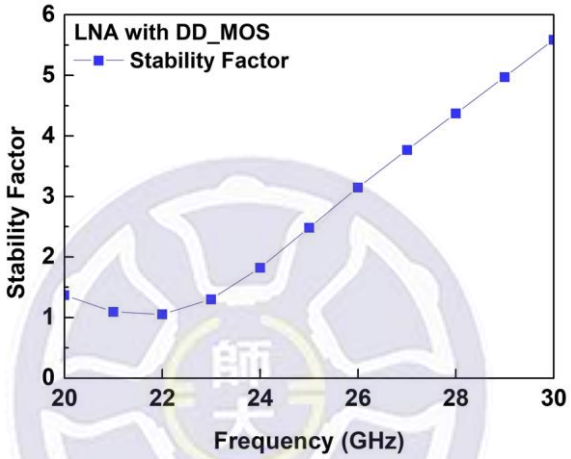


Fig. 3.8. Whole-chip ESD protection of LNA with DD_MOS.



(a) (b)



(c)

Fig. 3.9. Simulated (a) s-parameters, (b) noise figure, and (c) stability factor, of LNA with DD_MOS.

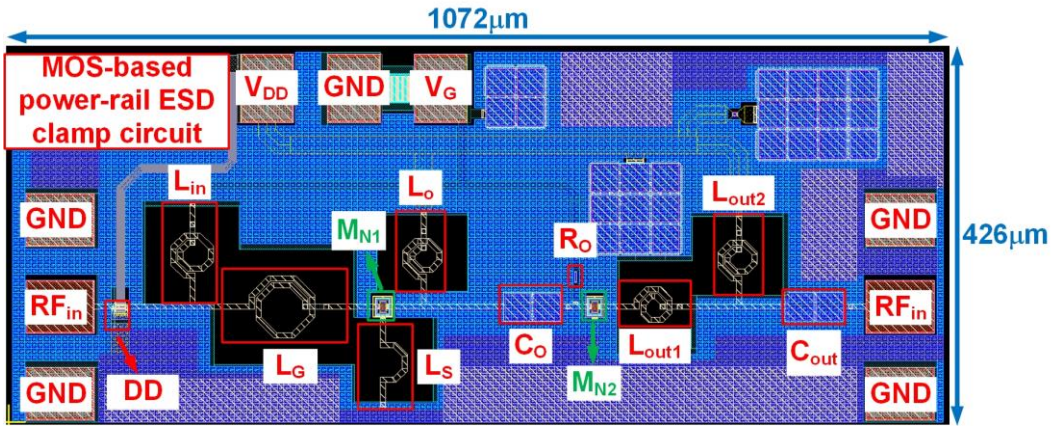


Fig. 3.10. The layout top view of LNA with DD_MOS.

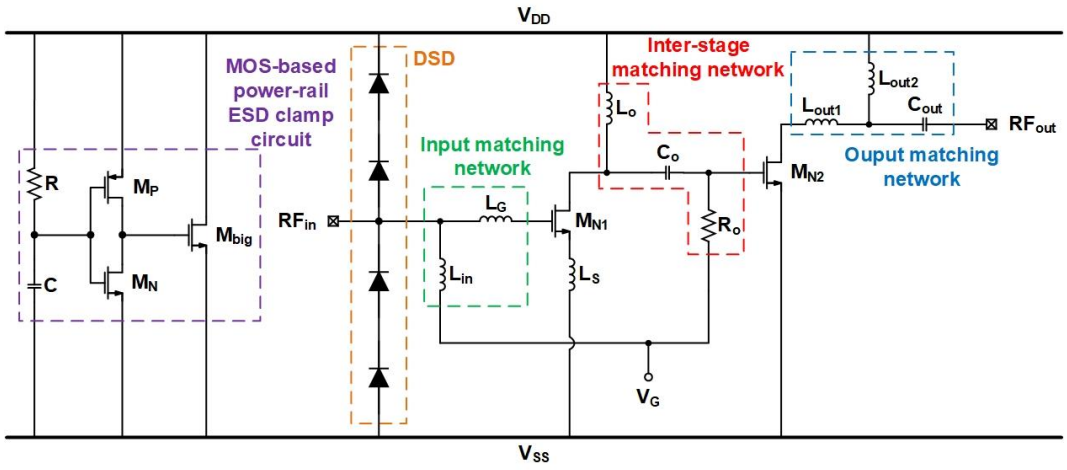


Fig. 3.11. Whole-chip ESD protection of LNA with DSD_MOS.

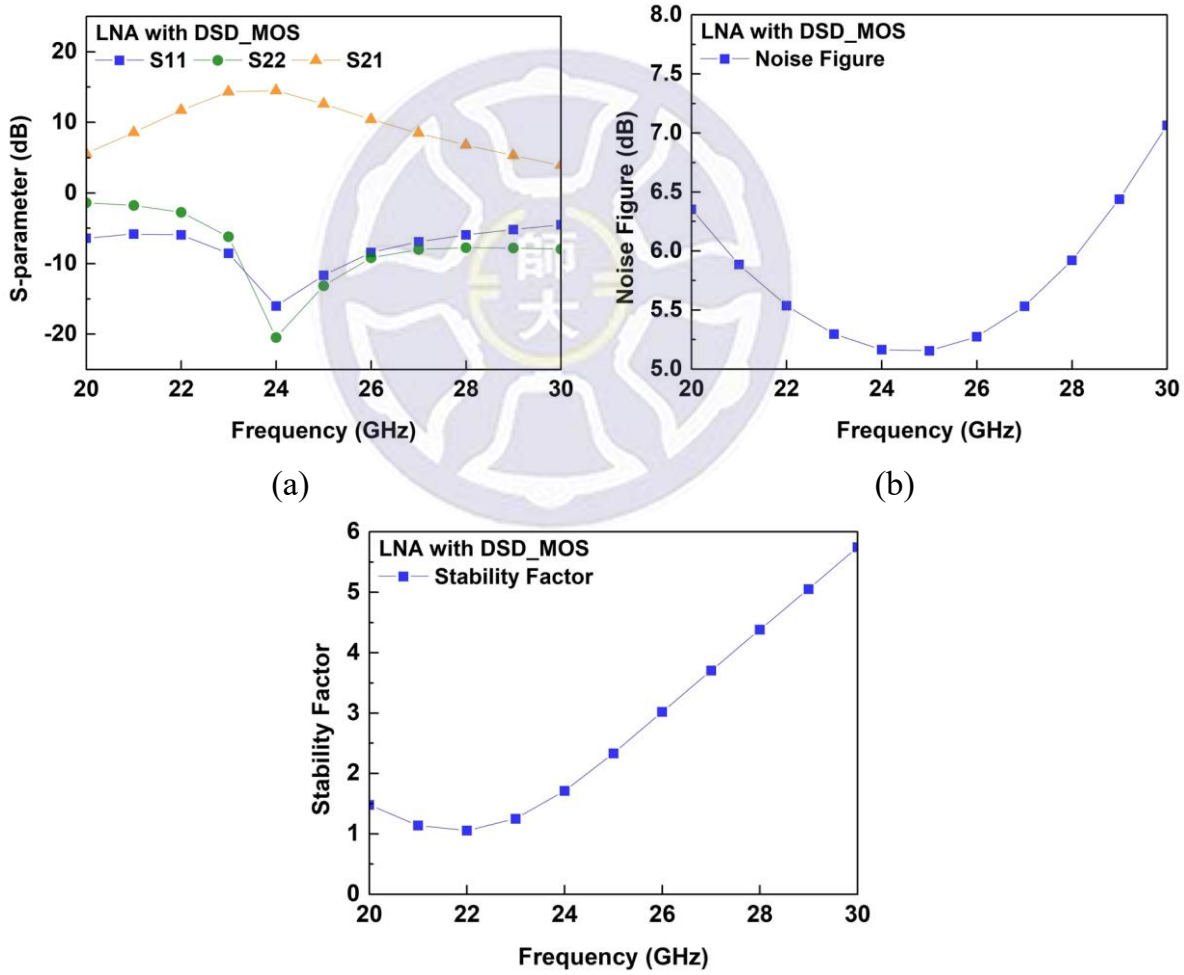


Fig. 3.12. Simulated (a) s-parameters, (b) noise figure, and (c) stability factor, of LNA with DSD_MOS.

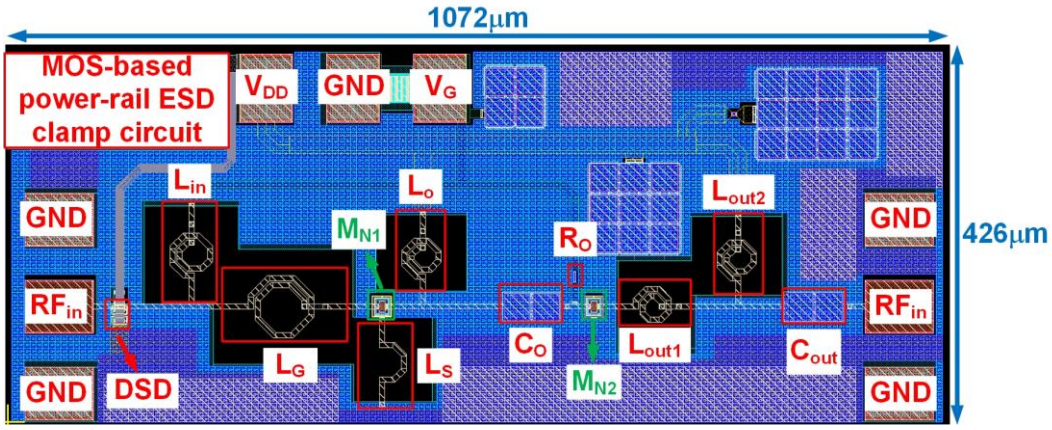


Fig. 3.13. The layout top view of LNA with DSD_MOS.

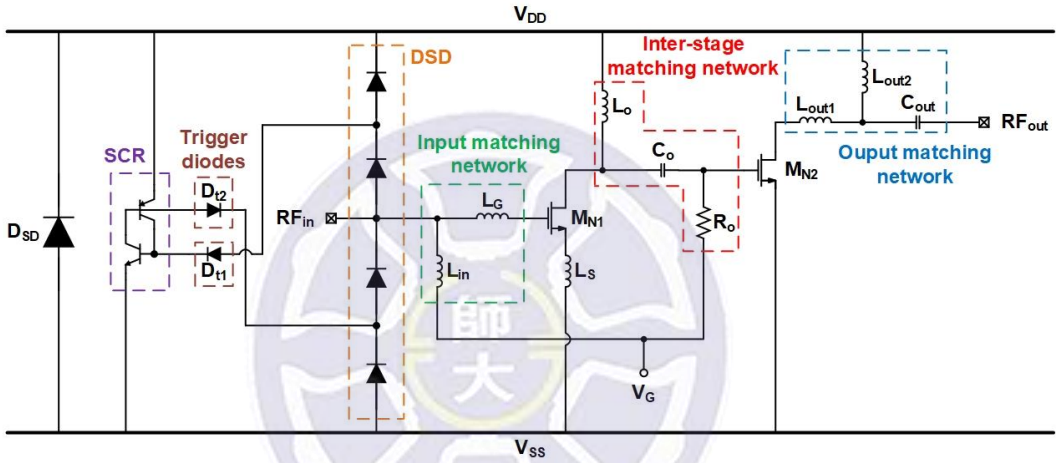
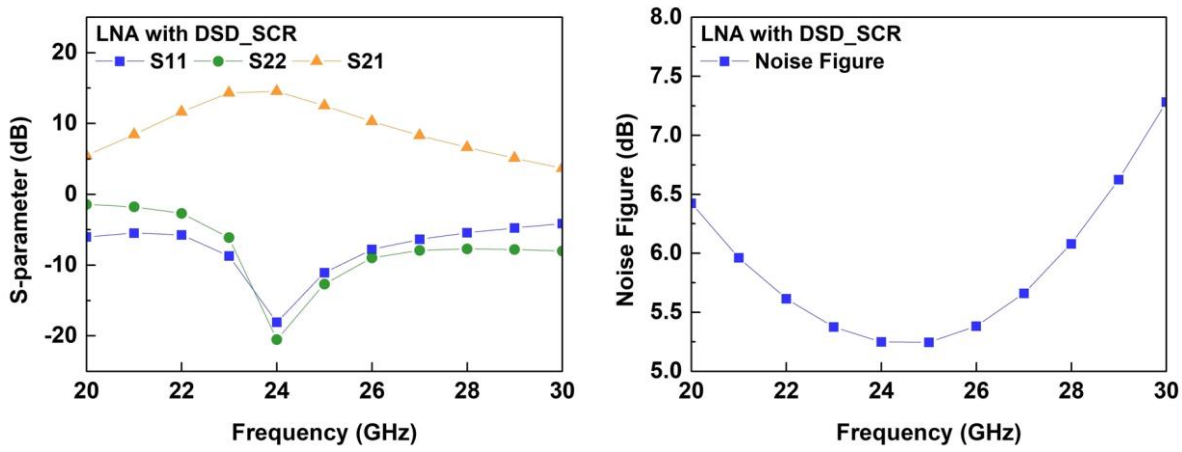
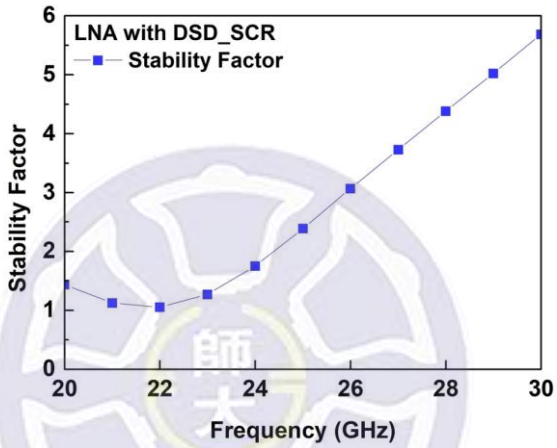


Fig. 3.14. Whole-chip ESD protection of LNA with DSD_SCR.



(a) (b)



(c)

Fig. 3.15. Simulated (a) s-parameters, (b) noise figure, and (c) stability factor, of LNA with DSD_SCR.

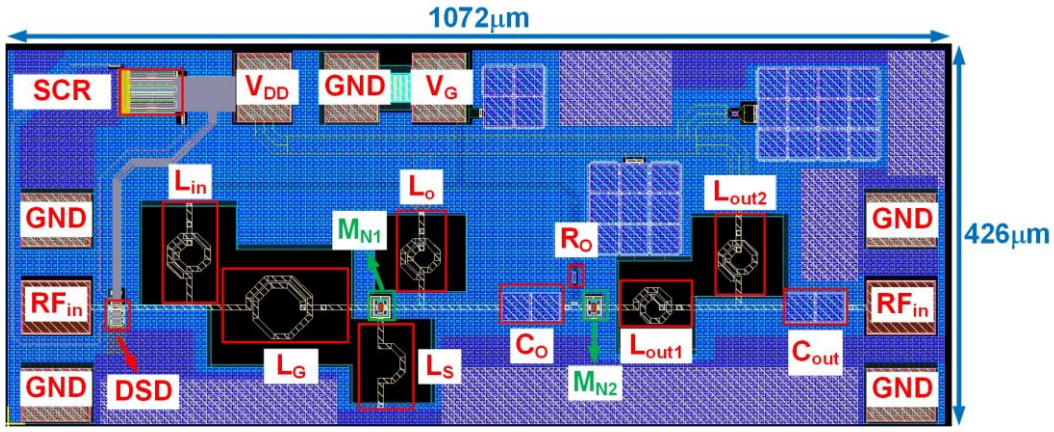


Fig. 3.16. The layout top view of LNA with DSD_SCR.

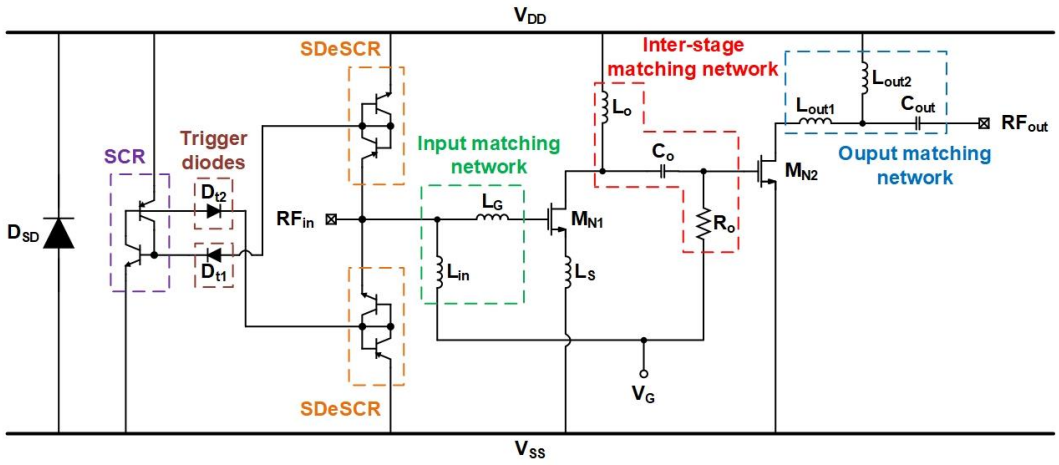


Fig. 3.17. Whole-chip ESD protection of LNA with SDeSCR_SCRs.

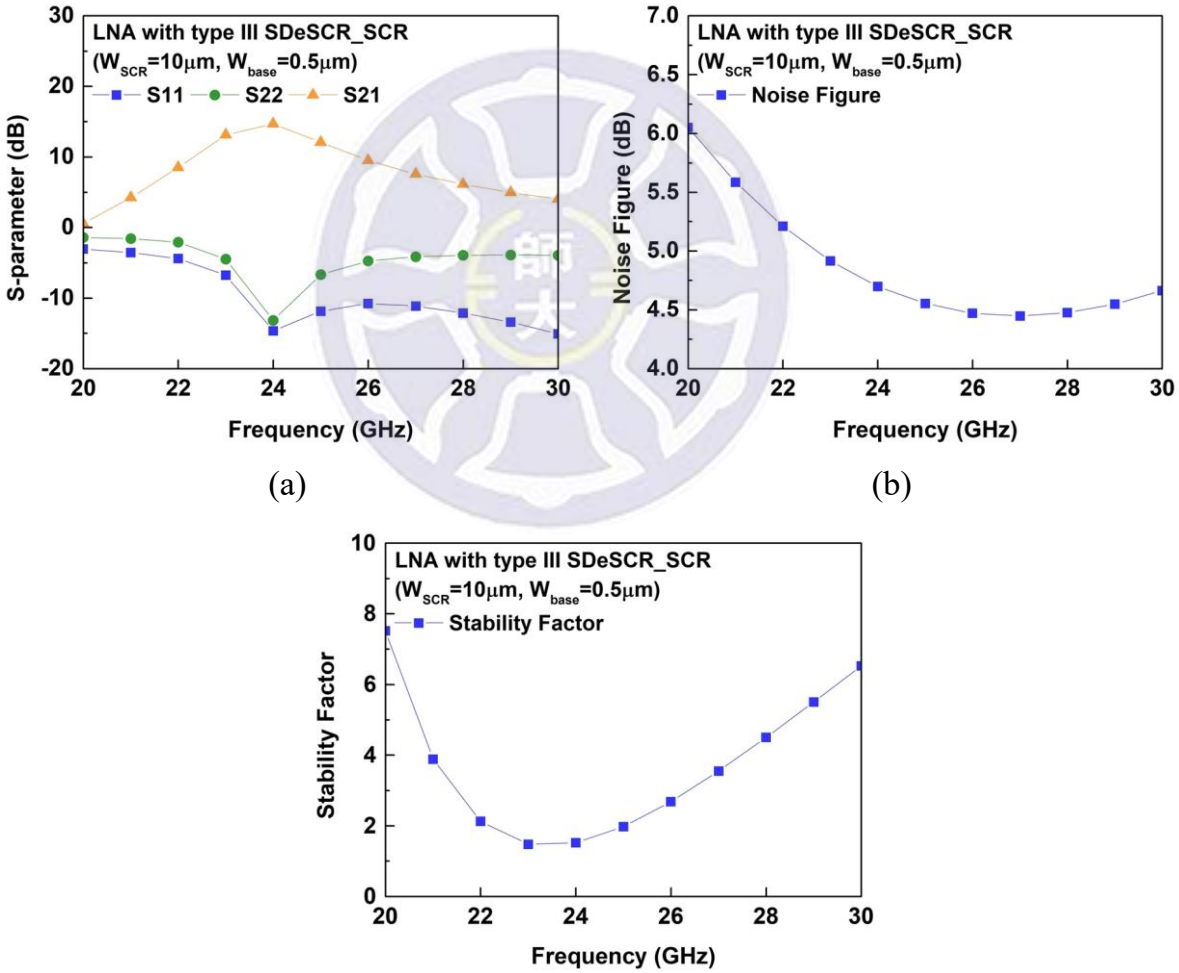


Fig. 3.18. Simulated (a) s-parameters, (b) noise figure, and (c) stability factor, of LNA with type III SDeSCR_SCR.

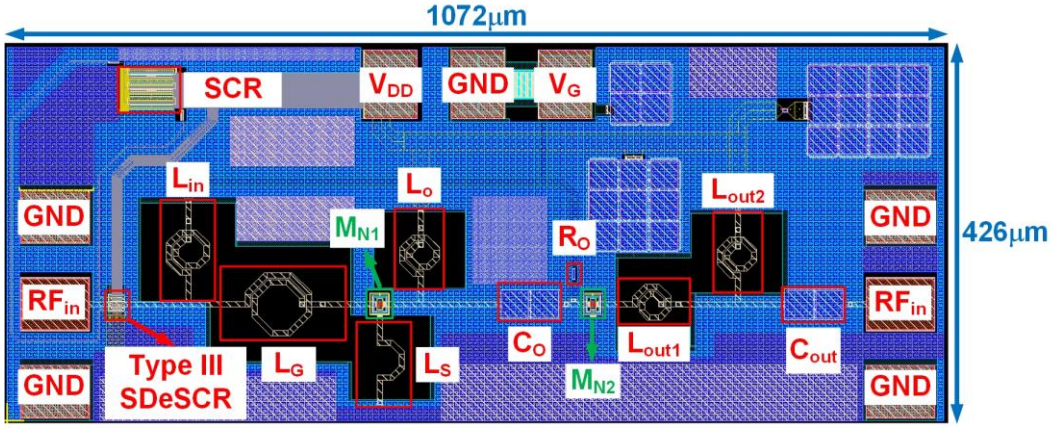


Fig. 3.19. The layout top view of LNA with type III SDeSCR_SCR.

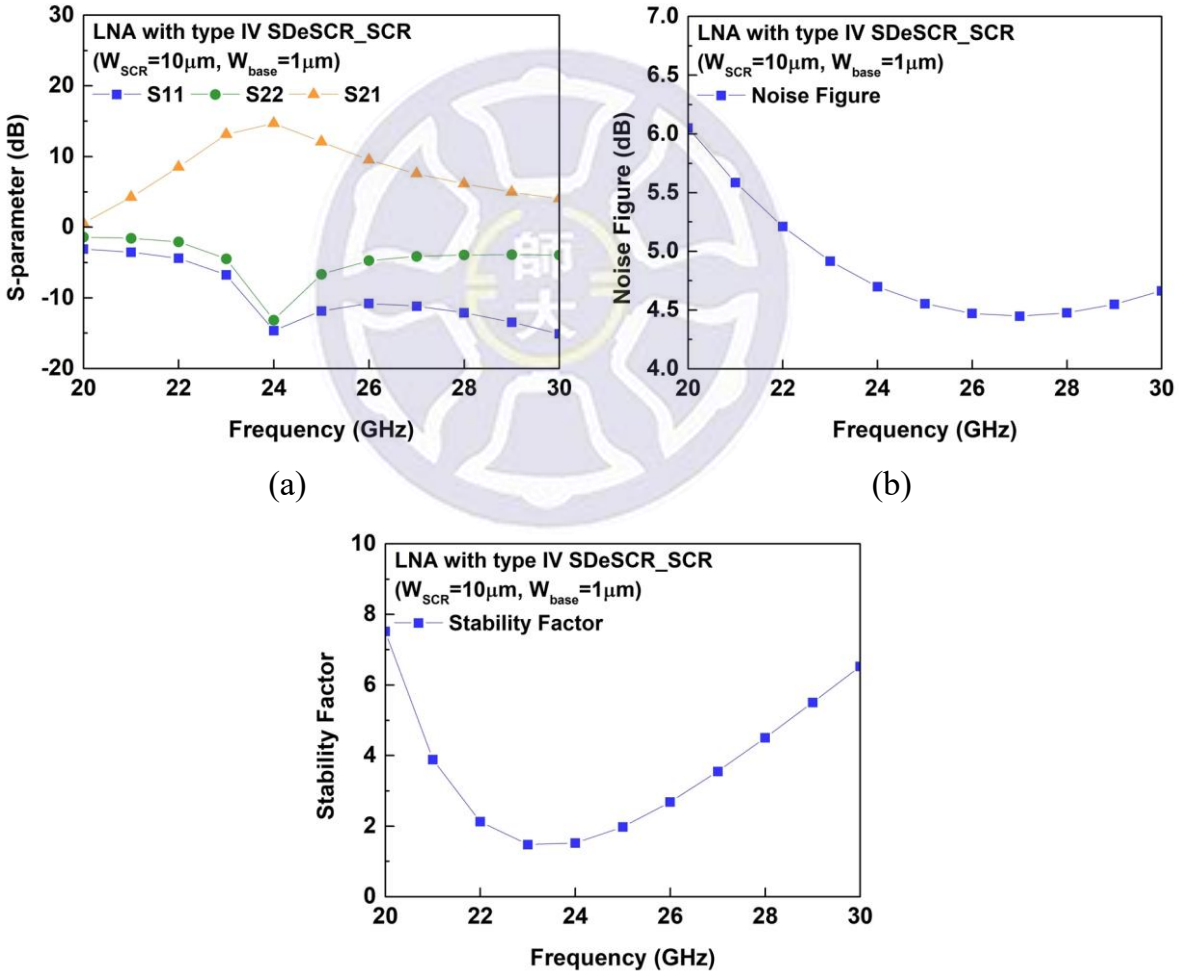


Fig. 3.20. Simulated (a) s-parameters, (b) noise figure, and (c) stability factor, of LNA with type IV SDeSCR_SCR.

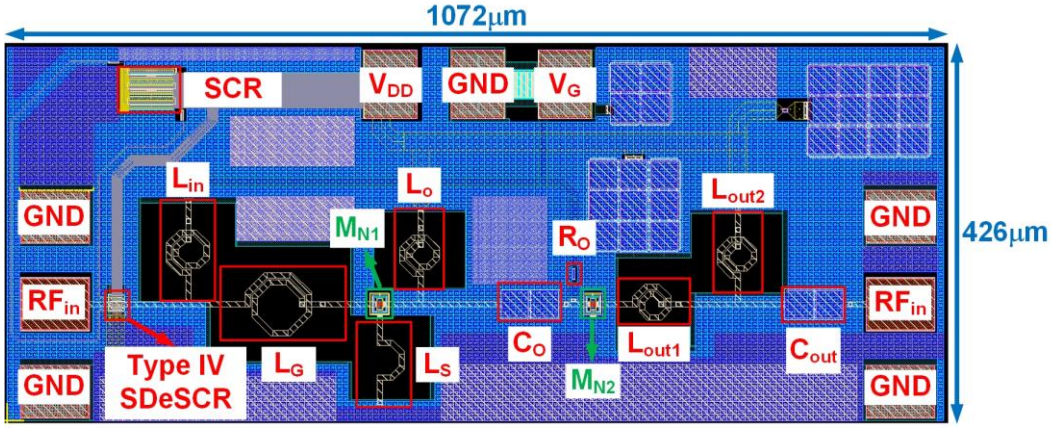


Fig. 3.21. The layout top view of LNA with type IV SDeSCR_SCR.

3.1.4 Measured 24-GHz Low-Noise Amplifier

In high-frequency measurement, a set of PGP probes and two sets of GSG probes are needed, and the V_{DD} and V_G are given 1.2 V and 0.8 V. The chip photo and the characteristics of the LNA without ESD protection are shown in Fig. 3.22 and Fig. 3.23. The S11, S22, S21, and noise figure are -22.37 dB, -16.57 dB, 9.89 dB, and 5.99 dB, respectively. The chip photo of LNA with DD_MOS is shown in Fig. 3.24, and the characteristics of the LNA with DD_MOS are shown in Fig. 3.25. The S11, S22, S21, and noise figure of LNA with DD_MOS at 24-GHz are -26.89 dB, -13.51 dB, 9.91 dB, and 5.78 dB, respectively. The chip photo of the LNA with DSD_MOS is shown in Fig. 3.26, and the characteristics of the LNA with DSD_MOS are shown in Fig. 3.27. The S11, S22, S21, and the noise figure of the LNA with DSD_MOS at 24-GHz are -21.65 dB, -14.55 dB, 9.89 dB, and 5.79 dB, respectively. The chip photo of the LNA with DSD_SCR is shown in Fig. 3.28, and the characteristics of the LNA with DSD_SCR are shown in Fig. 3.29. The S11, S22, S21, and noise figure of the LNA with DSD_SCR at 24-GHz are -15.92 dB, -13.25 dB, 9.88 dB, and 5.92 dB, respectively. The chip photo of the LNA with SDeSCR_SCR is shown in Fig. 3.30, and the characteristics of the LNA with type III SDeSCR_SCR are shown in Fig. 3.31. The S11, S22, S21, and noise figure

of the LNA with type III SDeSCR_SCR at 24-GHz are -15.59 dB, -15.72 dB, 9.76 dB, and 6.83 dB, respectively. The LNA with type IV SDeSCR_SCR is shown in Fig. 3.32. The S11, S22, S21, and noise figure of the LNA with type IV SDeSCR_SCR at 24-GHz are -15.4 dB, -15.7 dB, 9.89 dB, and 6.81 dB, respectively.

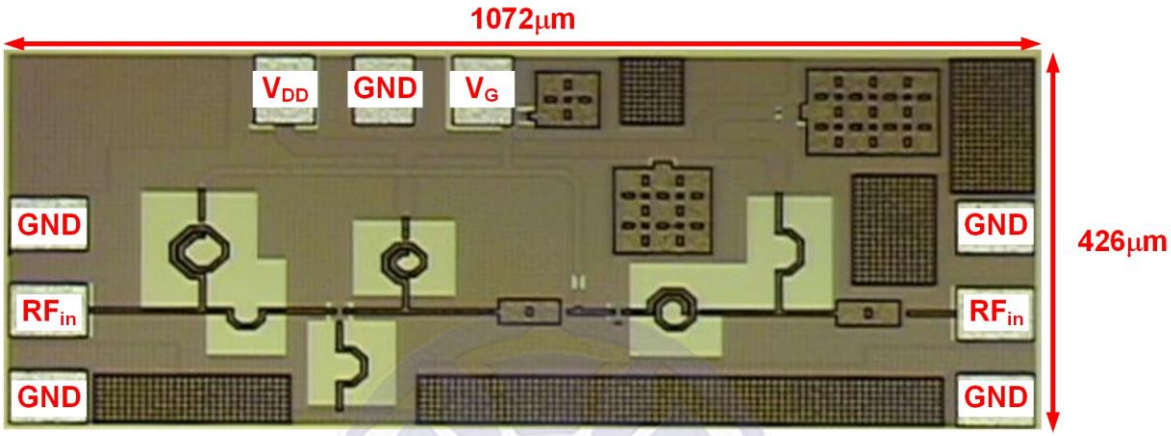
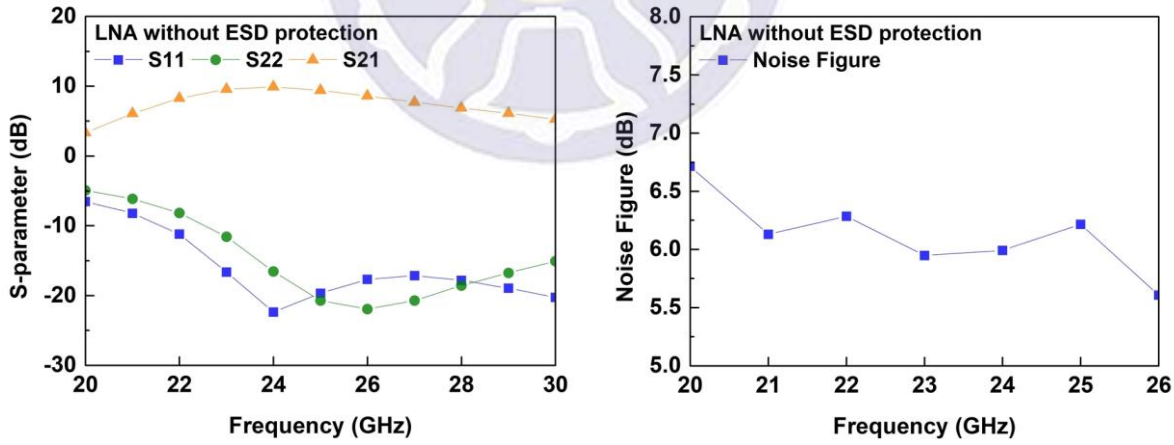


Fig. 3.22. Chip photo of LNA without ESD protection.



(a) (b)

Fig. 3.23. Measured (a) s-parameter and (b) noise figure of LNA without ESD protection.

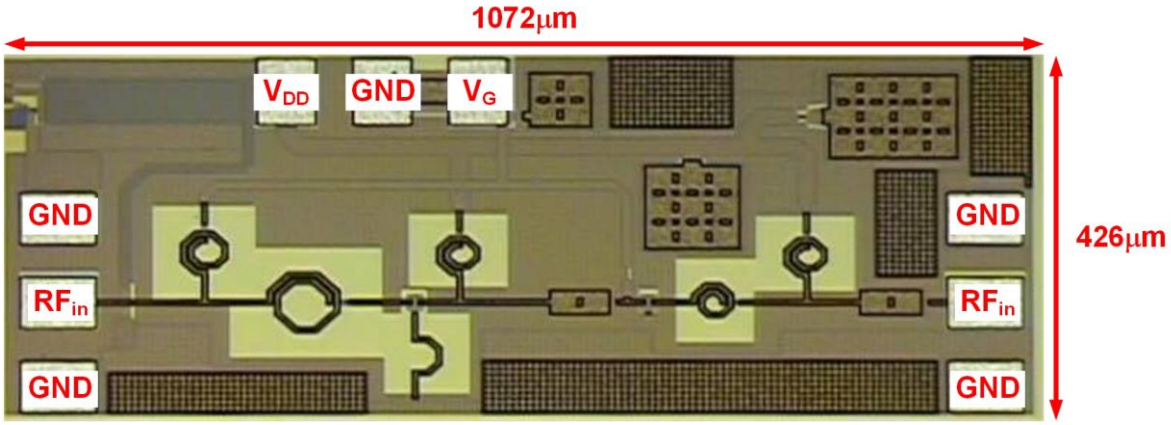
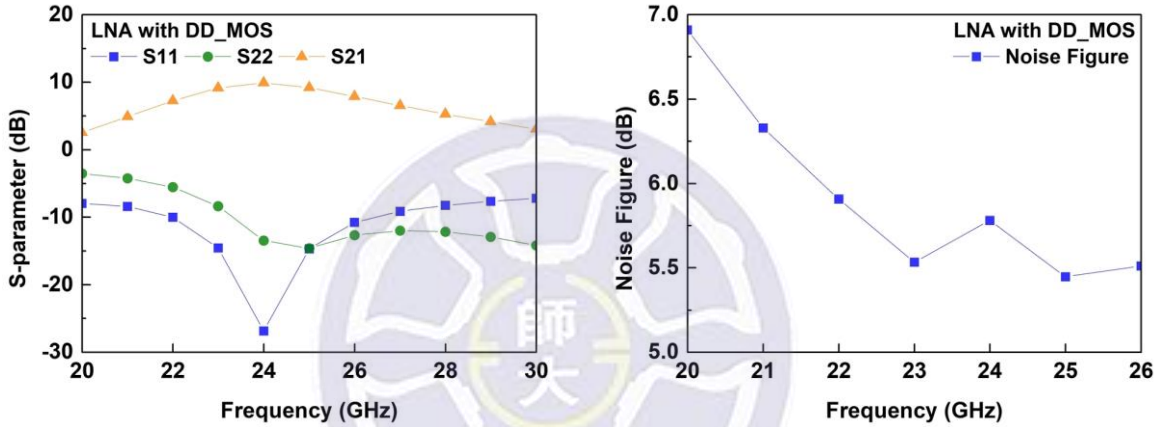


Fig. 3.24. Chip photo of LNA with DD_MOS.



(a) (b)

Fig. 3.25. Measured (a) s-parameter and (b) noise figure of LNA with DD_MOS.

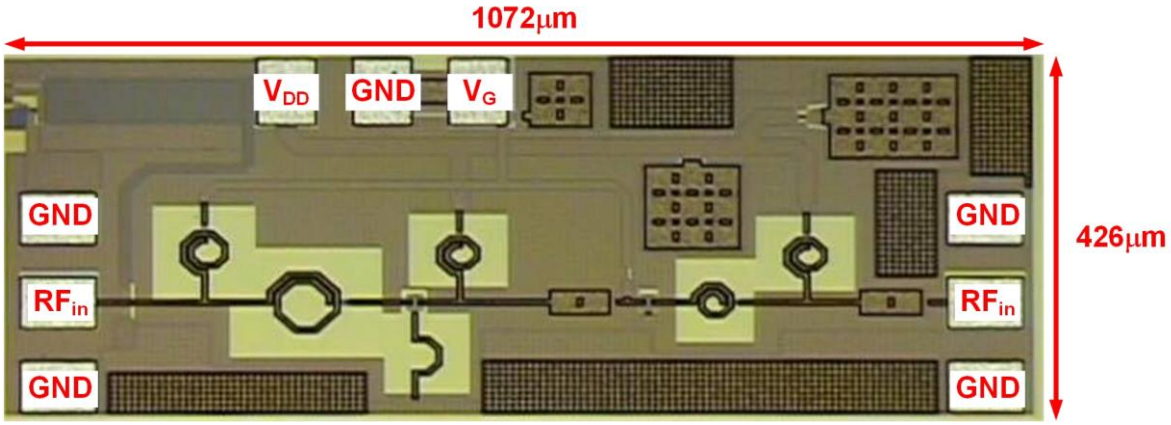
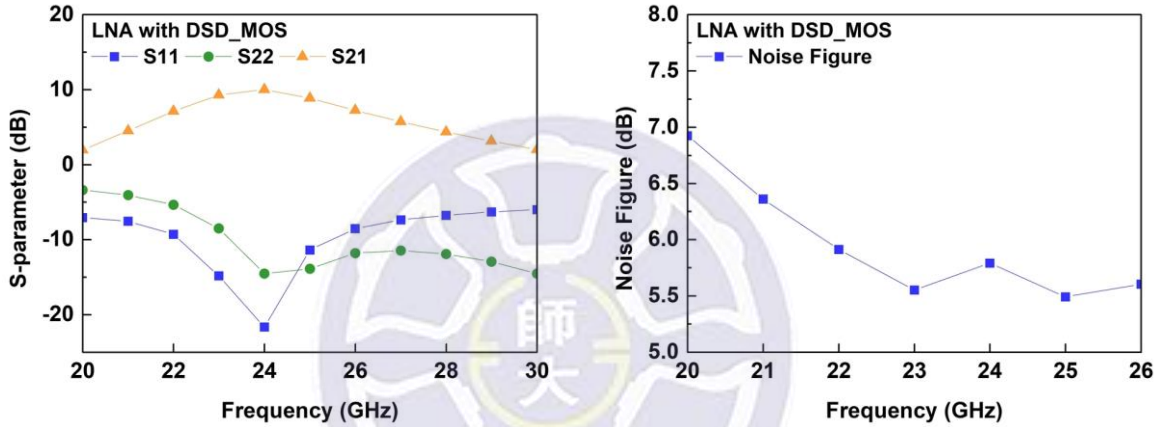


Fig. 3.26. Chip photo of LNA with DSD_MOS.



(a) (b)

Fig. 3.27. Measured (a) s-parameter and (b) noise figure of LNA with DSD_MOS.

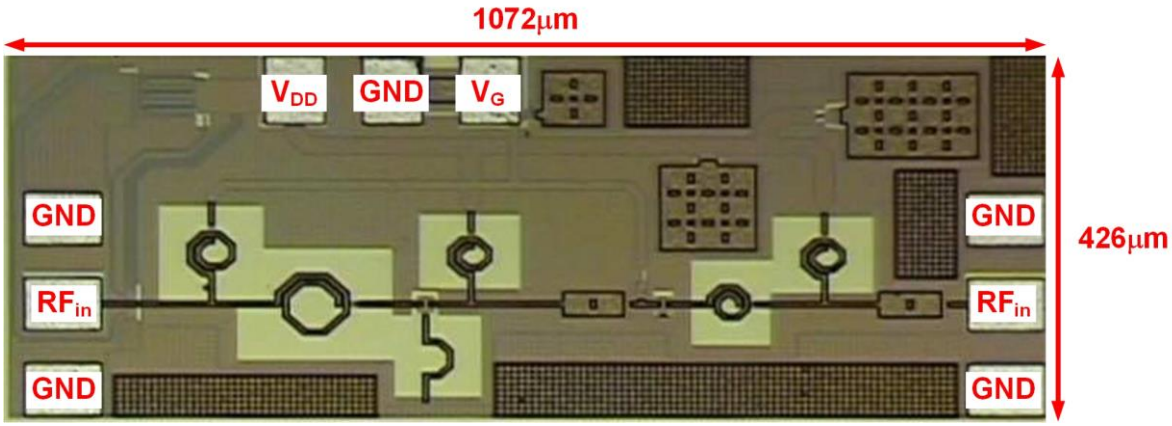
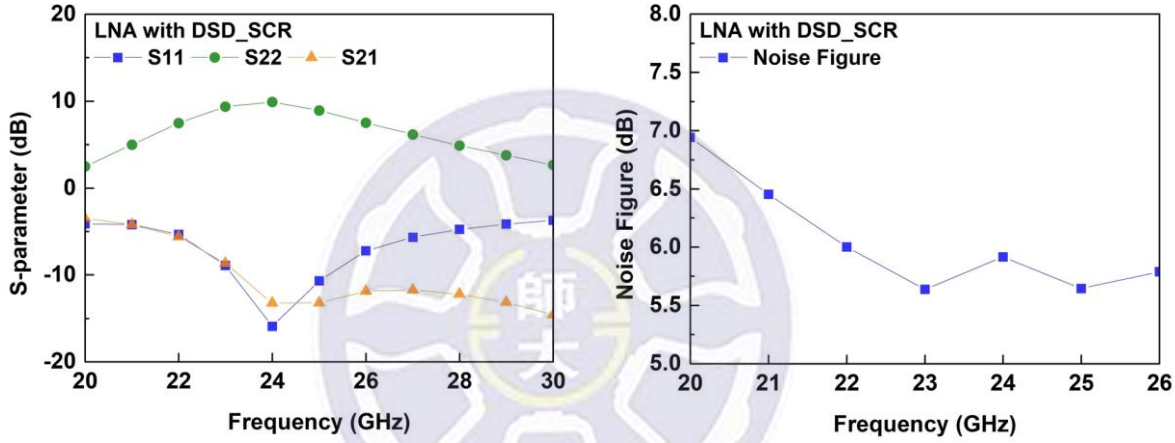


Fig. 3.28. Chip photo of LNA with DSD_SCR.



(a) (b)

Fig. 3.29. Measured (a) s-parameter and (b) noise figure of LNA with DSD_SCR.

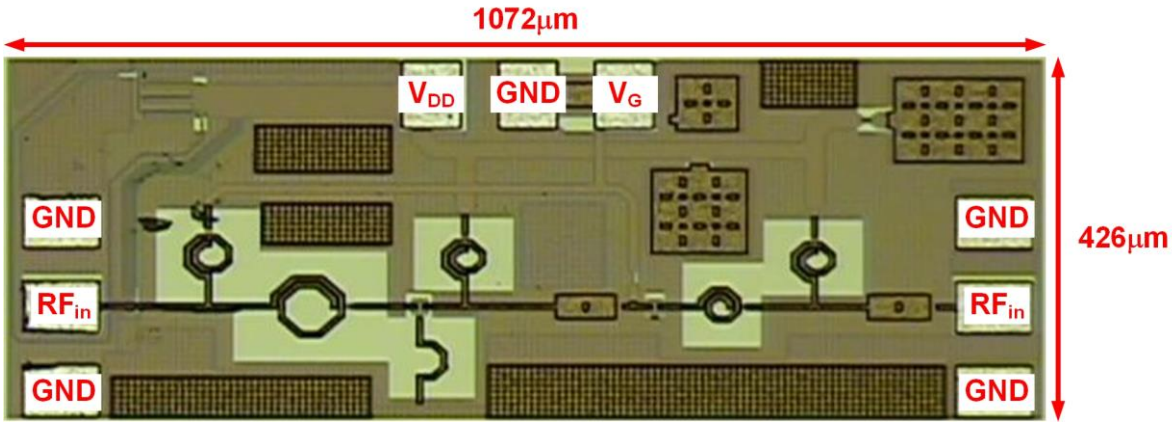
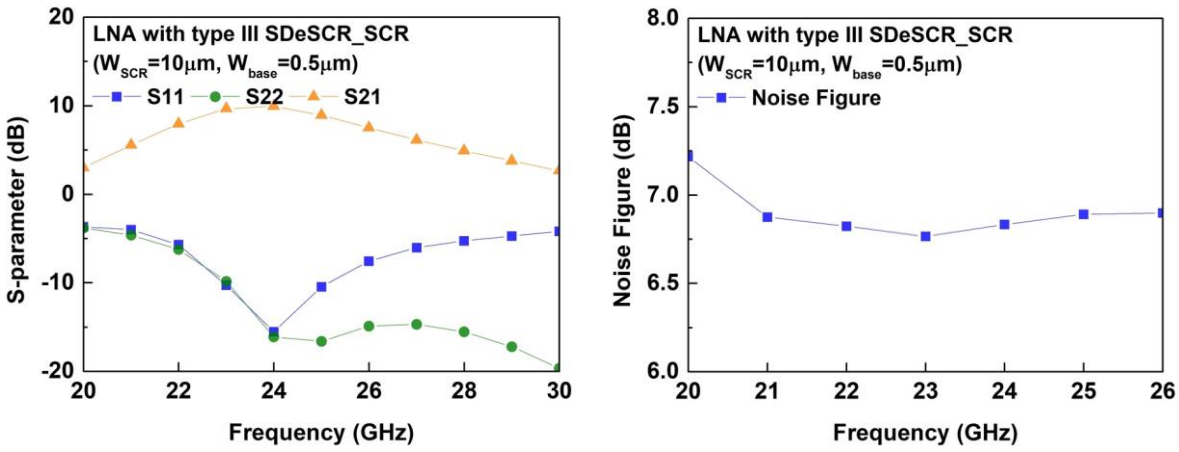
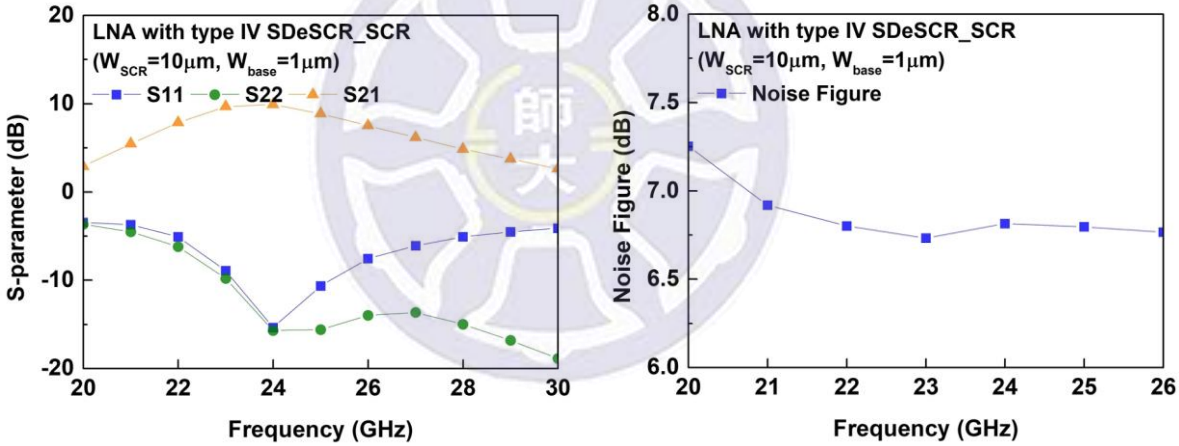


Fig. 3.30. Chip photo of LNA with SDeSCR_SCR.



(a) (b)

Fig. 3.31. Measured (a) s-parameter and (b) noise figure of LNA with type III SDeSCR_SCR.



(a) (b)

Fig. 3.32. Measured (a) s-parameter and (b) noise figure of LNA with type IV SDeSCR_SCR.

3.2 Verification of 24-GHz Low-Noise Amplifier in Component-Level ESD

3.2.1 TLP I-V Curves of 24-GHz Low-Noise Amplifier

In order to determine whether the LNAs damaged or not, observing leakage current of devices is a way. When the leakage current suddenly increases, it represents devices short. When leakage current suddenly decreases from large to small, it represents metal lines open. Measured TLP I-V curves of LNA with traditional devices and SDeSCR_SCRs are shown in Fig. 2.32 and Fig. 3.34. At PS mode, the anode and cathode are connected to RF_{in} and V_{SS}, respectively, and the RF_{in} is given 0.8 V. At PD mode, the anode and cathode are connected to RF_{in} and V_{DD}, respectively, and the RF_{in} is given 0.4 V. At NS mode, the anode and cathode are connected to V_{SS} and RF_{in}, respectively, and the V_{SS} is given -0.8 V. At ND mode, the anode and cathode are connected to V_{DD} and RF_{in}, respectively, and the V_{DD} is given 0.4 V. From Fig. 3.33(a) and 3.33(c), the leakage current of the LNA with DD_MOS is larger than LNA with DSD_MOS and LNA with DSD_SCR. Because the bias voltage is set to 0.8 V causing that diode between I/O pad and V_{DD} is turned on, so that the leakage current increases. The leakage current of the LNA with ESD devices is slightly higher than ESD devices because adding the LNA leads to increase the leakage current. From the I_{t2} of LNA with ESD protection, LNA with DD_MOS has the lower I_{t2} than LNA with DSD_MOS and DSD_SCR at PD mode. At PS mode, the LNA with DSD_SCR, type III SDeSCR_SCR, and type IV SDeSCR_SCR have the lowest I_{t2} than other modes, as shown in Table 3.1.

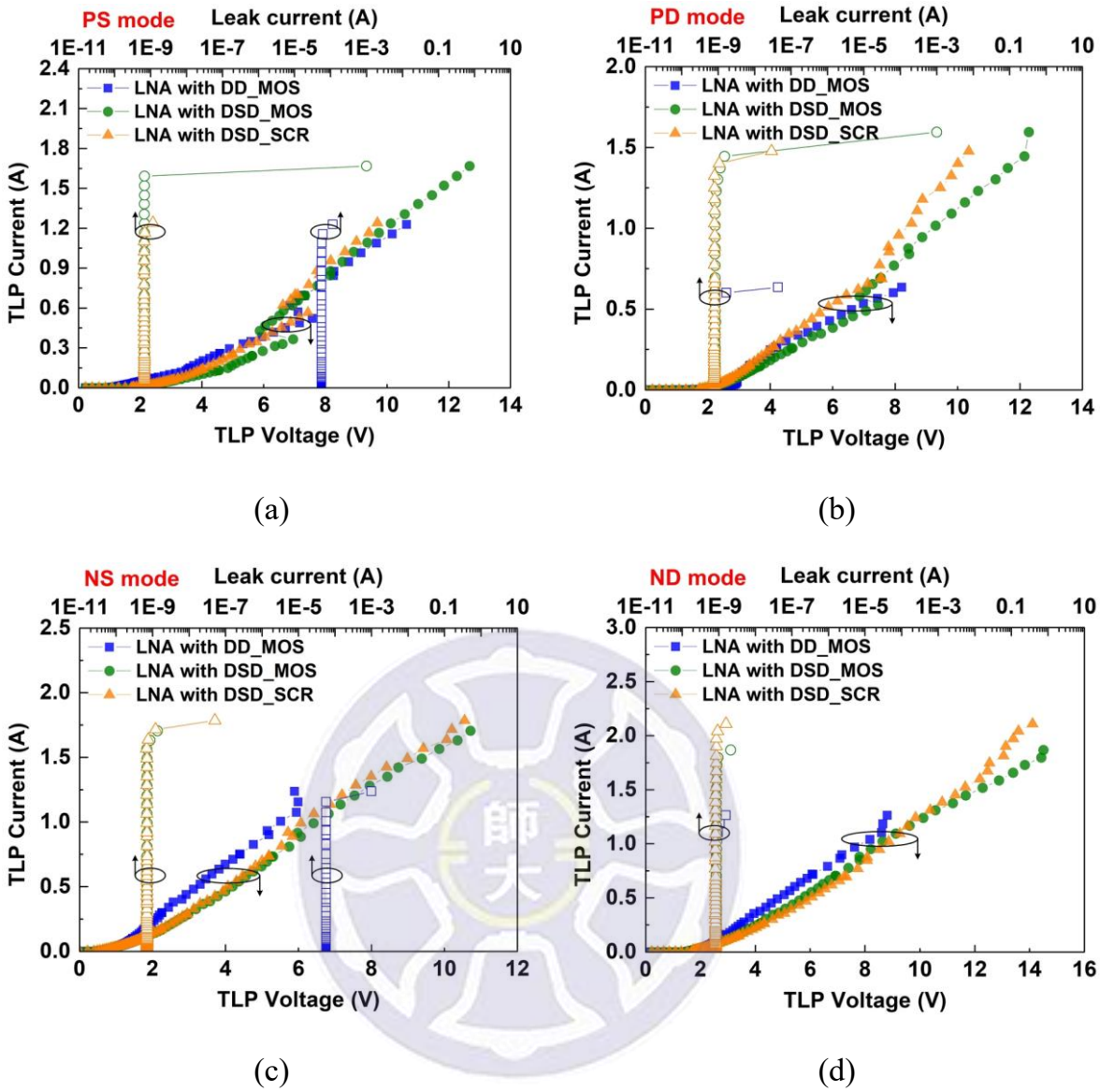


Fig. 3.33. Measured TLP I-V curves of LNA with traditional devices at (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

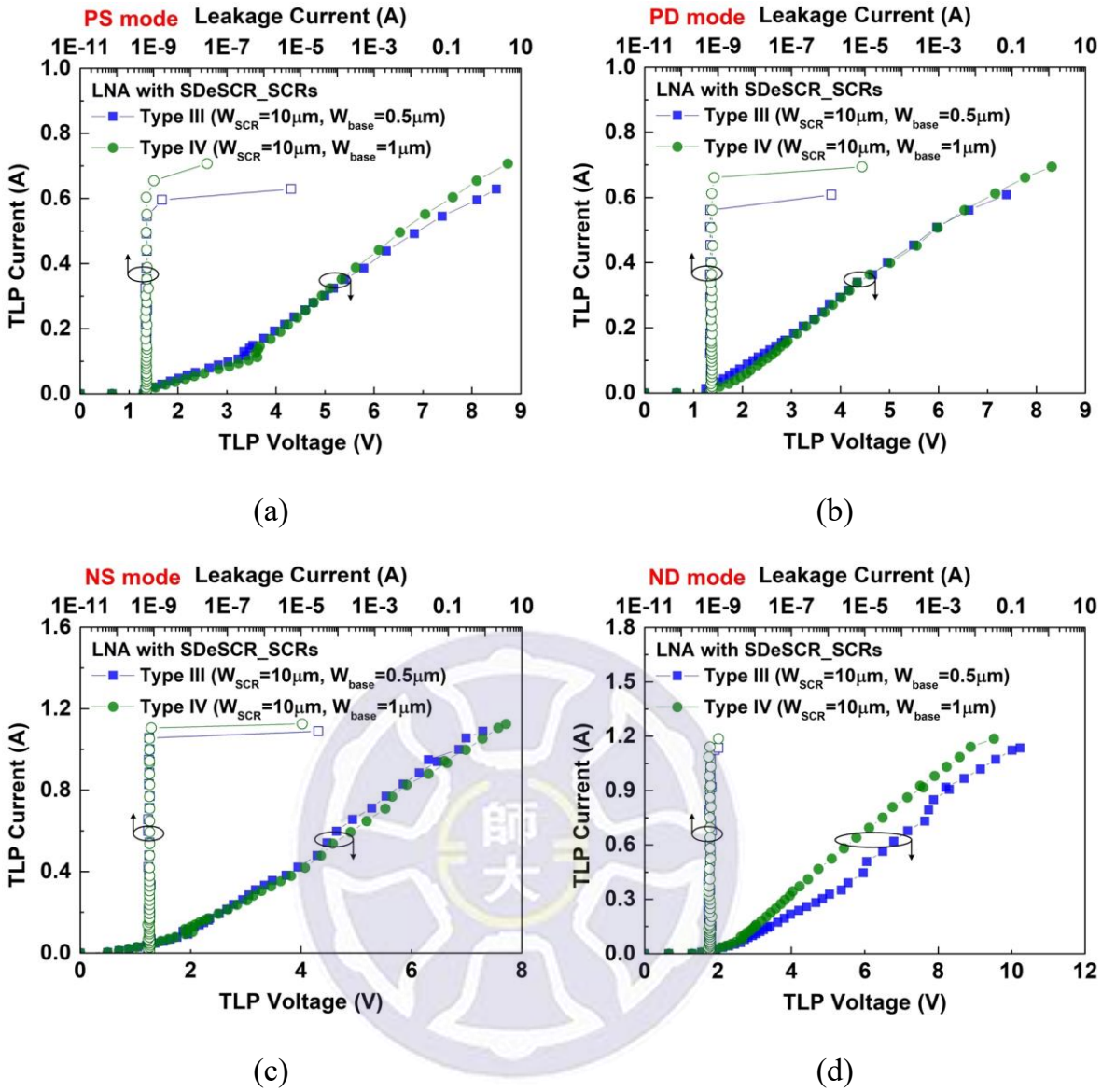


Fig. 3.34. Measured TLP I-V curves of LNA with type III and type IV SDeSCR_SCRs at (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

Table 3.1

I_{t2} of LNA with ESD protection at different modes.

Test devices	I_{t2} (A)			
	PS	PD	NS	ND
LNA with DD_MOS	1.2	0.6	1.2	1.1
LNA with DSD_MOS	1.6	1.3	1.6	1.8
LNA with DSD_SCR	1.2	1.3	1.6	2
LNA with type III SDeSCR_SCR	0.5	0.6	1.1	1.2
LNA with type IV SDeSCR_SCR	0.6	0.7	1.1	1.1

3.2.2 ESD Stresses on 24-GHz Low-Noise Amplifier

Using HBM tester gives different HBM stresses to test LNA. If the characteristics of the LNA are changed, it can prove that the LNA has been damaged. In addition, measured leakage current from RF_{in} to V_{SS} of the LNA is also a method to judge whether the circuit is damaged. The HBM test also has PS mode, PD mode, NS mode, and ND mode. At PS mode, anode terminal gives a positive ESD stresses to RF_{in}, and the V_{SS} connects to the cathode terminal. At PD mode, the anode terminal gives a positive ESD stresses to the RF_{in}, and the V_{DD} connects to the cathode terminal. At NS mode, the anode terminal gives a negative ESD stresses to the RF_{in}, and the V_{SS} connects to the cathode terminal. At ND mode, the anode terminal gives a negative ESD stresses to the RF_{in}, and the V_{DD} connects to the cathode terminal. One HBM level gives one ESD stress at the same mode, each 0.5 kV one step, and gradually increases HBM level until the characteristics or the leakage current of the LNA different from original LNA. After 0.5 kV HBM stresses, the LNA without ESD protection changes its original characteristics because the LNA has been damaged. The leakage current of the LNA

without ESD protection increases rapidly after 0.5 kV HBM stresses. According to the measurement results, the LNA cannot bear 0.5 kV or even lower of ESD stress, as shown in Fig. 3.35.

The LNA with DD_MOS, DSD_MOS, DSD_SCR, type III SDeSCR_SCR, and type IV SDeSCR_SCR also use the same test. As shown in Fig. 3.36 to Fig. 3.38, after 2.5 kV HBM stresses, the LNA with DD_MOS, DSD_MOS, and DSD_SCR change its original characteristics because the LNAs have been damaged. Besides, the leakage current of the LNA with DD_MOS gradually increases after 2 kV and 2.5 kV HBM stresses. The leakage current of the LNA with DSD_MOS and DSD_SCR increases rapidly after 2.5 kV HBM stresses. The LNA with type III and type IV SDeSCR_SCRs do not change its original characteristics because the LNAs have not suffered damage yet. Besides, the leakage current of the LNAs increases rapidly after 2 kV HBM stresses.

Therefore, from the leakage current of the LNA can judge how much HBM level the LNA can bear. The HBM level of the LNA with DD_MOS, DSD_MOS, and DSD_SCR are 1.5 kV, 2 kV, and 2 kV, respectively. The LNA with type III and type IV SDeSCR_SCRs can bear 1.5 kV HBM stresses, but LNAs cannot bear over 2 kV HBM stresses, as shown in Fig. 3.39 and Fig. 3.40. Table 3.2 shows the performance of the LNAs and references. The gain of the LNA without and with ESD protection are 9.9 dB at 24-GHz. The noise figure of the LNA without ESD protection at 24-GHz is 6 dB. The noise figure of the LNA with DD_MOS, DSD_MOS, DSD_SCR, type III SDeSCR_SCR, and type IV SDeSCR_SCR at 24-GHz are 5.8 dB, 5.8 dB, 5.9 dB, 6.8 dB, and 6.8 dB, respectively. Although the proposed LNA with type III and type IV SDeSCR_SCRs have a lower HBM level than LNA with DSD_MOS and DSD_SCR, the LNA with type III and type IV SDeSCR_SCRs can still provide 1.5 kV HBM ESD level. The layout area of the LNA with type III and type IV SDeSCR_SCRs are less than

a quarter of the LNA with DD_MOS and with DSD_MOS, and reference [38].

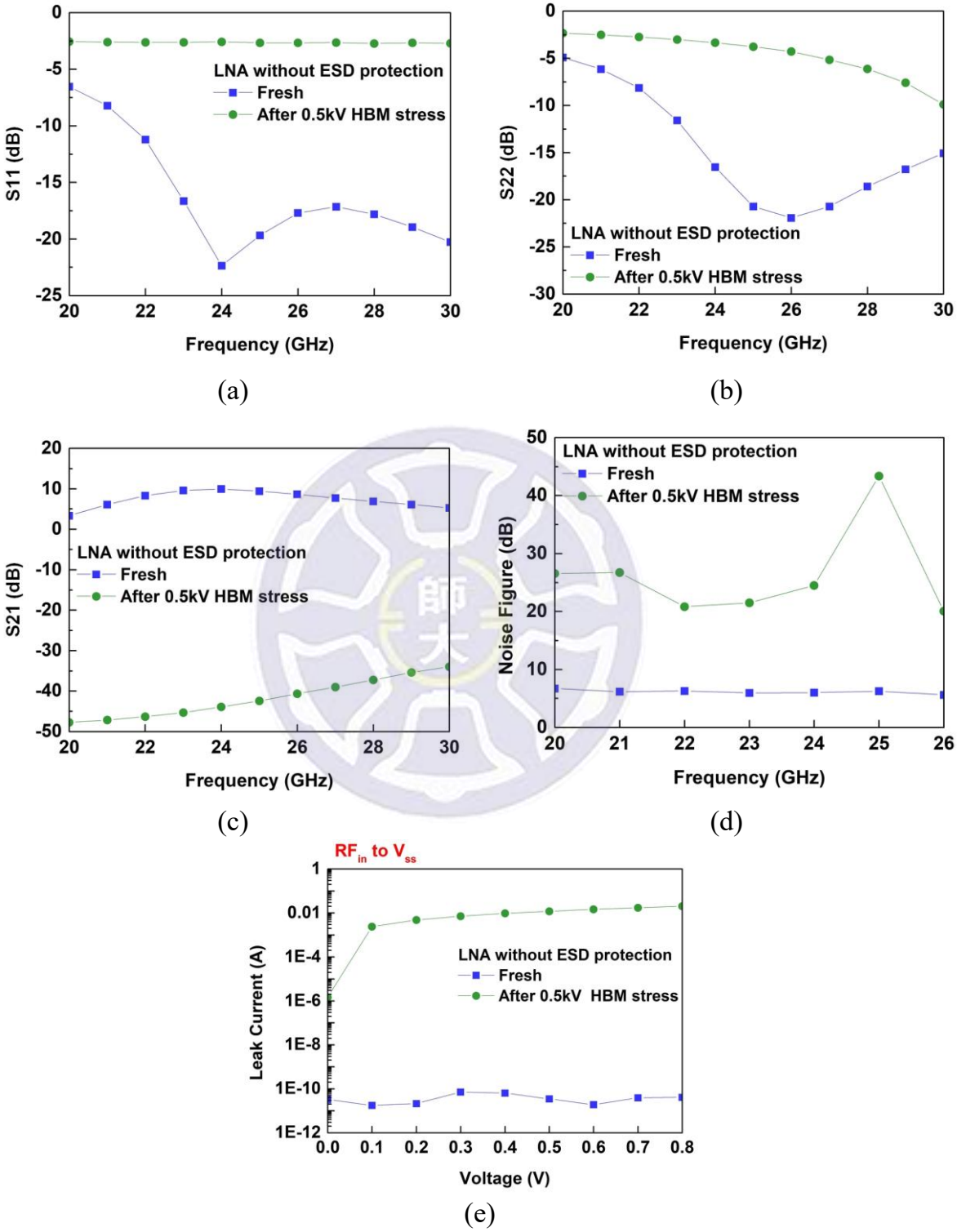


Fig. 3.35. Measured (a) S11, (b) S22, (c) S21, (d) noise figure, and (e) leak current, of LNA without ESD protection after HBM stress.

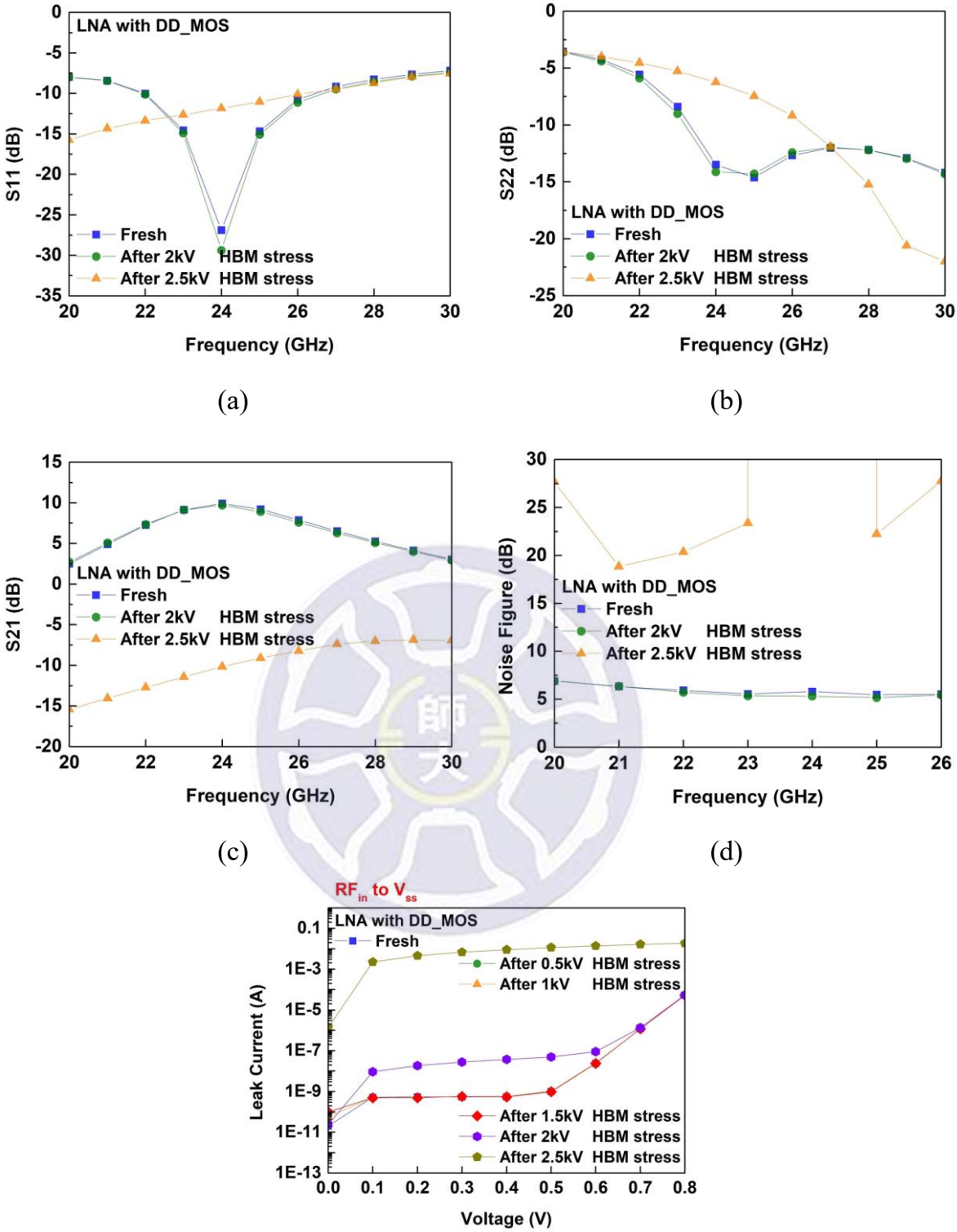


Fig. 3.36. Measured (a) S11, (b) S22, (c) S21, (d) noise figure, and (e) leak current, of LNA with DD_MOS after HBM stress.

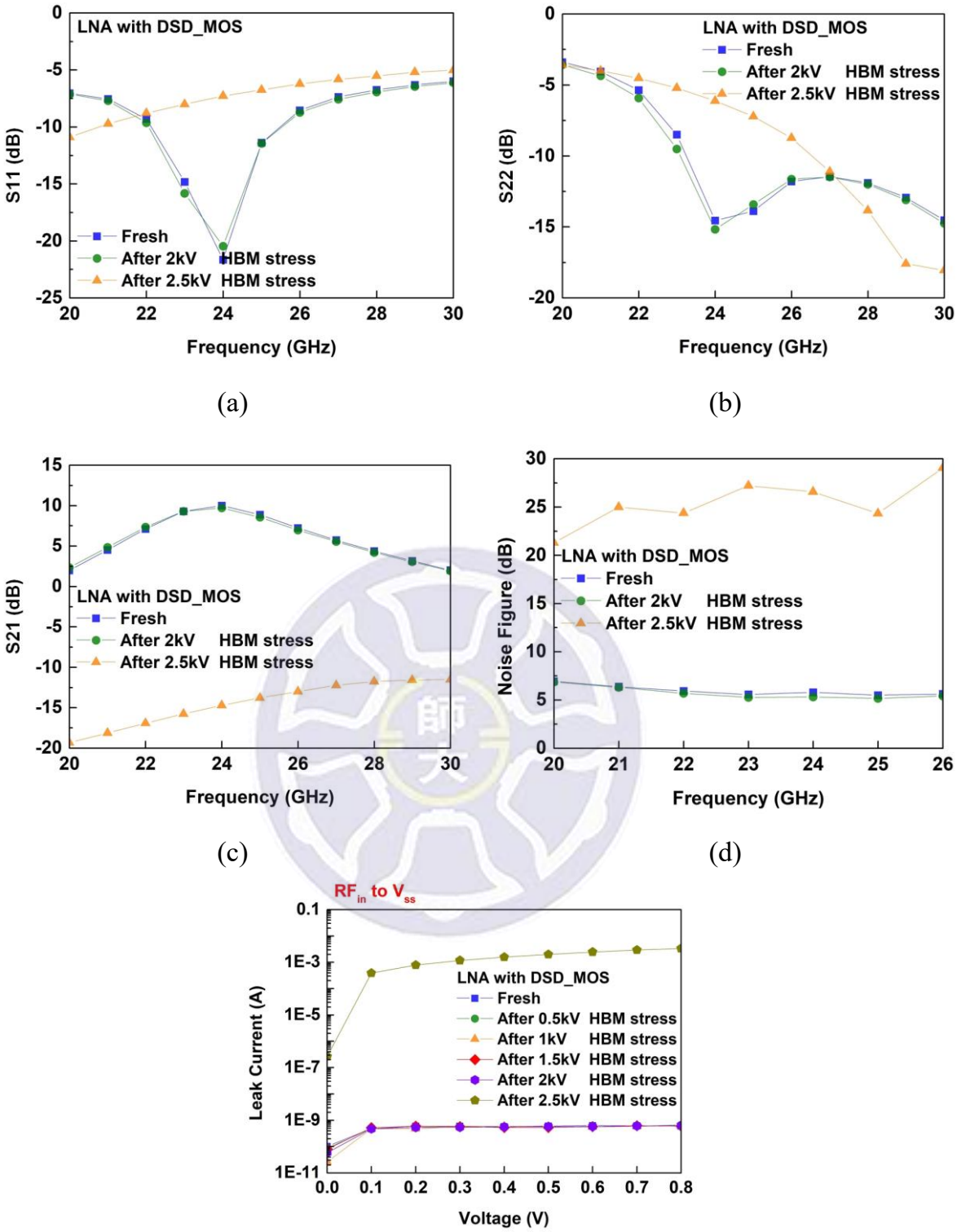


Fig. 3.37. Measured (a) S11, (b) S22, (c) S21, (d) noise figure, and (e) leak current, of LNA with DSD_MOS after HBM stress.

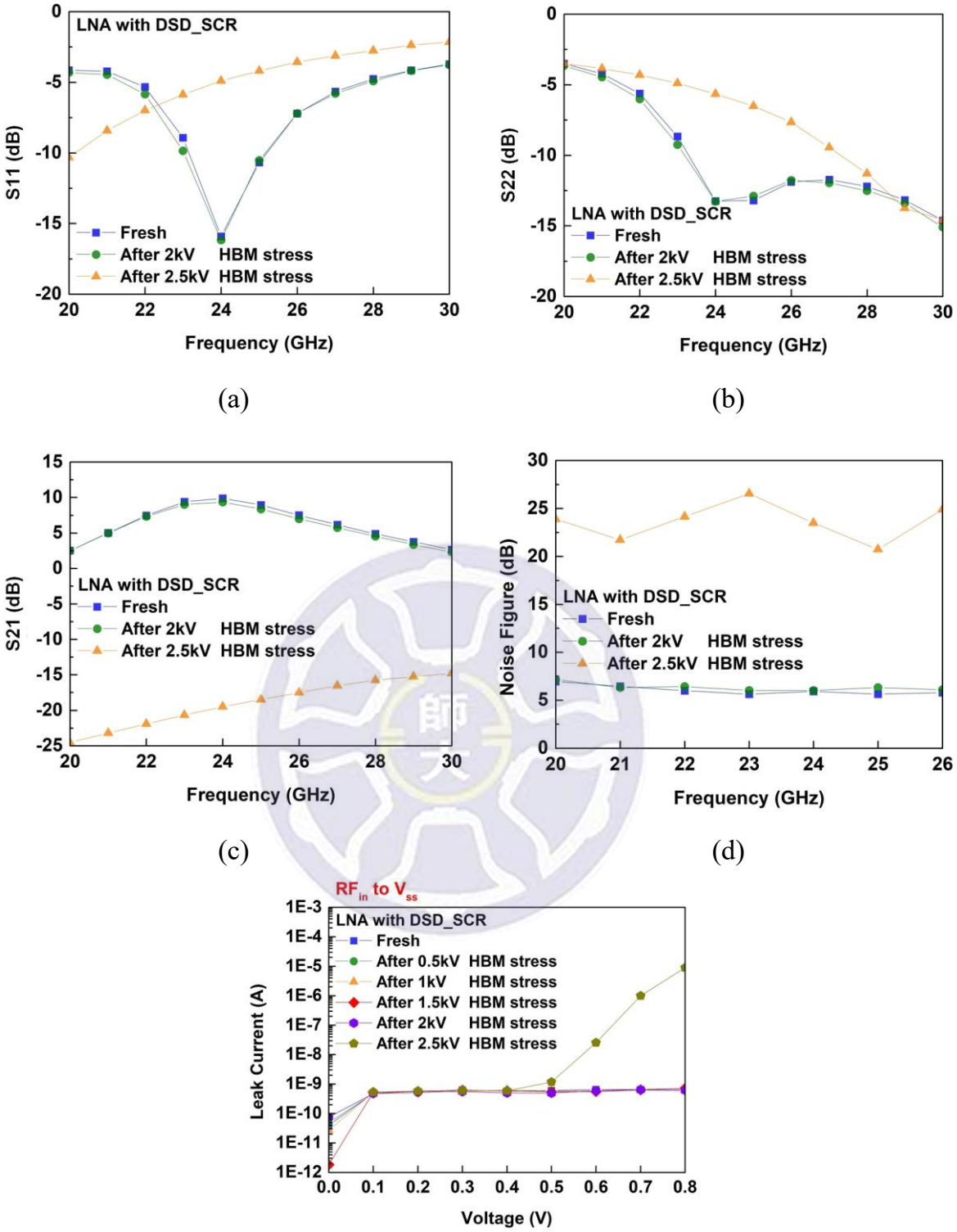


Fig. 3.38. Measured (a) S11, (b) S22, (c) S21, (d) noise figure, and (e) leak current, of LNA with DSD_SCR after HBM stress.

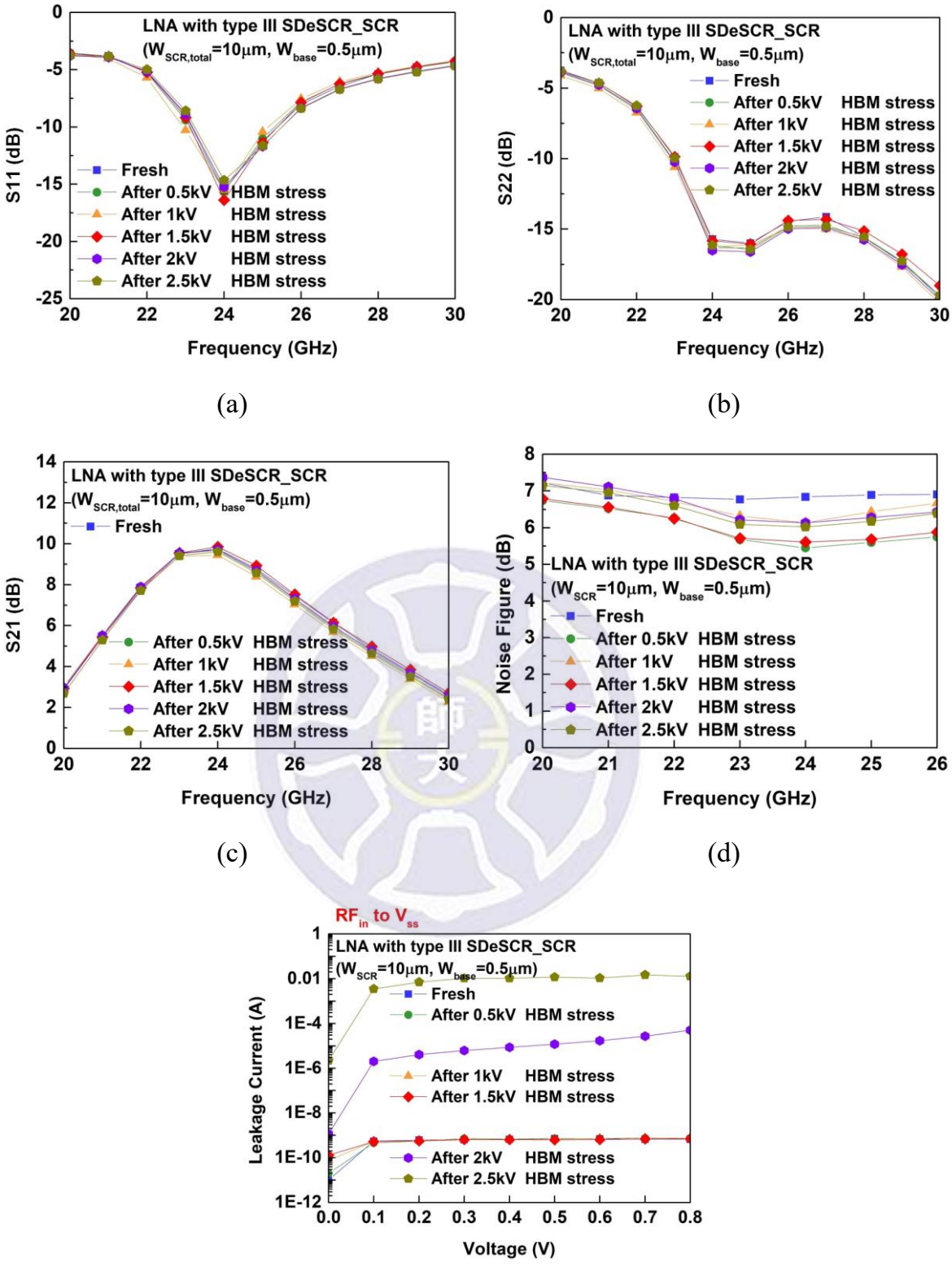


Fig. 3.39. Measured (a) S11, (b) S22, (c) S21, (d) noise figure, and (e) leak current, of LNA with type III SDeSCR_SCR after HBM stress.

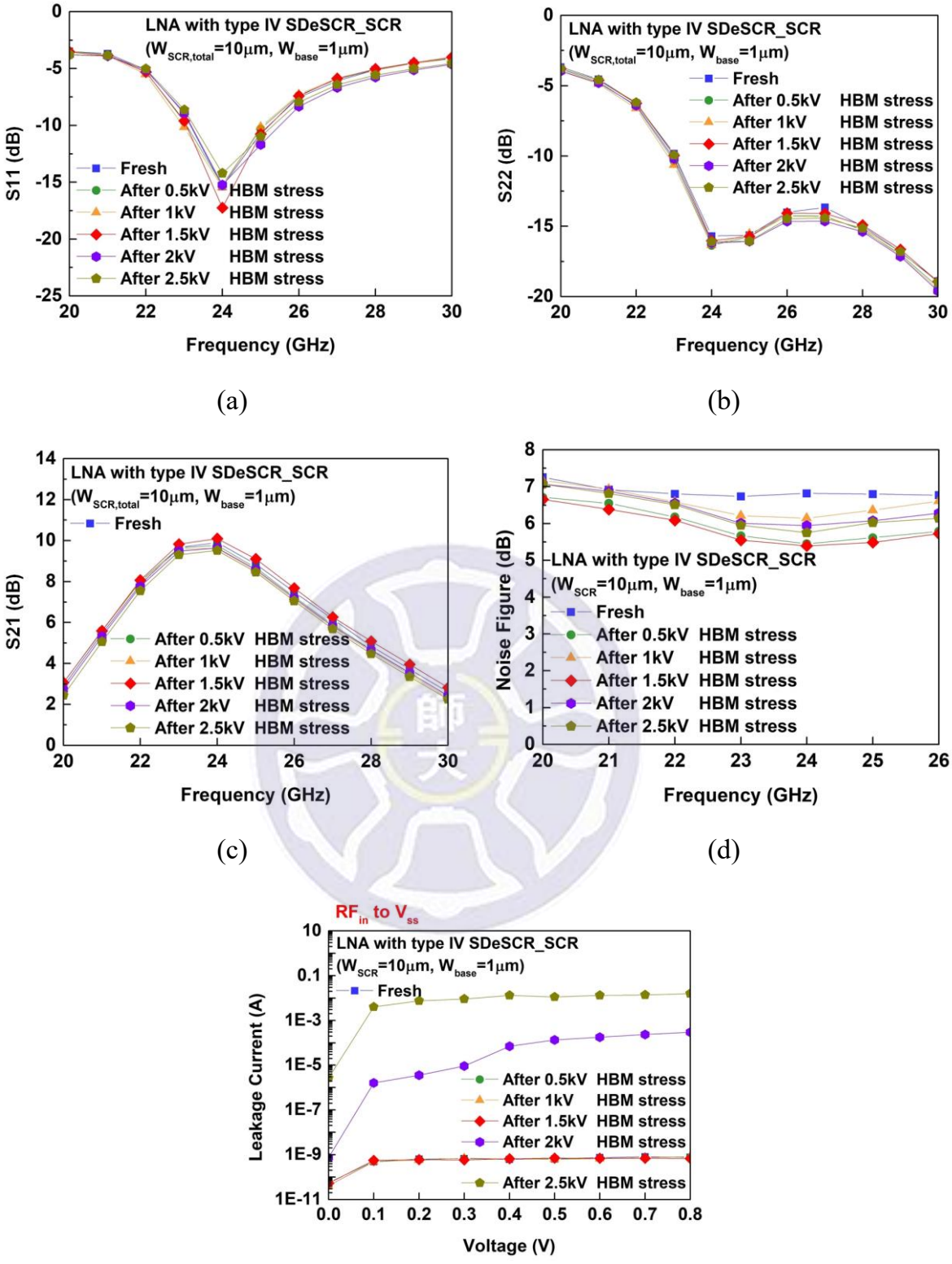


Fig. 3.40. Measured (a) S11, (b) S22, (c) S21, (d) noise figure, and (e) leak current, of LNA with type IV SDeSCR_SCR after HBM stress.

Table 3.2

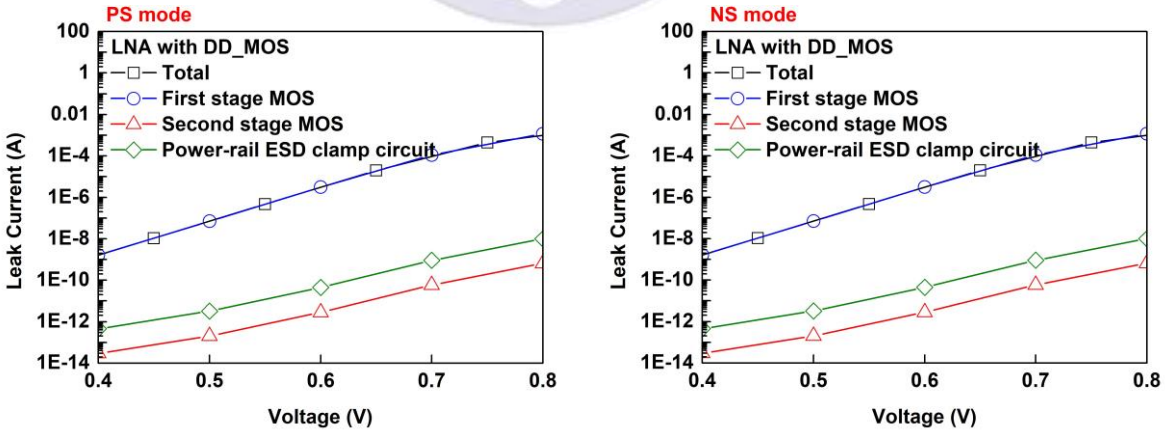
Performance summary.

Cell name	Frequency	Process	V_{DD} (V)	Gain (dB)	Noise figure (dB)	ESD protection area (μm^2)	HBM level (kV)
LNA without ESD protection	24-GHz	0.18-μm CMOS	1.2	9.9	6	N/A	< 0.5
LNA with DD_MOS					5.8	15995	1.5
LNA with DSD_MOS					5.8	16427	2
LNA with DD_SCR					5.9	4342	2
LNA with type III SDeSCR_SCR					6.8	4020	1.5
LNA with type IV SDeSCR_SCR					6.8	4060	1.5
Reference [38]		0.13-μm RF CMOS		10	6.8	16800	2
Reference [39]				36	6.9	unknown	2

3.3 Discussion and Summary

3.3.1 Debug

This section will discuss why the leakage current of the LNA with DD_MOS has increased significantly at PS mode and NS mode. According to the TLP measurement results in Section 3.2.1, the leakage current of the LNA with DD_MOS is larger than those with DSD_MOS and DSD_SCR at PS mode and NS mode. The leakage current of LNA with DD_MOS and DSD_MOS are simulated in normal operation, as shown in Fig. 3.41. At PS mode, the anode and cathode are connected to RF_{in} and V_{SS}, respectively, and the RF_{in} is given 0.8 V. At NS mode, the anode and cathode are connected to V_{SS} and RF_{in}, respectively, and the V_{SS} is given -0.8 V. At PS mode and NS mode, the LNA with DD_MOS has a larger leakage current because the first stage MOS (M_{n1}) is turned on. In addition, the leakage current at PDS mode does not increase significantly because first stage MOS and second stage MOS are not turned on in normal operation. Therefore, LNA with DD_MOS has no problem of the leakage current in normal operation.



(a) (b)

Fig. 3.41. Simulated leak current of LNA with DD_MOS at (a) PS mode and (b) NS mode.

3.3.2 Summary

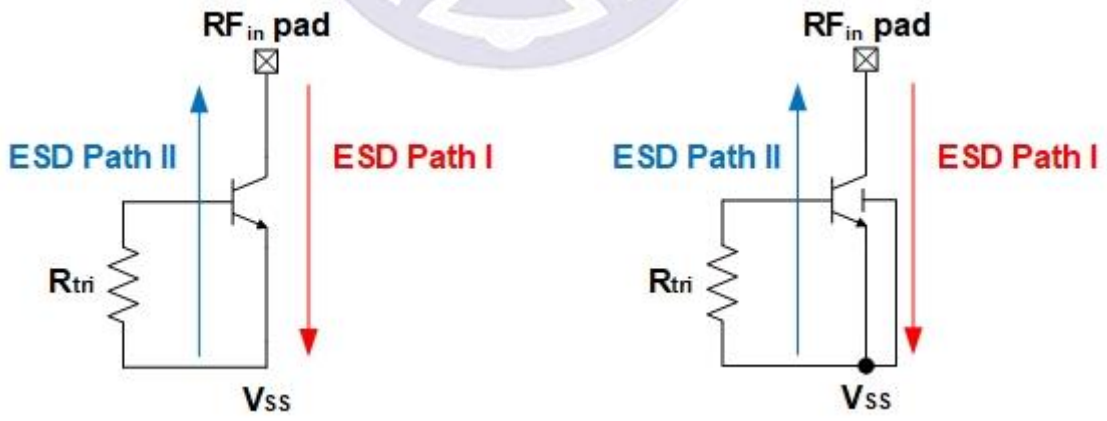
The 24-GHz LNA uses two-stage and common source topology, and the LNAs with ESD devices have been fabricated in 0.18-μm CMOS technology. The HBM robustness and the leakage current of the LNA without and with ESD protection are measured. The LNA without ESD protection circuit cannot bear 0.5 kV or even lower of HBM stresses, and the leakage current increases rapidly after 0.5 kV HBM stresses. Although attaching DD_MOS and DSD_MOS to the LNA can improve HBM robustness, traditional devices have the disadvantages of large layout area and large parasitic capacitance. Therefore, the proposed SDeSCR_SCRs mend these disadvantages. The SDeSCR_SCRs that have a small layout area are attached to the LNA. Although the LNA with type III and type IV SDeSCR_SCRs have a lower HBM ESD level than LNA with DSD_MOS and DSD_SCR, the proposed designs can provide 1.5 kV HBM ESD level. The layout area of the LNA with type III and type IV SDeSCR_SCRs are less than LNA with DSD_SCR or even a quarter of the LNA with DD_MOS and DSD_MOS.

Chapter 4

Investigation of Vertical NPN Devices for Gigahertz Low-Noise Amplifier in BiCMOS Technology

4.1 Structure of Vertical NPN Devices

The model of the VNPN device is provided by foundry, which can be used to simulate the device characteristics. Fig. 4.1(a) and (b) show the VNPN devices without ground ring and with ground ring [40], respectively. In VNPN devices, the ESD currents flow from RF_{in} pad to V_{SS} through the two paths to protect internal circuits during ESD events: through ESD path I if the ESD is positive at RF_{in} pad, and through ESD path II if it is negative at RF_{in} pad.



(a) (b)

Fig. 4.1. The VNPN devices (a) without ground ring and (b) with ground ring.

The structure top view of the VNPN device is shown in Fig. 4.2. Along X-X', it includes P-substrate, N^+ buried layer (NBL), N^+-EPI (NEPI), deep trench isolation (DTI), P^+, and N^+. The cross-sectional view of the VNPN device without ground ring is shown in Fig. 4.3(a). The ESD path I (N^+/NBL/NEPI/P^+/N^+) from RF_{in} pad to V_{SS} discharges the ESD current during positive ESD event at RF_{in} pad, and the ESD path II (N^+/P^+/NBL/NEPI/N^+) from V_{SS} to RF_{in} pad discharges the ESD current during negative ESD event at RF_{in} pad. The other design is the VNPN device with ground ring, and the cross-sectional view of the VNPN device with ground ring is shown in Fig. 4.3(b). The ESD path I (N^+/NBL/NEPI/P^+/N^+) from RF_{in} pad to V_{SS} discharges the ESD current during positive ESD event at RF_{in} pad, and the ESD path II (P^+/P-substrate/NBL/NEPI/N^+) from V_{SS} to RF_{in} pad discharges the ESD current during negative ESD event at RF_{in} pad. In VNPN device with ground ring, the substrate and emitter are shorted, and the substrate to collector forms p-n junction just like a diode. The trigger voltage of the VNPN device with ground ring is low and quickly turn-on during positive ESD event at RF_{in} pad. However, the VNPN device without ground ring increases trigger voltage causing the VNPN device cannot quickly turn-on to protect internal circuit during negative ESD event at RF_{in} pad.

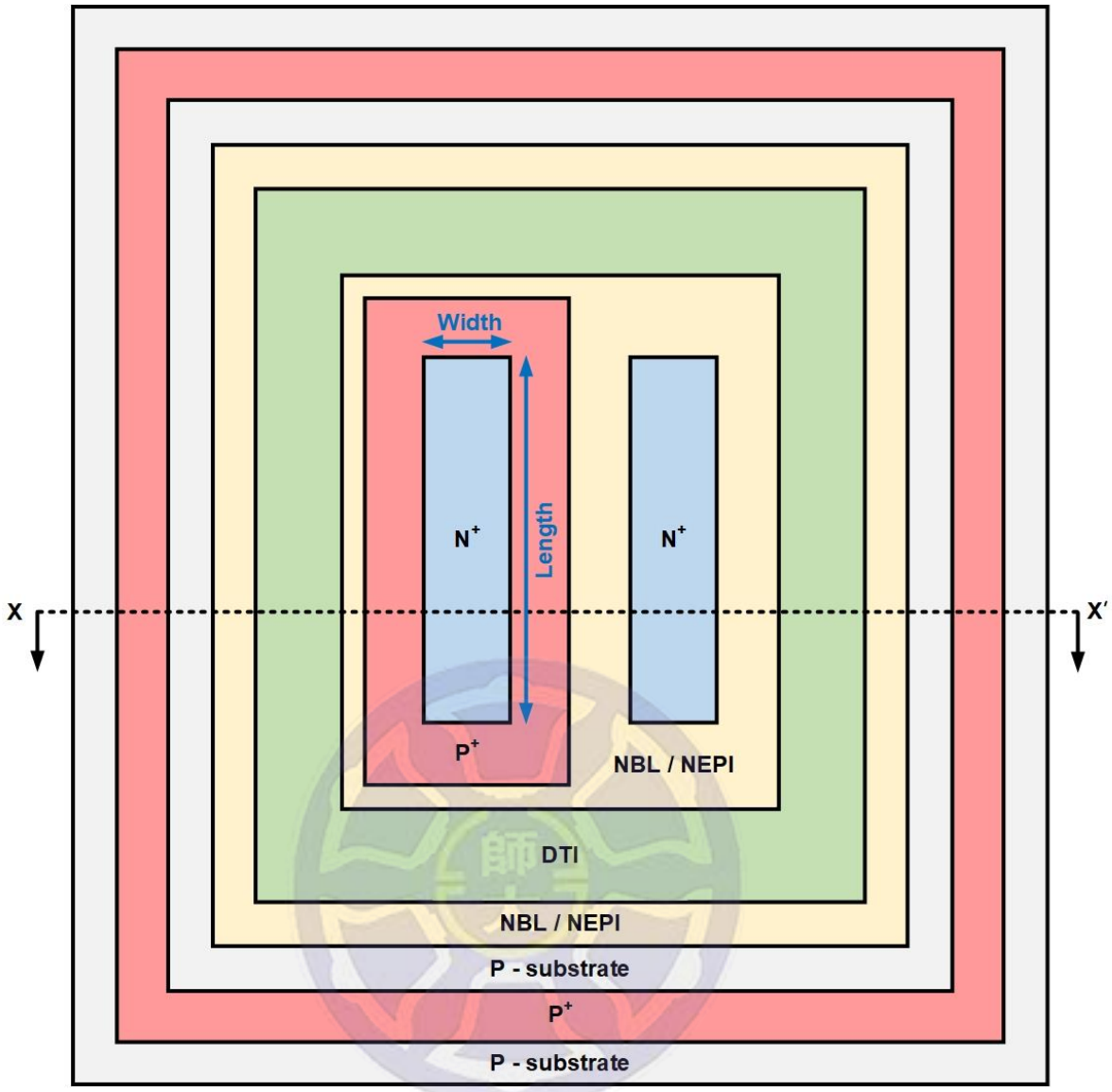
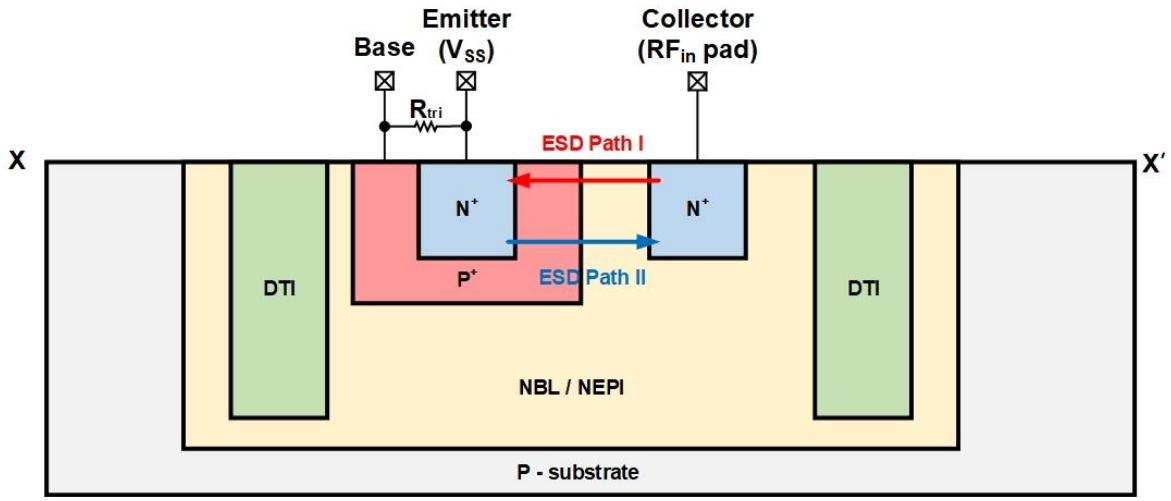
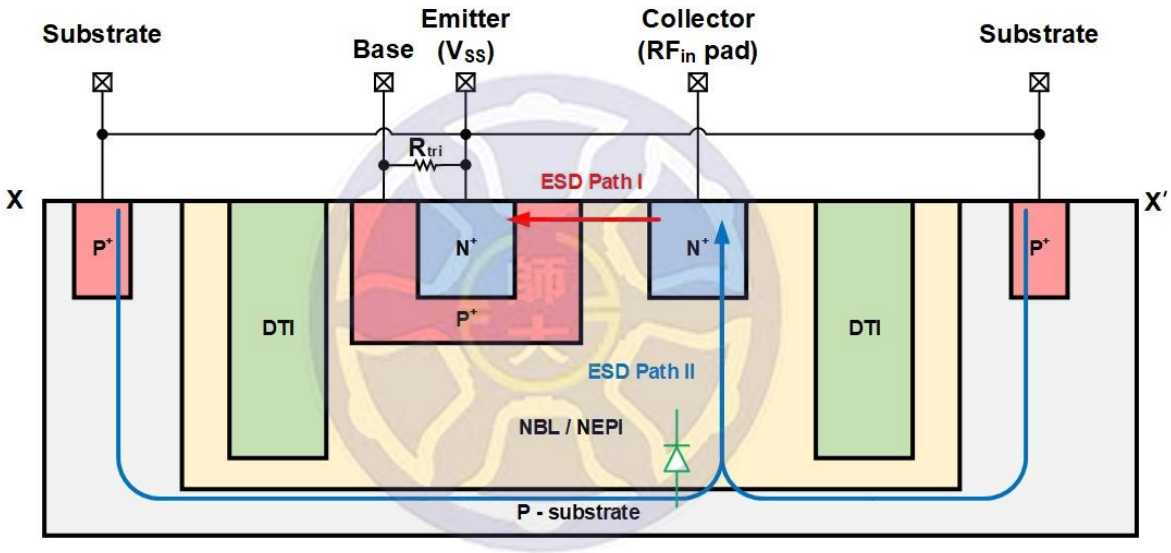


Fig. 4.2. The structure top view of VNPN device.



(a)

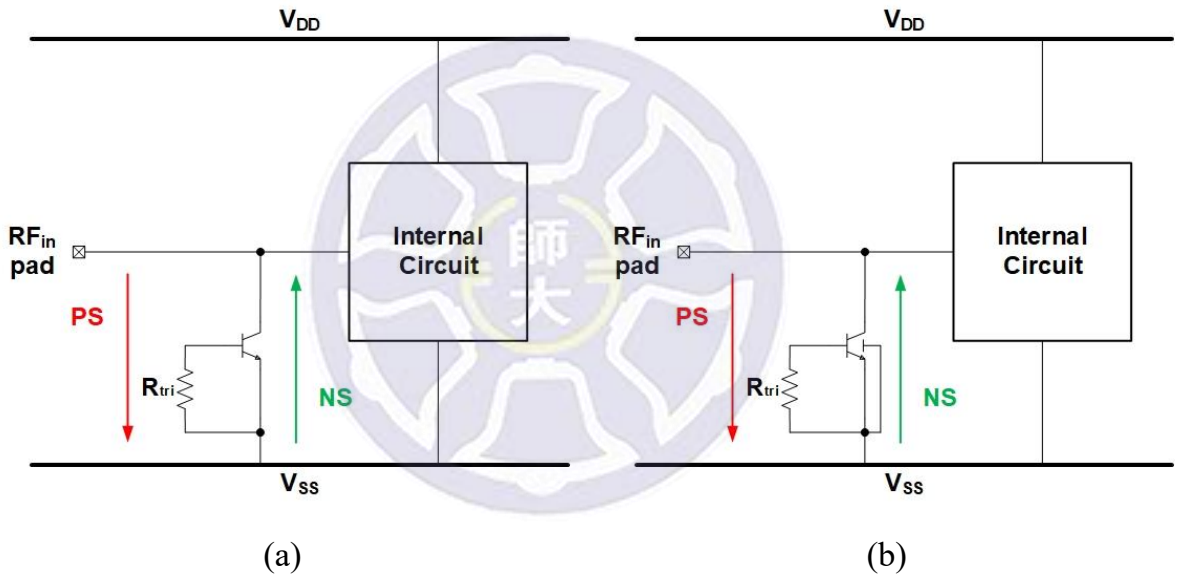


(b)

Fig. 4.3. The cross-sectional view of VNPN devices (a) without ground ring and (b) with ground ring.

After the structure of the VNPN device is explained, the VNPN devices connect to the input of the internal circuit, as shown in Fig. 4.4. Most of the devices are unidirectional path, like diode. The proposed VNPN devices have bidirectional ESD paths. The ESD devices as much as possible reduce the layout area and parasitic effects. The TLP characteristic, HBM robustness, parasitic capacitance, and layout area of the

VNPN devices are compared in Section 4.2.3 and 4.2.4. The layout top view of the VNPN devices without ground ring and with ground ring is shown in Fig. 4.5 and Fig. 4.6, respectively. The layout area of the VNPN devices without ground ring is 2.697 μm^2, 5.487 μm^2, and 9.372 μm^2. The layout area of the VNPN devices with ground ring is 2.343 μm^2, 4.686 μm^2, and 11.069 μm^2. The metal lines are stacked, and the total width of metal lines is more than 10 μm. This consideration is to ensure that the metal lines do not be burned before ESD device during ESD events. Therefore, the metal width as much as possible increases to avoid the above problems.



(a) (b)

Fig. 4.4. Attaching the VNPN devices (a) without ground ring and (b) with ground ring to input of internal circuit to input of internal circuit.

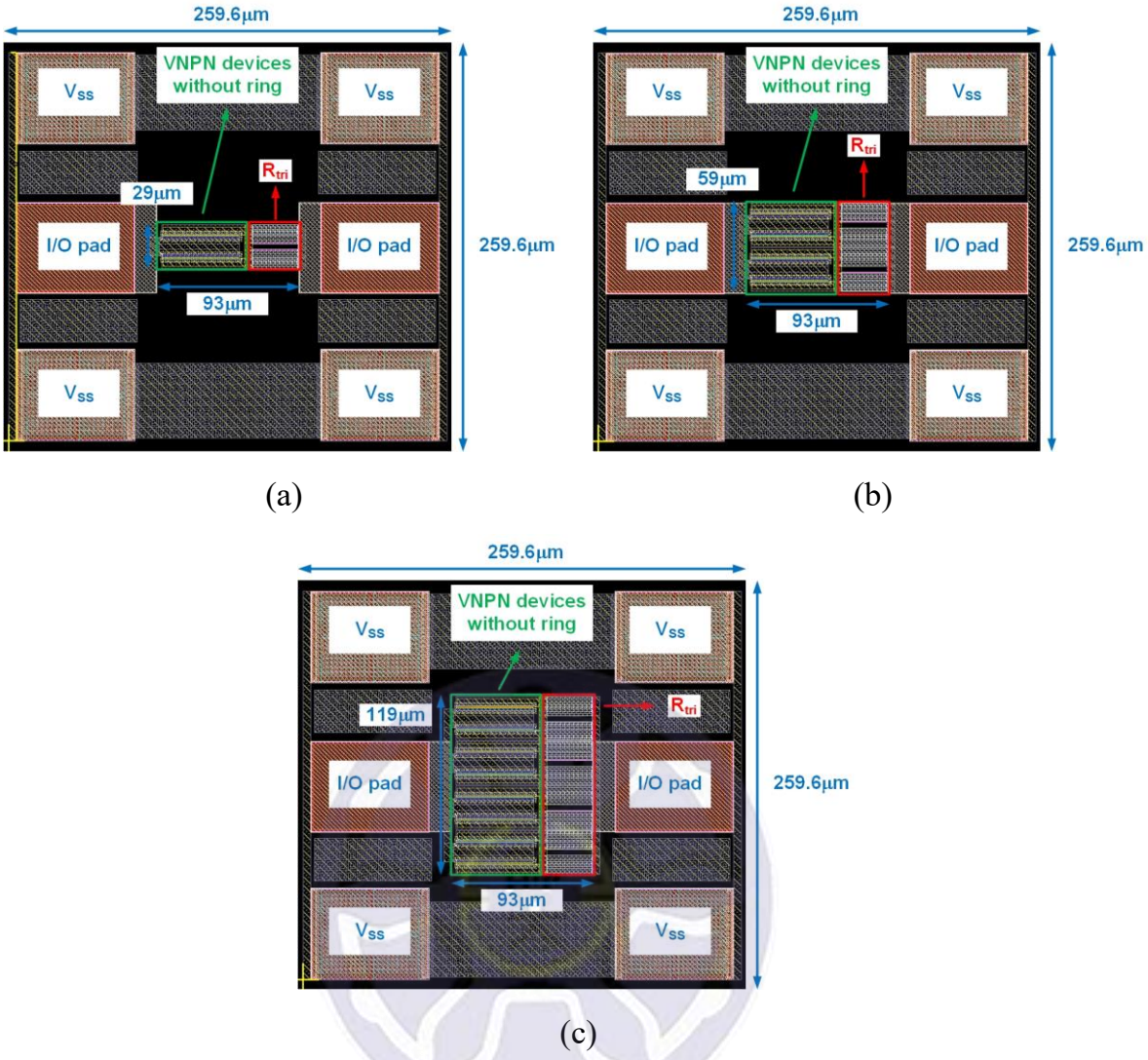


Fig. 4.5. The layout top view of VNPN devices without ground ring which length are (a) 100 µm, (b) 200 µm, and (c) 400 µm.

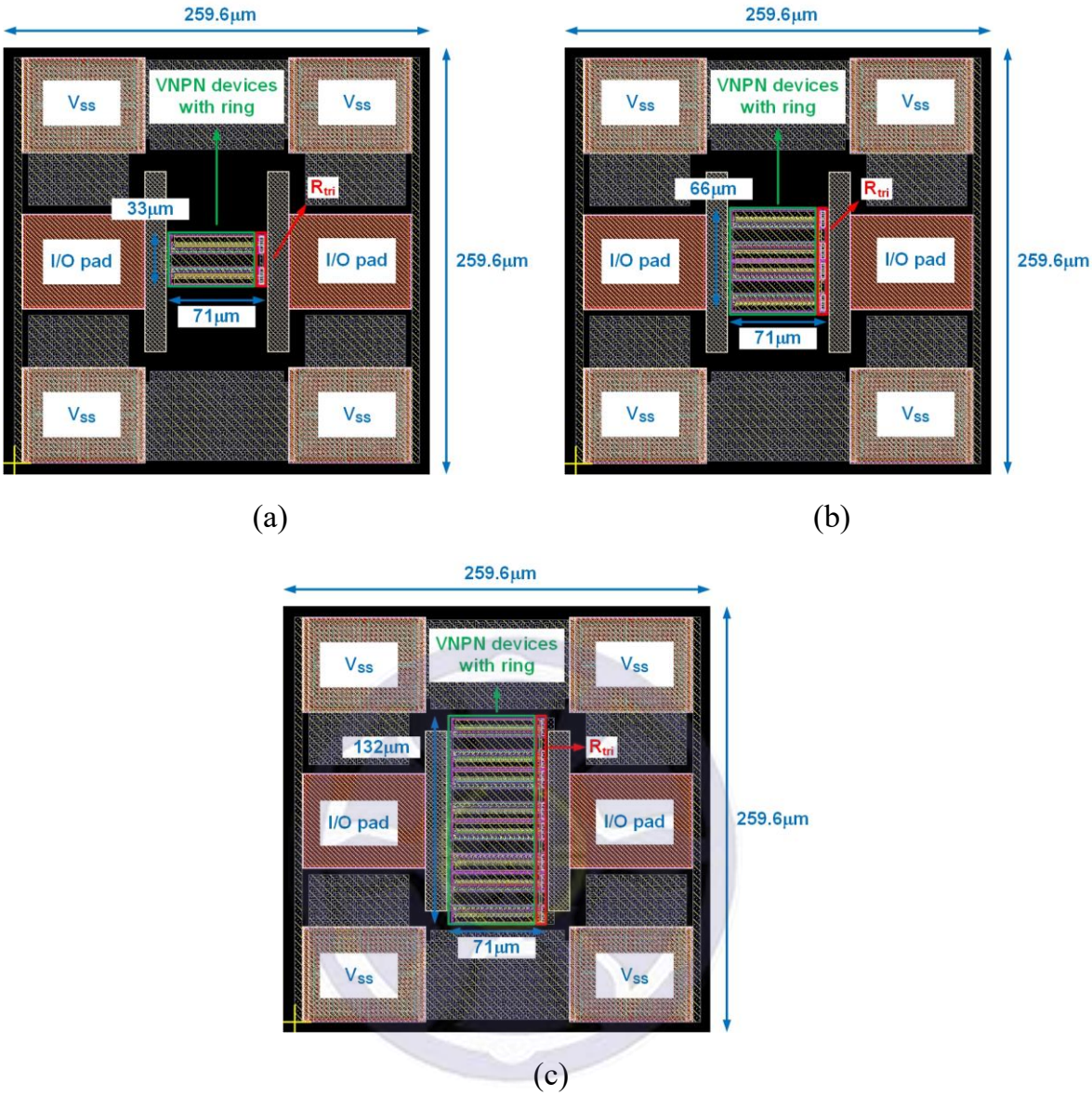


Fig. 4.6. The layout top view of VNPN devices with ground ring which length are (a) 100 µm, (b) 200 µm, and (c) 400 µm.

4.2 Verification of Vertical NPN Devices

4.2.1 Parameters of VNPN Devices

The VNPN devices without ground ring and with ground ring have been fabricated in BiCMOS technology. Table 4.1 shows the different sizes of the VNPN devices, in which all the widths of test devices are 0.2 μm and the lengths include 100 μm, 200 μm, and 400μm. The resistance values of the R_{tri} in VNPN devices without ground ring and with ground ring include 50 kΩ and 5 kΩ.

Table 4.1

Different sizes of test devices.

VNPN devices	without ground ring	with ground ring
R_{tri} (kΩ)	50	5
Width (μm)	0.2	
Length (μm)	100 / 200 / 400	

4.2.2 The Equipment of ESD Test and High-Frequency Measurement

The test environment has been introduced in Section 2.4.2. In high-frequency measurement, all the ground pads are connected together, and the VNPN devices are connected between two signal pads. To measure s-parameters, the anode gives bias voltage to the signal pad of the RF_{in}, and the cathode is connected to ground, as shown in Fig. 4.7. The picture under the microscope of the VNPN devices is shown in Fig. 4.8.

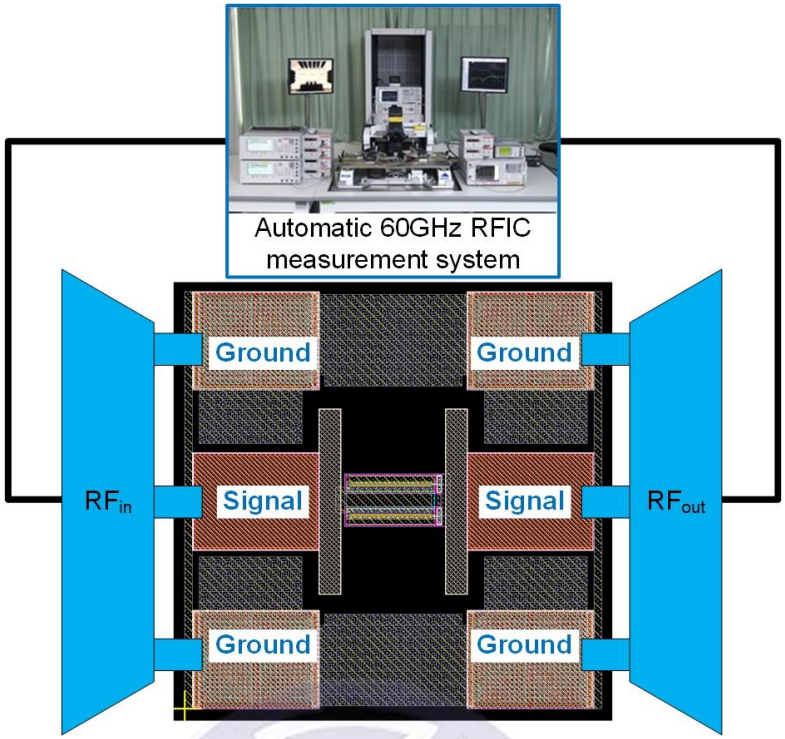


Fig. 4.7. The diagram of VNPN devices in high-frequency measurement.

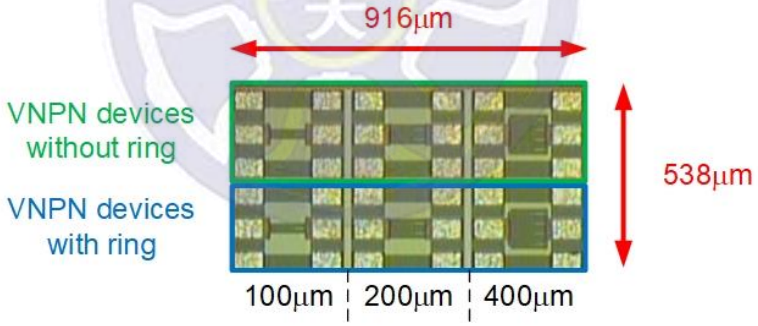
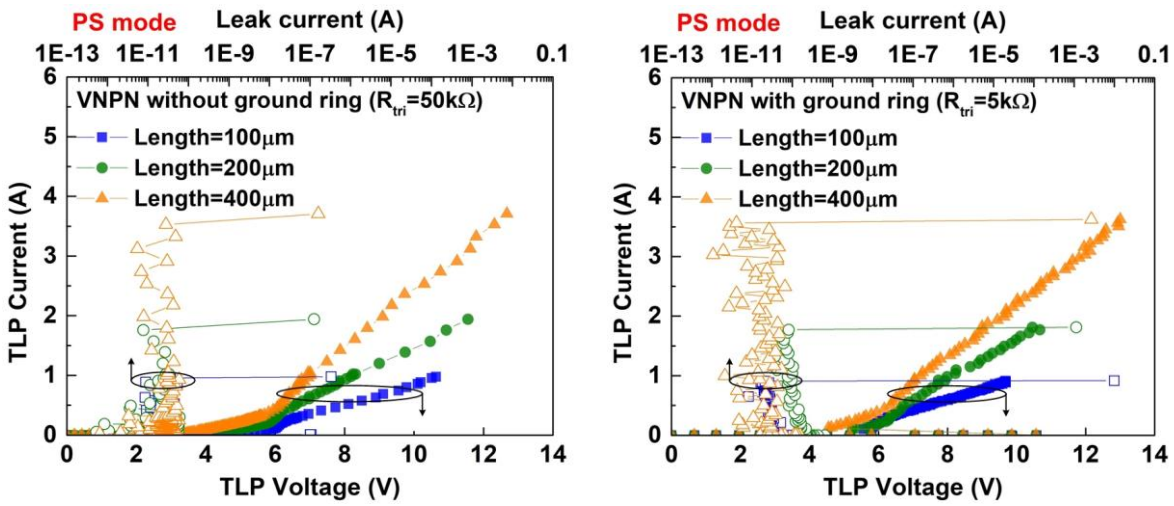


Fig. 4.8. The picture under the microscope of VNPN devices.

4.2.3 TLP I-V Curves

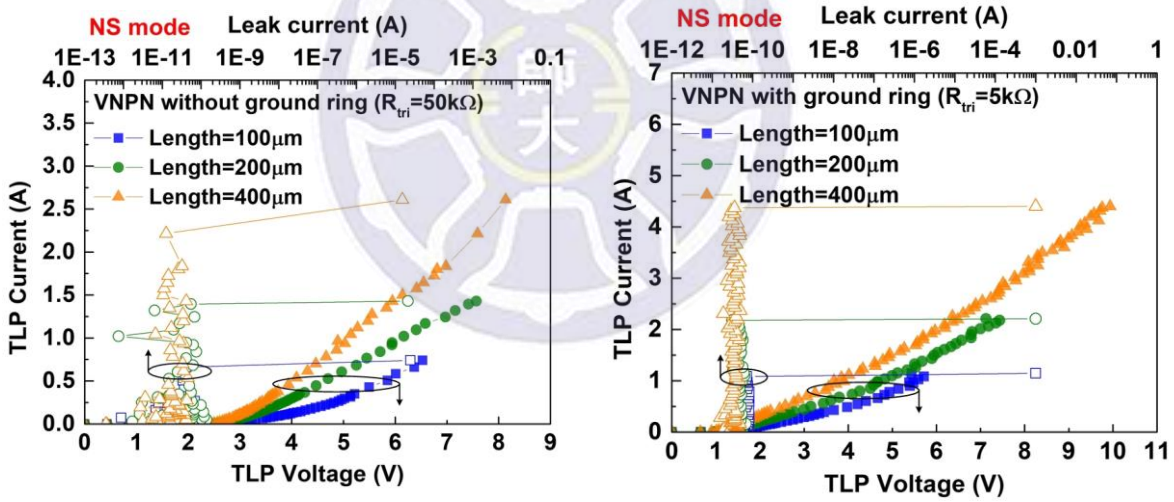
To judge the test device is damaged or not, the way is the same as in Section 2.4.3. The TLP I-V curves of the VNPN devices during positive stresses at RF_{in} pad are shown in Fig. 4.9(a) and 4.9(b). The measurement results show that the VNPN devices with ground ring have higher trigger voltage than VNPN devices without ground ring. Owing to the R_{tri} of the VNPN devices is a key, the R_{tri} relates to the trigger voltage of the VNPN devices. In the VNPN device, the resistance from base to emitter (R_{BE}) is smaller than the resistance from collector to base (R_{CB}), the resulting V_{BE} is relatively small. The small R_{tri} is not enough to trigger the base to emitter (N^+-P^+) junction of the VNPN devices. It is noteworthy that Fig. 4.9(b) has the phenomenon of snapback. V_{BE} is enough large to trigger the VNPN devices, the channel from collect to emitter is turned on, and its can bear larger current.

The other hand, the TLP I-V curves of the VNPN devices during negative stresses at RF_{in} pad are shown Fig. 4.10(a) and 4.10(b). The VNPN devices with ground ring have a lower trigger voltage than that without ground ring because the ground ring is added. The ground ring is connected to the emitter of the VNPN devices. The ESD currents flow from substrate to collector, and the p-n junction turn-on about 1 V. Due to the DTI is deeper than shallow trench isolation (STI), the path from substrate to collector is longer. Both the second breakdown current (I_{t2}) of the VNPN devices increases as size increases during positive and negative stresses at RF_{in} pad. The measurement results of the TLP characteristics and HBM robustness are summarized in Table 4.2.



(a) (b)

Fig. 4.9. VNPN devices (a) without ground ring (R_{tri}=50 kΩ) and (b) with ground ring (R_{tri}=5 kΩ), during positive stresses at RF pad.



(a) (b)

Fig. 4.10. VNPN devices (a) without ground ring (R_{tri}=50 kΩ) and (b) with ground ring (R_{tri}=5 kΩ), during negative stresses at RF pad.

Table 4.2

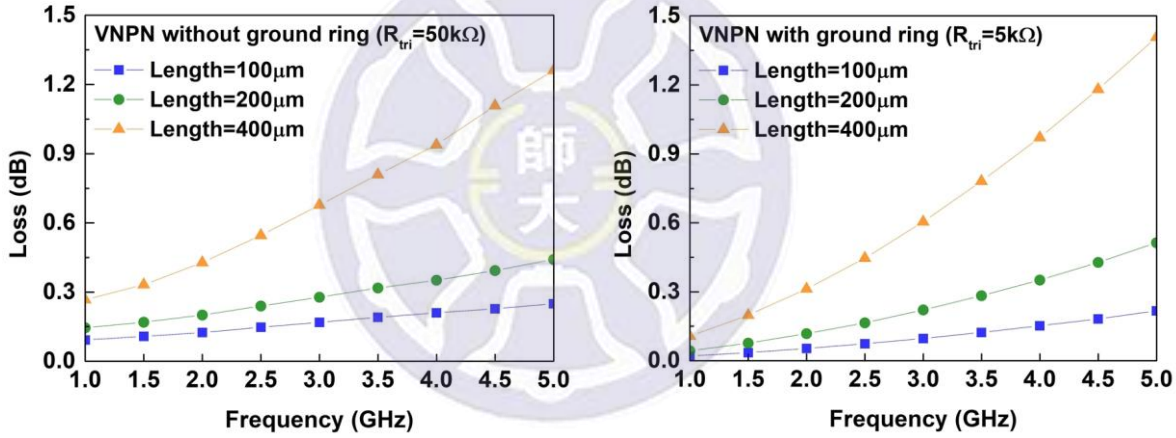
Measured TLP characteristic and HBM robustness of test devices.

VNPN devices		without ground ring			with ground ring		
Width (μm)		0.2					
R_{tri} (kΩ)		50			5		
Length (μm)		100	200	400	100	200	400
Layout area (μm^2)		2697	5487	9372	2343	4686	11069
Positive stresses at RF_{in} pad	V_{t1} (V)	6.8	5.8	6.0	10.3	10.3	10.3
	V_h (V)	6.8	5.8	6.0	5.4	5.1	4.4
	I_{t2} (A)	1.0	1.8	3.5	0.9	1.8	3.6
	R_{on} (Ω)	4.2	3.0	1.9	4.2	2.9	1.8
	HBM level (kV)	1.5	3	5.5	1.5	2.5	5.5
Negative stresses at RF_{in} pad	V_{t1} (V)	2.8	2.6	2.5	1.1	1.0	0.9
	V_h (V)	2.8	2.6	2.5	1.1	1.0	0.9
	I_{t2} (A)	0.7	1.4	2.4	1.1	2.2	4.4
	R_{on} (Ω)	2.3	2.1	2.3	1.1	1.8	3.4
	HBM level (kV)	0.5	1.5	3	1	2	4.5

4.2.4 The High-Frequency Characteristics

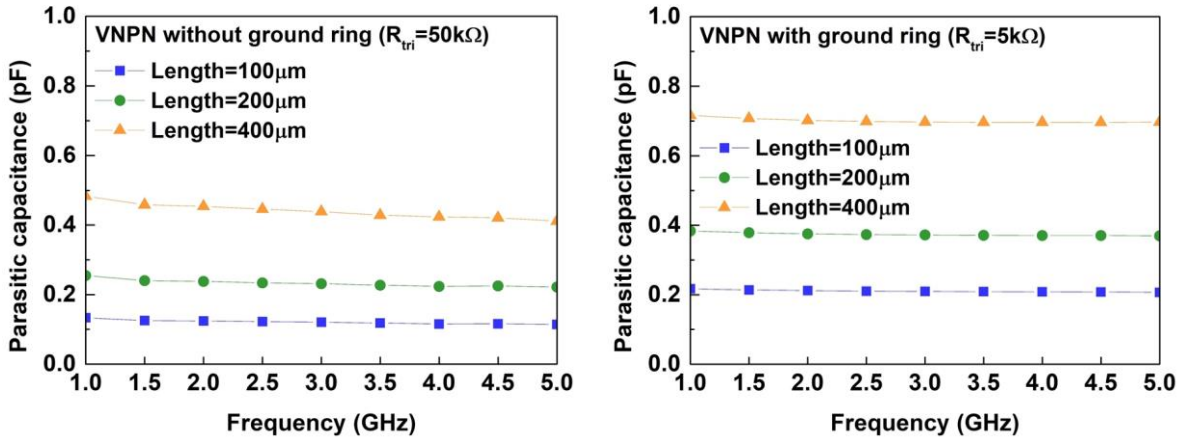
Using the RFIC measurement system measures the s-parameter of the VNPN devices, as shown in Fig. 4.11. From the measurement results, it can be observed that the larger size VNPN devices have larger loss, and loss increases as size of VNPN devices increases. The loss of the VNPN devices at 2.4-GHz is 0.14 dB, 0.23 dB, and 0.52 dB in lengths 100 μm, 200 μm, and 400 μm, respectively. The loss of the VNPN devices at 2.4-GHz is 0.07 dB, 0.16 dB, and 0.42 dB in lengths 100 μm, 200 μm, and

400 μm, respectively. Besides, the characteristics of the RF circuits will be more affected when the parasitic capacitance of the ESD device is relatively large. As shown in Fig. 4.12, the parasitic capacitance of the VNPN devices at 2.4-GHz is 0.21 pF, 0.37 pF, and 0.7 pF in lengths 100 μm, 200 μm, and 400 μm, respectively. The parasitic capacitance of the VNPN devices at 2.4-GHz is 0.12 pF, 0.23 pF, and 0.45 pF in lengths 100 μm, 200 μm, and 400 μm, respectively. The parasitic capacitance of the VNPN devices with ground ring way is larger than VNPN devices without ground ring way because ground ring is inserted. Measured loss and parasitic capacitance of the VNPN devices are summarized in Table 4.3.



(a) (b)

Fig. 4.11. Measured loss of VNPN devices (a) without ground ring (R_{tri}=50 kΩ) and (b) with ground ring (R_{tri}=5 kΩ).



(a) (b)

Fig. 4.12. Measured parasitic capacitance of VNPN devices (a) without ground ring (R_{tri}=50 kΩ) and (b) with ground ring (R_{tri}=5 kΩ).

Table 4.3

Measured loss and parasitic capacitance of VNPN devices.

VNPN devices	without ground ring			with ground ring		
Width (μm)	0.2					
R_{tri} (kΩ)	50			5		
Length (μm)	100	200	400	100	200	400
Loss (dB) at 2.4-GHz	0.14	0.23	0.52	0.07	0.16	0.42
Parasitic capacitance (pF) at 2.4-GHz	0.21	0.37	0.70	0.12	0.23	0.45

4.2.5 Comparison

The VNPN devices with two different approaches are designed in 0.18-μm SiGe BiCMOS technology. Proposed VNPN device with ground ring is added P^+-substrate, which has lower trigger voltage. The VNPN devices without and with ground ring have almost HBM robustness, during positive HBM stresses. On the contrary, the VNPN

device with ground ring has better HBM robustness than VNPN device without ground ring, during negative HBM stresses. Table 4.5 shows the VNPN devices are compared with other ESD devices.

Table 4.4

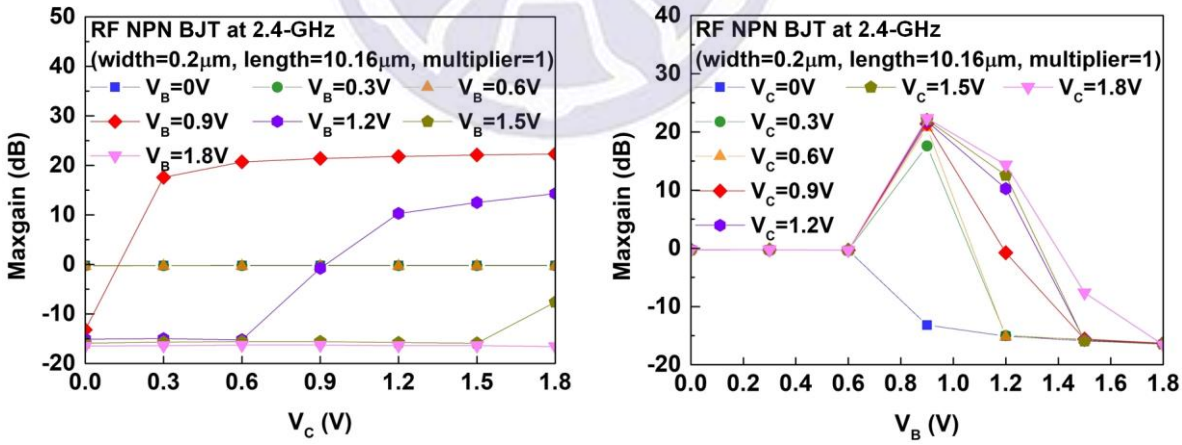
Comparison the VNPN devices with references.

ESD devices		Process	Layout area (μm^2)	Parasitic capacitance (pF)	Positive HBM level (kV)
VNPN without ground ring (R_{tri}=50 kΩ)		0.18-μm SiGe BiCMOS	2697	0.21 @2.4-GHz	1.5
			5487	0.37 @2.4-GHz	3
			11067	0.7 @2.4-GHz	5.5
VNPN with ground ring (R_{tri}=5 kΩ)			2343	0.12 @2.4-GHz	1.5
			4686	0.23 @2.4-GHz	2.5
			9372	0.45 @2.4-GHz	5.5
Reference [45]	ggNMOS		1433	0.45 @5.5-GHz	2
	gcNMOS		4160	0.76 @5.5-GHz	2

4.3 Simulated 2.4-GHz Low-Noise Amplifier with VNPN Devices

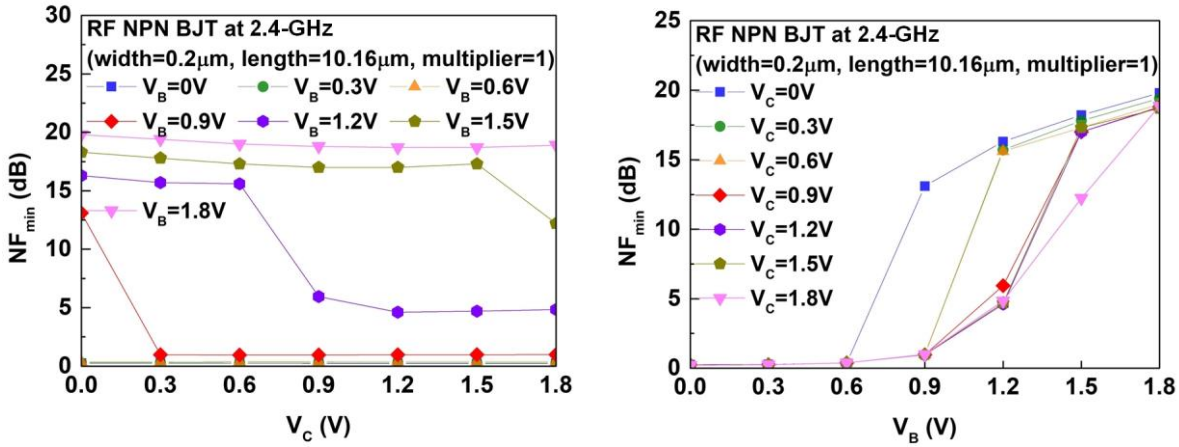
4.3.1 Design Steps of Low-Noise Amplifier at 2.4-GHz

The design steps of the 2.4-GHz LNA are the same as Section 3.1.1. The design targets of the 2.4-GHz LNA are that S11 and S22 are less than -15 dB, S21 is more than 20 dB, and noise figure is less than 5 dB. The V_C and V_B are swept from 0 V to 1.8 V to obtain maximum gain and minimum noise figure of transistor, and the V_C and V_B are selected 1.8 V and 0.9 V, as shown in Fig. 4.13 and Fig. 4.14. Changing the length or multiple of transistor does not influence with max gain and noise figure, as shown in Fig. 4.15 and Fig. 4.16. In the 2.4-GHz LNA design, the V_C and V_B are selected 1.8 V and 0.9 V. The width, length, and multiplier are selected 0.2 μm 4.16 μm, and 1, respectively. Following the above steps, a single transistor can achieve maximum performance, and the matching network design of the LNA will be introduced in next.



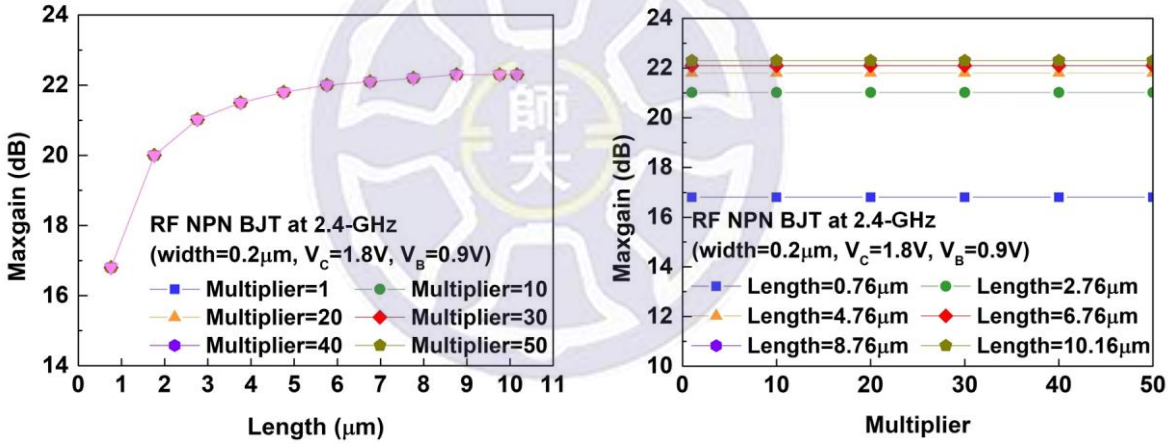
(a) (b)

Fig. 4.13. Simulated Max gain of RF NPN BJT (width=0.2 μm, length=10.16 μm, multiplier=1) with various (a) V_C and (b) V_B at 2.4-GHz.



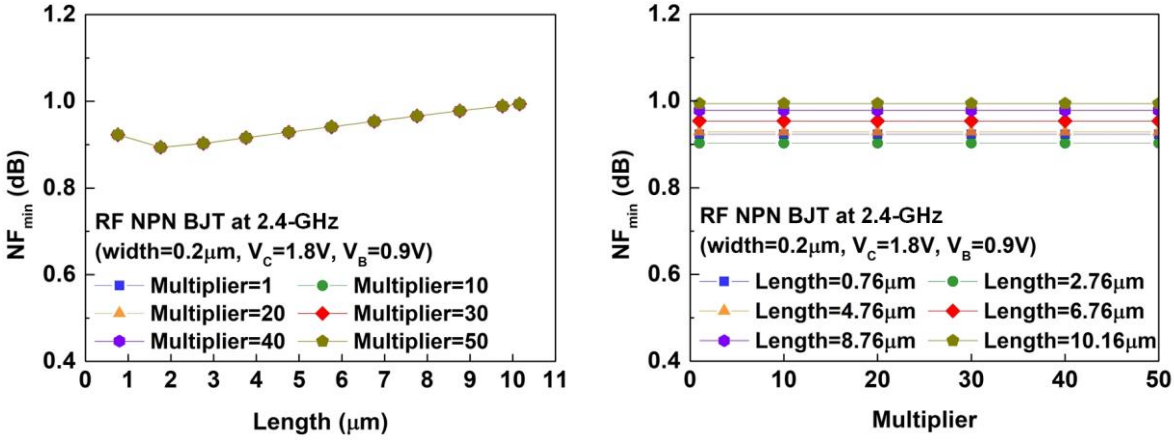
(a) (b)

Fig. 4.14. Simulated NF_{min} of RF NPN BJT (width=0.2 μm, length=10.16 μm, multiplier=1) with various (a) V_C and (b) V_B at 2.4-GHz.



(a) (b)

Fig. 4.15. Simulated Max gain of RF NPN BJT (width=0.2 μm, V_C =1.8 V, V_C =0.9 V) with various (a) length and (b) multiplier at 2.4-GHz.

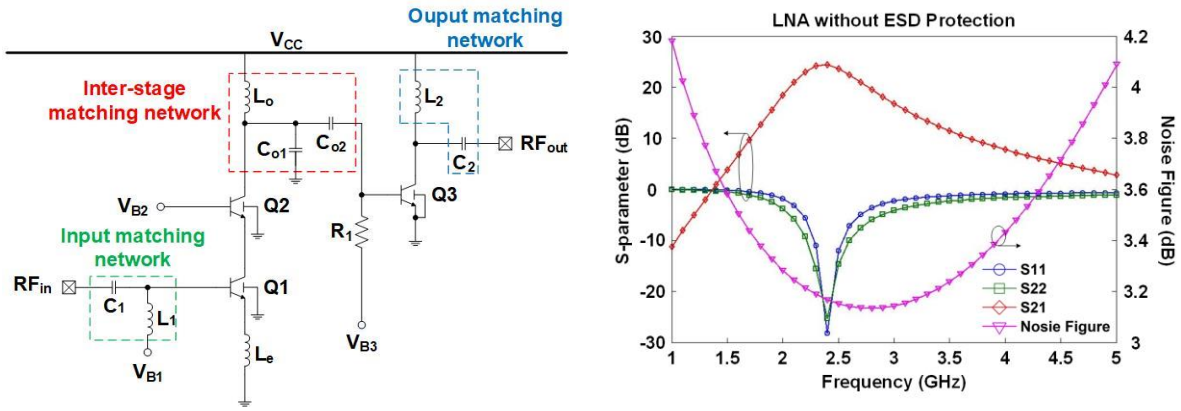


(a) (b)

Fig. 4.16. Simulated NF_{min} of RF NPN BJT (width=0.2 μm, V_C =1.8 V, V_C =0.9 V) with various (a) length and (b) multiplier at 2.4-GHz.

4.3.2 Application of VNPN Devices to 2.4-GHz Low-Noise Amplifier

Fig. 4.17(a) shows the architecture of a 2.4-GHz LNA which use two-stage and cascode topology [41]-[44], and Fig. 4.17(b) shows the simulation results. In Fig. 4.17(a), the input matching network, output matching network, and inter-stage matching network are labeled by the green, blue, and red lines, respectively. The input matching network that is conjugate match is composed of C_1 and L_1, V_{B1} via L_1 that is RF choke give bias to avoid RF signal loss to ground. The bias voltage V_{B1}, V_{B2}, V_{B3}, and V_{CC} are designed 0.9 V, 2.5 V, 0.9 V, and 3.3 V, respectively, and the power dissipation of the LNA is 6.2 mW. Since the input impedance is designed 50 Ω, the emitter of BJT adds an inductor to reduce noise figure degradation, and the value of inductor L_E can adjust the cutoff frequency, which are designed at 5-GHz. In order to allow the previous stage of the signal deliver to the next stage, adding the inter-stage matching network that compose of C_{o1} and C_{o2} is necessary, another component R_1 has the same function as the inductor, which is designed less than 5 kΩ. The output matching network is composed of C_2 and L_2, and the V_{CC} via L_2 that is RF choke give bias to avoid RF signal loss.



(a) (b)

Fig. 4.17. The (a) architecture and (b) simulation result of 2.4-GHz LNA.

The new design parameter of the VNPN devices are shown in Table 4.5, and the test circuits of the LNA without and with ESD protection circuits have been simulated in the same BiCMOS process. The VNPN device with ground ring is used as the ESD protection, which is connected to the RF_{in} pad of the 2.4-GHz LNA, as shown in Fig. 4.18. According to the measurement results in Section 4.2.3, using dozens of kΩ as the R_{tri} may be enough to trigger VNPN devices. Therefore, the resistance value of the R_{tri} is chosen as 50 kΩ, and the length of the VNPN device is increased to obtain better ESD robustness.

Table 4.5

Different sizes of test devices attaching to 2.4-GHz LNA.

VNPN devices	with ground ring
R_{tri} (kΩ)	50
Width (μm)	0.2
Length (μm)	100 / 200 / 400

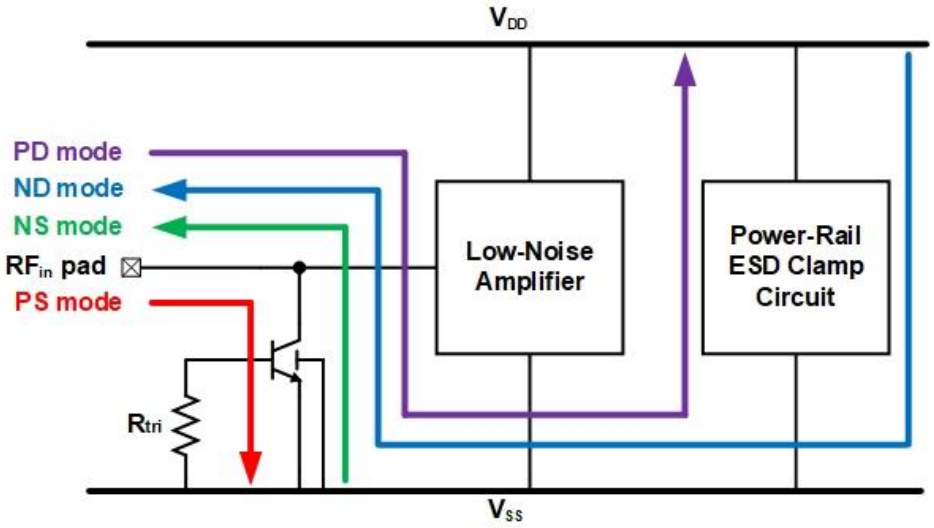
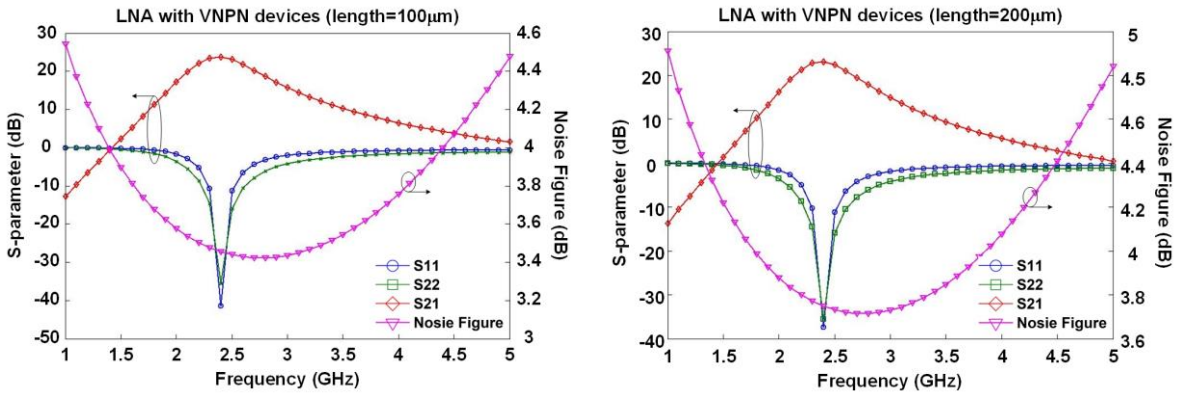
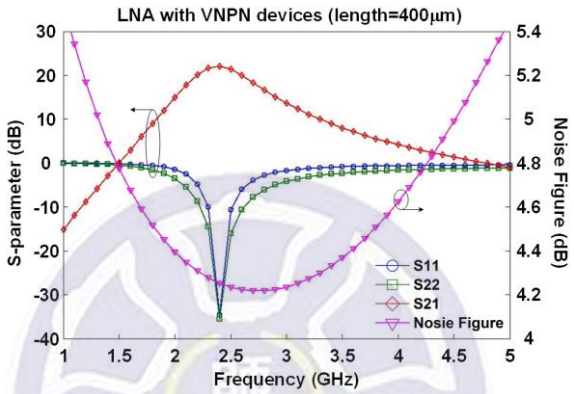


Fig. 4.18. LNA with ESD protection circuits.

After adding the VNPN devices with ground ring, the simulation results show that the RF characteristics of the LNA circuits are not degraded, as shown in Fig. 4.19. Table 4.6 summarizes the simulation results of attaching the different sizes VNPN devices with ground ring to the 2.4-GHz LNA. Both S11 and S22 are less than -15 dB, and the S21 of minimum size and maximum size of the VNPN devices varies about 10.8%. The noise figure increases as size increases from 3.7 dB to 5.0 dB.



(a) (b)



(c)

Fig. 4.19. The simulation result of attaching the length of VNPN devices are (a) 100 μm, (b) 200 μm, and (c) 400 μm, with ground ring (R_{tri}=50 kΩ) to the 2.4-GHz LNA.

Table 4.6

The simulation results of attaching the different sizes of VNPN devices with ground ring to the 2.4-GHz LNA.

		LNA with ESD protection circuit	LNA with different sizes of ESD protection circuit		
VNPN devices with ground ring	R_{tri} (kΩ)	N/A	50		
	Width (μm)	N/A	0.2		
	Length (μm)	N/A	100	200	400
S11 (dB)		-28.2	-37.2	-37.7	-33.2
S22 (dB)		-25.3	-35.5	-35.5	-35.5
S21 (dB)		24.4	23.1	22.1	20.6
Noise Figure (dB)		3.2	3.7	4.3	5.0

4.4 Summary

The VNPN devices with two different approaches are designed in 0.18-μm SiGe BiCMOS technology, and the VNPN devices are applied to the 2.4-GHz LNA. Proposed VNPN devices with ground ring is added P^+-substrate, which has a lower trigger voltage. Besides, using HBM tester tests VNPN devices. The VNPN device without ground ring is weaker than that with ground ring during negative stresses at RF pad. The R_{tri} is related to the trigger voltage of the VNPN devices, and using dozens of kΩ can be reduced from about 10 V to 6 V. In applications, adding the VNPN devices to the input of the LNA does not sacrifice the original characteristics of the LNA.

Chapter 5

Conclusions and Future Works

5.1 Conclusion

In Chapter 2, the traditional ESD devices and SDeSCR devices have been fabricated in 0.18-μm CMOS technology. The ESD devices have DD, DSD, and SDeSCR devices, which collocate the MOS-based power-rail ESD clamp circuit and SCR-based power-rail ESD clamp circuit. The TLP I-V curves, dc I-V curves, HBM robustness, leakage current, loss, and parasitic capacitance of test devices are measured. The SDeSCR_SCRs provide at least 1 kV and 3 kV HBM ESD level when W_{SCR} is 10 μm and 25 μm. Although the SDeSCR_SCRs have almost the same HBM robustness as traditional devices, the layout area of the SDeSCR_SCRs have only a quarter of DD_MOS and DSD_MOS. From the defined FOM values, it can be demonstrated that SDeSCR_SCRs have better performance that traditional devices.

In Chapter 3, the 24-GHz LNA uses two-stage and common source topology, and the LNAs with ESD devices have been fabricated in 0.18-μm CMOS technology. The LNA without ESD protection circuit cannot bear 0.5 kV or even lower of HBM stresses. Although attaching DD_MOS, DSD_MOS, and DSD_SCR to the LNA can improve HBM robustness, the traditional devices have the disadvantages of the large layout area and large parasitic capacitance. The SDeSCR_SCRs that have the small layout area are attached to the LNA. Although the LNA with type III and type IV SDeSCR_SCRs have a lower HBM ESD level than LNA with DSD_MOS and DSD_SCR, the proposed

designs can provide 1.5 kV HBM ESD level. The layout area of the LNA with type III and type IV SDeSCR_SCRs are less than LNA with DSD_SCR or even a quarter of the LNA with DD_MOS and DSD_MOS.

In Chapter 4, proposed VNPN devices without ground ring and with ground ring are designed in 0.18-μm BiCMOS technology. The large size of R_{tri} and ground ring can decrease the trigger voltage of the VNPN devices at PS mode and NS mode. The VNPN device with ground ring has a higher ESD robustness than that without ground ring at unit parasitic capacitance. Changing the values of the R_{tri} from 5 kΩ to 50 kΩ reduces the trigger voltage of the VNPN devices from about 10 V to 6 V. Finally, the VNPN devices are attached to the input of 2.4-GHz LNA to protect the circuit, and the characteristics of the LNA with VNPN devices are simulated. It can be observed from the simulation results and does not sacrifice its original characteristics.

5.2 Future Works

Attaching the VNPN devices to the input terminal of the LNA verifies its characteristics in 0.18-μm SiGe BiCMOS technology. Besides, each bias needs a bypass circuit which is better ac ground for RF circuit. As shown in Fig. 5.1, the bypass circuit design consists of resistors and capacitors, but the layout area is large. In the bypass circuit design, loss must be less than -15 dB, and the impedance needs between 1 Ω and 5 Ω. However, the power-rail ESD clamp circuit which is equivalent a large capacitor provides ESD path from V_{DD} to V_{SS} or V_{SS} to V_{DD}. It is important part of the whole-chip ESD protection design. Combining the functions of the bypass circuit and power-rail ESD clamp circuit propose a new design. The new design is adding an inductor to the

power-rail ESD clamp circuit, the inductor and power-rail ESD clamp circuit resonate below the designed frequency to make loss less than -15 dB, and the impedance is between 1 Ω and 5 Ω. The new power-rail ESD clamp circuit has the ability, which can withstand ESD and be regulated. As a result, each bias add the new power-rail ESD clamp circuit not only has ESD protection ability but also save the layout area.

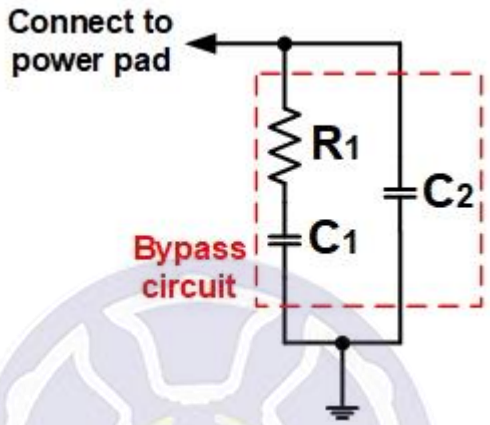


Fig. 5.1. The conventional bypass circuit.

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