國立臺灣師範大學電機工程學系

碩士論文

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應用於寬頻之靜電放電防護設計

ESD Protection Design for Broadband Circuits

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摘　　要

本論文提出了一種應用於寬頻積體電路之全晶片靜電放電防護設計，在0.18μm CMOS 製程下，以矽控整流器元件搭配分散式電路的設計，並與既有二極體元件的設計相比較。

當內部電路的操作頻率上升，寄生電容造成的訊號損耗也益加嚴重，單級的靜電放電防護設計不再適用於高頻電路，為了維持原有的防護效果，本論文提出π型架構的設計，將單級的防護元件以小尺寸分散至兩級，藉由匹配元件的使用，來降低訊號通過時的損耗，傳統的π型架構設計使用的是二極體元件，本論文則是採用矽控整流器元件搭配π型架構，矽控整流器在單位面積下具有高的靜電放電耐受度，藉由二極體串的觸發，導通速度得以提升，並藉由電感的使用來達到良好的寬頻表現，

最後，將傳統二極體設計與本設計應用於 K 波段下的低雜訊放大器，透過電路的量測結果，驗證對電路的影響與實際的防護效果。

關鍵字：寬頻、矽控整流器、匹配元件、低雜訊放大器

ESD Protection Design for Broadband Circuits

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ABSTRACT

This thesis proposed a whole-chip electrostatic discharge (ESD) protection design for broadband circuits. In 0.18μm CMOS process, the silicon-controlled rectifier (SCR) is designed with distributed circuit in comparison with traditional design by diode.

As the operating frequency of IC increases, the signal loss caused by ESD protection device is more severe. The ESD protection design with one stage is no longer suitable for high-frequency applications. π-model structure is proposed to solve this problem. The device is divided into two sections. Two parts are connected with an inductor. By the use of matching element, the signal loss is reduced. Traditional π-model structure is realized with diode. This thesis proposed a π-model design with SCR. SCR has great ESD robustness per unit area. With the trigger diodes, the turn-on efficiency of SCR can be improved. With the help of matching inductor, the broadband performance is maintained. Traditional design and proposed design are realized with K-band low-noise amplifier (LNA) to learn the protective effect.

Keyword ： broadband, silicon-controlled rectifier, matching element, low-noise amplifier

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首先，我要感謝我的爸媽，辛苦地將我一路栽培到大學畢業，也使我在研究所生涯能夠經濟無虞地致力於研究，更是我心靈上最大的支柱。

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Chapter 1

Introduction

1.1 Motivation

Semiconductor industry is one of the important economical sources of our country. However, Electrostatic-discharge (ESD) events may cause great damage to integrated circuits [1]. Gross output value of IC products decreases due to the permanent failures caused by ESD stress. Learning how to design ESD protection circuits is an effective way to enhance the production value of semiconductor industry. With the advance of processing technology, the size of transistor is minimized to increase the operating speed. In addition, the gate oxide of transistor becomes thinner with decreasing size. Thin dielectric layer is more easily punched through by the ESD stress [2]. The robustness of electronic circuits decreases accordingly. However, there are still strict specifications for commercial IC products. The semiconductor industry is faced with more severe challenges about the reliability of integrated circuits. With the development of mobile communication, the radio-frequency integrated circuits (RFICs) are widely used in CMOS process. As the operating frequency of electronic circuits increases, it is more difficult to protect ICs from ESD damage effectively. The parasitic capacitance existing in protection elements causes signal loss on input signal. The radio-frequency signal attenuation occurs when the ESD protection circuits are equipped [3]. In order not to degrade the high-frequency characteristics of internal circuit, the parasitic effect of protection device needs to be considered for different applications.

1.2 ESD Background

ESD is a phenomenon that the charges transfer between different objects forming the discharging path. ESD current is up to several amps (A) and can be generated in nanoseconds (ns). When the large current flows into internal circuit instantly, some parts inside the circuit are unable to operate functionally. Since the semiconductor industry started to develop, ESD problems have existed in electronics circuits. In addition, different kinds of ESD events are found with process evolution. The cost of mask for advanced nanoscale CMOS process is up to hundreds of millions. However, IC products must be equipped with ESD protection circuit to ensure the reliability during operation. Further, the use of ESD protection designs can keep the cost down in the manufacturing process.

1.3 ESD Test Standards

Reliability is an important issue for commercial IC products. The electronic circuits have to pass related tests during manufacturing. Some associations such as US military standard (MIL-STD), Joint Electron Device Engineering Council (JEDEC), and Electrostatic Discharge Association (ESDA) built the standards for ESD tests. Before assembled into the products, the components are required to accept ESD tests. The tests for electronic components is defined as component-level test. Based on the cause of ESD and discharging method, component-level tests are classified as human-body model (HBM), machine model (MM), and charged-device model (CDM). However, the specific HBM level can ensure a minimum MM level. There is a reduction of MM test in recent years. The equivalent circuits and test standards of HBM and CDM are introduced in following part.

(1) Human-Body Model (HBM)

Human body accumulates charges as the feet rub itself on the floor by walking. The IC products are touched by people, and then the discharging path is formed. ESD current flows into IC instantly and causes damage to it. The model of HBM (MIL-STD-883C method 3015.7) is shown in Fig. 1.1. The equivalent capacitance of HBM is 100pF, and the equivalent resistance of that is 1.5kΩ. The human body is charged as a 100pF capacitor and discharges the charges to ground through IC as a 1.5kΩ resistor [4], [5]. The target level of HBM ESD is shown in Table 1.1 [6]. The components of commercial IC products are required to pass 2kV HBM test.

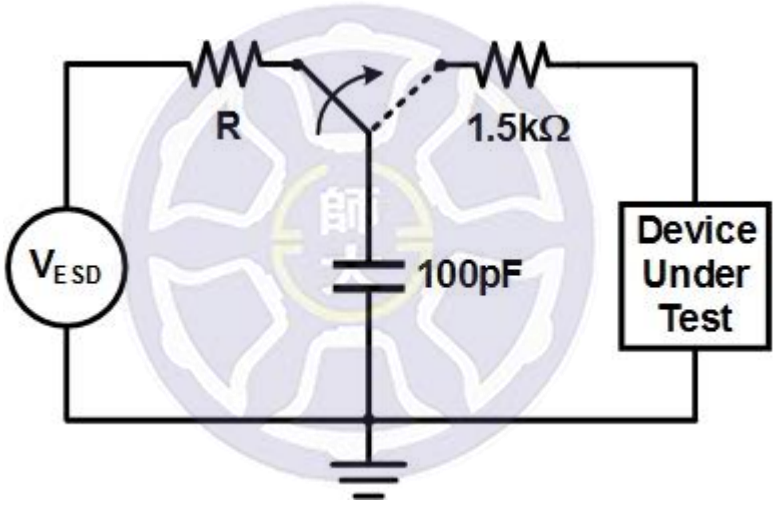


Fig. 1.1. The equivalent circuit of HBM.

Table 1.1. The target level of HBM

HBM Level	Impact on manufacturing environment
100V to <500V	Detailed ESD control method
500V	Basic ESD control methods for safe manufacturing
1kV	
2kV	

(2) Charged-Device Model (CDM)

IC may accumulate charges itself in the manufacturing process. Once the pin of IC comes into contact with ground, the discharging path is formed. The ESD current flowing from charged device leads to internal damage. The model of CDM is shown in Fig. 1.2 [7], [8]. The discharging time of CDM is much shorter than HBM and MM [9]. IC suffers permanent damage more easily. Besides, it is hard to simulate the discharging mechanisms of CDM. As shown in Table 1.2, the components of commercial IC products are required to pass 250V CDM test [10].

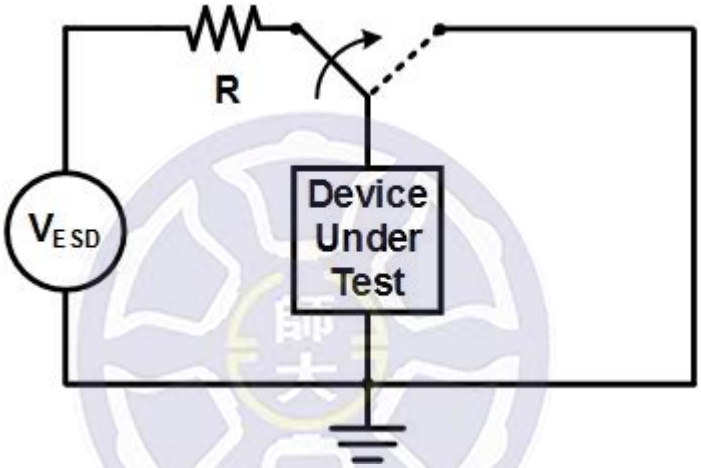


Fig. 1.2. The equivalent circuit of CDM.

Table 1.2. The target level of CDM

CDM Level	ESD Control Requirements
$V_{CDM} \leq 125V$	Basic ESD control methods, Process specific measures, Charging/discharging measurements at each process step.
$125V \leq V_{CDM} \leq 250V$	Basic ESD control methods, Process specific measures.
$V_{CDM} \geq 250V$	Basic ESD control methods,

Different package types of IC and its contact angles lead to different discharging results. In recent years, the package technology is improved. Specific package is designed to be applied in different markets [11]. The impact of package on CDM strongly depends on the package type. Therefore, CDM test is not implemented in this work.

1.4 Design Concepts of ESD Protection

ESD event is inevitable in our daily life and has great impact on electronic circuits. Designs of ESD protection circuits are necessary for IC products to prevent the damage that ESD stress causes. Among all the pins in integrated circuits, the I/O terminal is easily hit by ESD stress from outside. The gate-oxide is generally controlled by the bias applied to input pad [12]. Therefore, ESD protection circuits are usually placed near I/O pad to discharge the ESD current in time before it flows into internal circuit. Besides, the protection circuits are also necessary between the power rails to prevent from ESD damage. The whole-chip ESD protection design is realized with power-rail ESD clamp circuit as shown in Fig. 1.3.

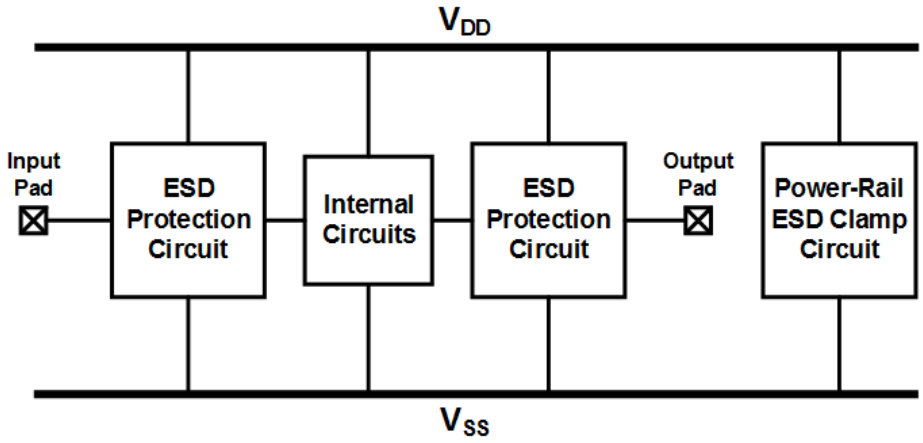


Fig. 1.3. Whole-chip ESD protection design.

ESD design window is defined as a guideline for designing protection circuits. As shown in Fig. 1.4, X-axis shows the measured voltage of device under test, and Y-axis shows the measured current value. Supply voltage (V_{DD}) is the maximum voltage value for the operation of internal circuit. Internal circuit may have permanent failure when the operating voltage is more than breakdown voltage (V_{BD}). Therefore, ESD protection device is designed to operate in the range between V_{DD} and V_{BD}. Generally, the lower limit is $1.1\times V_{DD}$, and the upper limit is $0.9\times V_{BD}$.

There are some properties of ESD protection circuit [13]. Protection device must be kept off to reduce the power consumption when internal circuit operates below V_{DD}. In addition, ESD protection design is not allowed to interfere with internal circuit during normal operation. When ESD stress hits, ESD protection device has to turn on before the breakdown of internal circuit. It means that the trigger voltage (V_{t1}) must be lower than V_{BD}. Some protection devices have snapback phenomenon that the voltage cross the protection device drops a lot during conduction. Therefore, the power consumption can be smaller for lower holding voltage (V_h). However, V_h must be higher than V_{DD} to prevent latch-up effect. The slope of I-V curve is defined as the reciprocal of on-resistance (R_{on}). The protection device turns on with lower R_{on} can discharge ESD current with better voltage clamping ability. When ESD current is higher than the secondary breakdown current (I_{t2}), protection device is damaged permanently. The robustness is proportional to I_{t2}.

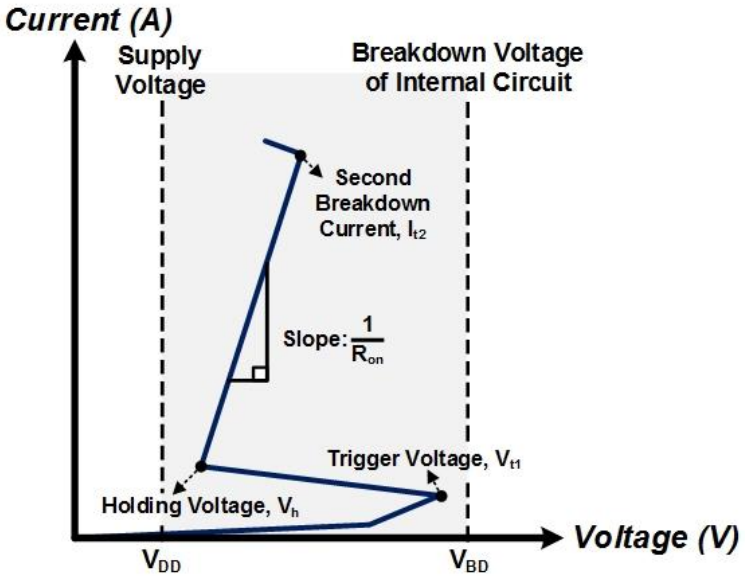


Fig. 1.4. ESD design window.

There are four pin-combinations such as positive I/O-to-V_{SS} (PS mode), positive I/O-to-V_{DD} (PD mode), negative I/O-to-V_{SS} (NS mode), and negative I/O-to-V_{DD} (ND mode). Equipped with power-rail ESD clamp circuit, the discharging path is shown in Fig. 1.6.

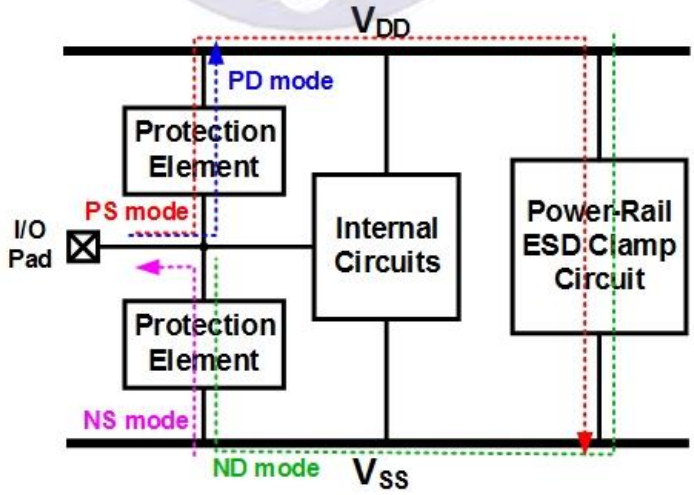


Fig. 1.5. Whole-chip ESD protection design with corresponding path.

1.5 Organization about This Thesis

There are five chapters in this thesis. The motivation of this research is introduced in chapter 1. In addition, the background of the reliability issue is also introduced. In chapter 2, some studies of ESD protection designs for high-frequency applications are presented. In chapter 3, the device which is selected for proposed design and the design flow are noted. The simulation data and measurement results are recorded at the end of this chapter. At last, the proposed ESD protection circuit is verified with low-noise amplifier (LNA). There are the simulation and measurement results in chapter 4. The conclusions and future works are discussed in chapter 5.

Chapter 2

Studies of ESD Protection Designs for High-Frequency Applications

2.1 Consideration of ESD Protection Design at High Frequencies

As the operating frequency increases, ESD protection circuit used for RFIC faces more severe challenges. The parasitic capacitance formed by ESD protection circuit is equivalent to low impedance at high frequencies [14]. The RF signal originally transported to internal circuit flows to ground (V_{SS}) through protection device. As shown in Fig. 2.1, the signal loss caused by protection device has to be considered as ESD protection circuit is applied.

ESD protection circuit must provide ICs with enough robustness against ESD stress. The size of protection device is proportional to ESD level. ESD protection device must be sufficiently large. However, larger device leads to more parasitic capacitance. It is difficult to design the ESD protection circuit for high-frequency applications without distorting input signal [15], [16]. When ESD protection circuit is designed for high-frequency applications, there is a trade-off between ESD robustness and high-frequency performance.

Diode, NMOS, and silicon-controlled rectifier (SCR) are commonly used devices for ESD protection in CMOS process [17]. The I-V curve of diode is plotted in Fig. 2.2. Forward biased diode discharges high current and clamps the voltage at a low level. Diode is suitable for ESD protection due to its characteristics. When diode reversely breaks down, it discharges current as well. However, the power dissipation of reverse-

biased diode is much higher due to high breakdown voltage.

NMOS is also used as an ESD protection device with gate connected to ground. In order to reduce unnecessary power dissipation, the channel of NMOS is kept off with gate connected to ground under normal operation. The I-V curve of NMOS is plotted in Fig. 2.3. When ESD stress hits, the parasitic NPN inside NMOS turns on to discharge ESD current accompanied by the slight snapback phenomenon. The trigger voltage of NMOS is higher than diode because it is conducted after the breakdown of P-N junction.

SCR is a p-n-p-n four-layer device composed of embedded NPN and PNP [18]. The I-V curve of SCR is plotted in Fig. 2.4. It turns on with the leakage current flowing through the resistance between the base and emitter. The positive-feedback mechanism is formed when SCR is conducted. As a result, SCR can discharge high current with strong snapback phenomenon [19].

Structurally, diode and SCR have lower capacitance value than NMOS. Without appropriate design, NMOS is seldom used for high-frequency applications. In next chapter, diode and SCR will be introduced in detail.

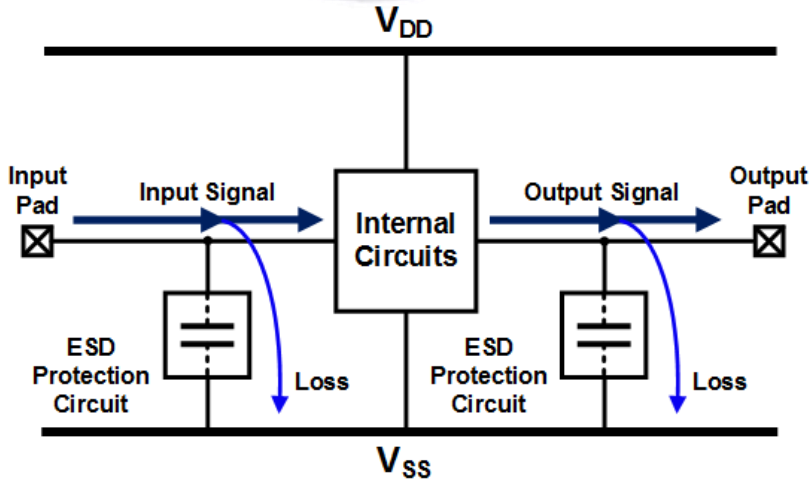


Fig. 2.1. Signal loss at high frequencies.

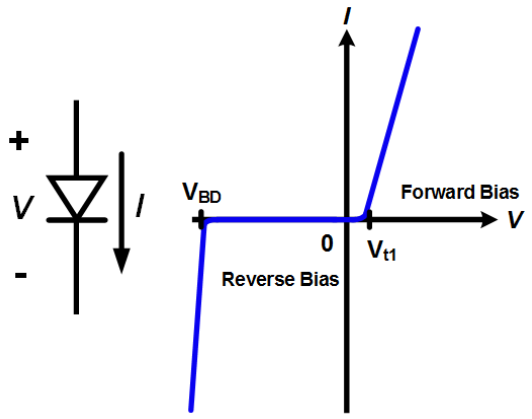


Fig. 2.2. The I-V curve of diode.

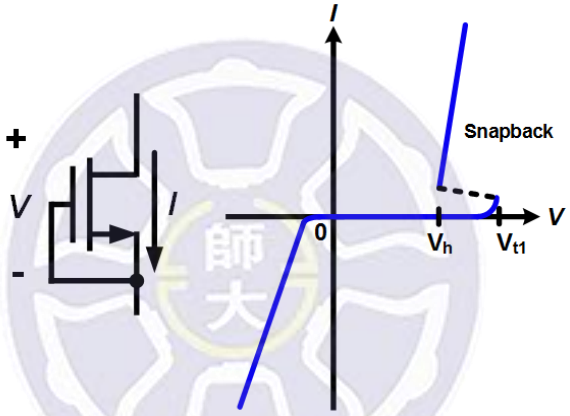


Fig. 2.3. The I-V curve of NMOS.

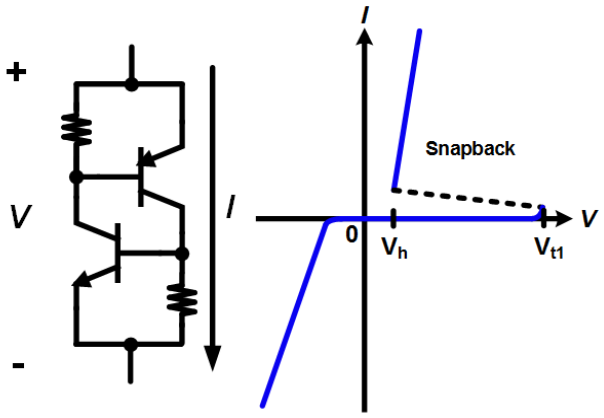


Fig. 2.4. The I-V curve of SCR.

2.2 ESD Protection Designs for High-Frequency Application

2.2.1 Capacitive ESD Protection Circuit

(1) Dual Diodes [20]

As shown in Fig. 2.5, a pair of diodes near I/O pad are the most commonly used ESD protection circuit. When positive ESD stress hits I/O pad, the diode placed from I/O to V_{DD} (D_{P1}) form the path for positive I/O-to-V_{DD} (PD mode). When negative ESD stress hits I/O pad, the diode placed from V_{SS} to I/O pad (D_{N1}) form the path for negative I/O-to-V_{SS} (NS mode). In assistance with power-rail ESD clamp circuit, the whole-chip ESD protection can be realized. The path of the positive I/O-to-V_{SS} (PS mode) is formed by the diode (D_{P1}) in series with power-rail ESD clamp circuit. In series with power-rail ESD clamp circuit, the diode (D_{N1}) form the path of the negative I/O-to-V_{DD} (ND mode). To reduce the parasitic effect, the size of diode is cut down to lower the capacitive load. However, the ESD robustness decreases with reducing size.

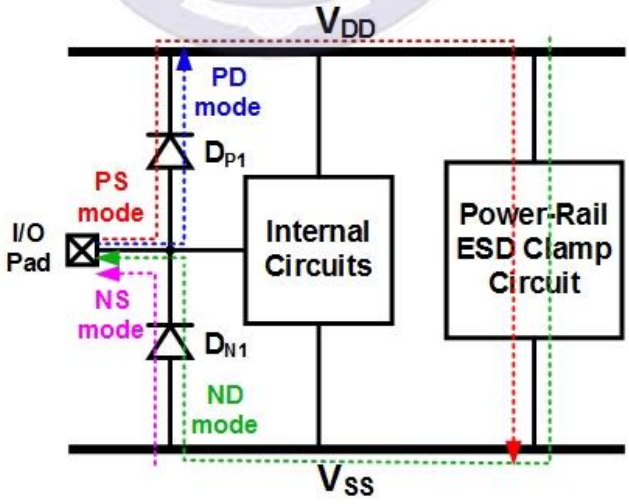


Fig. 2.5. ESD protection design of dual diodes [20].

(2) Dual Stacked Diodes [21]

For the high-frequency applications, the parasitic capacitance of protection circuit has to be reduced to lower the signal loss. In addition to smaller device, an improved configuration is proposed to solve this problem by stacking diodes. As shown in Fig. 2.6, two stacked diodes are placed from V_{SS} to I/O pad (D_{N1}, D_{N2}) and I/O pad to V_{DD} (D_{P1}, D_{P2}). The discharging path of dual stacked diodes is the same as the dual diodes. Whole-chip ESD protection is realized with the help of power-rail ESD clamp circuit. In this improved structure, the parasitic capacitance is reduced to half by parallel connection. However, the turn-on efficiency of stacked diodes is not enough. Stacked diodes may fail to turn on in time and cause damage to internal circuit.

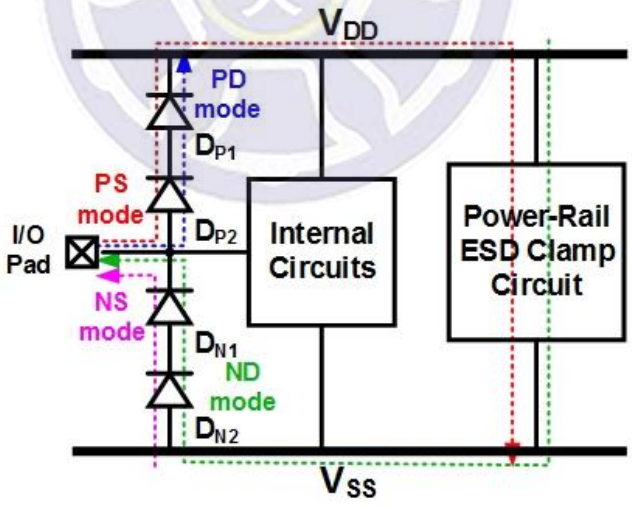


Fig. 2.6. ESD protection design of dual stacked diodes [21].

(3) Diode-triggered SCR (DTSCR) [22]

SCR is a useful ESD protection device in CMOS process due to high robustness. In addition, the SCR device can be applied at high frequencies because it has low parasitic capacitance per layout area. The SCR device discharges high ESD current with positive-feedback mechanism.

SCR has many advantages for ESD protection. However, the trigger voltage is too high so that SCR is unable to be used alone. The trigger speed can be improved by increasing the current which flows through the resistance between the base and emitter. The triggering of SCR is presented in Fig. 2.7. Diode string is a simple trigger device of SCR. As shown in Fig. 2.8, the diodes are conducted at first when I/O pad is hit by ESD stress. The current of diodes flows into the base of NPN. The voltage across R_{Sub} is increased to turn on the embedded NPN, and further turn on the PNP. The SCR is fully triggered on and discharges ESD current so that the internal circuit is safe from damaging.

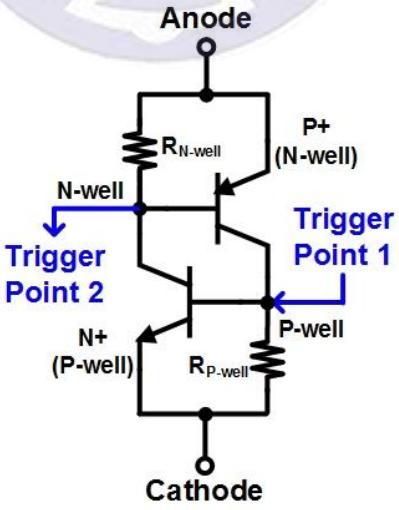


Fig. 2.7. The triggering of SCR.

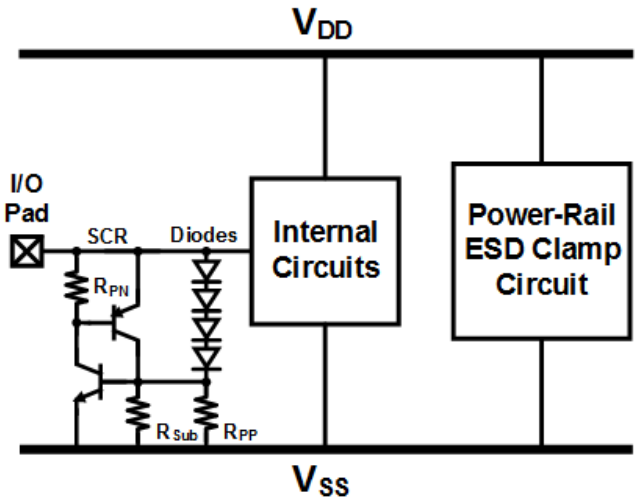


Fig. 2.8. ESD protection design of diode-triggered SCR (DTSCR) [22].

2.2.2 Capacitive ESD Protection Circuit with Inductor

Although the parasitic capacitance of ESD protection circuit has an adverse effect on signal transmission, the performance of internal circuit at high frequencies can be maintained with proper design methods. The capacitive ESD protection device is combined with the inductor to resonates with.

(1) Inductor-Triggered SCR (LTSCR) [23]

As shown in Fig. 2.9, the inductor-triggered SCR (LTSCR) is proposed for 60GHz-application in the previous study. The main discharging path of LTSCR is formed by SCR. To improve the trigger speed, the SCR device has to be equipped with trigger element.

In this design, PMOS in series with an inductor is connected to the base of NPN inside SCR. The gate of triggering PMOS is tied to the RC network applied in power-rail ESD clamp circuit. Under normal operation, the capacitor of RC network can be charged to V_{DD}. The gate of PMOS is pull to a high level in order to keep off the SCR device. When ESD events happen, the voltage of I/O pad increases suddenly, and the triggering PMOS is turned on. The current flows into the resistance between the base

and emitter of NPN through PMOS. The SCR is fully triggered on to discharge ESD current.

The inductor can resonate with the parasitic capacitance of triggering PMOS and SCR. Therefore, the signal loss is kept low at 60GHz. LTSCR has great high-frequency performance at 60GHz with high ESD robustness.

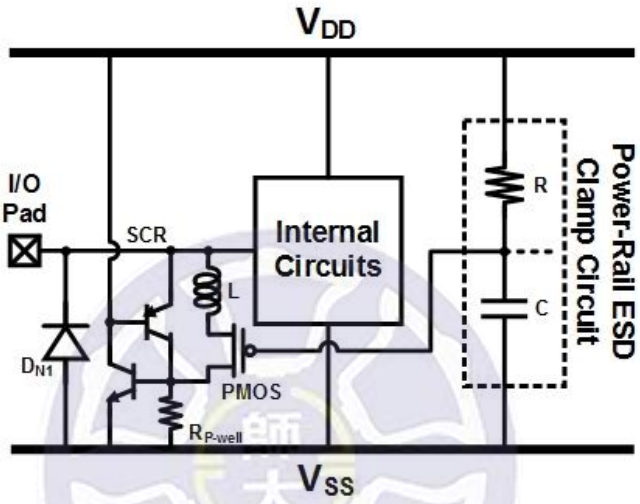


Fig. 2.9. ESD protection design of inductor-triggered SCR (LTSCR) [23].

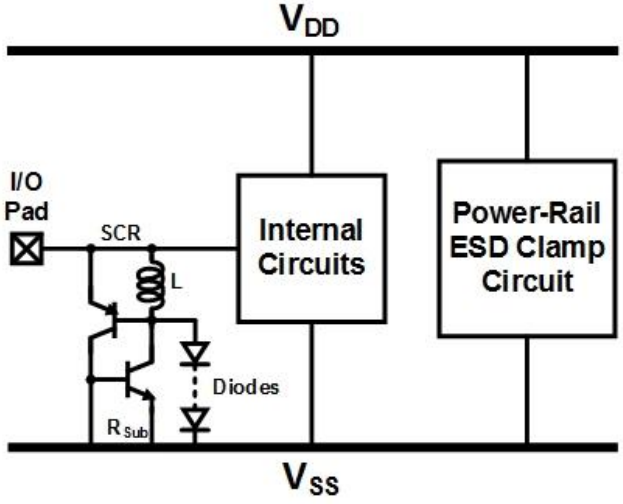


Fig. 2.10. ESD protection design of inductor-assisted SCR (LASCR) [24].

(2) Inductor-Assisted SCR (LASCR) [24]

Another ESD protection design with inductor is presented in Fig. 2.10. LASCR is composed of diode string, inductor, and SCR. SCR forms the discharging path of ESD current. To enhance the turn-on efficiency, diode string with lower trigger voltage is connected between the base of PNP and the emitter of NPN. The SCR device is triggered with the current of diode string.

Assisted with the inductor, the parasitic effects of LASCR is reduced. The inductor resonates with the parasitic capacitance of SCR to keep high-frequency performance. In addition, the inductor forms the discharging path from V_{SS} to I/O pad under NS mode.

2.2.3 Distributed ESD Protection Circuit (DESD)

The parasitic capacitance of ESD protection circuit near I/O pad is harmful for high-frequency performance. To solve this problem, the protection device is cut down on size. However, the size is proportional to the ESD robustness. Smaller device achieves relatively low ESD level.

There is another way to design the ESD protection circuit for high-frequency applications [25]. Dividing one device into many sections is an effective way to maintain the ESD robustness. To achieve good high-frequency performance, these parts of protection device are connected with matching elements such as inductor. The inductor can resonate with the parasitic capacitance caused by device. Therefore, the RF signal is transmitted with less distorting.

As shown in Fig. 2.11, the distributed ESD protection circuit is composed of two sections (D_{P1}, D_{N1} and D_{P2}, D_{N2}). The matching element used to sustain the broadband performance is an inductor (L). The diodes can provide the discharging path under forward bias for PD mode and NS mode. With the help of power-rail ESD clamp circuit, the ESD stress under PS mode and ND mode can be discharged as well.

The different way to match the dual diodes is presented in Fig. 2.12. The device is divided into three sections (D_{P1}, D_{N1}, D_{P2}, D_{N2}, and D_{P3}, D_{N3}) and with three inductors (L_1, L_2, and L_3). Each part of protection device can be much smaller. However, the layout area is increased with more inductors in use. Both two structures can achieve good broadband performance and present great ESD robustness.

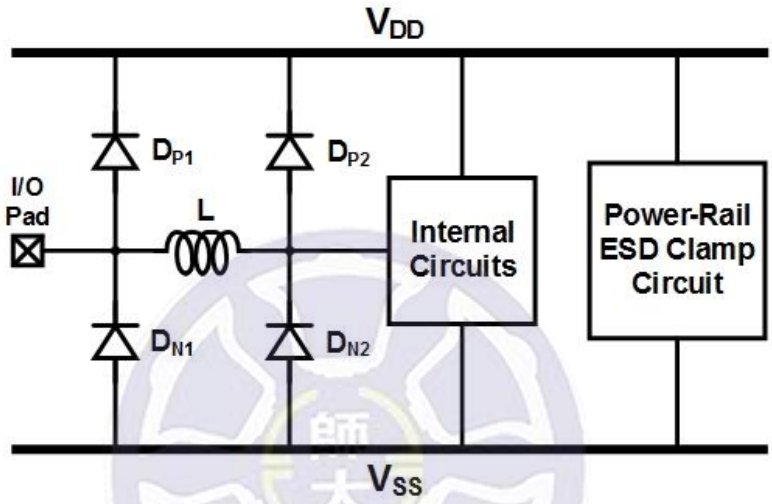


Fig. 2.11. ESD protection design of two-section distributed circuit [25].

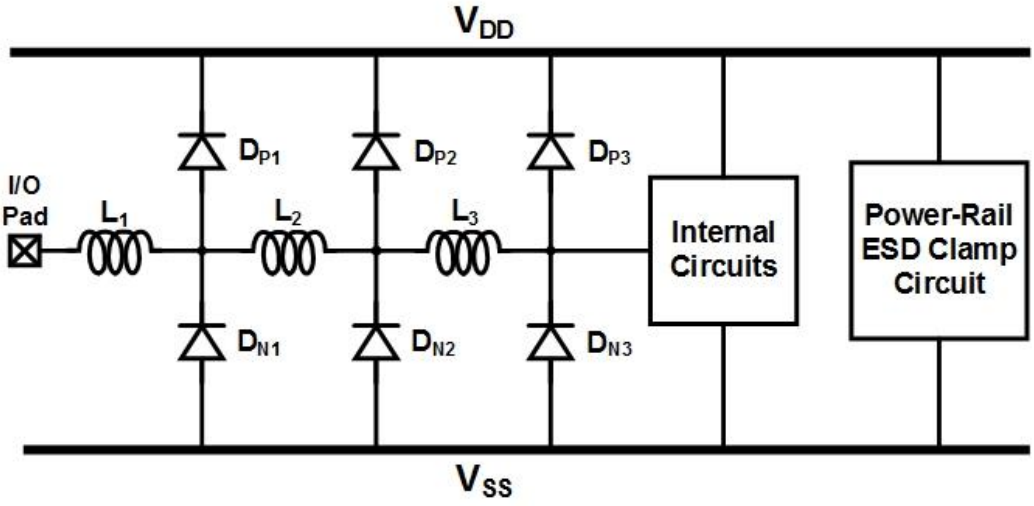


Fig. 2.12. ESD protection design of multi-section distributed circuit [25].

2.2.4 Comparison of ESD Protection Design for High-Frequency Applications

The ESD protection designs applied to high-frequency circuits are introduced in previous section. The design complexity of these protection circuits are different due to different components. The complexity of dual diodes is the lowest because it is only designed with two diodes. There are more diodes in dual stacked diodes, and the layout type is more difficult.

DTSCR is composed of diode string and the SCR device. The layout type has an effect on performance. The design of DTSCR is more complex than the design with diodes. With the use of inductor, it is hard to place other components. Therefore, the design complexity for LTSCR, LASCR, and distributed circuit are the most difficult.

Due to the parasitic capacitance, the dual diodes design is available for a narrow band. The parasitic capacitance of dual stacked diodes is reduced to half in series connection. The range of operating frequency can be increased. The high-frequency performance of DTSCR worsen because of additional parasitic capacitance of diode string. It is suitable for narrow band applications about 0 to 5GHz. The inductor can resonate with the parasitic capacitance of protection device to reduce the parasitic effect. With the resonance of LC, the ESD protection designs can be applied in high-frequency circuit. In parallel connection, the LTSCR shows good performance at specific frequency.

Dual diodes and dual stacked diodes turn on to discharge ESD current with forward-biased diodes. The diodes provide the discharging path of NS mode and PD mode. The DTSCR is able to discharge ESD current of PS mode. To realize whole-chip ESD protection, the power-rail ESD clamp circuit is necessary. The base of embedded PNP inside LTSCR is connected to V_{DD} to provide the additional path of PD mode. The LTSCR is available for PS mode and PD mode. The emitter and base of PNP in LASCR

is connected with the inductor. Therefore, the SCR device discharges bidirectional ESD current. Table 2.1 shows the comparison of ESD protection designs for high-frequency applications.

Table 2.1. Comparison of ESD protection design for high-frequency applications

ESD Protection Design	**Operating Frequency**	**Design Complexity**	**Discharging Mode**
Dual Diodes [20]	Narrow Band 0~5GHz	Low	PD mode NS mode
Dual Stacked Diodes [21]	Broadband 0~10GHz	Medium	PD mode NS mode
DTSCR [22]	Narrow Band 0~5GHz	Medium	PS mode
LTSCR [23]	Specific Frequency 60GHz	High	PS mode PD mode
LASCR [24]	Specific Frequency 30GHz	High	PS mode NS mode
DESD [25]	Broadband 0~15GHz	High	PD mode NS mode

Chapter 3

Design of π-Model Silicon-Controlled Rectifier (π-SCR)

3.1 Design Concepts of Distributed Circuit

As the mobile communication industry flourishes, the market of radio-frequency integrated circuits (RFICs) grows up continuously. The RF circuits are used widely so that the ESD protection for high-frequency application becomes important increasingly. Traditional ESD protection designs applied to electronic circuits are no longer suitable for RFICs [26]. Owing to the parasitic capacitance near I/O pad, the input signal may be affected by protection device. The impedance of capacitor decreases as the operating frequency rises. It means that the protection device beside the input terminal causes the signal loss. To achieve high ESD level, the protection device has to be in large size. However, the parasitic capacitance affects the normal operation of internal circuit severely. Some methods are proposed to lower the parasitic effects, such as distributed ESD protection circuit [27], [28].

The protection device is divided into two smaller parts. One part is near the I/O pad, and the other part is close to internal circuits. To sustain the characteristics of RF circuit, two parts of protection devices are connected by a matching element. Matching element can resonate with the parasitic capacitance of two stages. Therefore, two-section distributed circuit can stand high ESD level with less signal loss. The parasitic capacitance of the devices placed from V_{SS} to I/O and I/O to V_{DD} are parallel when analyzed in the ac state. As shown in Fig. 3.1, the high-frequency equivalent circuit is like a π shape.

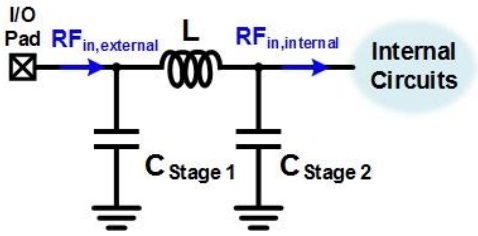


Fig. 3.1. High-frequency equivalent circuit of π-model circuit.

$C_{Stage\ 1}$ and $C_{Stage\ 2}$ are from the protection element in two stages such as SCR and diode. The value of parasitic capacitance is decided by the size of protection device. According to the expected specification, the selected device is equipped to discharge the ESD current. Therefore, the size of the device has to be large enough. The PN junction and side-wall of protection element lead to parasitic capacitance. The junction capacitance increases with larger layout area. The longer perimeter of PN junction makes the side-wall capacitance rise.

In the proposed design, the value of capacitance caused by stage 1 is close to stage 2. The π-model can be simplified into two L-models as shown in Fig. 3.2. The expression of input impedance for the second L-model is expressed in 3.1. As expresses in 3.2, the imaginary part of input impedance has to be zero. Then the inductor value (L) can be calculated with the characteristic impedance (Z_0) of internal circuit and resonant frequency (ω_0) as shown in 3.3.

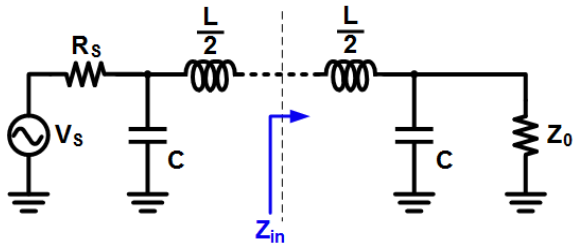


Fig. 3.2. Two simplified L-models of π-model circuit.

$$Z_{in} = \frac{j\omega_0 L}{2} + \frac{1}{j\omega_0 C + \frac{1}{Z_0}} \tag{3.1}$$

$$\mathrm{Im}(Z_{in}) = \frac{2\omega_0 L(1+(Z_0\omega_0 C)^2) - 4{Z_0}^2\omega_0 C}{4+4(Z_0\omega_0 C)^2} \tag{3.2}$$

$$L = \frac{2{Z_0}^2 C}{1+(Z_0\omega_0 C)^2} \tag{3.3}$$

3.2 Traditional π-Model Diode (π-Diode)

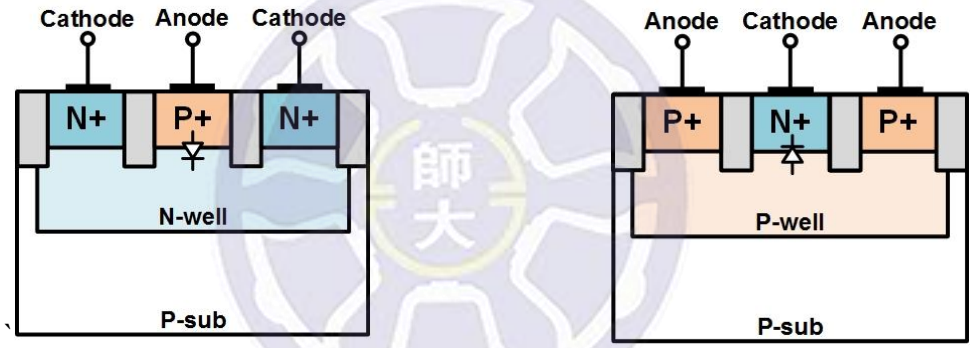
Diode is a common ESD protection device in CMOS technology. It is composed of both P-type and N-type semiconductor. There are two ways to realize p-n junction on chip. As shown in Fig 3.3 (a), P-type diode has its P+ as anode and its N-well as cathode. As shown in Fig 3.3 (b), the anode of N-type diode is P-well and the cathode of that is N+.

When it is conducted under forward bias, the diode turns on and discharges current at low voltage. Diode can also discharge current under reverse bias, but the clamping voltage is higher than the forward biased diode. It has high ESD robustness on account of low power dissipation. The characteristics like a switch make it suitable for ESD protection. In addition, diode is used as a trigger device for SCR, MOSFET, and BJT.

Traditional π-model diode (π-diode) is a two-section distributed circuit with diodes as device. The whole-chip ESD protection circuit with π-diode is shown in Fig 3.4. Stage 1 is composed of diodes placed from V_{SS} to I/O (D_{N1}) and from I/O to V_{DD} (D_{P1}), and stage 2 is composed of diodes placed from V_{SS} to I/O (D_{N2}) and from I/O to V_{DD} (D_{P2}). The power-rail ESD clamp circuit is equipped to discharge the ESD current between V_{DD} and V_{SS}.

The ESD current under PD mode can be discharged by $D_{P1}$and D_{P2}. The ESD current under NS mode is discharged by D_{N1} and D_{N2}. The ESD current between V_{DD} and V_{SS} is discharged by the power-rail ESD clamp circuit. The ESD current under ND mode can be discharged by the power-rail ESD clamp circuit in series with D_{N1} and D_{N2}. The ESD current under PS mode is discharged by D_{P1} and D_{P2} in series with the power-rail ESD clamp circuit.

The test cells of whole-chip ESD protection circuit with π-diode are listed in Table 3.1. The layout top view of each cell is shown below. The width of diode used in π-diode is 5μm (as shown in Fig 3.5.), 15μm (as shown in Fig 3.6.), and 25μm (as shown in Fig 3.7.) respectively.



(a) (b)

Fig. 3.3. Cross-sectional view of symmetrical (a) P-type and (b) N-type diode.

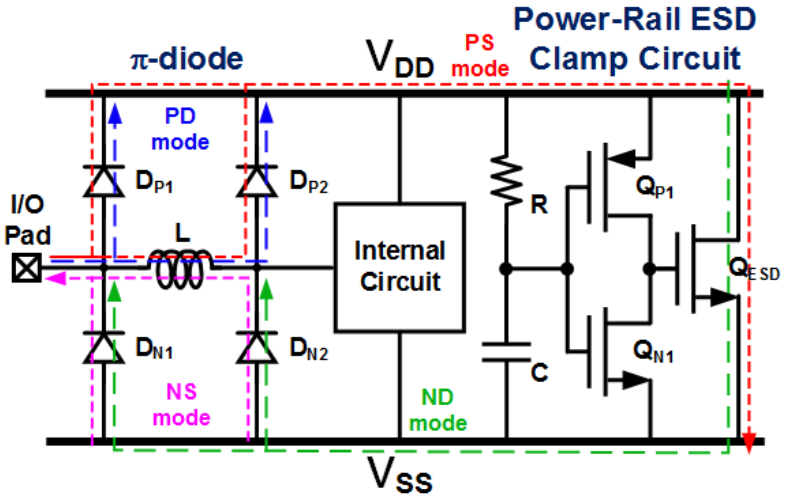


Fig. 3.4. Whole-chip ESD protection circuit with traditional π-diode.

Table 3.1. The test cell of π-diode

Cell Name	Stage 1		Stage 2	
	Device	Width	Device	Width
π-diode_5_5	D_{P1}	5μm	D_{P2}	5μm
	D_{N1}	5μm	D_{N2}	5μm
π-diode_15_15	D_{P1}	15μm	D_{P2}	15μm
	D_{N1}	15μm	D_{N2}	15μm
π-diode_25_25	D_{P1}	25μm	D_{P2}	25μm
	D_{N1}	25μm	D_{N2}	25μm

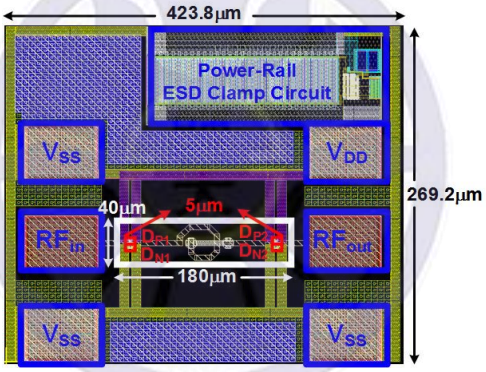


Fig. 3.5. Layout top view of π-diode_5_5.

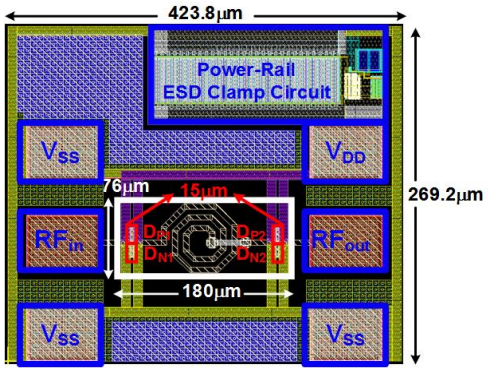


Fig. 3.6. Layout top view of π-diode_15_15.

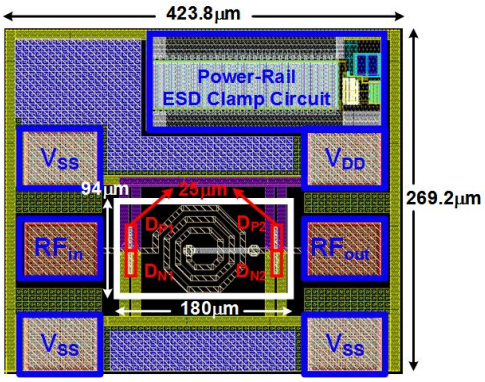
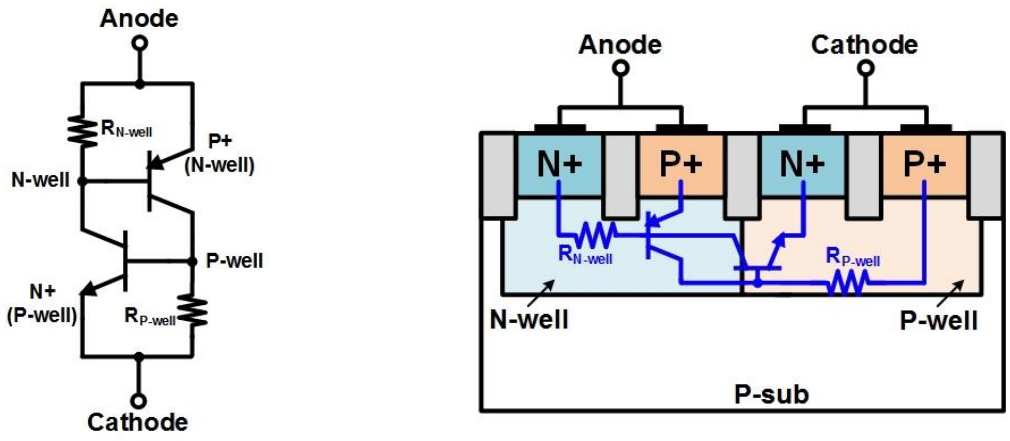


Fig. 3.7. Layout top view of π-diode_25_25.

3.3 Proposed π-Model SCR (π-SCR)

Silicon-controlled rectifier (SCR) is a device which is composed of p-n-p-n (P+/N-well/P-well/N+) four-layer semiconductor in CMOS technology. The equivalent circuit of SCR is shown in Fig 3.8 (a). The cross-sectional view of SCR is shown in Fig 3.8 (b). The P+/N-well/P-well formed the PNP, and the N-well/P-well/N+ formed the NPN inside SCR. The base of parasitic PNP is connected to the collector of parasitic NPN, and the base of parasitic NPN is connected to the collector of parasitic PNP. When SCR is fully conducted, it can discharge high current due to positive-feedback mechanism [29]. The voltage across SCR decreases rapidly during conduction. The snapback phenomenon of SCR reduces the power dissipation when ESD current flows. Therefore, SCR has high ESD robustness per unit layout area.

The trigger voltage of SCR device is high. There are many researches about improving turn-on efficiency [30], [31]. Among those triggering methods, diode string is a common way for SCR to be triggered with. Diode string is an appropriate trigger device with low parasitic capacitance. Because of low clamping voltage, SCR cannot be turned off as internal circuit operates normally. The latch-up problems must be considered when ESD protection circuit is designed with SCR device.



(a) (b)

Fig. 3.8. (a) Equivalent circuit and (b) cross-sectional view of SCR.

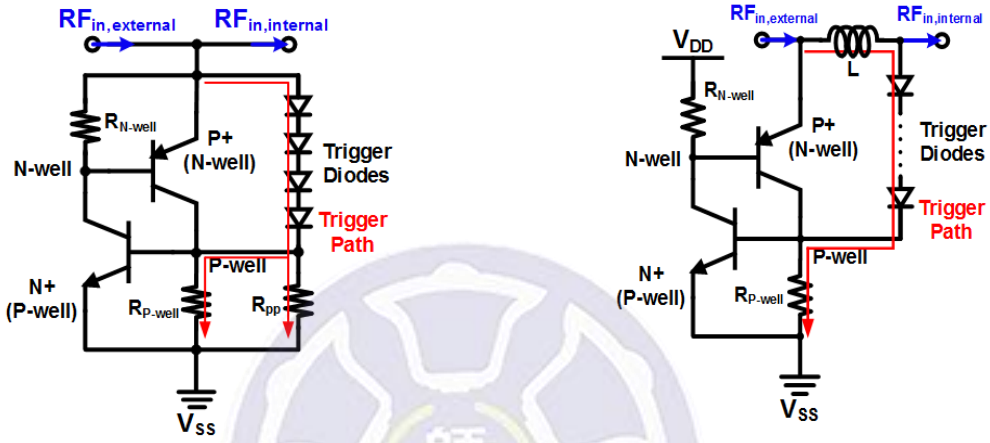
SCR has low parasitic capacitance per layout area. Therefore, it can also be used for ESD protection in high-frequency applications. In order to improve the practicality, trigger device is added to speed up its turn-on efficiency. As shown in Fig 3.9 (a), diode-triggered SCR (DTSCR) is a commonly used ESD protection design.

With small layout area and low parasitic capacitance, diode string is selected as the trigger device for SCR in proposed design. The trigger voltage of SCR can be regulated with different amount of trigger diodes to meet the requirement of internal circuit. However, the parasitic capacitance of SCR as well as trigger device causes signal loss to RF signal.

Proposed π-model SCR (π-SCR) realizes DTSCR with two-section distributed circuit for high-frequency applications as shown in Fig 3.9 (b). By the use of matching inductor, the signal loss of RF signal can be reduced. In addition, the turn-on efficiency of DTSCR is enough. The N-well of parasitic PNP inside π-SCR is tied to V_{DD} to form a discharging path with parasitic diode (P+/N-well).

The octagonal spiral inductor is adopted as the matching element as shown in Fig 3.10. The metal width of inductor is 6μm. The length of each sections in inductor is

reduced by 2μm. The shape of the conversion between different layers is also octagonal in order not to reduce the cross-sectional area instantaneously. In addition, three-layer metal (metal 3 to metal 5) is used together to increase the thickness. The structure of proposed matching inductor is shown in Fig 3.11. As shown in Fig 3.12, the SCR device can be realized in symmetrical structure to enhance the equivalent width.



(a) (b)

Fig. 3.9. Equivalent circuit of (a) diode-triggered SCR (DTSCR) and (b) proposed π-SCR.

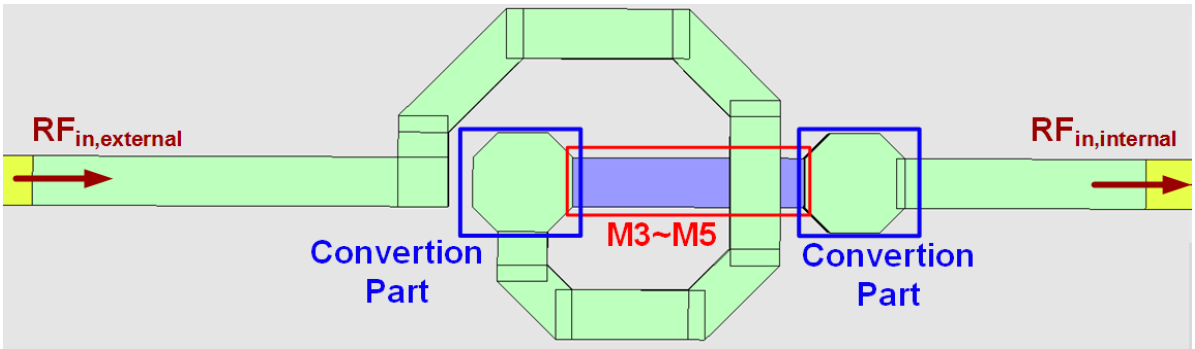


Fig. 3.10. The top view of matching inductor.

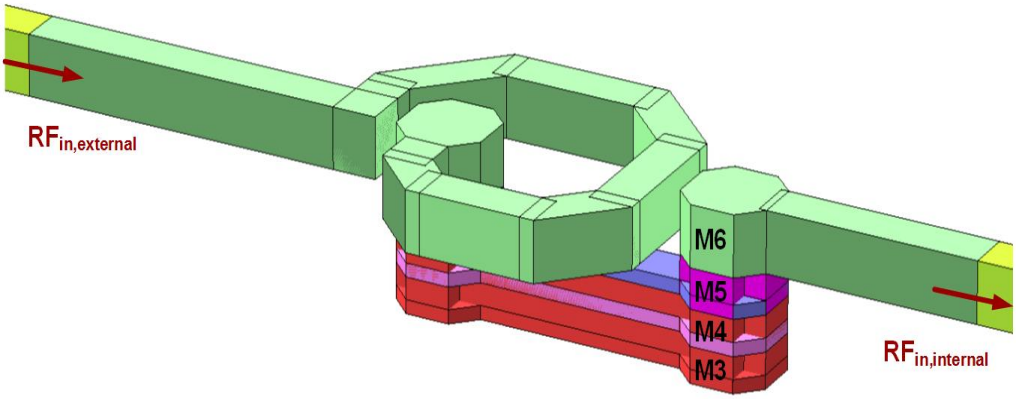


Fig. 3.11. The structure of matching inductor.

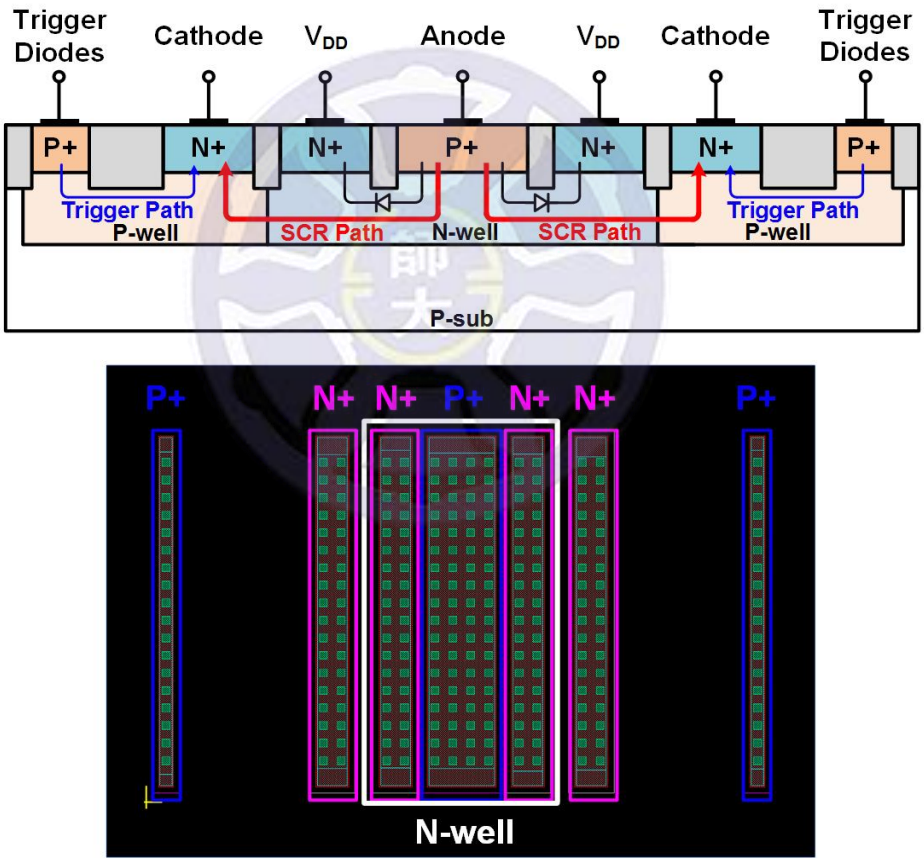


Fig. 3.12. Cross-sectional view and layout top view of π-SCR in symmetrical structure.

3.3.1 π-Model SCR Type 1 (π-SCR$_1$)

In π-model SCR type 1 (π-SCR$_1$), the SCR device is put at stage 1 near I/O pad to form the main discharging path. Stage 2 near internal circuit is composed of trigger diodes and NS diode. There is a matching inductor between two stages. As shown in Fig. 3.13, π-SCR$_1$ is equipped with power-rail ESD clamp circuit to realize the whole-chip ESD protection.

The primary discharging path for PS mode is formed by SCR (P+/N-well/P-well/N+). The SCR device is able to discharge high ESD current with the trigger current from diode string. Three trigger diodes ($D_{trigger}$) in small size turn on first when ESD stress hits. The trigger current flows through the resistance of P-well ($R_{P\text{-}well}$) and increases the voltage across the base and emitter of NPN inside SCR.

A discharging path for PD mode is formed by connecting N-well to V_{DD}. The parasitic diode inside the SCR discharges the ESD current. The NS diode (D_{NS}) provides the discharging path for ESD current under NS mode. The ESD current between V_{DD} and V_{SS} is discharged by the power-rail ESD clamp circuit. In series with the power-rail ESD clamp circuit, D_{NS} discharges the ESD current under ND mode. The matching element between stage 1 and stage 2 is realized with an octagonal spiral inductor. It resonates with parasitic capacitance of SCR and $D_{trigger}$ in parallel with D_{NS}. The impact of protection device on RF signal can be reduced.

First, calculate the parasitic capacitance of stage 1 ($C_{Stage\ 1}$) caused by the junction of SCR. Then calculate the parasitic capacitance of stage 2 ($C_{Stage\ 2}$) caused by $D_{trigger}$ in parallel with D_{NS}. The size of SCR and D_{NS} are designed to be equal. So that, the inductance (L) in this design can be calculated.

The test devices of π-SCR$_1$ are listed in Table 3.2. The proposed design is fabricated in 0.18μm CMOS process. The width of SCR used in π-SCR$_1$_10 is 10μm in symmetrical structure, the width of $D_{trigger}$ is 5μm, and the width of D_{NS} is 10μm as

shown in Fig. 3.14. The width of SCR used in π-SCR$_1$_30 is 30μm in symmetrical structure, the width of $D_{trigger}$ is 5μm, and the width of D_{NS} is 30μm as shown in Fig. 3.15. The width of SCR used in π-SCR$_1$_50 is 50μm in symmetrical structure, the width of $D_{trigger}$ is 5μm, and the width of D_{NS} is 50μm as shown in Fig. 3.16. The area of each test device is 423.8* 269.2μm^2.

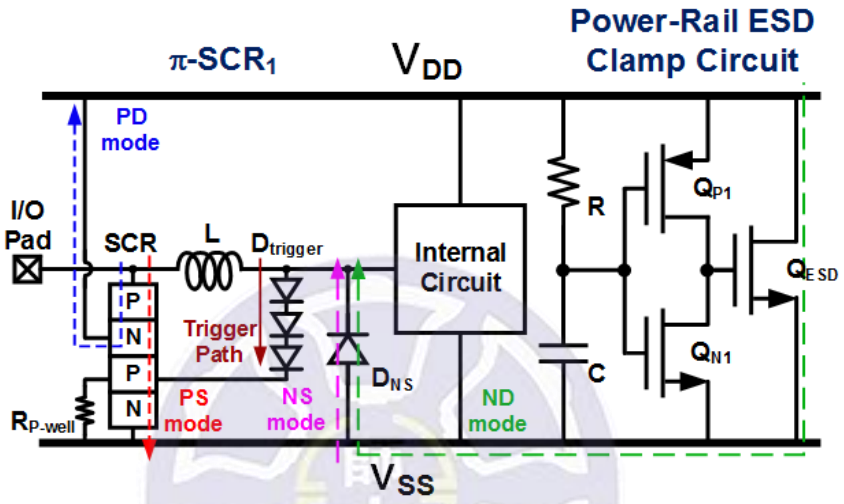


Fig. 3.13. Whole-chip ESD protection circuit with π-SCR$_1$.

Table 3.2. The test cell of π-SCR$_1$

Cell Name	Stage 1		Stage 2	
	Device	Width	Device	Width
π-SCR$_1$_10	SCR	10μm	$D_{trigger}$	5μm
			D_{NS}	10μm
π-SCR$_1$_30	SCR	30μm	$D_{trigger}$	5μm
			D_{NS}	30μm
π-SCR$_1$_50	SCR	50μm	$D_{trigger}$	5μm
			D_{NS}	50μm

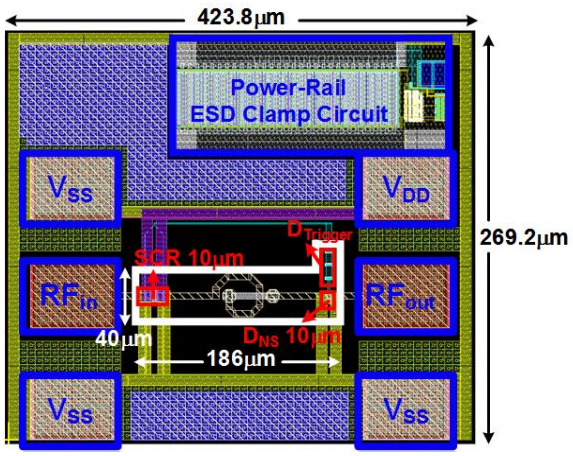


Fig. 3.14. Layout top view of π-SCR$_1$_10.

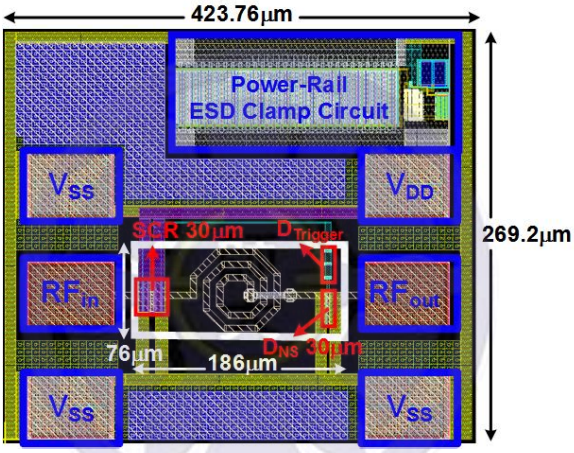


Fig. 3.15. Layout top view of π-SCR$_1$_30.

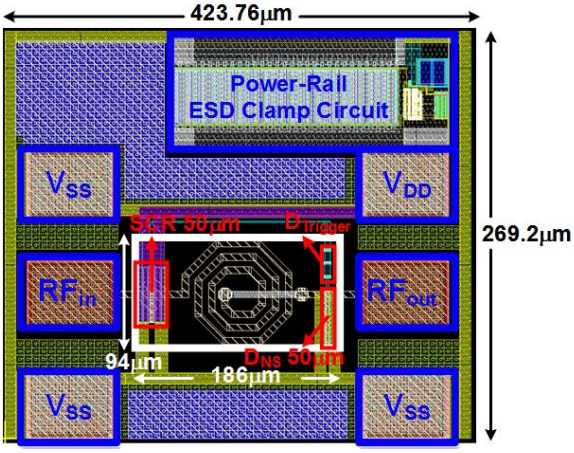


Fig. 3.16. Layout top view of π-SCR$_1$_50.

3.3.2 π-Model SCR Type 2 (π-SCR$_2$)

There are two SCR devices in proposed π-model SCR type 2 (π-SCR$_2$). NS diode is also divided into two sections in two stages. One is put at stage 1, and the other is put at stage 2, and trigger diodes ($D_{trigger}$) is at stage 2 only. Compared to π-SCR$_1$, the SCR device as well as NS diode is equally divided into two stages. Therefore, two SCR devices (SCR1, SCR2) and two NS diodes (D_{NS1}, D_{NS2}) can discharge ESD current simultaneously. The matching element used to connect stage 1 and stage 2 is an octagonal spiral inductor. Equipped with power-rail ESD clamp circuit, the whole-chip ESD protection circuit with π-SCR$_2$ is shown in Fig. 3.17. The power-rail ESD clamp circuit can discharge ESD current between V_{DD} and V_{SS}.

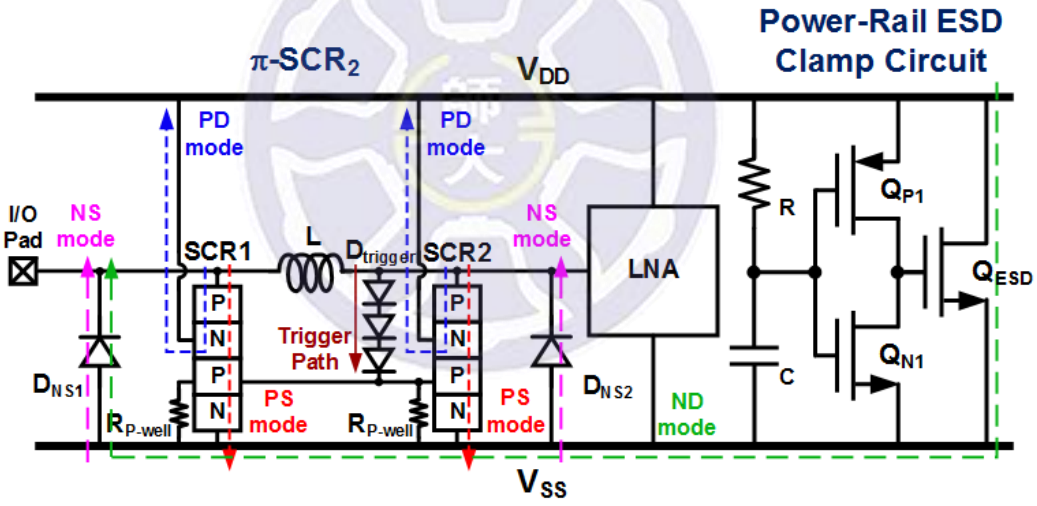


Fig. 3.17. Whole-chip ESD protection circuit with π-SCR$_2$.

The discharging path of PS mode is formed by the SCRs from both stages. The SCR device is able to discharge high ESD current with the help of trigger diodes. The trigger diodes can turn on first when ESD stress hits. The trigger current flows into the resistance of P-well ($R_{P\text{-well}}$) in the SCR of both stages. The voltage across the base and emitter of NPN inside SCR is then increased. The parasitic diodes of two SCRs form

the discharging path for PD mode. D_{NS1} and D_{NS2} have the discharging path for ESD current of NS mode. The ESD current between V_{DD} and V_{SS} is discharged by the power-rail ESD clamp circuit. In series with the power-rail ESD clamp circuit, D_{NS1} and D_{NS2} discharge the ESD current of ND mode.

$C_{Stage\ 1}$is the parasitic capacitance of the junction of SCR1 in parallel with D_{NS1}, and $C_{Stage\ 2}$ is the parasitic capacitance of the junction of SCR2 in parallel with D_{NS2}. The size of SCR1 is equal to SCR2, and the size of D_{NS1} is equal to D_{NS2}. The value of $C_{Stage\ 1}$ is almost the same as $C_{Stage\ 2}$. The inductance (L) of π-SCR_2 can be calculated.

The test devices of π-SCR_2 are listed in Table 3.3. The width of π-SCR_2 is 5μm, 15μm, and 25μm in symmetrical structure respectively. The width of NS diodes is also 5μm, 15μm, and 25μm. The layout top view is shown in Fig. 3.18, Fig. 3.19, and Fig. 3.20.

Table 3.3. The test cell of π-SCR_2

Cell Name	**Stage 1**		**Stage 2**	
	Device	**Width**	**Device**	**Width**
π-SCR_2_5_5	SCR1	5μm	$D_{trigger}$	5μm
			SCR2	5μm
	D_{NS1}	5μm	D_{NS2}	5μm
π-SCR_2_15_15	SCR1	15μm	$D_{trigger}$	5μm
			SCR2	15μm
	D_{NS1}	15μm	D_{NS2}	15μm
π-SCR_2_25_25	SCR1	25μm	$D_{trigger}$	5μm
			SCR2	25μm
	D_{NS1}	25μm	D_{NS2}	25μm

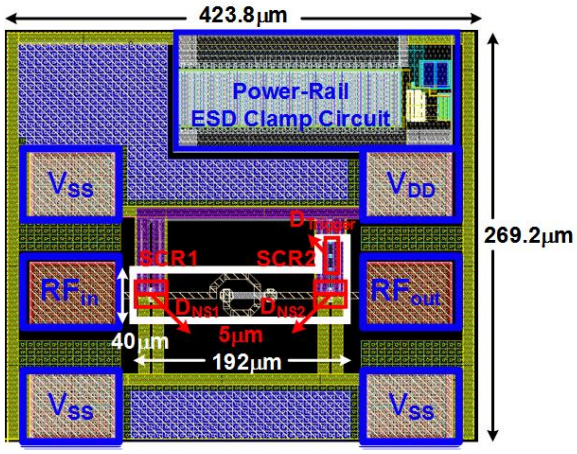


Fig. 3. 18. Layout top view of π-SCR$_2$_5_5.

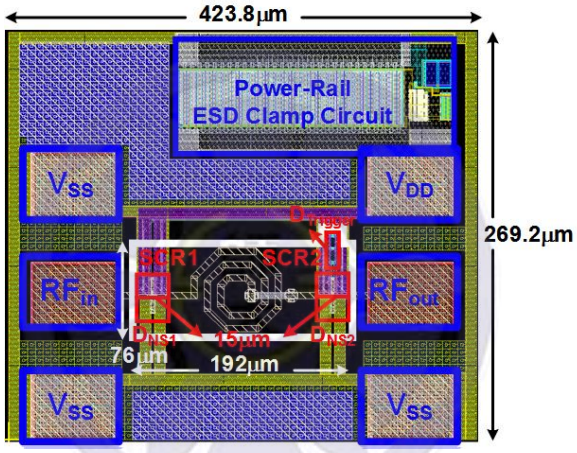


Fig. 3.19. Layout top view of π-SCR$_2$_15_15.

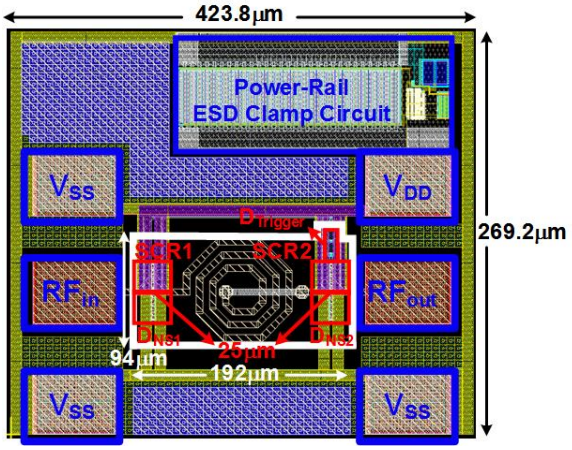


Fig. 3.20. Layout top view of π-SCR$_2$_25_25.

3.4 Simulation Results

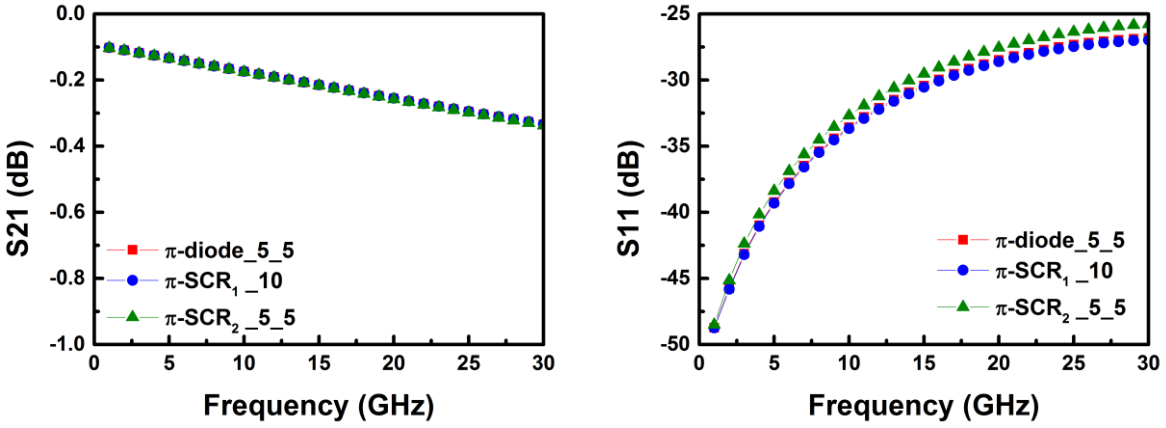
The high-frequency performance of traditional π-diode and proposed π-SCR are evaluated by S-parameter. By examining S21 and S11, the impact of proposed ESD protection device on high-frequency applications is found out.

Larger S21 means that the signal is passed to another terminal with less loss. Smaller S11 means that the signal is delivered with less reflection. The proposed ESD protection device is designed to keep the S21 approach to 0 and make the S11 as smaller as possible.

Advanced design system (ADS) is used to simulate the S-parameter of all the protection device. The matching inductor is simulated with SONNET electromagnetic (EM) software. The simulation results of proposed design are compared with traditional design in similar size.

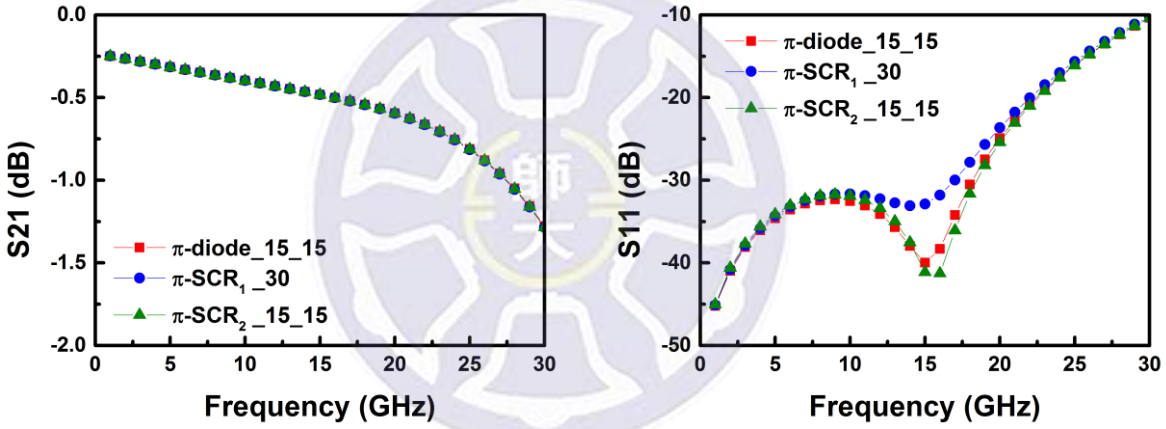
Simulated S-parameter of π-diode_5_5 is compared with π-SCR_1_10 and π-SCR_2_5_5 in Fig. 3.21. Simulated S-parameter of π-diode_15_15 is compared with π-SCR_1_30 and π-SCR_2_15_15 in Fig. 3.22. Simulated S-parameter of π-diode_25_25 is compared with π-SCR_1_50 and π-SCR_2_25_25 in Fig. 3.23. Simulated S-parameter at 10GHz is listed in Table 3.4.

The parasitic capacitance of diode and SCR with the same dimension is almost the same. Therefore, test devices in similar size use the same matching inductor to connect between two stages. From the simulation results, there is little difference between traditional device and proposed design. In addition, the S21 of all the test cells at 10GHz is higher than -1dB.



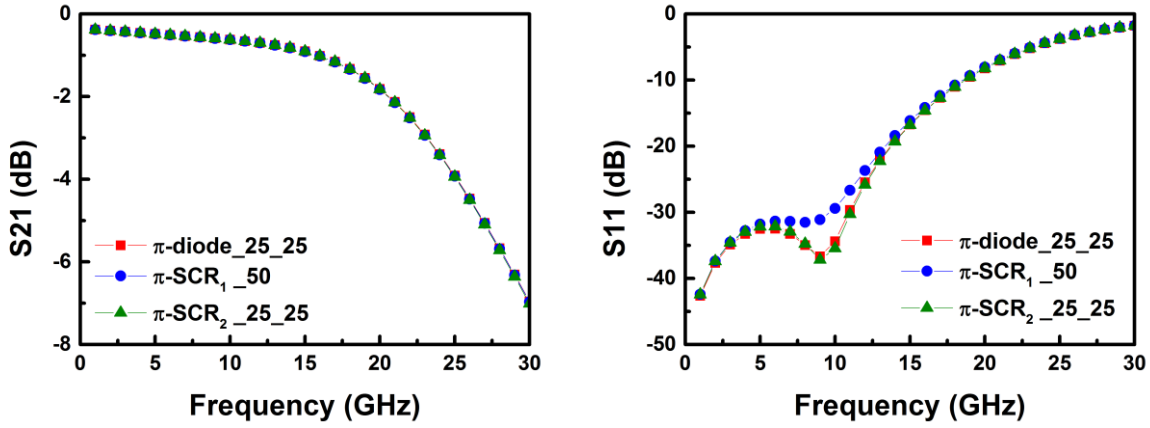
(a) (b)

Fig. 3.21. The simulated S-parameter of π-diode_5_5, π-SCR1_10, and π-SCR2_5_5.



(a) (b)

Fig. 3.22. The simulated S-parameter of π-diode_15_15, π-SCR1_30, and π-SCR2_15_15.



(a) (b)

Fig. 3.23. The simulated S-parameter of π-diode_25_25, π-SCR1_50, and π-SCR2_25_25.

Table 3.4. Simulated S-parameter at 10GHz

Cell Name	S21 (dB) at 10GHz	S11 (dB) at 10GHz
π-diode_5_5	-0.17	-33.57
π-diode_15_15	-0.4	-32.52
π-diode_25_25	-0.62	-34.4
π-SCR1_10	-0.17	-33.68
π-SCR1_30	-0.4	-31.68
π-SCR1_50	-0.63	-29.41
π-SCR2_5_5	-0.18	-32.69
π-SCR2_15_15	-0.4	-31.91
π-SCR2_25_25	-0.63	-35.47

3.5 Measurement Results

All the test devices are fabricated in 0.18μm CMOS process. The chip photograph is shown in Fig. 3.24. The width is 1298μm, and the length is 1517μm. There are three kinds of ESD protection devices, π-diode, π-SCR_1, and π-SCR_2 in different size. The measurement results are introduced in following section.

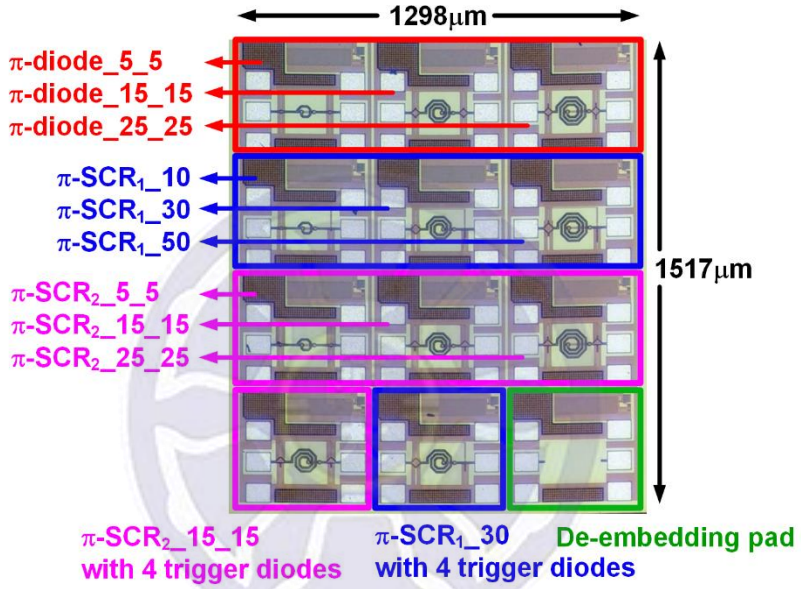


Fig. 3.24. The chip photograph of test device.

3.5.1 High-Frequency Performance

As shown in Fig. 3.25, the S-parameter is measured by 67GHz RFIC parameter measurement system with 2-port GSG probes. However, the measured S-parameter includes the effect of pad. The S-parameter of de-embedding pad is measured at first as a reference in Fig. 3.26 (a). Then the S-parameter of the test device is measured in Fig. 3.26 (b). The de-embedding technique is used to remove the effects of pad to extract the real characteristics of device [32]. After the de-embedding technique is applied, the measured results are shown as follows.

Measured S-parameter of π-diode_5_5 is compared with π-SCR_1_10 and π-SCR_2_5_5 in Fig. 3.27. Measured S-parameter of π-diode_15_15 is compared with π-SCR_1_30 and π-SCR_2_15_15 in Fig. 3.28. Measured S-parameter of π-diode_25_25 is compared with π-SCR_1_50 and π-SCR_2_25_25 in Fig. 3.29. Measured S-parameter at 10GHz is listed in Table 3.5.

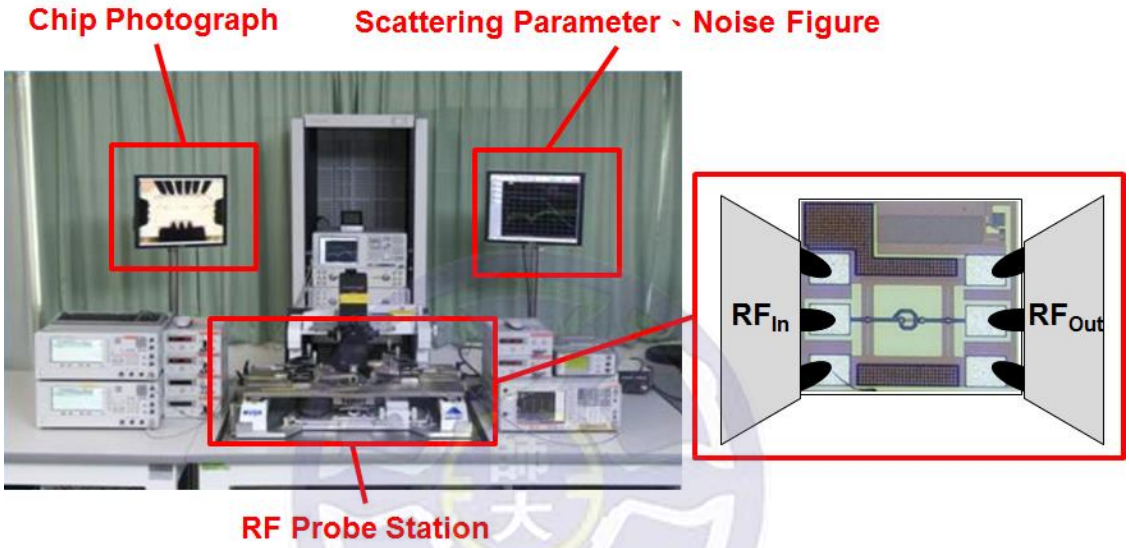
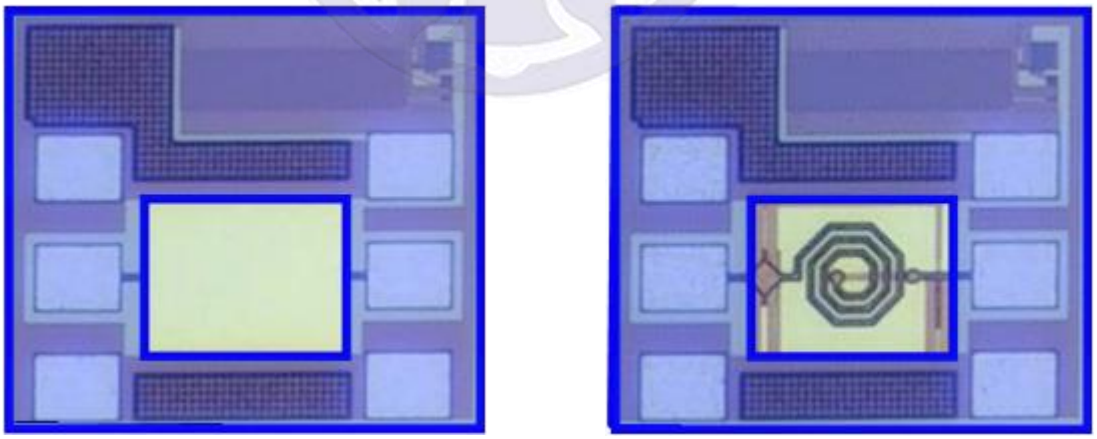
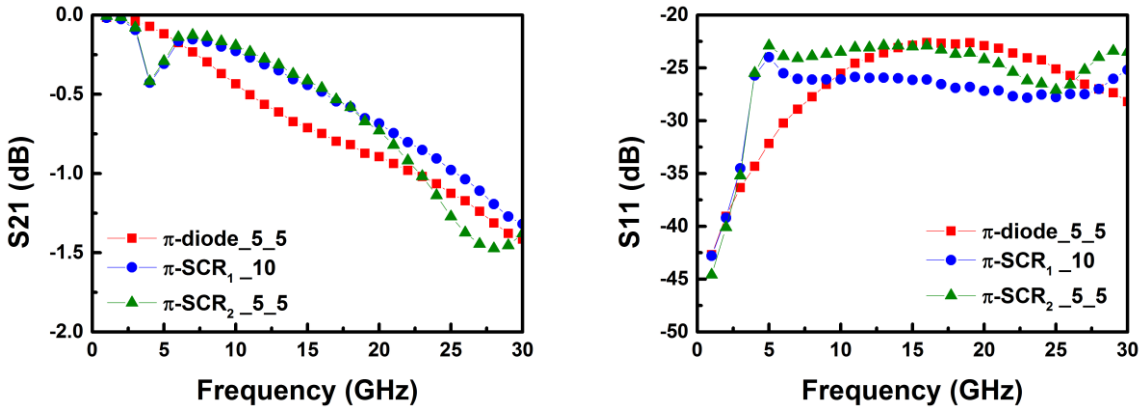


Fig. 3.25. The setup of high-frequency measurement system.



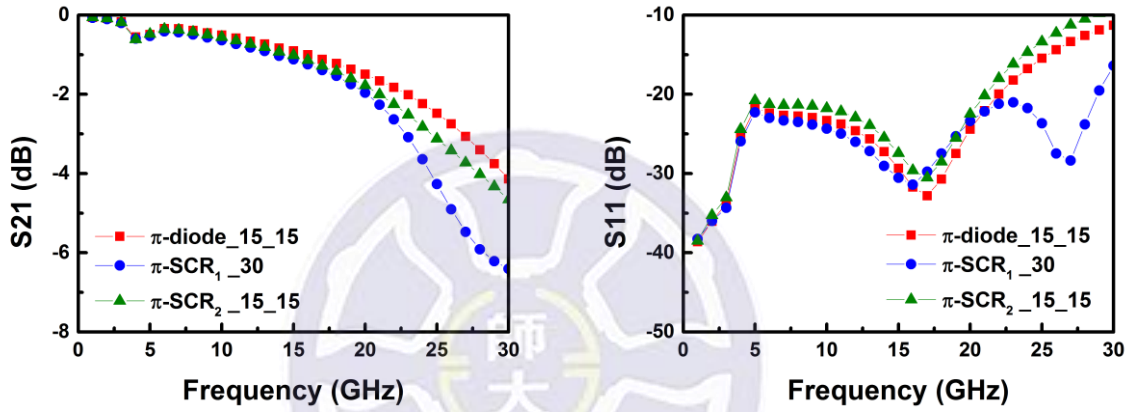
(a) (b)

Fig. 3.26. The photograph of (a) de-embedding pad and (b) test device.



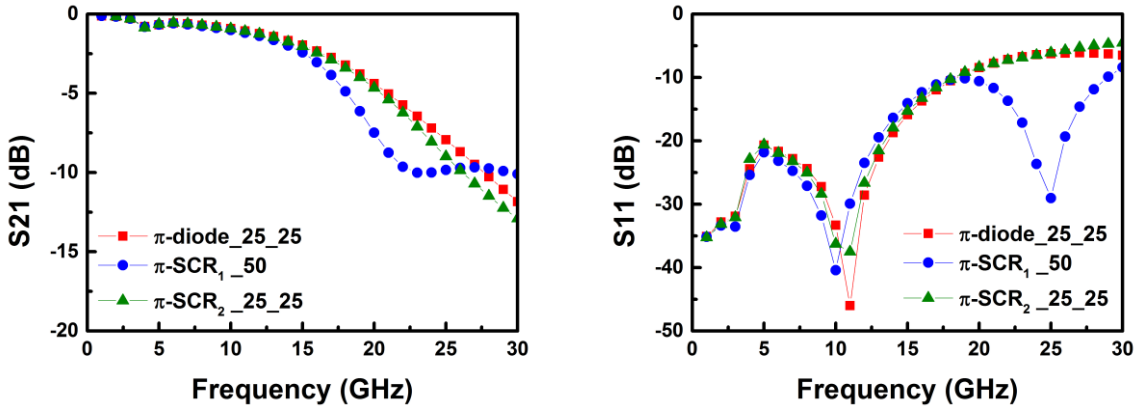
(a) (b)

Fig. 3.27. The measured S-parameter of π-diode_5_5, π-SCR1_10, and π-SCR2_5_5.



(a) (b)

Fig. 3.28. The measured S-parameter of π-diode_15_15, π-SCR1_30, and π-SCR2_15_15.



(a) (b)

Fig. 3.29. The measured S-parameter of π-diode_25_25, π-SCR1_50, and π-SCR2_25_25.

From the measurement results, the smaller devices such as π-diode_5_5, π-SCR_1_10, and π-SCR_2_5_5 show the better high-frequency performance. However, with the smallest device dimension, the ESD robustness is the worst. The S21 of π-diode_5_5, π-SCR_1_10, and π-SCR_2_5_5 are higher than -1dB from 0 to 20GHz. The high-frequency performance of test devices degraded as the size rises. The S21 of π-diode_15_15, π-SCR_1_30, and π-SCR_2_15_15 are higher than -1dB from 0 to 15GHz. The S21 of π-diode_25_25, π-SCR_1_50, and π-SCR_2_25_25 are higher than -1dB from 0 to 10GHz. The S21 of all the test device is higher than -1dB at 10GHz, and the S11 is lower than -20dB.

Compared to π-SCR_1, the SCR device and NS diode of π-SCR_2 are more equally divided into two stages. Another matching method leads to better high-frequency performance. The S21 of π-SCR_1_30 declines faster than π-SCR_2_15_15 and π-diode_15_15 about 20GHz. In addition, the S21 of π-SCR_1_50 declines faster than π-SCR_2_25_25 and π-diode_25_25 about 15GHz.

Table 3.5. Measured S-parameter at 10GHz

Cell Name	**S21 (dB) at 10GHz**	**S11 (dB) at 10GHz**
π-diode_5_5	-0.43	-25.51
π-diode_15_15	-0.5	-23.31
π-diode_25_25	-0.92	-33.31
π-SCR_1_10	-0.23	-26.09
π-SCR_1_30	-0.64	-24.35
π-SCR_1_50	-1.01	-40.41
π-SCR_2_5_5	-0.19	-23.48
π-SCR_2_15_15	-0.56	-21.77
π-SCR_2_25_25	-0.93	-36.28

3.5.2 TLP I-V Curves

The characteristics of ESD protection devices are obtained by the transmission-line-pulsing (TLP) system. TLP systems generates high-energy pulse to simulate the current of ESD events. A set of voltage and current value is recorded for one pulse. All the data form the TLP I-V curves [15]. TLP system used in this work is shown in Fig. 3.30.

Trigger voltage (V_{t1}), holding voltage (V_h), turn-on resistance (R_{on}), and the secondary breakdown current (I_{t2}) can be observed from TLP I-V curves. The criterion to determine the failure of device in TLP measurement is that the leakage current changes by 30%. The devices are measured under PS mode, PD mode, NS mode, and ND mode respectively. The It_2 of all the test devices are recorded in Table 3.6.

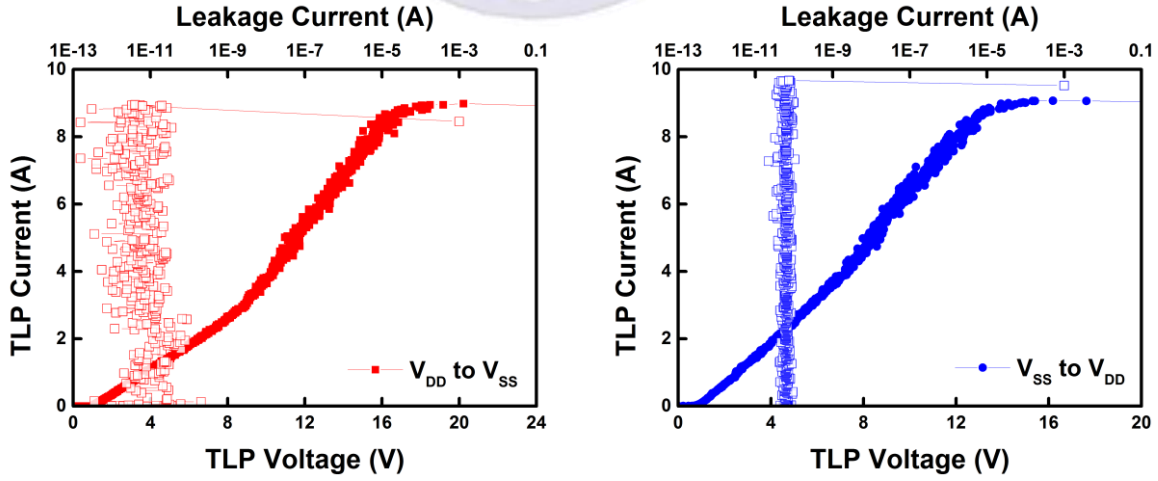
Fig. 3.30. Transmission-line pulsing (TLP) system.

(1) Power-Rail ESD Clamp Circuit

Power-rail ESD clamp circuit provides the ESD current path between V_{DD} and V_{SS}. It consists of a transient-detect circuit and a discharging device. The discharging path is formed by the NMOS device. The length is 0.36μm, the width is 50μm, and the multiple is 60.

During normal operation, the supply voltage rises in several microseconds. RC network has enough time to be charged to a high level. Through the inverter, the channel of NMOS is turned off. However, RC network is floating when ESD stress hits V_{DD}. The channel of NMOS is turned on by the RC network. The parasitic NPN is then turned on to discharge the ESD current as the voltage across it rises. The parasitic diode inside NMOS also provides the ESD current path from V_{SS} to V_{DD}.

As shown in Fig. 3.31, the TLP I-V curves of power-rail ESD clamp circuit used in traditional π-diode and proposed design is measured first. From V_{DD} to V_{SS}, the power-rail ESD clamp circuit is triggered at 1.9V, and the I_{t2} is 8.9A. From V_{SS} to V_{DD}, the power-rail ESD clamp circuit is triggered at 0.6V, and the I_{t2} is 9.7A.



(a) (b)

Fig. 3.31. TLP I-V curves of power-rail ESD clamp circuit (a) from V_{DD} to V_{SS} and (b) V_{SS} to V_{DD}.

(2) PS Mode

Traditional π-diode discharges ESD current of PS mode through the diodes placed from I/O pad to V_{DD} in series with power-rail ESD clamp circuit. Two types of π-SCR discharge ESD current of PS mode through the SCR device with the help of trigger diodes. The TLP I-V curve of π-diode_5_5 is compared with π-SCR_1_10 and π-SCR_2_5_5 in Fig. 3.32 (a). The TLP I-V curve of π-diode_15_15 is compared with π-SCR_1_30 and π-SCR_2_15_15 in Fig.3.32 (b). The TLP I-V curve of π-diode_25_25 is compared with π-SCR_1_50 and π-SCR_2_25_25 in Fig. 3.32 (c).

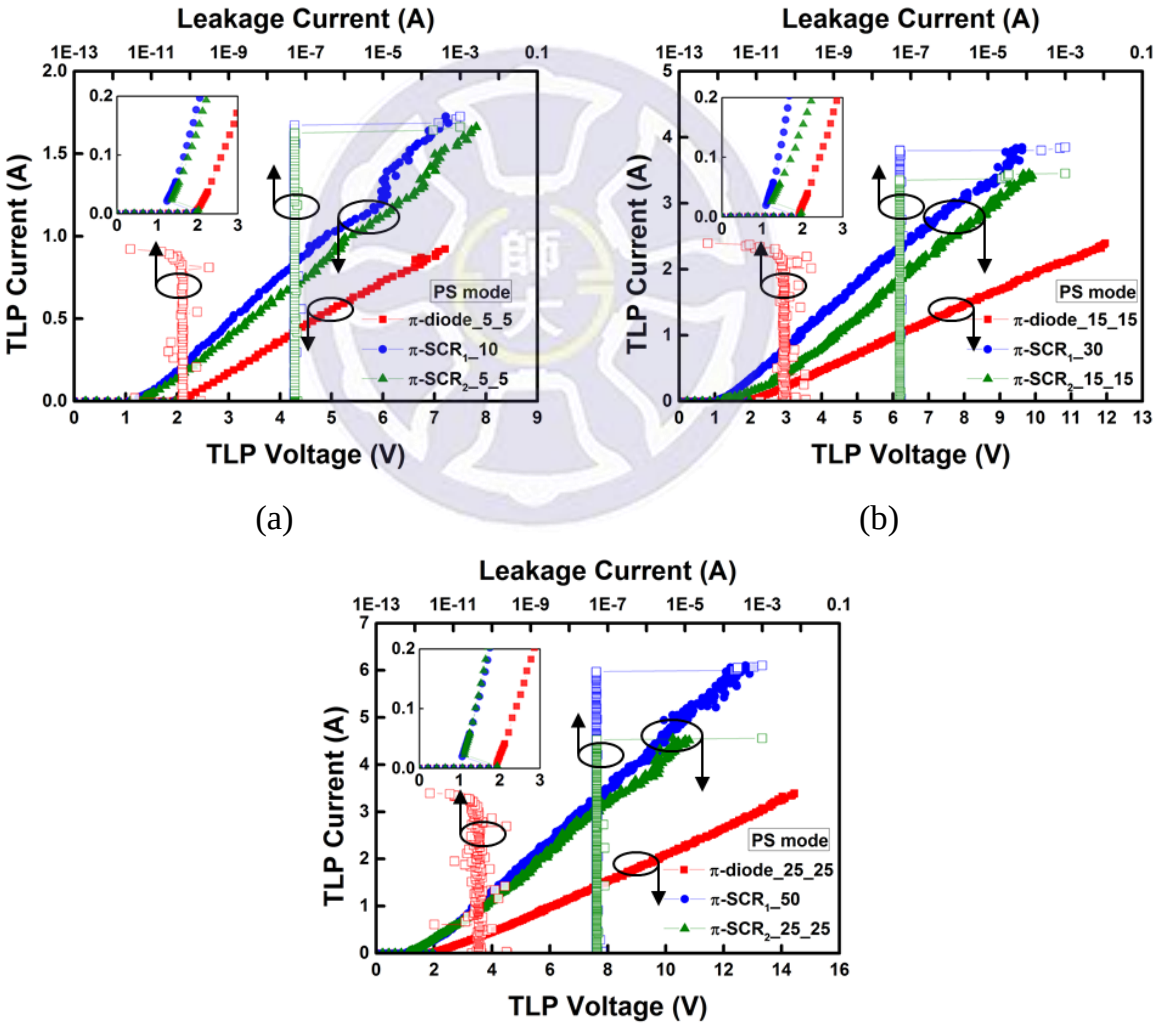


Fig. 3.32. TLP I-V curves of test devices under PS mode.

(3) PD Mode

The π-diode discharges ESD current of PD mode through the diodes placed from I/O pad to V_{DD}. Two types of π-SCR discharge ESD current of PD mode through the parasitic diode inside SCR. The TLP I-V curve of π-diode_5_5 is compared with π-SCR_1_10 and π-SCR_2_5_5 in Fig. 3.33 (a). The TLP I-V curve of π-diode_15_15 is compared with π-SCR_1_30 and π-SCR_2_15_15 in Fig. 3.33 (b). The TLP I-V curve of π-diode_25_25 is compared with π-SCR_1_50 and π-SCR_2_25_25 in Fig. 3.33 (c).

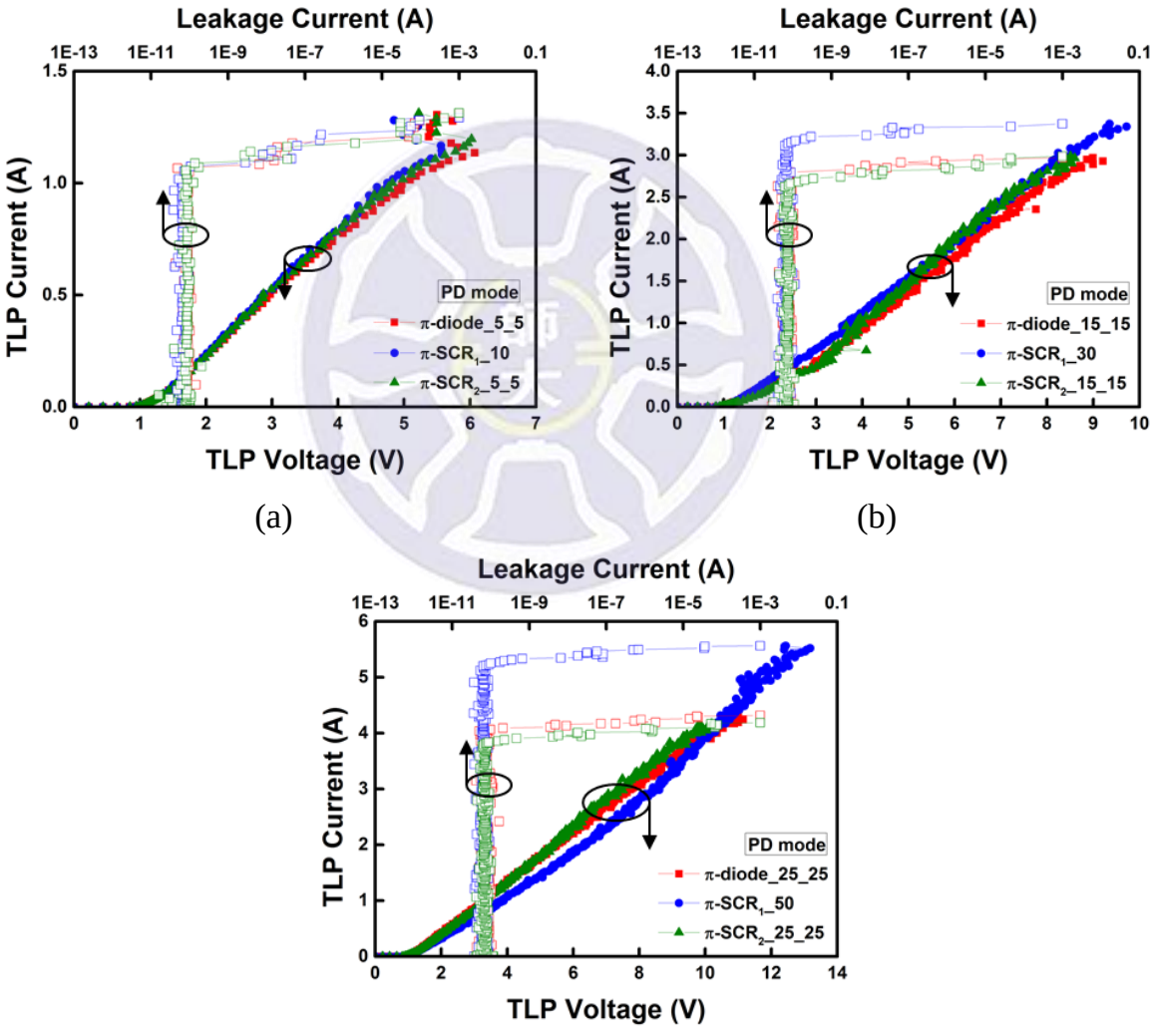
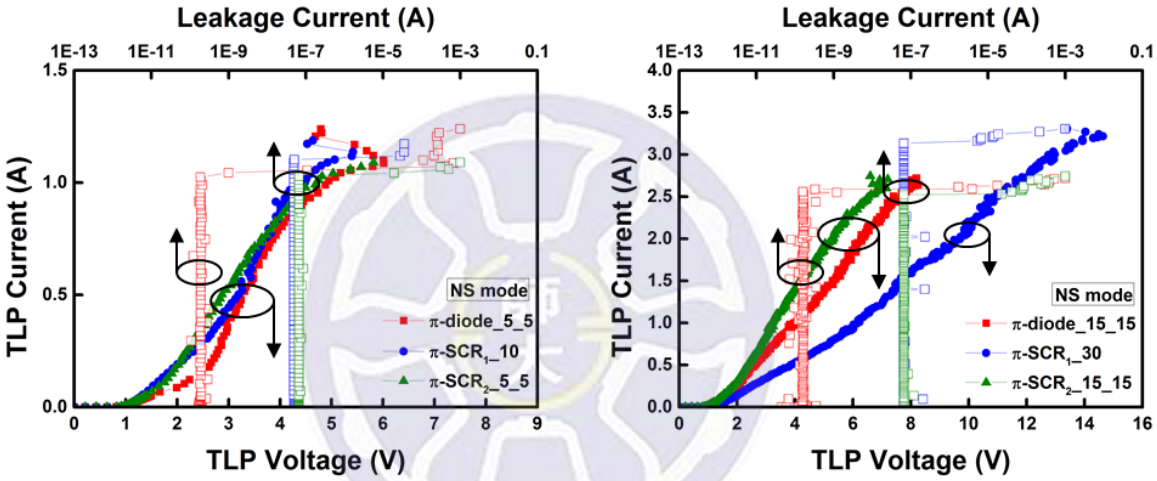


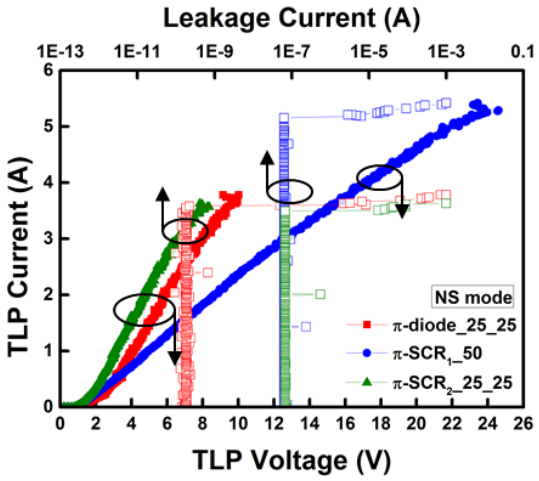
Fig. 3.33. TLP I-V curves of test devices under PD mode.

(4) NS Mode

The π-diode discharges ESD current of NS mode through the diodes placed from V_{SS} to I/O pad. Two types of π-SCR discharges ESD current of NS mode by the diodes placed from V_{SS} to I/O pad. The TLP I-V curve of π-diode_5_5 is compared with π-SCR_1_10 and π-SCR_2_5_5 in Fig. 3.34 (a). The TLP I-V curve of π-diode_15_15 is compared with π-SCR_1_30 and π-SCR_2_15_15 in Fig. 3.34 (b). The TLP I-V curve of π-diode_25_25 is compared with π-SCR_1_50 and π-SCR_2_25_25 in Fig. 3.34 (c).



(a) (b)

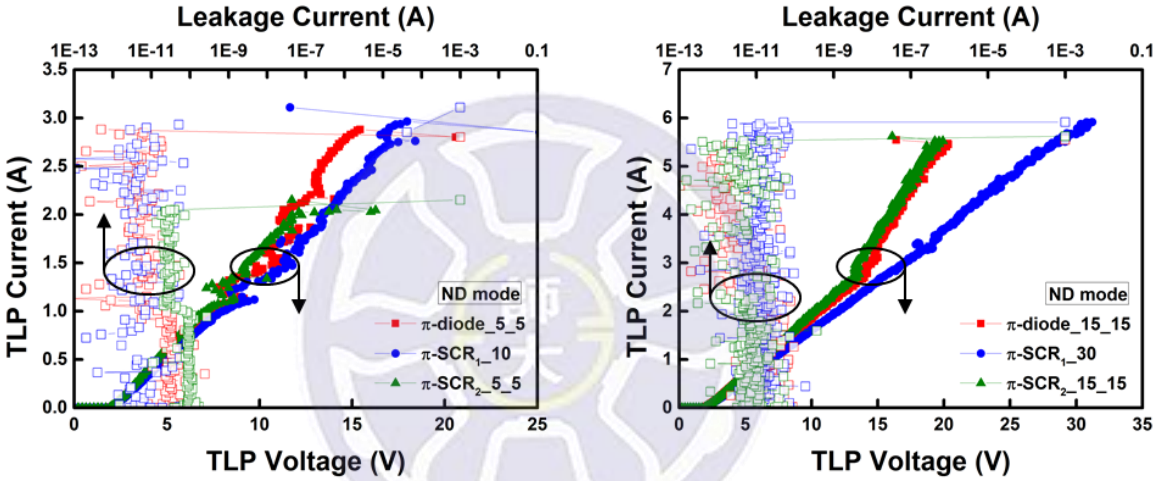


(c)

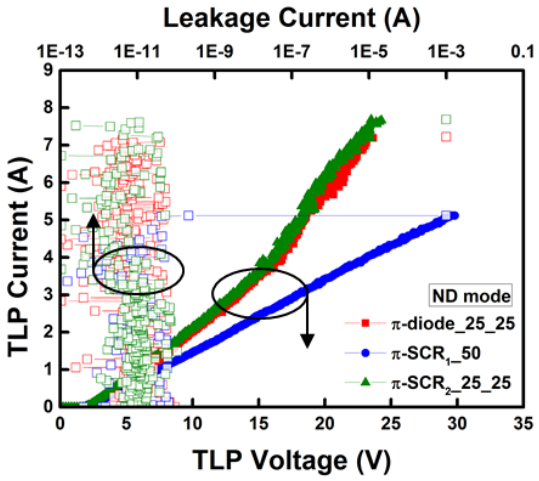
Fig. 3.34. TLP I-V curves of test devices under NS mode.

(5) ND Mode

The π-diode discharges ESD current under ND mode through the power-rail ESD clamp circuit and diodes placed from V_{SS} to I/O pad. Two types of π-SCR discharges ESD current under ND mode through the power-rail ESD clamp circuit and the diodes placed from V_{SS} to I/O pad. The TLP I-V curve of π-diode_5_5 is compared with π-SCR_1_10 and π-SCR_2_5_5 in Fig. 3.35 (a). The TLP I-V curve of π-diode_15_15 is compared with π-SCR_1_30 and π-SCR_2_15_15 in Fig. 3.35 (b). The TLP I-V curve of π-diode_25_25 is compared with π-SCR_1_50 and π-SCR_2_25_25 in Fig. 3.35 (c).



(a) (b)



(c)

Fig. 3.35. TLP I-V curves of test devices under ND mode.

Table 3.6. Measured I_{t2} results

Cell Name	I_{t2} (A)			
	PS mode	PD mode	NS mode	ND mode
π-diode_5_5	0.92	1.07	1.04	2.88
π-diode_15_15	2.39	2.8	2.59	5.43
π-diode_25_25	3.39	4.09	3.59	7.14
π-SCR_1_10	1.69	1.07	1.12	2.93
π-SCR_1_30	3.8	3.22	3.16	5.91
π-SCR_1_50	6	5.33	5.2	5.12
π-SCR_2_5_5	1.64	1.09	1.04	2.05
π-SCR_2_15_15	3.35	2.72	2.53	5.52
π-SCR_2_25_25	4.56	3.9	3.5	7.61

3.5.3 HBM Test

After measuring the TLP I-V curves, the secondary breakdown current (I_{t2}) is obtained. HBM tests are implemented to find out the ESD level of protection device. To determine the failure of device, the criteria is defined as the leakage current changes by 30%. As shown in Fig. 3.36, HBM test is implemented with HBM tester. The measurement results are listed in Table 3.7.

Fig. 3.36. HBM tester.

Table 3.7. HBM test results

Cell Name	HBM (kV)			
	PS mode	PD mode	NS mode	ND mode
π-diode_5_5	2	2	2	2
π-diode_15_15	5	5.5	3.5	4.5
π-diode_25_25	> 8	> 8	> 8	> 8
π-SCR_1_10	3.5	2	2	2
π-SCR_1_30	> 8	> 8	> 8	6
π-SCR_1_50	> 8	> 8	> 8	> 8
π-SCR_2_5_5	3.5	2.5	2	2
π-SCR_2_15_15	> 8	> 8	7.5	> 8
π-SCR_2_25_25	> 8	> 8	> 8	> 8

3.6 Comparison

The characteristics of protection device can be evaluated by the trigger voltage (V_{t1}), holding voltage (V_h), secondary breakdown current (I_{t2}), turn-on resistance (R_{on}), and the HBM level.

The measured data of all the test device are compared under PS mode as listed in Table 3.8. Traditional π-diode is triggered about 1.9V. V_{t1} decreases slightly with the larger size. Both π-SCR_1 and π-SCR_2 are triggered before 2V under PS mode. After snapback, V_h of them are about 1.2V. During conduction, R_{on} is about 3~5Ω.

Table 3.8. Comparison table under PS mode

Cell Name	PS mode				
	V_{t1} (V)	V_h (V)	I_{t2} (A)	R_{on} (Ω)	HBM (kV)
π-diode_5_5	1.93	2.17	0.92	2.6	2
π-diode_15_15	1.92	2.05	2.39	3.9	5
π-diode_25_25	1.91	2.01	3.39	2.9	> 8
π-SCR_1_10	1.95	1.27	1.69	2.3	3.5
π-SCR_1_30	1.91	1.13	3.8	3.4	> 8
π-SCR_1_50	1.9	1.1	6	2	> 8
π-SCR_2_5_5	1.98	1.37	1.64	2.3	3.5
π-SCR_2_15_15	1.96	1.24	3.35	4.2	> 8
π-SCR_2_25_25	1.95	1.13	4.56	1.7	> 8

*When the TLP current is more than 1mA, the voltage across the device is defined as trigger voltage (V_{t1}).

The discharging path of π-SCR_1 and π-SCR_2 under PD mode are through the parasitic diode inside SCR. The discharging path of π-SCR_2 under PD mode is almost the same as π-diode. Therefore, π-diode, π-SCR_1, and π-SCR_2 are triggered about 0.9V. The V_{t1} of all the test devices under PD mode decreases slightly with larger size.

The I_{t2} of the test device increases with the larger device dimension. There is a similar I_{t2} value for π-diode and π-SCR_2. π-SCR_1_50 has larger I_{t2} than π-diode_25_25 and π-SCR_2_25_25 in larger dimension. However, the R_{on} of π-SCR_2 is the lowest with the use of two devices in discharging path.

Table 3.9. Comparison table under PD mode

Cell Name	**PD mode**			
	V_{t1} (V)	**I_{t2} (A)**	**R_{on} (Ω)**	**HBM (kV)**
π-diode_5_5	0.87	1.07	4.04	2
π-diode_15_15	0.84	2.8	2.14	5.5
π-diode_25_25	0.83	4.09	2.34	> 8
π-SCR_1_10	0.87	1.07	3.89	2
π-SCR_1_30	0.84	3.22	2.41	> 8
π-SCR_1_50	0.83	5.33	2.14	> 8
π-SCR_2_5_5	0.87	1.09	4.04	2.5
π-SCR_2_15_15	0.84	2.72	1.84	> 8
π-SCR_2_25_25	0.82	3.9	1.97	> 8

*When the TLP current is more than 1mA, the voltage across the device is defined as trigger voltage (V_{t1}).

The discharging path of π-SCR_1 under NS mode are through NS diode in stage 2. The discharging path of π-SCR_2 under NS mode are through two stages of NS diodes. π-diode, π-SCR_1, and π-SCR_2 can be triggered about 0.8V. The V_{t1} of all the test devices under NS mode decreases slightly with larger size.

π-SCR_1 has the larger I_{t2} value than π-diode and π-SCR_2 under NS mode. However, the R_{on} of π-SCR_2 is the lowest with two stages of device in used.

Table 3.10. Comparison table under NS mode

Cell Name	**NS mode**			
	V_{t1} (V)	**I_{t2} (A)**	**R_{on} (Ω)**	**HBM (kV)**
π-diode_5_5	0.84	1.04	5.4	2
π-diode_15_15	0.81	2.59	3.6	3.5
π-diode_25_25	0.81	3.59	4.2	> 8
π-SCR_1_10	0.86	1.12	3.4	2
π-SCR_1_30	0.82	3.16	2.3	> 8
π-SCR_1_50	0.8	5.2	2.2	> 8
π-SCR_2_5_5	0.84	1.04	3.5	2
π-SCR_2_15_15	0.81	2.53	1.7	7.5
π-SCR_2_25_25	0.8	3.5	1.9	> 8

*When the TLP current is more than 1mA, the voltage across the device is defined as trigger voltage (V_{t1}).

With the use of power-rail ESD clamp circuit, the I_{t2} of all the test devices under ND mode are better than other mode. π-diode, π-SCR_1, and π-SCR_2 are triggered before 2V under ND mode. Among smaller devices, π-SCR_1_10 has the highest I_{t2} value. However, π-diode_25_25 and π-SCR_2_25_25 have higher I_{t2} and lower R_{on} than π-SCR_1_50 in larger device dimension.

Table 3.11. Comparison table under ND mode

Cell Name	**ND mode**			
	V_{t1} (V)	**I_{t2} (A)**	**R_{on} (Ω)**	**HBM (kV)**
π-diode_5_5	1.94	2.88	5.43	2
π-diode_15_15	1.91	5.43	3.98	4.5
π-diode_25_25	1.91	7.14	3.39	> 8
π-SCR_1_10	1.95	2.93	5.83	2
π-SCR_1_30	1.93	5.91	5.13	6
π-SCR_1_50	1.89	5.12	5.41	> 8
π-SCR_2_5_5	1.92	2.05	4.79	2
π-SCR_2_15_15	1.91	5.52	3.98	> 8
π-SCR_2_25_25	1.89	7.61	3.7	> 8

*When the TLP current is more than 1mA, the voltage across the device is defined as trigger voltage (V_{t1}).

3.7 Comparison with Traditional ESD Protection Device at High-Frequencies

Proposed π-model device is compared with other ESD protection devices applied at high frequencies as shown in Table 3.12. LTSCR and LASCR are designed to operate at specific frequency. DESD and proposed device can operate for a frequency band. In similar size, the S21 of proposed device is higher than -1dB at operating frequency. In addition, the HBM level of π-SCR_1_30 and π-SCR_2_15_15 are 6kV and 7.5kV.

Table 3.12. Comparison of ESD protection devices at high frequencies

ESD Protection Design	Process	Width of Device	ESD Robustness		High-Frequency Performance		
			I_{t2} (A)	HBM (kV)	Freq. (GHz)	S11 (dB)	S21 (dB)
LTSCR [23]	65nm CMOS	W_{SCR} =30μm	1.72	2.75	60	-24.6	-1.84
LASCR [24]	0.18μm CMOS	W_{SCR} =30μm	2.4	4	20~25	-15	-3
DESD [25]	0.25μm CMOS	4*W_{Diode} =20μm	No Provided	5.5	6	-12.5	-1.2
π-diode _15_15	0.18μm CMOS	2*W_{Diode} =30μm	2.39	3.5	10	-23.3	-0.5
π-SCR_1 _30	0.18μm CMOS	W_{SCR} =30μm	3.16	6	10	-24.4	-0.64
π-SCR_2 _15_15	0.18μm CMOS	2*W_{SCR} =30μm	2.53	7.5	10	-21.8	-0.56

3.8 Discussion

From the measurement results, the leakage current of proposed π-SCR1 and π-SCR2 are higher than traditional π-diode at 1.8V. However, the R_{on} of proposed π-SCR1 and π-SCR2 is smaller than traditional π-diode. It means that proposed devices are more suitable for advanced CMOS process. The leakage current versus bias of all the test devices are shown in Fig.3.37. With lower $V_{DD,}$ the leakage current of proposed device is almost the same as traditional design.

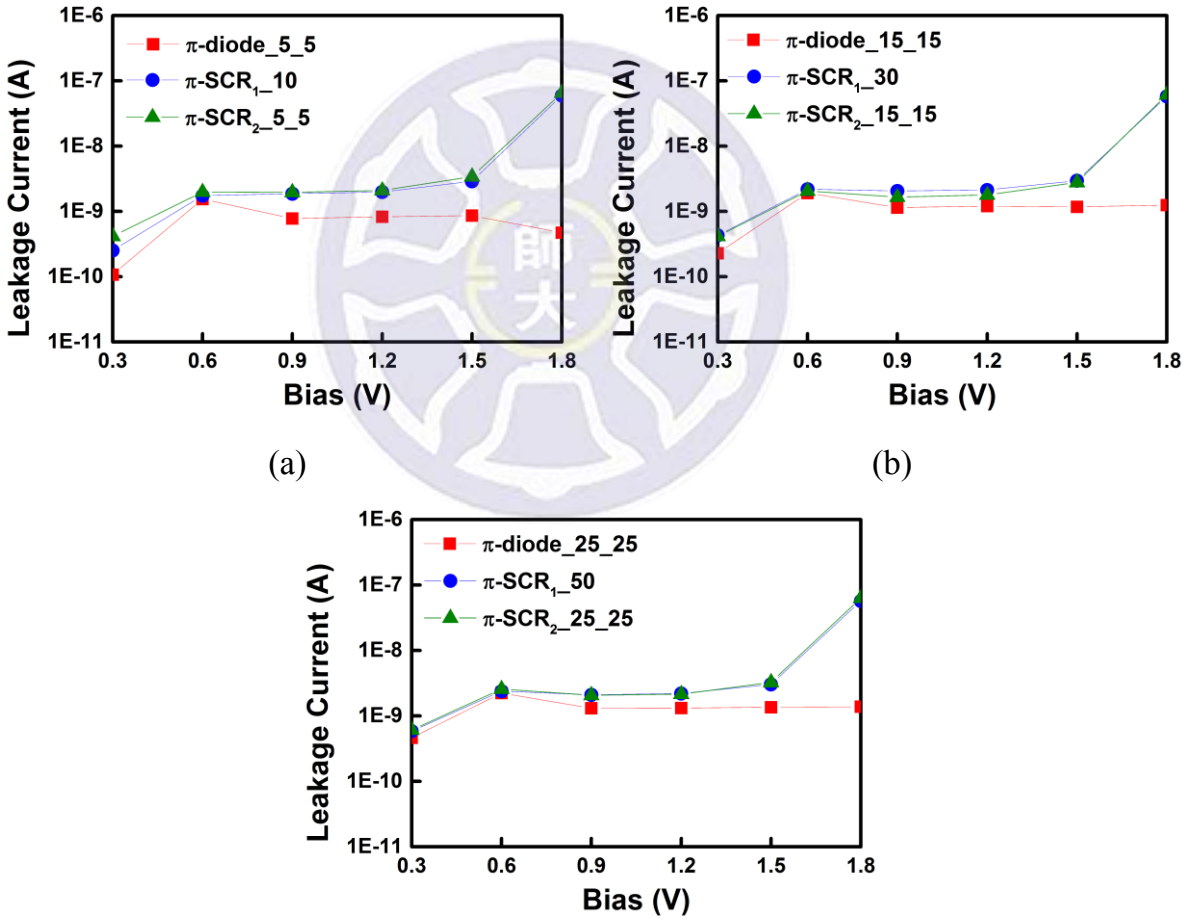


Fig. 3.37. Leakage current of all the test devices versus bias.

Proposed π-SCR_1 has only one device in each discharging mode. To improve it, the SCR device and NS diode are more equally divided into two stages in π-SCR_2. So π-SCR_2 has two discharging paths in each mode. The use of parallel paths for ESD current reduces the R_{on}. However, the decrease in resistance only show up in PD mode, NS mode, and ND mode. π-SCR_1 has little difference on the R_{on} of PS mode with π-SCR_2. Maybe it is because the trigger diodes are only at stage 2 in π-SCR_2. As for the high-frequency, the S21 of π-SCR_2 degrades slower than π-SCR_1. This matching method shows better performance.

3.9 Summary

Both proposed π-SCR and traditional π-diode are realized in silicon. From the S-parameter measurement results, the S21 of all the test device is higher than -1dB. In addition, the S11 is lower than -20dB. It can be used in high-frequency applications with less distorting. During TLP test, both π-SCR_1 and π-SCR_2 are triggered before 2V. The voltage across π-SCR holds at a low level after snapback. It means that the power dissipation of π-SCR is lower. Compared with π-diode, the R_{on} of π-SCR is smaller under PS mode. The smaller device (π-diode_5_5, π-SCR_1_10, and π-SCR_2_5_5) can reach at least 2kV ESD level. The larger device (π-diode_25_25, π-SCR_1_50, and π-SCR_2_25_25) can sustain more than 8kV HBM robustness.

In next chapter, the proposed design is added into K-band LNA to verify the capability of ESD protection.

Chapter 4

Realization of Proposed Design with K-Band LNA

4.1 Introduction

In recent years, the wireless communication, automotive electronics, and some related applications are noticed. As the usage of communication system rises, the transceiver system composed of transmitter and receiver is highly developed. Low-noise amplifier (LNA) plays an important role in the receiver system as shown in Fig. 4.1.

The signal received from antenna is interfered by noise. The radio-frequency (RF) system is sensitive to noise for signal processing. LNA is able to amplify signals and minimize the noise as well. The signal-to-noise ratio (SNR) is boosted by the use of LNA. Therefore, the knowledge about noise is necessary for designing it.

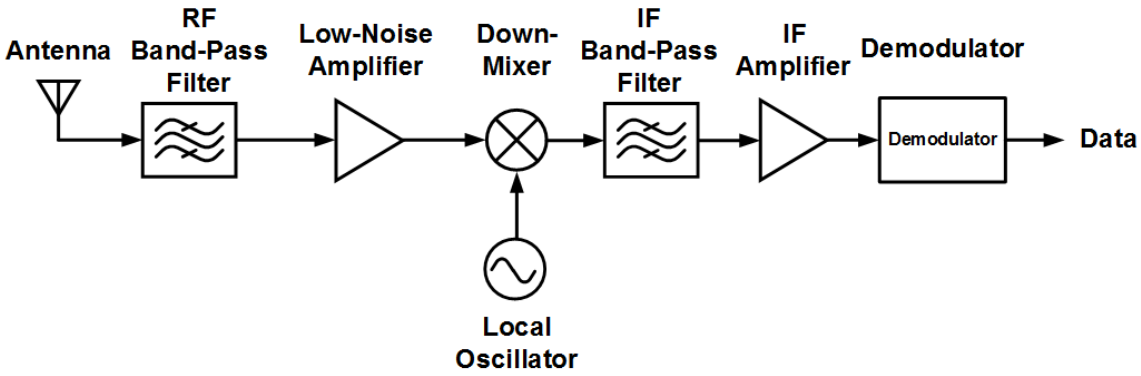


Fig. 4.1. The architecture of receiver system.

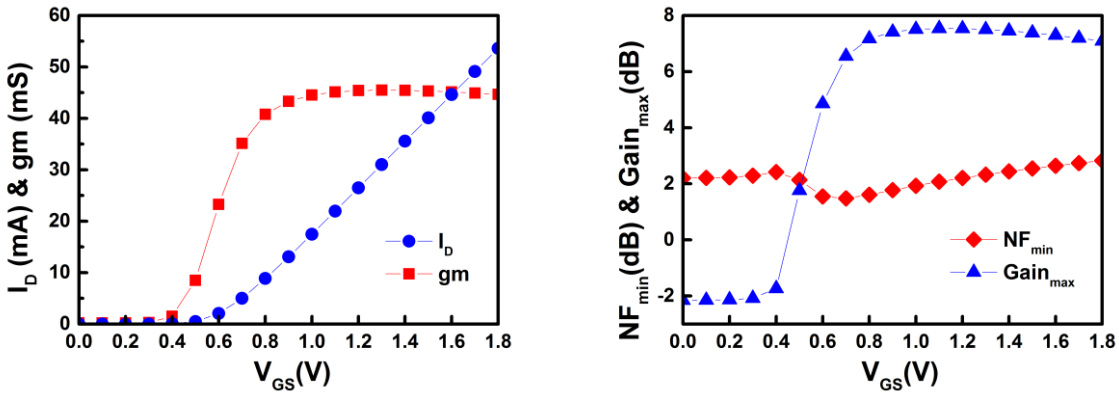
4.2 Design Steps of LNA

In order to reduce the noise figure, the amplifier is implemented with common-source configuration. The cascade LNA has less power consumption. Therefore, the two-stage cascade configuration is adopted to design the K-band LNA [33].

The gate bias of transistor (V_{GS}) is determined for appropriate transconductance value (gm) and drain current (I_D). Besides, the minimum noise figure (NF_{min}) and maximum gain ($Gain_{max}$) of amplifier are considered. The transconductance is gradually saturated when the gate bias is 0.8V as shown in Fig. 4.2 (a). The maximum gain is saturated and the minimum noise figure is in the acceptable range as the gate bias is 0.8V as shown in Fig. 4.2 (b). To lower the power consumption, the supply voltage of amplifier is set at 1.2V.

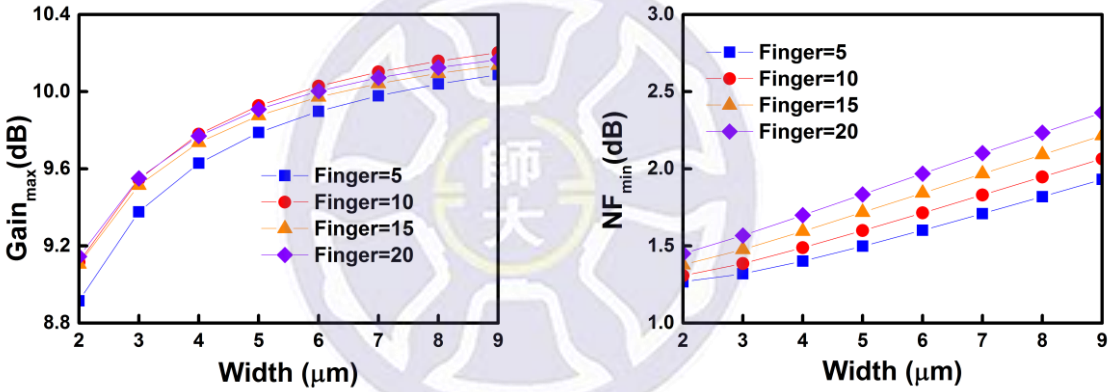
The size of transistor is decided by the channel length, finger width, and the amount of fingers. The channel length is fixed at 0.18μm to achieve the optimal driving force in a 0.18μm CMOS process. The maximum gain of amplifier is increased for larger width, but it is saturated with the rise in width as shown in Fig. 4.3 (a). In addition, the minimum noise figure becomes larger with larger width as shown in Fig. 4.3 (b). Therefore, the width is set at 6μm to achieve enough gain and lower noise figure. The noise figure rises with more fingers. The gain reaches the highest value as the number of fingers is 10. The transistors in LNA is realized with 10 fingers to achieve the highest gain in the acceptable range of noise figure.

The conjugate matching point is far away from the NF_{min} point on smith chart at high frequencies. Moving the conjugate matching point towards the NF_{min} point leads to decreased gain. It is harmful for the normal operating characteristics of LNA. The inductor in source terminal is designed to solve it. With the use of source degeneration inductor, the noise figure is reduced without dropping the gain of LNA.



(a) (b)

Fig. 4.2. (a) The plot of gm and I_D vs. V_{GS} and (b) the plot of NF_{min} and $Gain_{max}$ vs. V_{GS}.



(a) (b)

Fig. 4.3. (a) The plot of $Gain_{max}$ vs. finger width with different fingers and (b) the plot of NF_{min} vs. finger width with different fingers.

The maximum gain with different inductance value is shown in Fig. 4.4. There is a turning point of maximum gain with the use of source degeneration inductor. The turning point appeared at lower frequencies with larger inductance value. For the applications of K-band, the inductance value is designed to be 60~90pH. Therefore, the conjugate matching point is moved towards NF_{min} without losing gain.

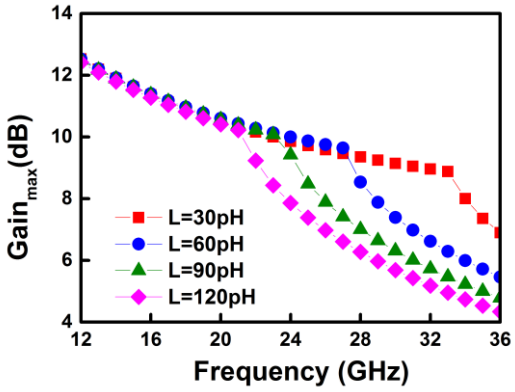


Fig. 4.4. The maximum gain with different degeneration inductor.

The architecture of two-stage cascade LNA is shown in Fig. 4.5. The matching network is necessary for input stage, stage-to-stage, and output stage. Each matching network has different functions. Noise match is implemented for input terminal to reduce the noise figure. The noise figure of following stage can be minimized due to good matching method for input stage. The output stage and stage-to-stage are adopted conjugate match to provide higher gain.

In general, the input matching network is designed at first. The input matching network of proposed LNA is shown in Fig. 4.6 (a). The capability of input matching network is to match the impedance point from 50Ω to NF_{min}. The use of source degeneration inductor (L_d) moves the impedance point toward NF_{min} slightly. With a shunt inductor (L_{i1}) and a series inductor (L_{i2}), the impedance is more close to NF_{min}.

The stage-to-stage matching network is shown in Fig. 4.6 (b). The input return loss (S11) of second stage has to be conjugate matched with output return loss (S22) of first stage. With the help of a shunt inductor (L_{SS}), the higher gain of amplifier can be delivered to next stage.

Other than stage-to-stage, the output stage is required to do the conjugate matching. The output return loss of second stage (S22) has to be conjugate with 50Ω. The output matching network is shown in Fig. 4.7 (a). A series inductor (L_{O2}) and a shunt inductor

(L_{O1}) are used to obtain the maximum gain. Bypass circuit is equipped to filter the high-frequency noise as shown in Fig. 4.7 (b).

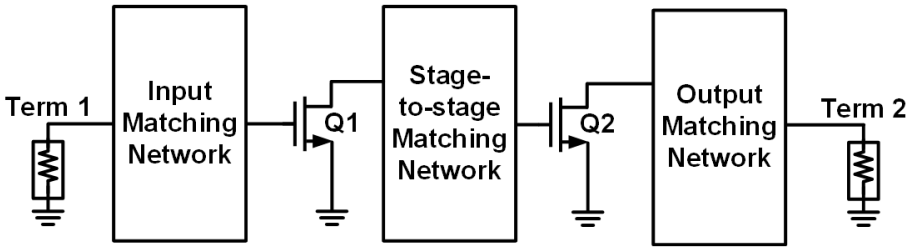
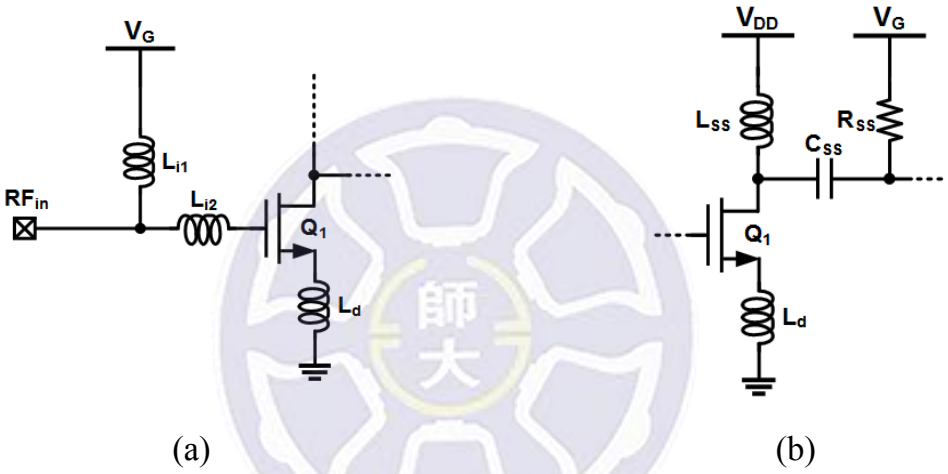
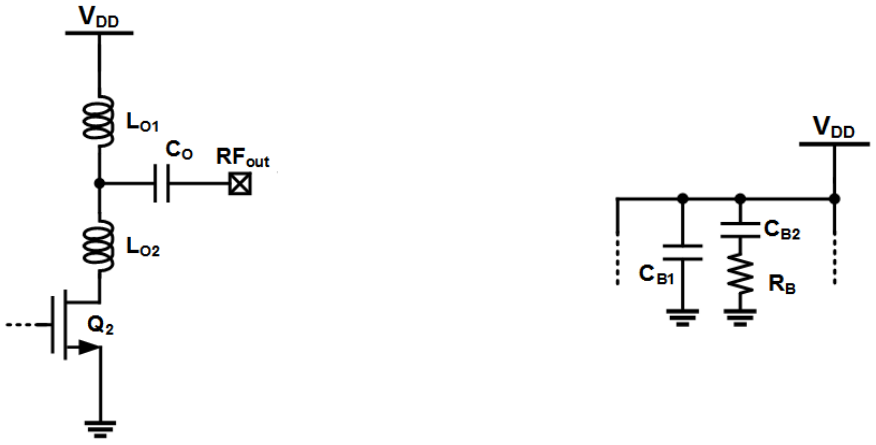


Fig. 4.5. Two-stage cascade LNA with matching network.



(a) (b)

Fig. 4.6. (a) Input and (b) stage-to-stage matching network.



(a) (b)

Fig. 4.7. (a) Output matching network and (b) bypass circuit.

4.3 Simulation Results of LNA

LNA circuits are equipped with traditional π-diode_5_5 and proposed π-SCR$_1$_10 to verify the capability of ESD protection. Advanced Design System (ADS) is used to simulate the S-parameter and noise figure of all the test circuits. SONNET electromagnetic (EM) is also used to do the electromagnetic simulation of inductor and metal routing.

4.3.1 LNA

The architecture of LNA is presented in Fig. 4.8. It is a two-stage common-source amplifier. The maximum voltage (V_{DD}) is 1.2V, and the bias voltage applied to gate (V_G) is 0.8V.

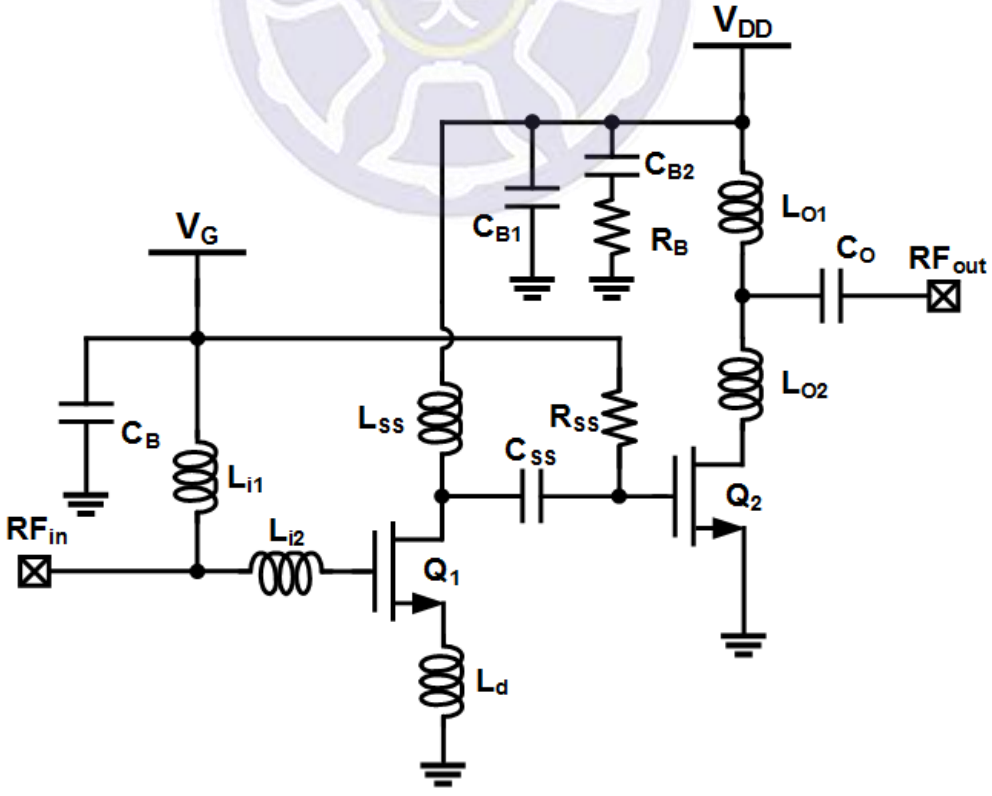


Fig. 4.8. The architecture of LNA.

As shown in Fig. 4.9, simulated S21 is 12.3dB, and S11 is -7.1dB at 22GHz. As shown in Fig. 4.10 (a), simulated noise figure of LNA is 7.1dB at 22GHz. In addition, LNA is stable for that K is greater than 1 as shown in Fig. 4.10 (b). Layout view of LNA is depicted in Fig. 4.11.

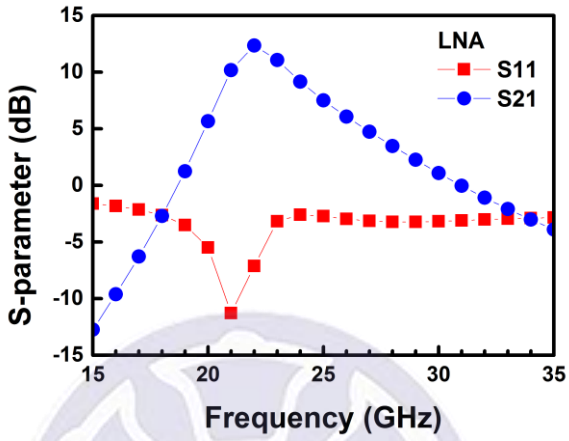
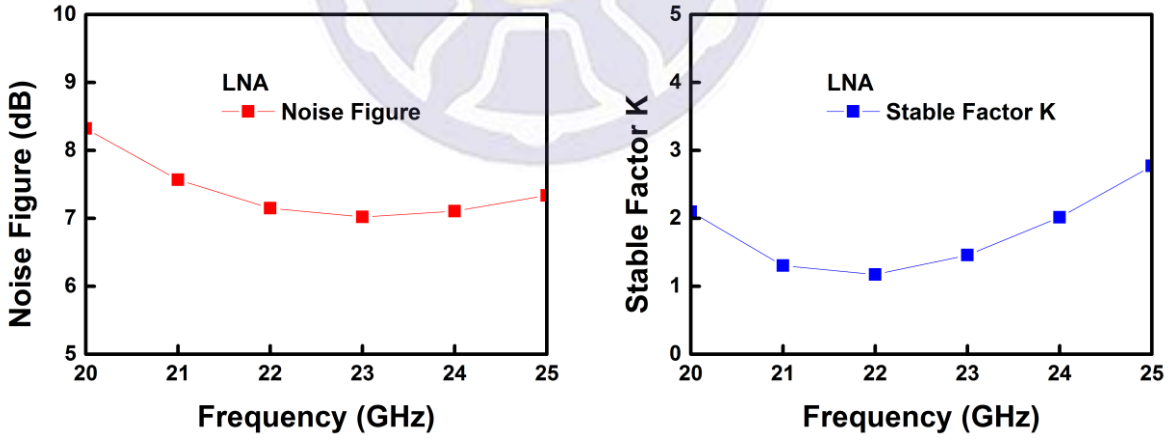


Fig. 4.9. Simulated S-parameter of LNA.



(a) (b)

Fig. 4.10. Simulated (a) noise figure and (b) stable factor K of LNA.

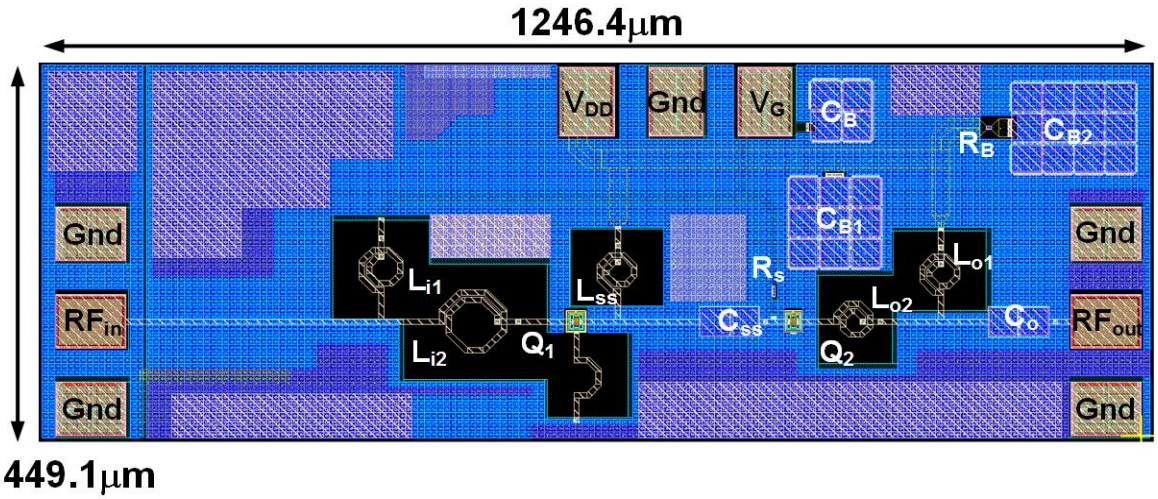


Fig. 4.11. Layout view of LNA.

4.3.2 LNA with Traditional π-Diode_5_5

The architecture of LNA with π-diode_5_5 is presented in Fig. 4.12. Compared to LNA, π-diode_5_5 and power-rail ESD clamp circuit are added into LNA. The length is 0.36μm, the width is 50μm, and the multiple of the NMOS in power-rail ESD clamp circuit is 60. In addition, the gate-grounded NMOS is also added as a protection element to discharge the ESD current from V_G pad. The length is 0.36μm, the width is 30μm, and the multiple of the protection element is 10.

As shown in Fig. 4.13, simulated S21 is 12.6dB, and S11 is -9.7dB at 22GHz. As shown in Fig. 4.14 (a), simulated noise figure of LNA with π-diode_5_5 is 6.6dB at 22GHz. In addition, LNA with π-diode_5_5 is stable for that K is greater than 1 as shown in Fig. 4.14 (b). Layout view of LNA with π-diode_5_5 is depicted in Fig. 4.15.

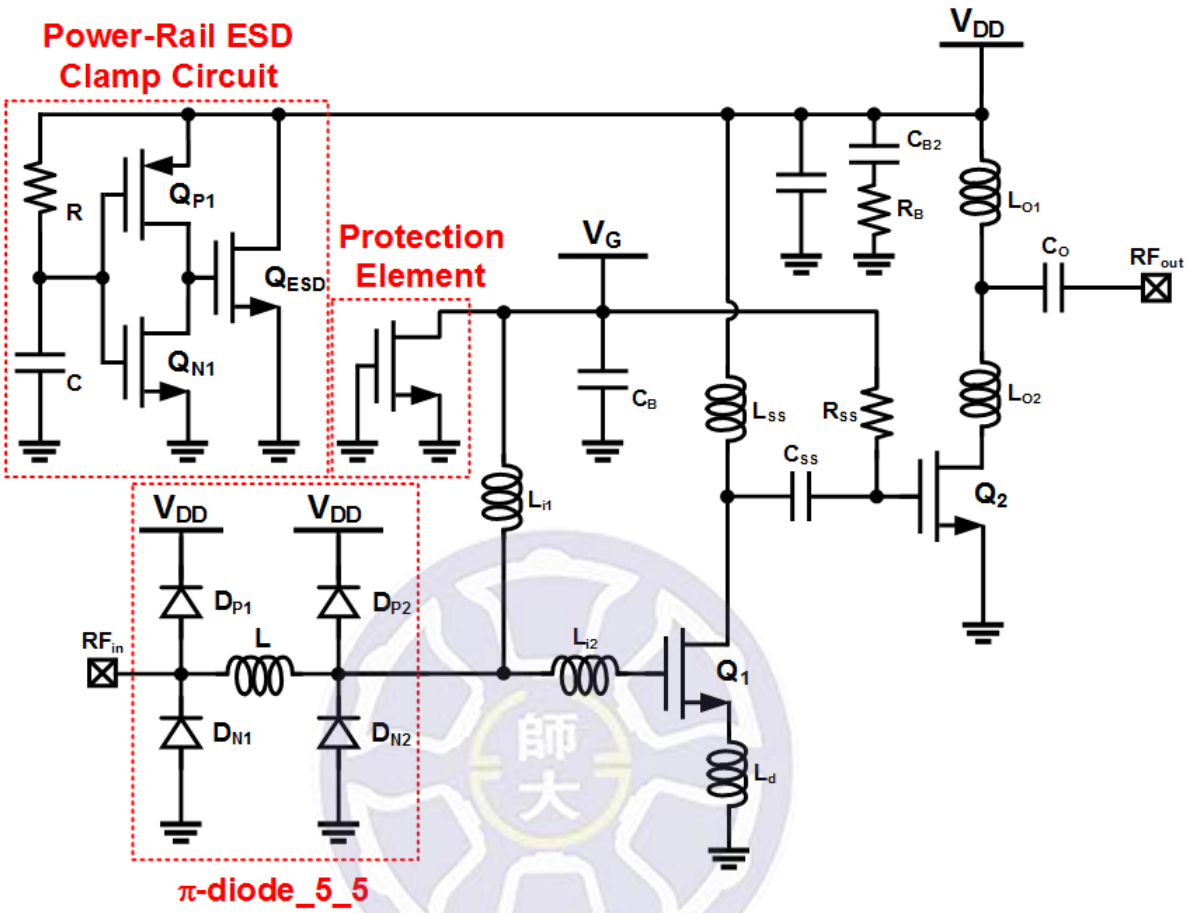


Fig. 4.12. The architecture of LNA with π-diode_5_5.

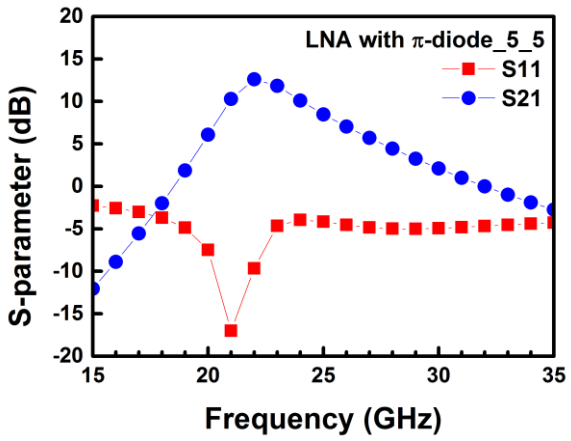
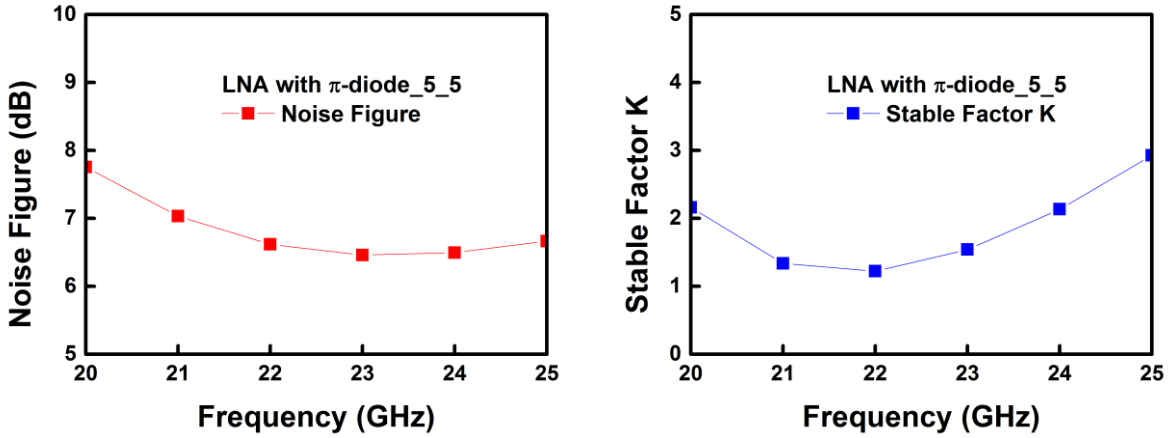


Fig. 4.13. Simulated S-parameter of LNA with π-diode_5_5.



(a) (b)

Fig. 4.14. Simulated (a) noise figure and (b) stable factor K of LNA with π-diode_5_5.

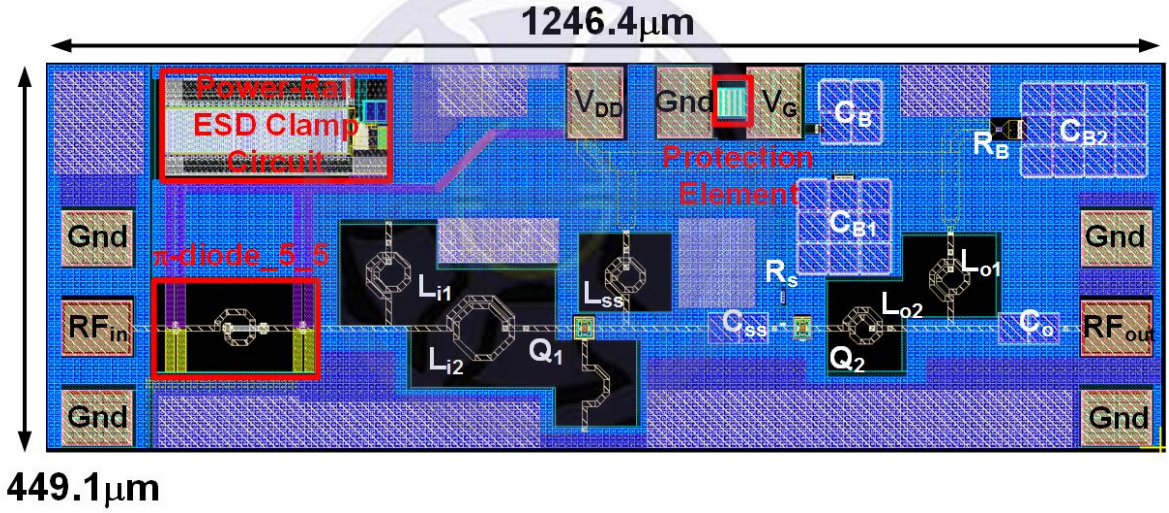


Fig. 4.15. Layout view of LNA with π-diode_5_5.

4.3.3 LNA with Proposed π-SCR$_1$_10

The architecture of LNA with π-SCR$_1$_10 is presented in Fig. 4.16. Compared to LNA, π-SCR$_1$_10 and power-rail ESD clamp circuit are added into LNA. The length is 0.36μm, the width is 50μm, and the multiple of the NMOS in power-rail ESD clamp circuit is 60. In addition, the gate-grounded NMOS is also added as a protection element to discharge the ESD current from V_G pad. The length is 0.36μm, the width is 30μm, and the multiple of the protection element is 10.

As shown in Fig. 4.17, simulated S21 is 12.6dB, and S11 is -9.7dB at 22GHz. As shown in Fig. 4.18 (a), simulated noise figure of LNA with π-SCR$_1$_10 is 6.6dB at 22GHz. In addition, LNA with π-SCR$_1$_10 is stable for that K is greater than 1 as shown as Fig. 4.18 (b). Layout view of LNA with π-SCR$_1$_10 is depicted in Fig. 4.19.

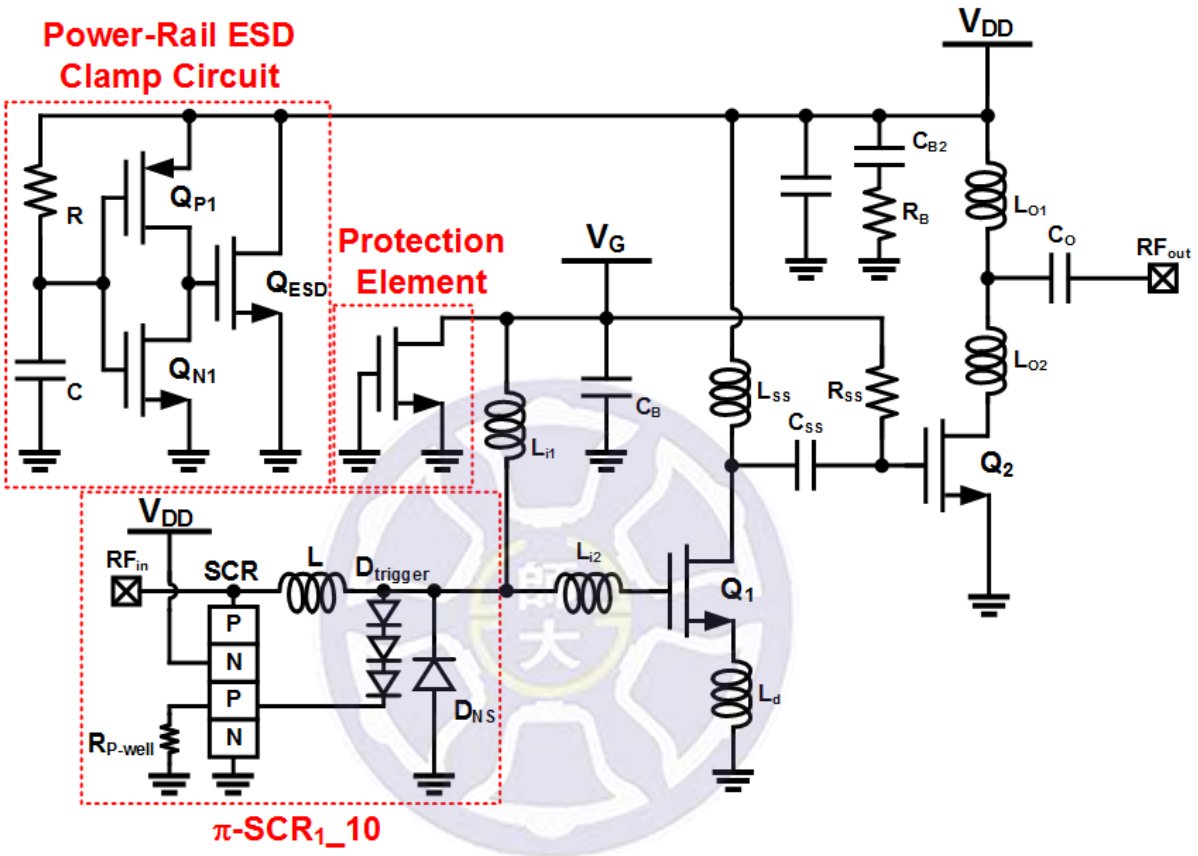


Fig. 4.16. The architecture of LNA with π-SCR$_1$_10.

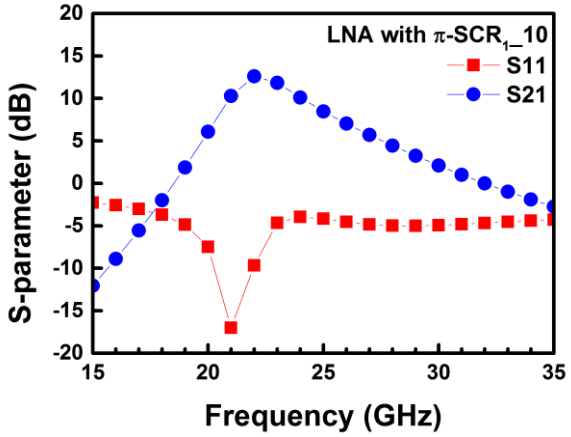
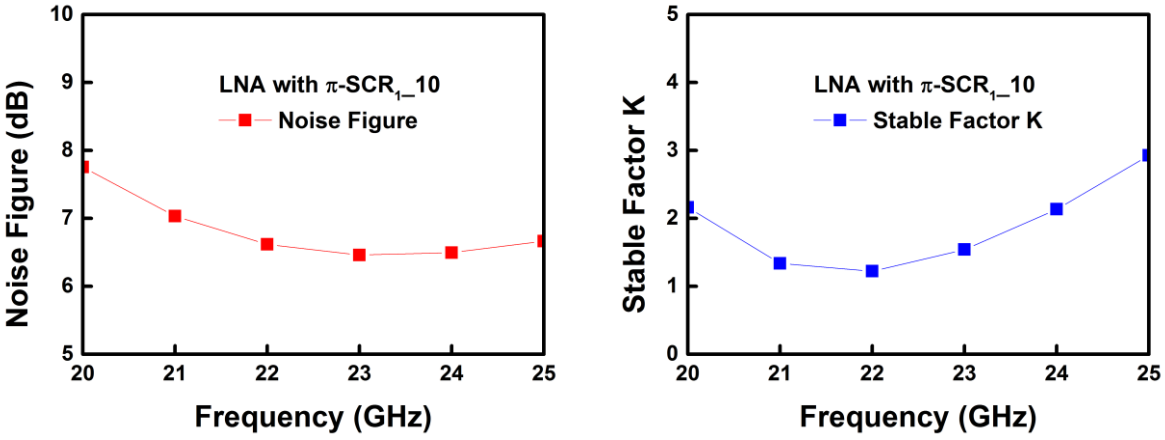


Fig. 4.17. Simulated S-parameter of LNA with π-SCR$_1$_10.



(a) (b)

Fig. 4.18. Simulated (a) noise figure and (b) stable factor K of LNA with π-SCR1_10.

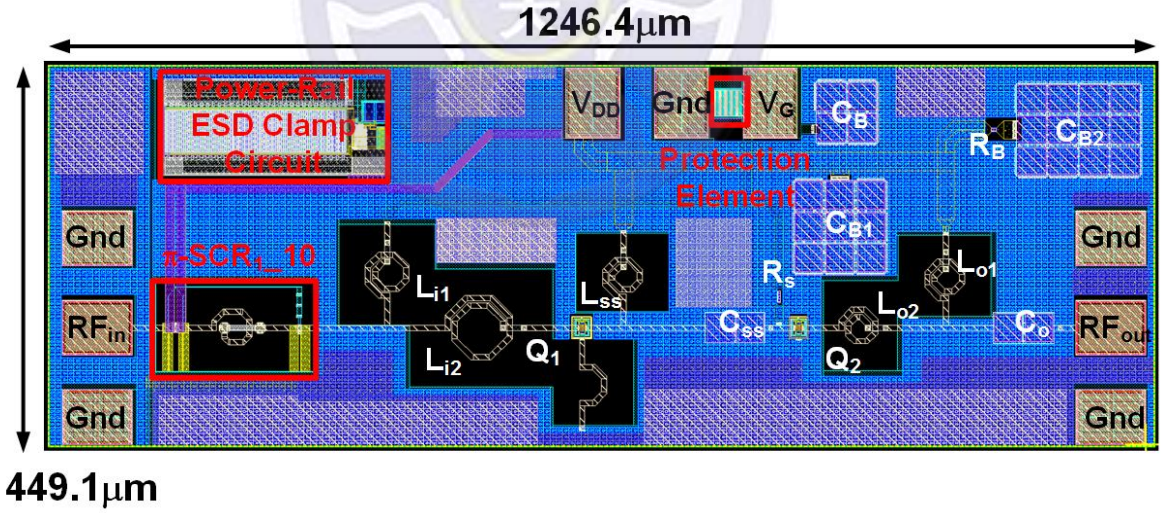


Fig. 4.19. Layout view of LNA with π-SCR1_10.

4.4 Measurement Results of LNA

Three LNA circuits are fabricated in 0.18μm CMOS process. One is without protection, another is equipped with π-diode_5_5, and the other is with π-SCR_1_10. The photograph is shown in Fig. 4.20. The width is 1246μm, and the length is 1298μm. S-parameter and noise figure are measured with RFIC parameter measurement system on 2-port GSG probe station. The voltage of power supply (V_{DD}) is 1.2V, and the gate bias (V_G) is 0.8V. HBM tests are also implemented to find out the ESD robustness. The measurement results are introduced in following section.

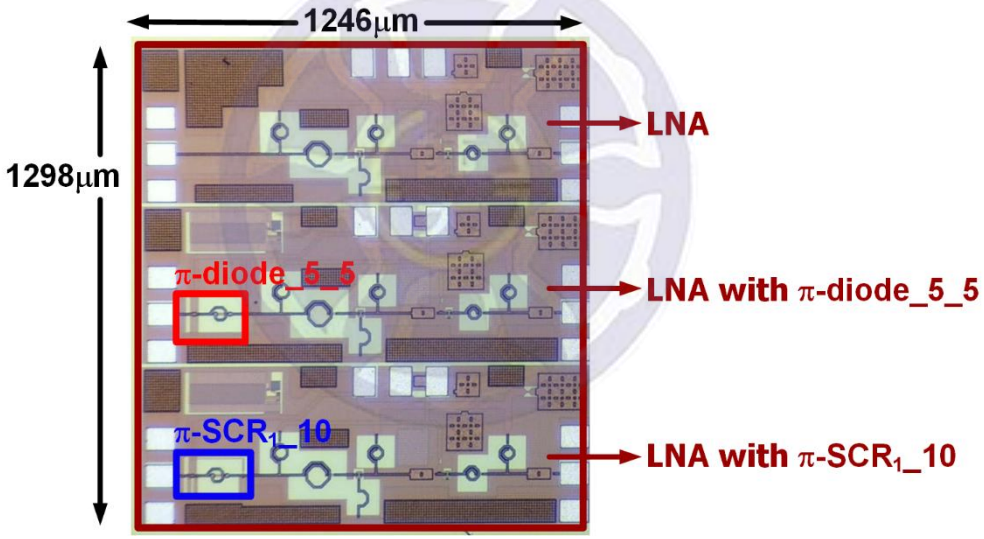


Fig. 4.20. The chip photograph of test LNA circuits.

4.4.1 LNA

The photograph is shown in Fig. 4.21. The width and the length of LNA circuit are 1246.4μm and 449.1μm, respectively.

As shown in Fig. 4.22 (a), measured S21 is 7.4dB, and S11 is -6.1dB at 22GHz. As shown in Fig. 4.22 (b), measured noise figure of LNA is 6dB at 22GHz.

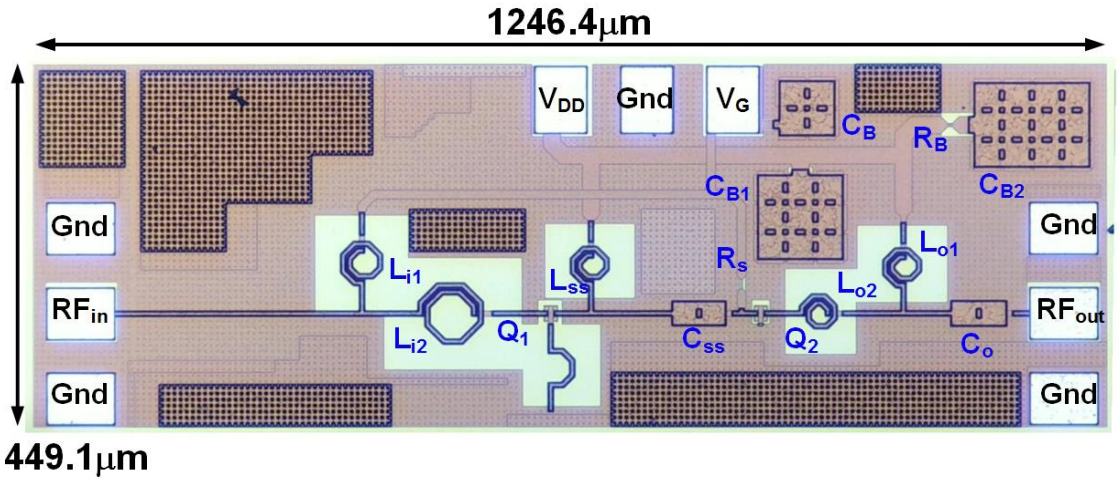
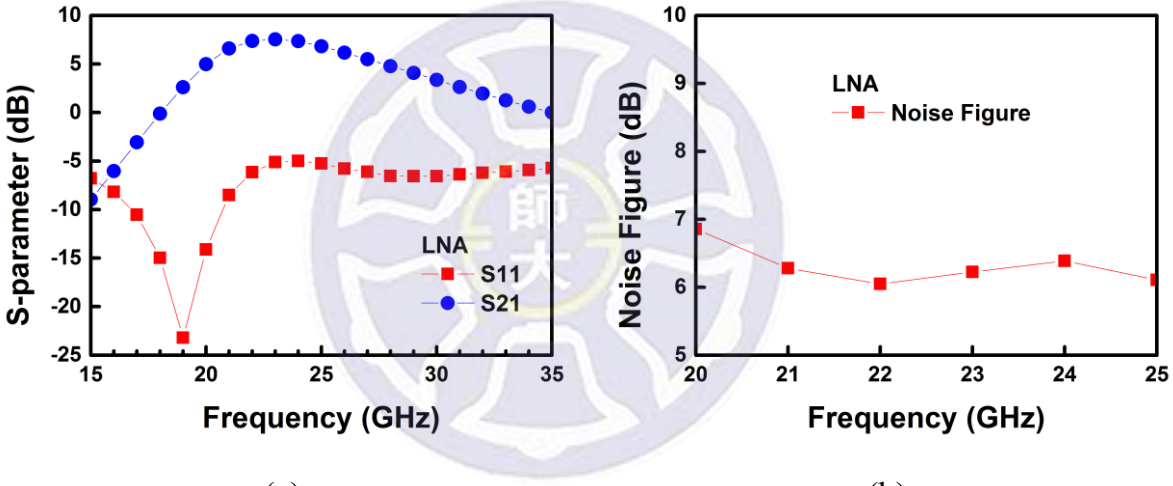


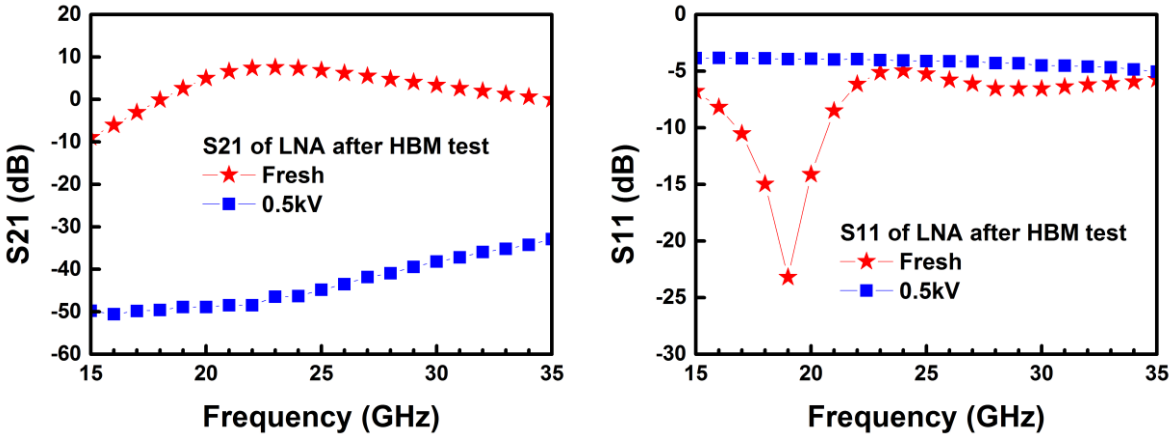
Fig. 4.21. Photograph of LNA.



(a) (b)

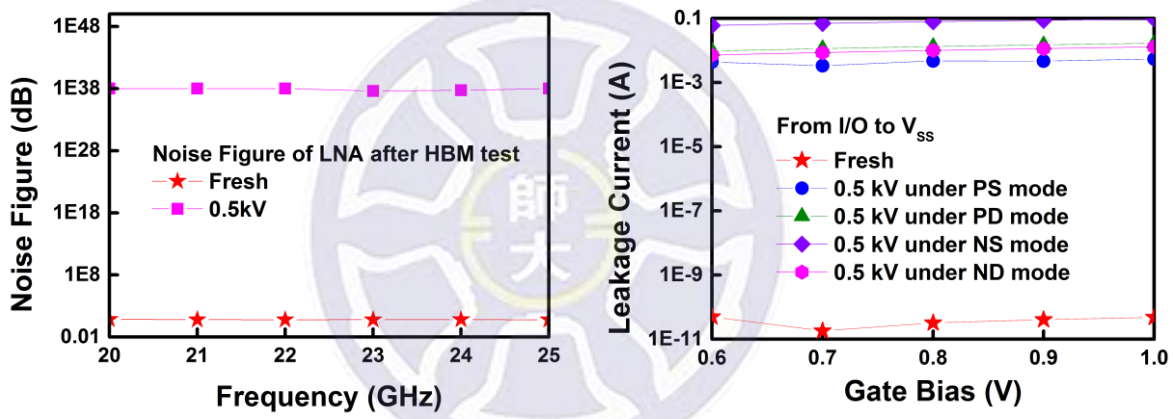
Fig. 4.22. Measured (a) S-parameter and (b) noise figure of LNA.

The ESD robustness of LNA can be learned by the HBM tests. After 0.5kV HBM test, S21 and S11 are both distorted as plotted in Fig. 4.23 (a) and Fig. 4.23 (b). In addition, the noise figure and leakage current rise sharply as shown in Fig. 4.24 (a) and Fig. 4.24 (b). It means that LNA circuit is damaged by ESD stress without any protection device after 0.5kV HBM test.



(a) (b)

Fig. 4.23. Measured (a) S21 and (b) S11 of LNA after HBM test.



(a) (b)

Fig. 4.24. Measured (a) noise figure and (b) leakage current of LNA after HBM test.

4.4.2 LNA with ESD Protection Circuit

Both traditional π-diode_5_5 and proposed π-SCR$_1$_10 are added into LNA circuits. The photograph of LNA with π-diode_5_5 is presented in Fig. 4.25, and the photograph of LNA with π-SCR$_1$_10 is presented in Fig. 4.26. The width and the length of LNA circuits are 1246.4μm and 449.1μm, respectively.

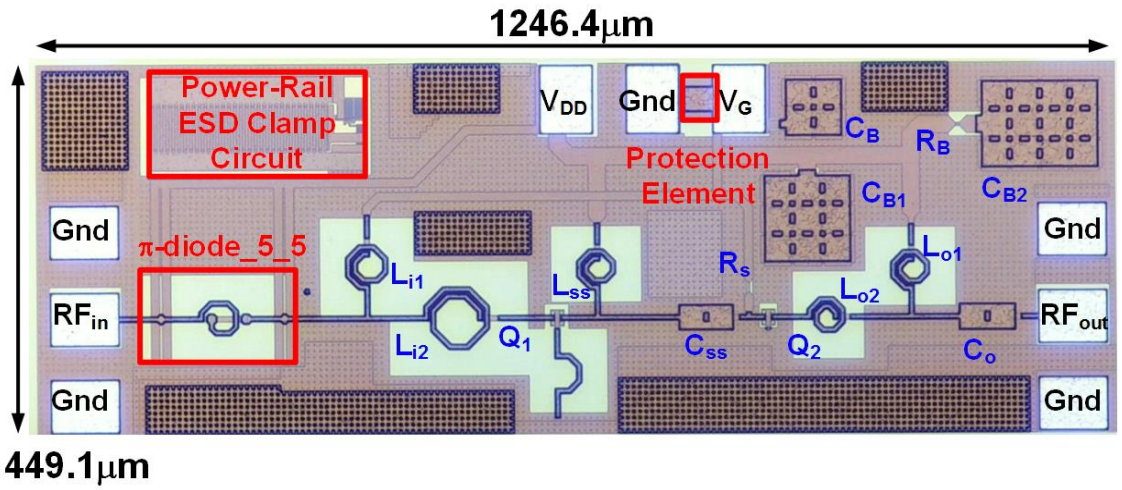


Fig. 4.25. Photograph of LNA with π-diode_5_5.

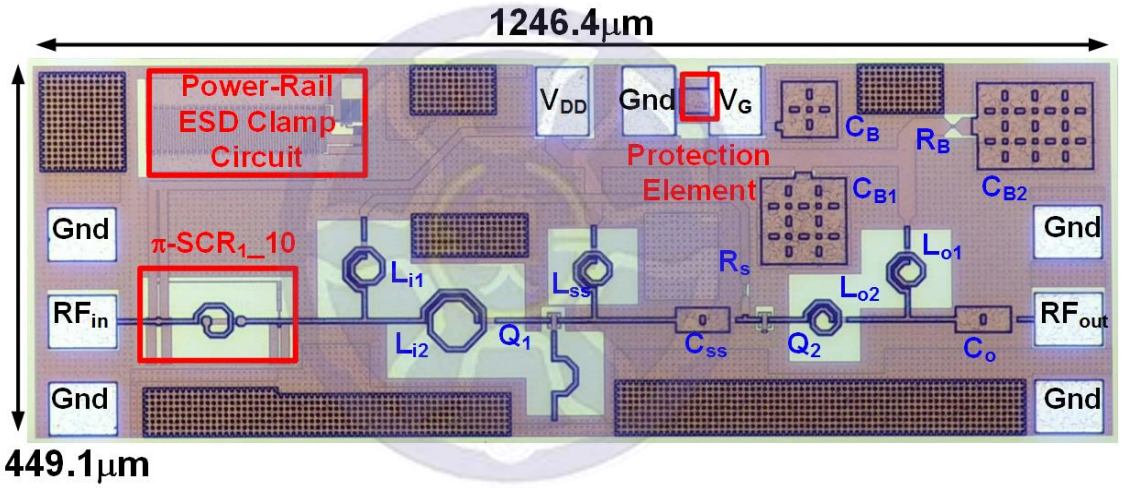
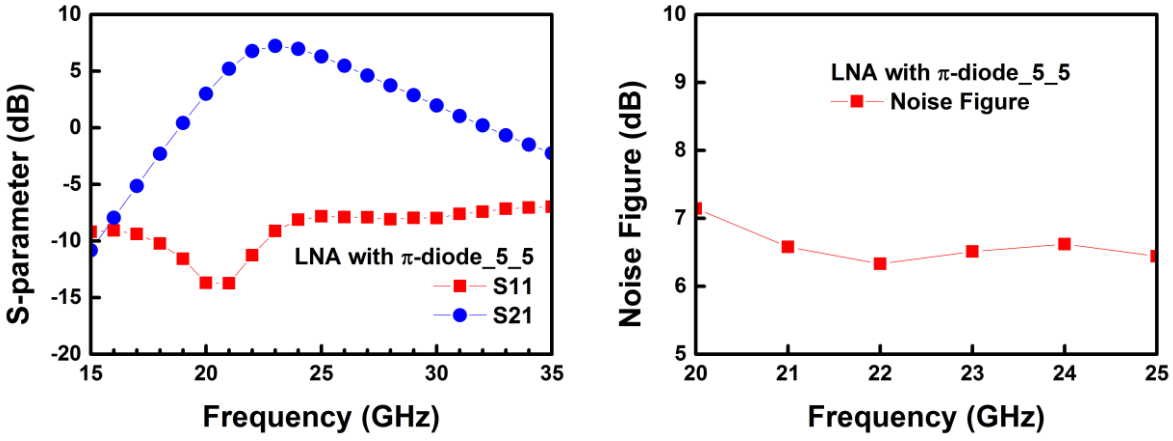


Fig. 4.26. Photograph of LNA with π-SCR_1_10.

(1) High-Frequency Performance

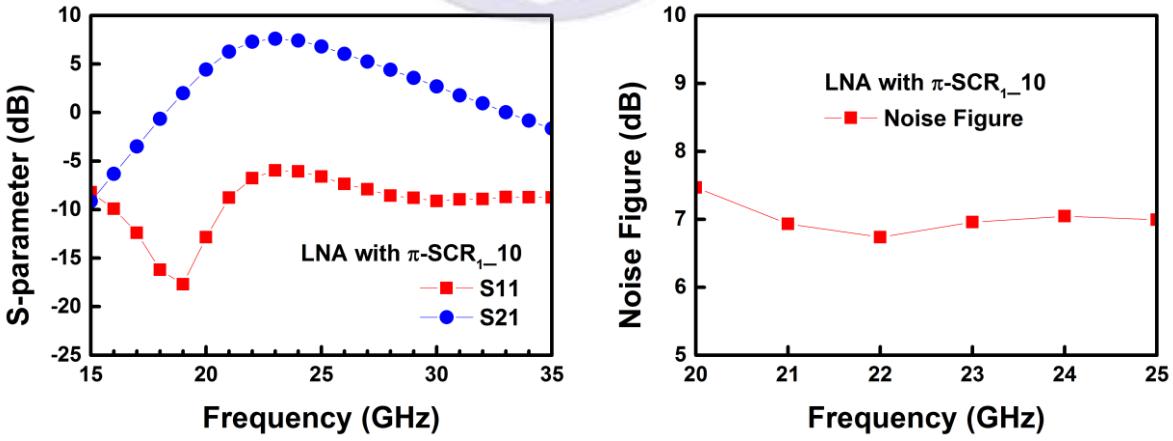
As shown in Fig. 4.27 (a), measured S21 is 6.8dB, and S11 is -11.3dB at 22GHz. As shown in Fig. 4.27 (b), measured noise figure of LNA with π-diode_5_5 is 6.3dB at 22GHz.



(a) (b)

Fig. 4.27. Measured (a) S-parameter and (b) noise figure of LNA with π-diode_5_5.

As shown in Fig. 4.28 (a), measured S21 is 7.3dB, and S11 is -6.8dB at 22GHz. As shown in Fig. 4.28 (b), measured noise figure of LNA with π-SCR$_1$_10 is 6.7dB at 22GHz. Compared with the LNA without protection device, S-parameter changes slightly. It means that proposed protection device has little effect on the high-frequency performance of LNA circuit.



(a) (b)

Fig. 4.28. Measured (a) S-parameter and (b) noise figure of LNA with π-SCR$_1$_10.

(2) TLP I-V Curves

After verifying the high-frequency performance, LNA with ESD protection devices are tested by TLP system to learn the characteristic. The TLP I-V curves of LNA with π-diode_5_5 and π-SCR_1_10 from V_{DD} to V_{SS} are compared in Fig. 4.29. The TLP I-V curves of LNA with π-diode_5_5 and π-SCR_1_10 under PS mode, PD mode, NS mode, and ND mode are compared in Fig. 4.30. The criterion to determine the failure of LNA in TLP measurement is that the leakage current changes by 30%.

From this measurement result, the TLP I-V curves show different turn-on resistance (R_{on}) between the use of π-diode_5_5 and π-SCR_1_10. To tell the difference, when the TLP current is 1A, the voltage across the device is defined as clamping voltage (V_{Clamp}). Under PS mode, the V_{Clamp} of LNA with π-diode_5_5 and π-SCR_1_10 is 7.5V and 5.4V. Under PD mode, the V_{Clamp} of LNA with π-diode_5_5 and π-SCR_1_10 is 6.9V and 6V. Under NS mode, the V_{Clmap} of LNA with π-diode_5_5 and π-SCR_1_10 is 4.8V and 4.4V. Under ND mode, the V_{Clmap} of LNA with π-diode_5_5 and π-SCR_1_10 is 7.5V and 7.6V.

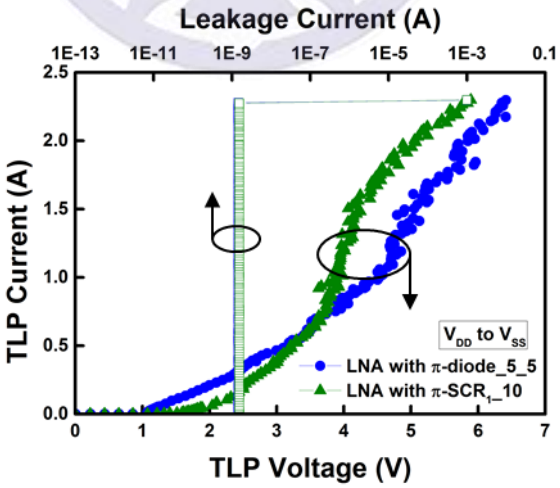


Fig. 4.29. Measured TLP I-V curves of LNA with π-diode_5_5 and π-SCR_1_10 from V_{DD} to V_{SS}.

The V_{Clamp} of LNA with π-SCR_1_10 is close to that with π-diode_5_5 under ND mode. Except for it, the V_{Clamp} of LNA with π-SCR_1_10 is lower than traditional design under PS mode, PD mode, and NS mode.

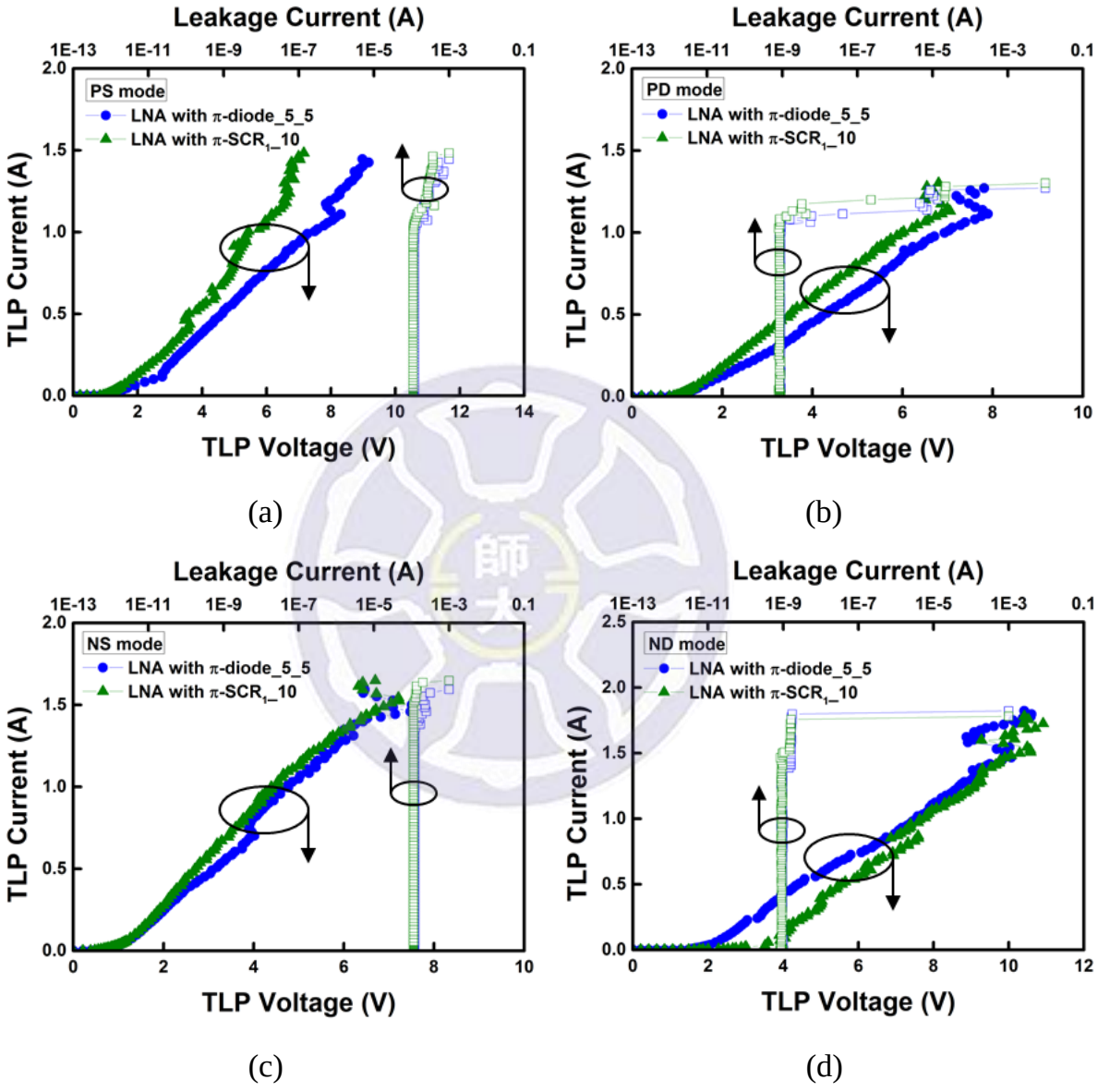
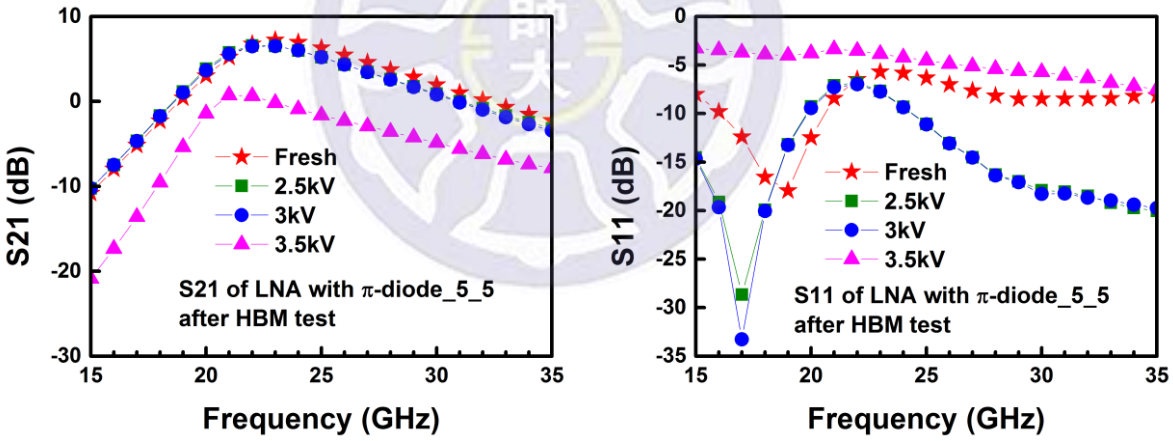


Fig. 4.30. Measured TLP I-V curves of LNA with π-diode_5_5 and π-SCR_1_10 under (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

(3) HBM Robustness

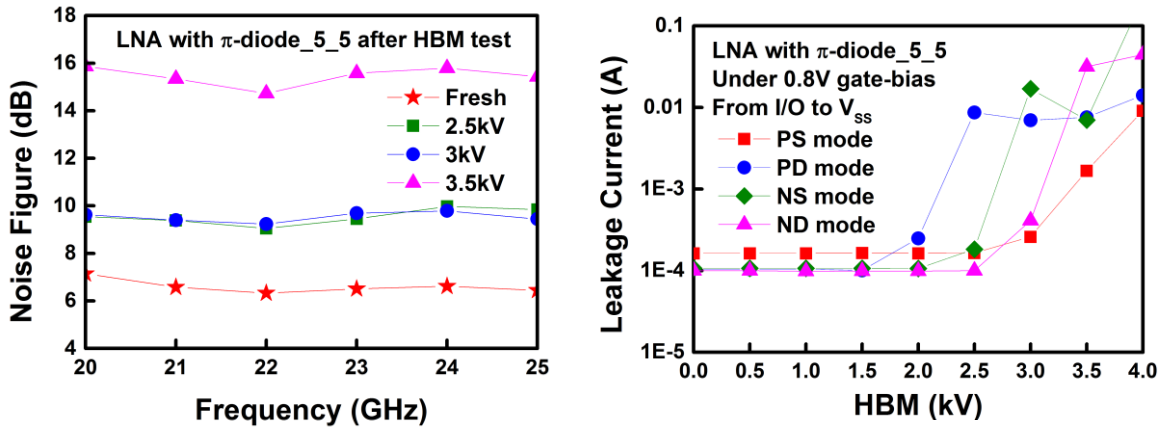
The secondary breakdown current (I_{t2}) is obtained by the TLP I-V curves. With this information, HBM robustness can be further estimated. S21 and S11 of LNA with π-diode_5_5 after HBM test are shown in Fig. 4.31 (a) and Fig. 4.31 (b). Measured noise figure and leakage current of LNA with π-diode_5_5 after HBM test are shown in Fig. 4.32 (a) and Fig. 4.32 (b).

The leakage current of LNA with π-diode_5_5 under PD mode increases after 2.5kV HBM test. However, the S21 and S11 are sustained. After 3.5kV HBM test, both S21 and S11 are distorted. In addition, the noise figure increased after 3.5kV HBM stress. It means that LNA with π-diode_5_5 is not functional after 3.5kV HBM test. The HBM level of LNA with π-diode_5_5 is 3kV.



(a) (b)

Fig. 4.31. Measured (a) S21 and (b) S11 of LNA with π-diode_5_5 after HBM test.

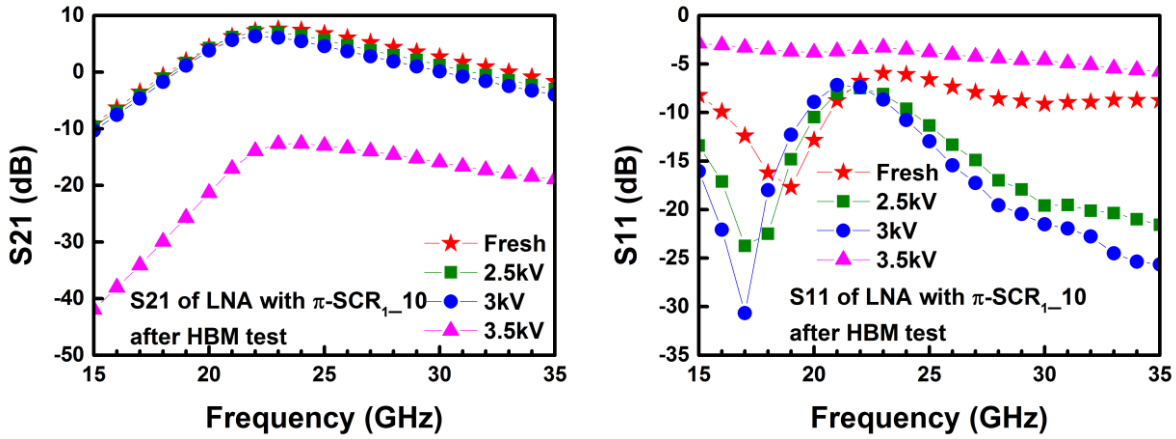


(a) (b)

Fig. 4.32. Measured (a) noise figure and (b) leakage current of LNA with π-diode_5_5 after HBM test.

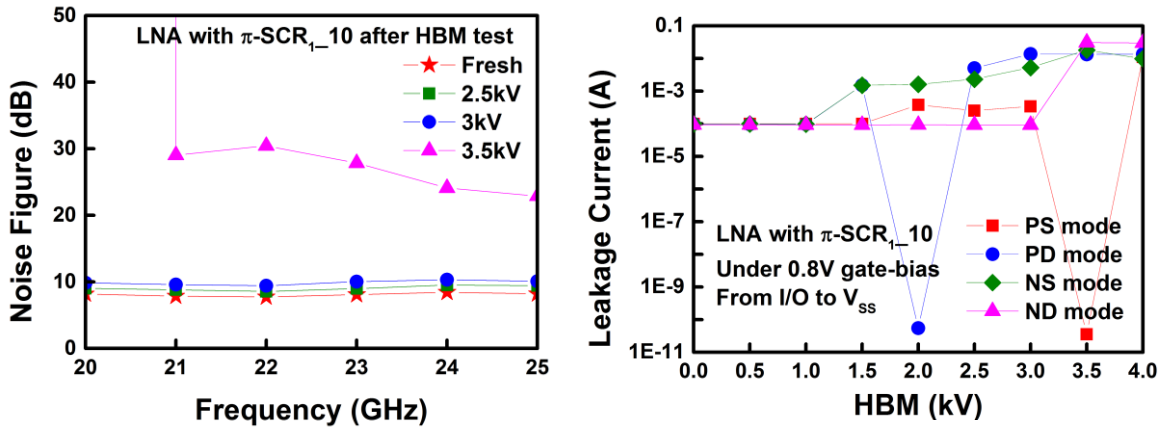
S21 and S11 of LNA with π-SCR$_1$_10 after HBM test are shown in Fig. 4.33 (a) and Fig. 4.33 (b). Measured noise figure and leakage current of LNA with π-SCR$_1$_10 after HBM test are shown in Fig. 4.34 (a) and Fig. 4.34 (b).

The S21 and S11 of LNA with π-SCR$_1$_10 is sustained after 3kV HBM test. However, both the S21 and S11 are distorted after 3.5kV HBM test, and the noise figure rises as well. The HBM level of π-SCR$_1$_10 is 3kV.



(a) (b)

Fig. 4.33. Measured (a) S21 and (b) S11 of LNA with π-SCR$_1$_10 after HBM test.



(a) (b)

Fig. 4.34. Measured (a) noise figure and (b) leakage current of LNA with π-SCR$_1$_10 after HBM test.

In chapter 3, both the traditional π-diode_5_5 and proposed π-SCR$_1$_10 are implemented with HBM test as the device. π-diode_5_5 and π-SCR$_1$_10 can achieve 2kV HBM level. In chapter 4, π-diode_5_5 and π-SCR$_1$_10 are added into LNA. In addition to the power-rail ESD clamp circuit, LNA circuits are equipped with protection element. It improves the capability of ESD protection. Therefore, LNA with π-diode_5_5 and π-SCR$_1$_10 can sustain 3kV HBM stress.

4.5 Comparison

As shown in Table 4.1, the measurement results of LNA equipped with traditional design and proposed device are compared with other LNA circuits. The gain of LNA without protection is 7.4dB. With the use of π-SCR_1_10, the gain decreases slightly to 7.3dB. The gain of LNA with π-diode is distorted to 6.8dB. LNA with proposed device and traditional design are functional after 3kV HBM test. The proposed π-SCR_1_10 is proved to have the ESD protection capability on K-band LNA with less signal distortion.

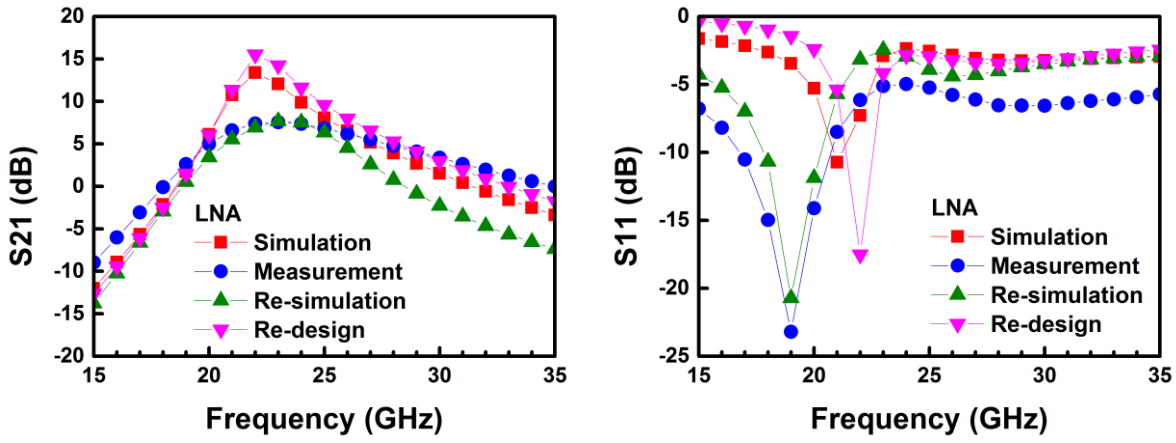
Table 4.1. Comparison of high-frequency applications with ESD protection device

Reference	**CMOS Process**	**Area**		**V_{Clamp} of PS mode (V)**	**HBM (kV)**	**Freq. (GHz)**	**Gain (dB)**	**NF. (dB)**
		ESD Device (μm^2)	**Total (mm^2)**					
[34]	40nm	No provid-ed	0.22	No pro-vided	2.8	24	13	3.2
[35]	0.13μm	7207	0.23	No pro-vided	2.5	24	14	5
[36]	90nm	43000	0.17	No pro-vided	4.5	0~16	12.5	6.5
LNA with π-diode _5_5	0.18μm	7200	0.56	7.5	3	22	6.8	6.3
LNA with π-SCR_1 _10	0.18μm	7560	0.56	5.4	3	22	7.3	6.7

As the progress of process technology, the transistor is scaled down. The breakdown voltage of gate-oxide is decreased. The ESD design window becomes narrower [33]. It causes ESD protection more challenging. Moreover, the discharging path under PS mode is the critical path in the whole-chip ESD protection network [20]. Under PS mode, the V_{Clamp} of LNA with π-diode_5_5 is 7.5V. However, the V_{Clamp} of LNA with proposed π-SCR_1_10 is 5.4V. Lower V_{Clamp} means that there is less power dissipation from current discharging. It proved that proposed π-SCR_1_10 is more suitable for advanced process technology than traditional design.

4.6 Discussion

There is some discrepancy in measurement and simulation results of LNA circuit. As shown in Fig. 4.35 (a) and Fig. 4.35 (b), S-parameter is re-simulated to find out the factors. The input matching network is composed of two inductors (L_{i1} and L_{i2}). In the re-simulation process, the inductance value of this two inductors are changed slightly to keep the right function of input matching network. With further adjustment, the re-designed S-parameter is shown in Fig. 4.35.



(a) (b)

Fig. 4.35. The re-simulated and re-designed (a) S21 and (b) S11 of LNA.

4.7 Summary

In this chapter, a two-stage cascade LNA applied in K-band is presented. The simulation and measurement results are shown. However, the high-frequency performance of LNA is distorted after the 0.5kV HBM test. Then the LNA is equipped with π-diode_5_5 and π-SCR_1_10. The gain of LNA is 7.4dB, and the noise figure is 6dB at 22GHz. With the use of π-diode_5_5, the gain of LNA is decreased to 6.8dB, and the noise figure is 6.3dB. With π-SCR_1_10, the gain of LNA is kept at 7.3dB, and the noise figure is 6.7dB. The high-frequency performance of LNA with proposed device has little distortion. However, the whole-chip ESD protection can be realized. LNA with π-SCR_1_10 stands 3kV HBM test.

In this work, traditional π-diode_5_5 and proposed π-SCR_1_10 with LNA are fabricated in 0.18μm CMOS. Based on the measurement results, both two devices are able to protect the RF circuits from ESD damage with less distorting. The advance of process technology makes gate oxide thinner, and the breakdown voltage of gate-oxide is reduced. The ESD deisgn window is more and more narrow. In the low-power applications, π-SCR has more advantages than π-diode due to lower clamping voltage (V_{Clamp}). It causes lower power dissipation as the ESD events happened.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In the beginning of this thesis, the background of ESD protection design is introduced. Related test standards and specifications are listed as well. In the following part, several studies about ESD protection designs for high-frequency applications are presented. The parasitic effect of protection device at high frequencies has to be considered. Distributed circuit is a common way for broadband circuit.

In chapter 3, the design flow of two types of π-SCR applied for broadband circuits is noted. The proposed design is in comparison with the traditional π-diode. Both proposed design and traditional design are fabricated in 0.18μm CMOS process. From the measurement results, the S21 of all test device are higher than -1dB at 10GHz. In addition, HBM level of all the device is higher than 2kV. R_{on} of proposed π-SCR is smaller than traditional π-diode under PS mode.

In chapter 4, π-SCR_1_10 and π-diode_5_5 are verified in a K-band LNA. The high-frequency performance of LNA can be maintained with the use of proposed ESD protection device. In addition, LNA with π-SCR_1_10 is functional after 3kV HBM test. With lower V_{Clamp}, proposed π-SCR_1_10 is more suitable for advanced process technology than traditional π-diode_5_5.

5.2 Future Work

This work combined DTSCR with the concepts of distributed circuit to realize the ESD protection for broadband circuit. The ESD current has to flow through STI region between anode and cathode in proposed π-SCR. To reduce the voltage overshoot during ESD events, the SCR device can be replaced with gated SCR to improve the turn-on efficiency [9]. The cross-sectional view of gated SCR is shown in Fig. 5.1. With the use of dummy gate, the discharging path of gated SCR between anode and cathode is reduced. The discharging path of parasitic diode inside gated SCR is reduced as well. However, the capacitance of gated SCR becomes larger. Additional parasitic capacitance caused by gated SCR can be resonated with the matching inductor. Therefore, the high-frequency performance of π-gated_SCR is maintained.

The diodes used in proposed design are STI diodes as shown in Fig. 5.2 (a). NS diodes and trigger diodes can be replaced with gated diodes (as shown in Fig. 5.2 (b)) to reduce the voltage overshoot during ESD events. More parasitic capacitance in gated device is tolerable with the use of matching element.

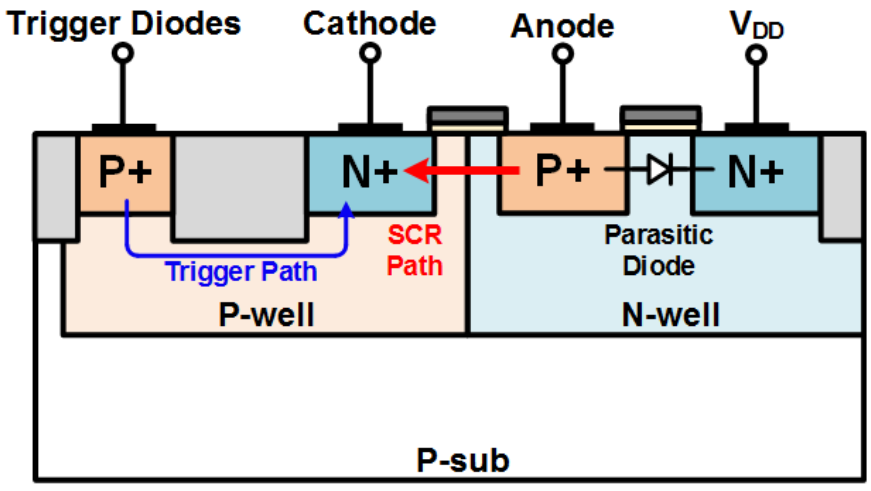
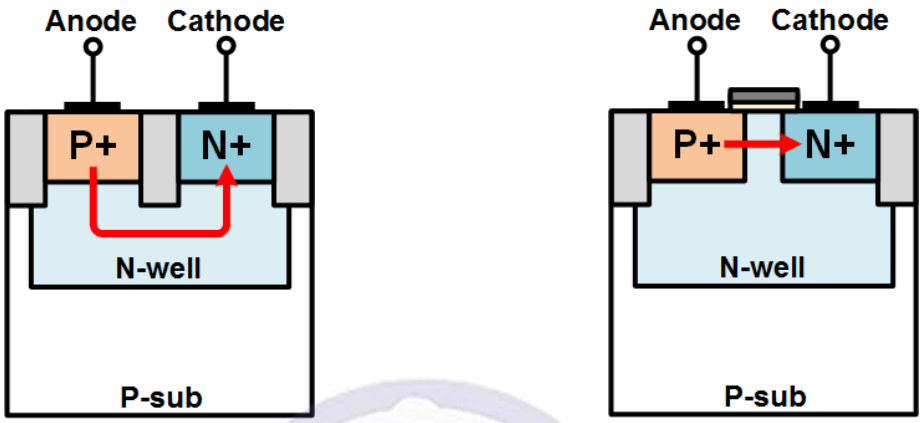


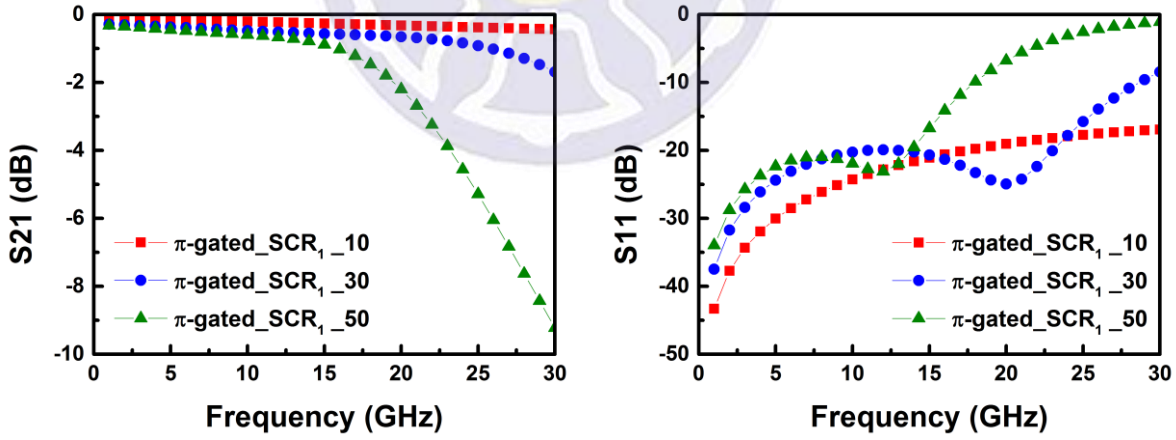
Fig. 5.1. The cross-sectional view of gated SCR.

The simulated S21 of π-gated_SCR1_10, π-gated_SCR1_30, π-gated_SCR1_50 are compared in Fig. 5.3 (a), and the simulated S11 of π-gated_SCR1_10, π-gated_SCR1_30 π-gated_SCR1_50 are compared in Fig. 5.3 (b).



(a) (b)

Fig. 5.2. The cross-sectional view of (a) STI diode and (b) gated diode.



(a) (b)

Fig. 5.3. The simulated S-parameter of π-gated_SCR1_10, π-gated_SCR1_30, and π-gated_SCR1_50.

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