國立臺灣師範大學電機工程學系

碩士論文

指導教授：林群祐 博士

應用於高頻與高壓電路之靜電放電防護設計

ESD Protection Designs for High-Frequency and High-Voltage Applications

研究生：彭柏維 撰

中 華 民 國 108 年 2 月

應用於高頻與高壓電路之靜電放電防護設計

學生：彭柏維　　指導教授：林群祐 博士

國立臺灣師範大學電機工程學系碩士班

摘　　要

為了避免積體電路遭受靜電放電的破壞，靜電放電防護元件通常被設計在電路的輸入/輸出端。操作在順偏條件的二極體適合被作為靜電放電防護元件，因此靜電放電防護二極體被廣泛應用在高頻以及高壓電路，然而靜電放電防護二極體的寄生電容卻嚴重地影響電路的高頻特性，導致信號不斷流失，為了解決信號損失的問題，靜電放電防護二極體的寄生電容必須被最小化。然而，防護元件的寄生電容能夠縮小的範圍仍然有限，一個元件同時擁有足夠的靜電放電防護能力以及小的寄生電容是相當困難的。因此，本論文提出一種低損耗焊墊的結構，能夠有效降低防護元件對高頻的影響，透過 LC 共振原理使 K/Ka-bands 中的信號損失降至最低。低損耗焊墊搭配靜電放電防護雙二極體已被實現在 0.18μm 互補式金氧半製程中，從高頻量測中證實，所提出之結構的信號損失較傳統結構低了六至十倍。最後，藉由各項靜電放電耐受度測試驗證，所提出之結構能夠擁有足夠高的靜電放電防護能力。

由於二極體為單向導通元件，僅適合提供一個靜電放電的路徑，需額外加入靜電放電箝制電路才能提供電路完整的防護，然而靜電放電電流透過靜電放電箝制電路排放，通常需要較遠的距離。因此，本論文提出一種雙向導通的 P 型二極體結構，藉由 PN 接面的空乏區控制其通道，當靜電放電事件發生時，通道的空乏區將消失並排放靜電電流，而在正常工作中，空乏區應切斷其通道並有足夠低

的漏電流，在高壓的應用中，橫向雙擴散電晶體經常被作為靜電放電防護元件，然而橫向雙擴散電晶體的結構複雜且不易設計，使得高壓操作中的靜電放電防護設計受到挑戰。二極體不但結構簡單且有足夠的靜電放電耐受度，因此本論文針對二極體的結構去進行改良，所提出的 P 型空乏二極體已被實現在 0.50μm 互補式金氧半製程中。從直流量測結果證實，在正常工作下 P 型空乏二極體有足夠低的漏電流，靜電放電耐受度測試中，透過通道排放靜電電流的想法是可行的但仍有需改進的地方。最後一章節的未來工作中將會提及一些改良的結構與想法。

關鍵字：二極體、靜電放電、高頻、高壓、低損耗、寄生電容。

ESD Protection Designs for High-Frequency and High-Voltage Applications

Student：Bo-Wei Peng　　Advisor：Dr. Chun-Yu Lin

Department Electrical Engineering

National Taiwan Normal University

Abstract

The electrostatic discharge (ESD) protection devices are generally designed and employed near the input/output (I/O) pad to avoid the impact of ESD events. The diode operated under forward-biased condition is widely used as an ESD protection device in the integrated circuits (ICs). However, the parasitic capacitance of ESD protection diode seriously affects the high-frequency characteristics of the circuit and causes the signal to be lost. In order to solve the problem of signal loss, the parasitic capacitance of ESD protection diode must be minimized. However, the parasitic capacitance of protection device can be reduced in a limited range. It is difficult for a device to have sufficient ESD protection level and small parasitic capacitance at the same time. Therefore, this thesis proposes a structure of low-loss I/O pad that can effectively reduce the effect of ESD protection diode at high frequency. The signal loss at K/Ka-bands is minimized by the principle of LC resonance. The low-loss I/O pad with dual-diode ESD protection has been implemented in 0.18μm CMOS process. It is confirmed from the high-frequency measurement that the signal losses of proposed structures are 6~10 times lower than the

traditional structure. Finally, it is verified by various ESD tests that the proposed structure has sufficiently high capability of ESD protection.

Since the diodes is a single-conducting device, it is only suitable for providing an ESD path. The circuit requires an additional power-rail ESD clamp to provide complete protection. However, the ESD current usually requires a long distance to discharge through a power-rail ESD clamp. Therefore, this thesis proposes a structure of bi-directional P-type diode, which is controlled by the depletion region of the PN-junction. When the ESD events occur, the depletion region of channel will disappear and discharge the ESD current. In the normal operation, the depletion region should close the channel and have a sufficiently low leakage current. For the high-voltage applications, the lateral double-diffused MOS (LDMOS) is often used as the ESD protection device. However, the structure of LDMOS is complex and difficult to design. The ESD protection design is challenged in high-voltage operation. The structure of diode is simple and it has sufficient ESD protection level. Therefore, this thesis aims to improve the structure of diode. The P-type depletion diodes have been fabricated in 0.50μm CMOS process. It is confirmed from the DC measurement that the P-type depletion diodes have a sufficiently low leakage current under the normal operation. From the ESD tests, the idea of discharging ESD current through the channel is feasible but there is still room for improvement. Some improved structures and ideas will be mentioned in the future work of the final chapter.

Keywords: Dual diodes, Electrostatic discharge (ESD), high-frequency, high-voltage, low-loss, parasitic capacitance.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

In modern nanoscale complementary metal-oxide-semiconductor (CMOS) processes, the transistor of integrated circuit (IC) must use a thin gate-oxide layer to achieve high speed and low power consumption. However, the electrostatic discharge (ESD) immunity of IC has been greatly weakened as the device continue to shrink. Therefore, the ESD protection design in nanoscale CMOS processes is quite difficult. Fig. 1.1 shows the IC destroyed by ESD and the characteristics of circuit is irreversible after suffering ESD damage. In addition, designer should consider the suitable ESD protection circuit for the different processes and applications. This thesis designs new types of ESD protection devices for the high-frequency circuit (0.18μm) and high-voltage process (0.50μm).

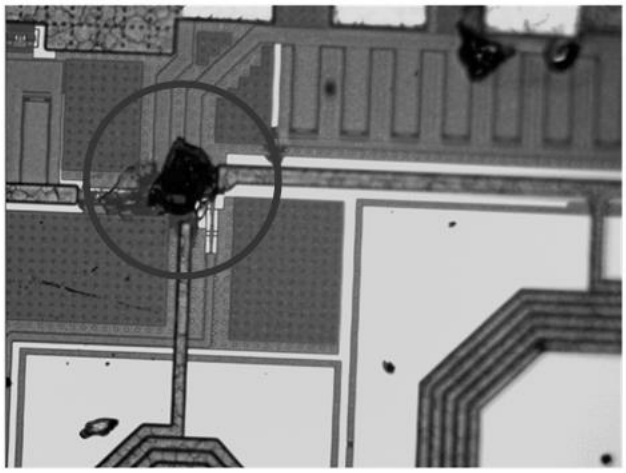


Fig. 1.1. The photo of an ESD damaged IC without ESD protection.

1.2 Background of ESD

When enough electrons are accumulated on two different objects, a phenomenon called electrostatic discharge (ESD) occurs in the air dielectric between the objects. The phenomenon of ESD has received great attention in the integrated circuit industry because it may cause damage to the product. Affected by ESD events, ICs experience a sharp rise in voltage and temperature, which causes the metal to melt and the oxide to evaporate [1]. The size of material is directly proportional to the robustness of the rapid heating of ESD event. Large device has higher heat capacity and can tolerate greater strikes of ESD. The IC industry continues to evolve toward smaller and smaller process to meet the demand of higher operating speed. Modern IC processes always have thin oxides, small PN junctions, narrow metal lines and small vias. These features are designed to fit smaller and faster devices. However, the problem is that ICs are more susceptible to ESD events. So ESD protection is important for IC design, which improves product quality.

1.3 Test Standards of ESD

Depending on the conditions, there are four models that simulate ESD events. The human body model (HBM) simulates an ESD event that occurs when a charged human's finger touches the IC [2]. The charge accumulates in the IC and then contacts the conductors of different potentials to produce a discharge phenomenon. The machine model (MM) simulates a situation where a charged machine contacts the IC and then discharges [3]. The charged device model (CDM) is a rapid discharge event between the IC and conductor [4]. The human metal model (HMM) applied on the component level to predict the ESD performance under the system level [5].

1.3.1 The Human Body Model (HBM)

The HBM consists of a 100 pF capacitor that is charged to high potential and then discharged through a series connection of a 1.5kΩ resistor and the device under test (DUT). The equivalent circuit of HBM is shown in Fig. 1.2. The stress range of HBM is 250V to 8kV. Compare to CDM and MM, HBM has the highest voltage level and smaller current level. Even so, HBM still has a current range of amp. In the case of general HBM event, the DUT suffers from a sharp current pulse of 1A by 10ns. The current through DUT slowly drops after reaching the peak. The discharge waveform of HBM is shown in Fig. 1.3.

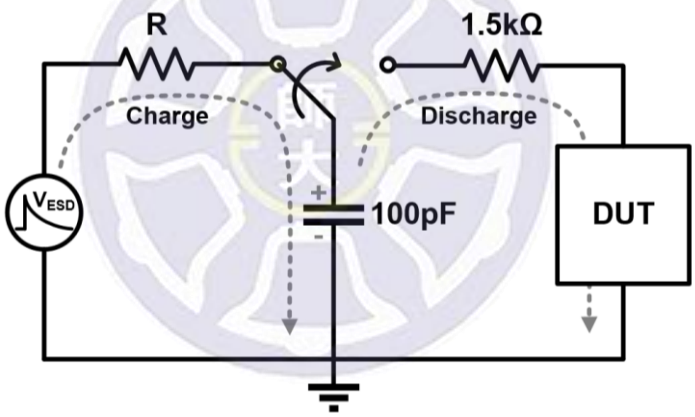


Fig. 1.2. The equivalent circuit of HBM.

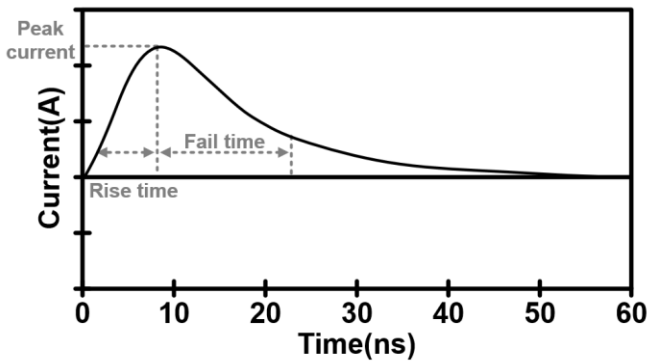


Fig. 1.3. The discharge waveform of HBM.

1.3.2 The Machine Model (MM)

Since the machine can store more electric charges than the human body, MM has a larger equivalent capacitance than HBM. The equivalent circuit of MM is shown in Fig. 1.4. The 200pF capacitor is charged to high potential and then discharged through the device under test (DUT). The voltage level of MM is lower than HBM and CDM. The stress range of MM is 25V to 400V. The discharge characteristics of MM is like CDM, which follow the RLC response. However, the equivalent capacitance of MM is much larger than CDM, which causes the rise time of MM to be slower than CDM. The discharge waveform of MM is shown in Fig. 1.5. Since the MM test has not received much attention in recent years, it is for reference only here.

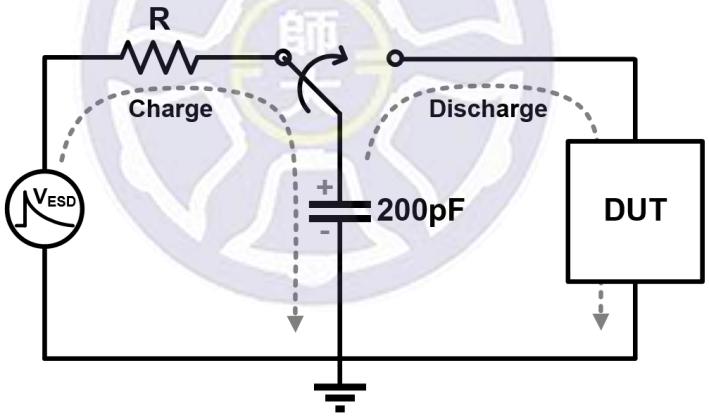


Fig. 1.4. The equivalent circuit of MM.

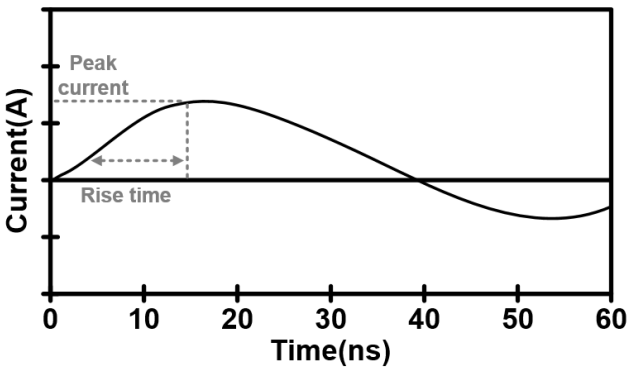


Fig. 1.5. The discharge waveform of MM.

1.3.3 The Charged Device Model (CDM)

The ESD event of CDM discharges higher current in a shorter time range than HBM and MM. Building a model of an ESD event for a charged device is a difficult task. Under high-frequency operation, the parasitic effects of devices and circuits determine the outcome of CDM event. As shown in Fig. 1.6, the CDM can be simply modeled as an RLC circuit. There is a great difference between CDM and HBM, which can be clearly observed from the discharge waveform, as shown in Fig. 1.7. The CDM event quickly reaches the peak current and the CDM is the most destructive ESD event due to the high current level. The stress range of CDM is 125V to 2kV. However, the CDM test is for the packaged IC so this thesis will not perform this measurement.

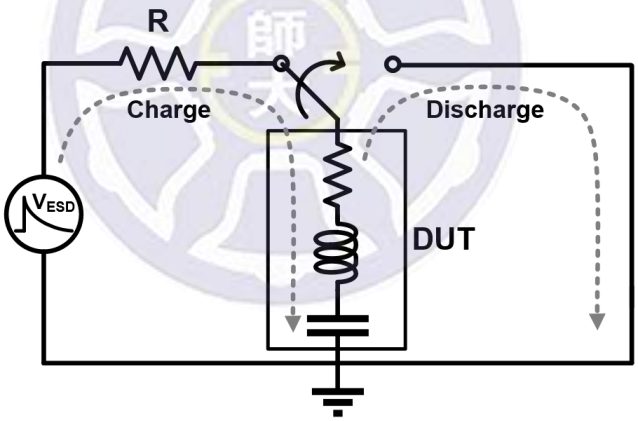


Fig. 1.6. The equivalent circuit of CDM.

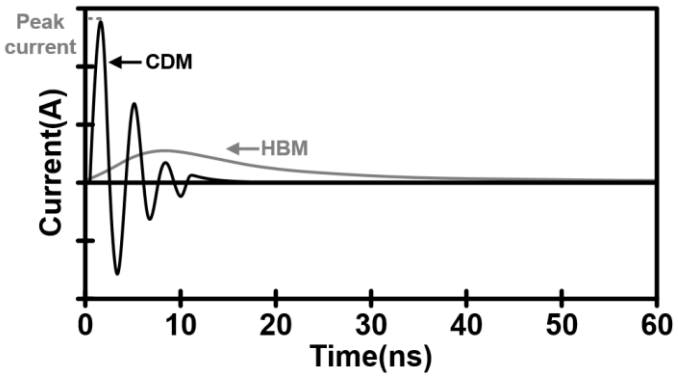


Fig. 1.7. The discharge waveform of CDM.

1.3.4 The Human Metal Model (HMM)

Due to the development of system on a chip (SoC) in recent years, the system-level ESD protection should be valued. The HMM test applied on the component-level to predict the ESD performance at the system-level. The HMM consists of a 150pF capacitor that is charged to high potential and then discharged through a series connection of a 330Ω resistor and the device under test (DUT). The equivalent circuit of HMM is shown in Fig. 1.8. HMM has a larger equivalent capacitance and smaller equivalent resistance than HBM. Therefore, HMM has more storage charge and high current level. The discharge waveform of HMM is shown in Fig. 1.9.

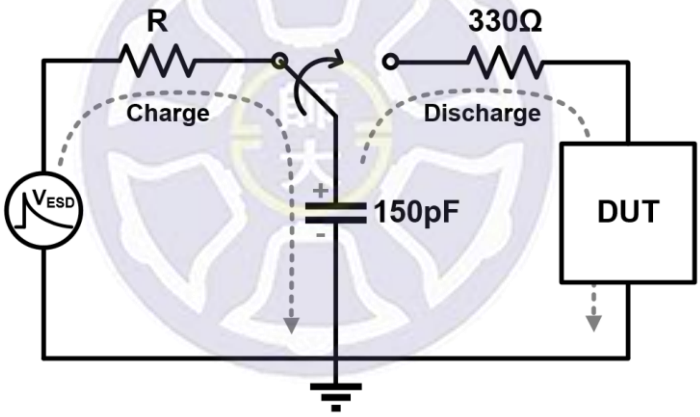


Fig. 1.8. The equivalent circuit of HMM.

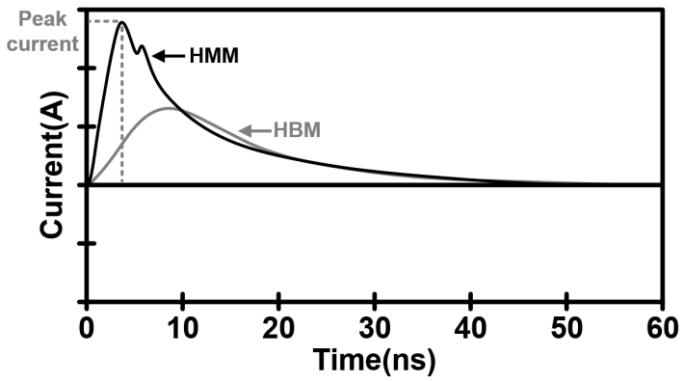


Fig. 1.9. The discharge waveform of HMM.

1.3.5 Electrostatic Discharge Sensitive (ESDS)

In order to avoid the effects of ESD events, the electrostatic discharge sensitive (ESDS) of HBM, MM, and CDM are presented in Table 1.1. The HBM is classified into eight levels from 125V to 8kV and the MM is classified into four levels from 100V to 400V [6]. The CDM is classified into seven levels from 150V to 2kV [7], [8]. This information can be used to design a more effective solution of ESD protection. The ESDS of products will increase year by year, so we should pay attention to the issue of ESD events in industrial manufacturing.

Table 1.1

The ESDS of HBM, CDM, and MM.

ESD event	Class	Voltage range (V)
HBM ANSI/ESD STM5.1	0A	< 125
	0B	125 to < 250
	1A	250 to < 500
	1B	500 to < 1000
	1C	1000 to < 2000
	2	2000 to < 4000
	3A	4000 to < 8000
	3B	≥ 8000
MM ANSI/ESD STM5.2	M1	< 100
	M2	100 to < 200
	M3	200 to < 400
	M4	≤ 400
CDM ANSI/ESD STM5.3.1	C1	< 150
	C2	150 to < 250
	C3	250 to < 500
	C4	500 to < 1000
	C5	1000 to < 1500
	C6	1500 to < 2000
	C7	≥ 2000

1.4 Basic ESD Protection Design for I/O Pad

The I/O (input/output) pad provides a connection between the integrated circuit and the outside of the chip. Due to the I/O pad is the only window of the internal circuit, it has a direct relationship to the ESD events. Therefore, a complete ESD protection circuit must be configured between the I/O pad and the internal circuit. Fig. 1.10 shows the basic ESD protection circuit for I/O pad. The devices can be used as an ESD protection circuit such as diode, thin/thick-oxide device, bipolar junction transistor (BJT), silicon-controlled rectifier (SCR), etc. The selection of ESD protection device should consider the circuit application and the process of IC. The diode has a simple structure and good ESD protection level. So this thesis used diodes to implement new architectures of ESD protection. In addition, the traditional diode and the improved diode structures of previous literature will be mentioned in the second chapter.

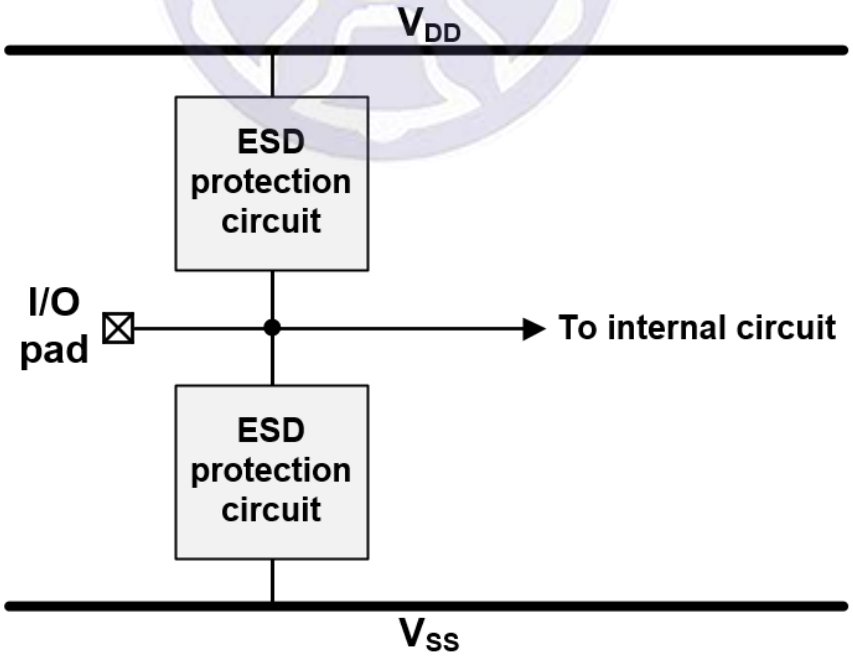


Fig. 1.10. The basic ESD protection circuit for I/O pad.

1.4.1 ESD-Protection Design Window

In order to establish a suitable ESD protection circuit, the I-V curve of ESD protection device must be designed in the ESD-protection design window [9], as shown in Fig. 1.11. The boundaries of ESD protection design window are defined by the power-supply voltage (V_{DD}) of the internal circuit and the gate-oxide breakdown voltage (V_{BD}) of the transistor. In order to adapt to the differences of IC manufacturing and environmental [10], the boundaries are compressed inward by 10%~20% to ensure no worries on the product. The trigger voltage and holding voltage of the ESD protection device are V_{t1} and V_h, respectively. Some ESD protection devices have a phenomenon of snapback. Therefore, it is necessary to ensure that V_h is higher than V_{DD} or a problem of latch-up will occur. Ron is the turn-on resistance of ESD protection device, which should be minimized to reduce the joule heat generated by ESD. Finally, the second breakdown current (I_{t2}) is the current that the ESD protection device burns out.

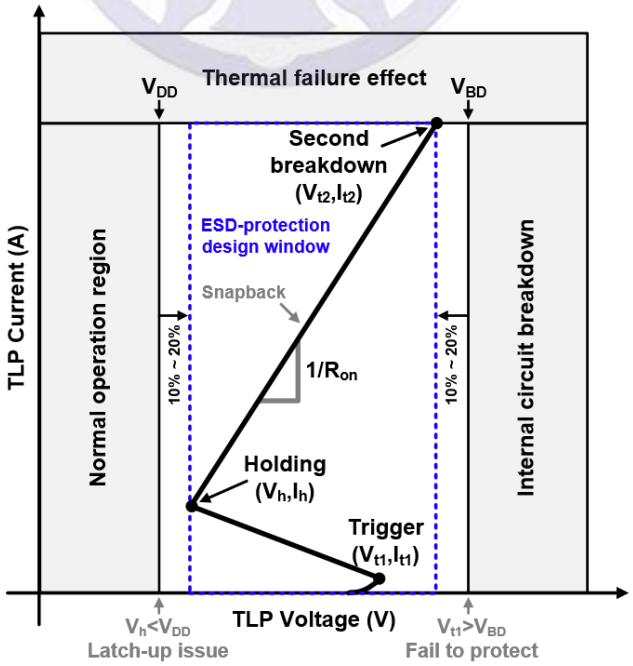


Fig. 1.11. The ESD-protection design window

1.4.2 The Considerations of High-Frequency Application

As the volume of transmission continues to grow each year, higher transmission rates must be met. However, the existing spectrum is already saturated and it is necessary to detect the higher frequency of millimeter waves. Fig. 1.12 shows the spectrum of millimeter wave. The K-band (18-27GHz) and Ka-band (27-40GHz) are used in radar, broadband satellite, and 5G mobile communication systems [11]-[13]. However, designing ESD protection devices is quite difficult in gigahertz bands.

In general, the ESD protection circuit of I/O pad is in parallel with the internal circuit [14]. The ESD protection circuit should ideally be equivalent to an open circuit under normal operation. Unfortunately, any ESD protection device has parasitic effects, which is especially serious at high-frequency [15]. The most serious impact is the parasitic capacitance of ESD protection circuit [16]. Since the capacitor exhibits a low impedance state at high-frequency, the input signal will continue to be loss [17], as shown in Fig. 1.13. In order to effectively protect the IC from ESD damage without losing the original characteristics, the parasitic capacitance of ESD protection circuit should be minimized.

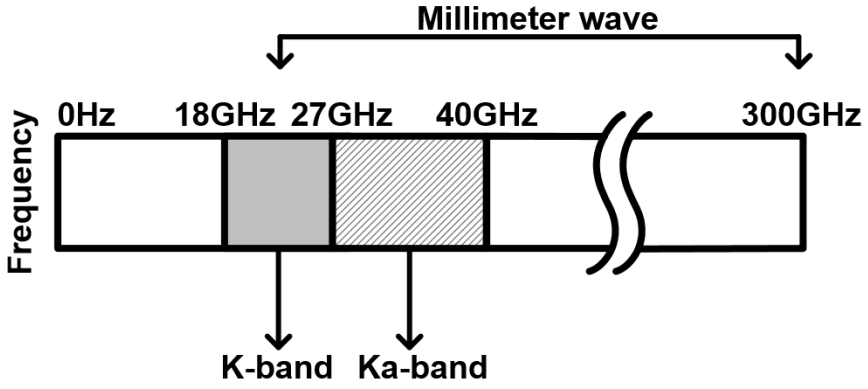


Fig. 1.12. The spectrum of millimeter wave.

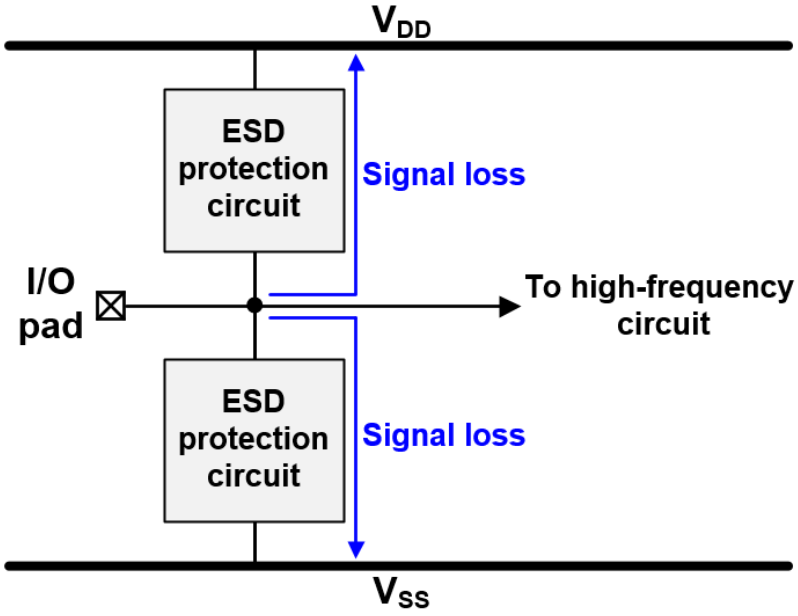


Fig. 1.13. The signal losses caused by ESD protection circuits.

1.4.3 The Considerations of High-Voltage Application

In modern times, more and more applications of IC require high-voltage interface. These include power management, power conversion, and automotive chip with the interfaces between 12V and 100V [18]. In addition, the LCD and OLED display technologies require a driver voltage between 10V and 40V [19]. The high operating voltage and complex process architecture of high-voltage IC make ESD protection design difficult. The lateral double-diffused MOS transistor (LDMOS) has been widely used in the high-voltage circuit [20], [21]. To ensure that the high-voltage ICs have sufficient ESD protection levels, foundries typically provide special layout rules for LDMOS at I/O pad [22]. However, the LDMOS with special layers will result in a decrease in driven capability and an increase in chip dimension. In addition, the large size of LDMOS will causes the problem of non-uniform conduction, as shown in Fig. 1.14. Therefore, this thesis abandons the scheme of LDMOS and uses a novel structure of diode to achieve the ESD protection of high-voltage circuit.

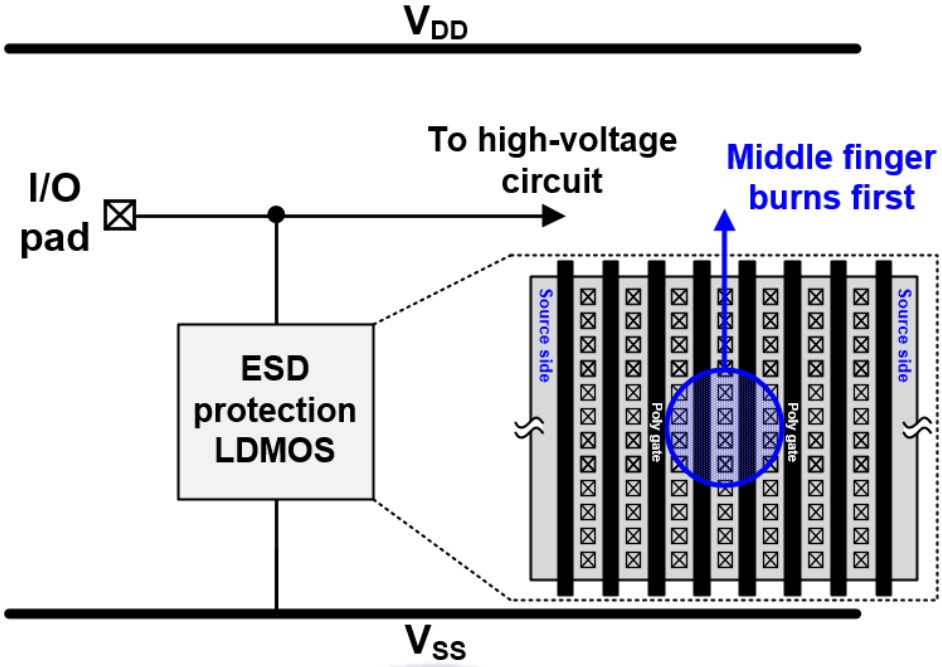


Fig. 1.14. The middle finger of LDMOS burned first.

1.5 Organization of This Thesis

This thesis consists of five chapters and it is outlined as follows. In Chapter 1, the background of ESD and the test models such as HBM, MM, CDM, and HMM are introduced. The basic ESD protection of I/O pad and the considerations of high-frequency/voltage applications are also mentioned. In Chapter 2, the traditional ESD protection diode and the improved structures such as stacked diodes are introduced. The whole-chip ESD protection circuit design is also organized. In Chapter 3, the low-loss I/O pads with stacked inductor and dual-diode ESD protection will be introduced, including the design steps and the measurement results. In Chapter 4, the depletion diodes for high-voltage application will be introduced, including design principle and measurement results. In Chapter 5, summarizes all the research and some proposals for future works are given.

Chapter 2

Introduction of ESD Protection Devices

2.1 Diode

In nanoscale CMOS process, two diodes provide the most basic ESD protection circuit for I/O pad [23], as shown in Fig. 2.1. The diode is widely used as an ESD protection device because of the high current-discharging capability and the low turn-on voltage (V_{t1}). When the potential of I/O pad rises above the power-supply voltage (V_{DD}), the diode placed between the I/O and V_{DD} is turned on. Therefore, a positive charged ESD event can be discharged from I/O to positive power line (V_{DD}) through the P-type diode (PD-mode). Conversely, a negative charged ESD event can be discharged from I/O to negative power line (V_{SS}) through the N-type diode (NS-mode).

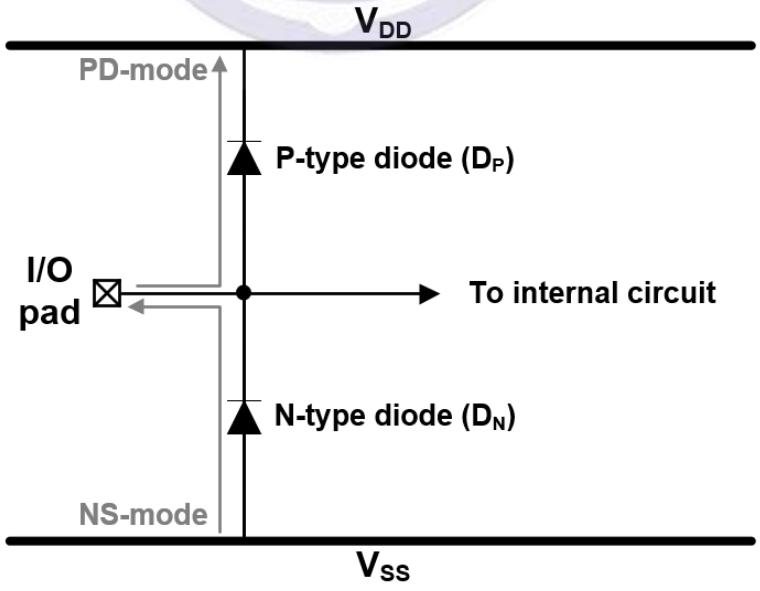


Fig. 2.1. The traditional ESD protection diodes for I/O pad.

The two types of ESD protection diodes including of P-type (P+/N-Well) and N-type (N+/P-Well) have been presented. The device cross-sectional and layout top views of P-type diode (D_P) are shown in Figs. 2.2 (a) and (b), respectively. The device cross-sectional and layout top views of N-type diode (D_N) are shown in Figs. 2.3 (a) and (b), respectively. The traditional diode has a simple structure and a good enough ESD protection level, so it is often used by ESD protection design. However, the traditional diode is no longer suitable for some applications. For the high-frequency applications, the parasitic capacitance of diode will cause the signal loss at gigahertz bands, as shown in Fig. 2.4. The C_P and C_N are the parasitic capacitances of D_P and D_N, respectively. The parasitic capacitance exhibits low impedance at high frequencies and cause signal loss. For high-voltage applications, the structure of traditional diode may not withstand high-voltage levels. Based on these, some improved structures of diode proposed in previous literature will be mentioned in the next section.

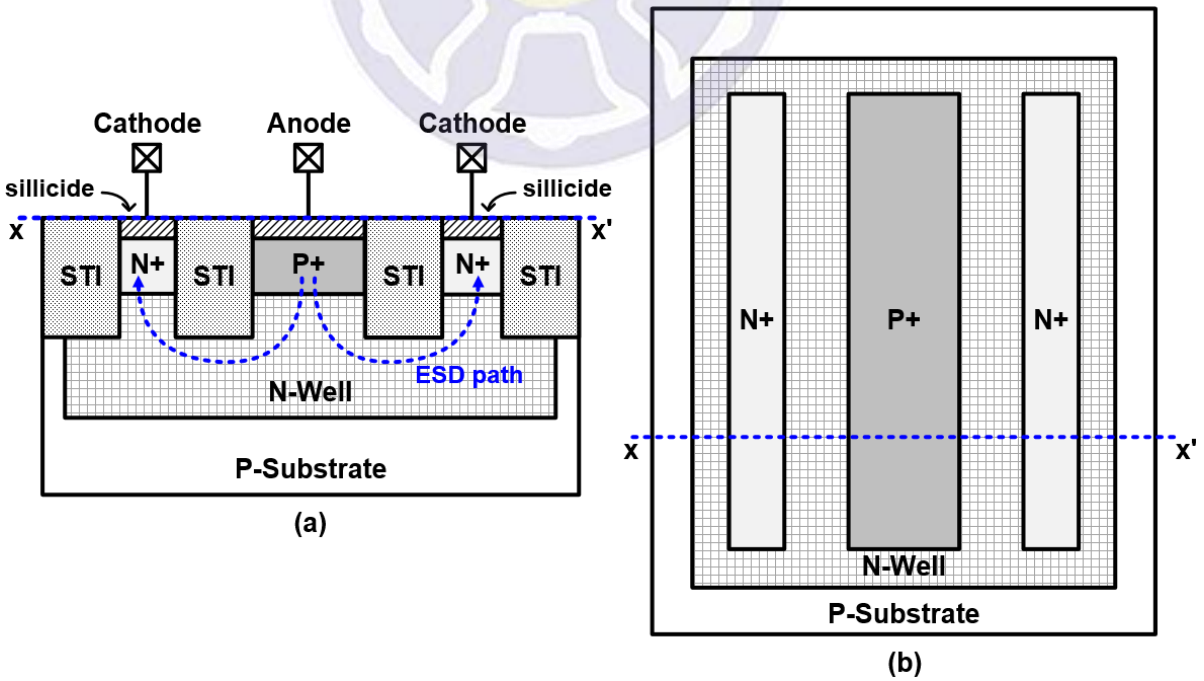


Fig. 2.2. The (a) device cross-sectional view and (b) layout top view of P-type diode (D_P).

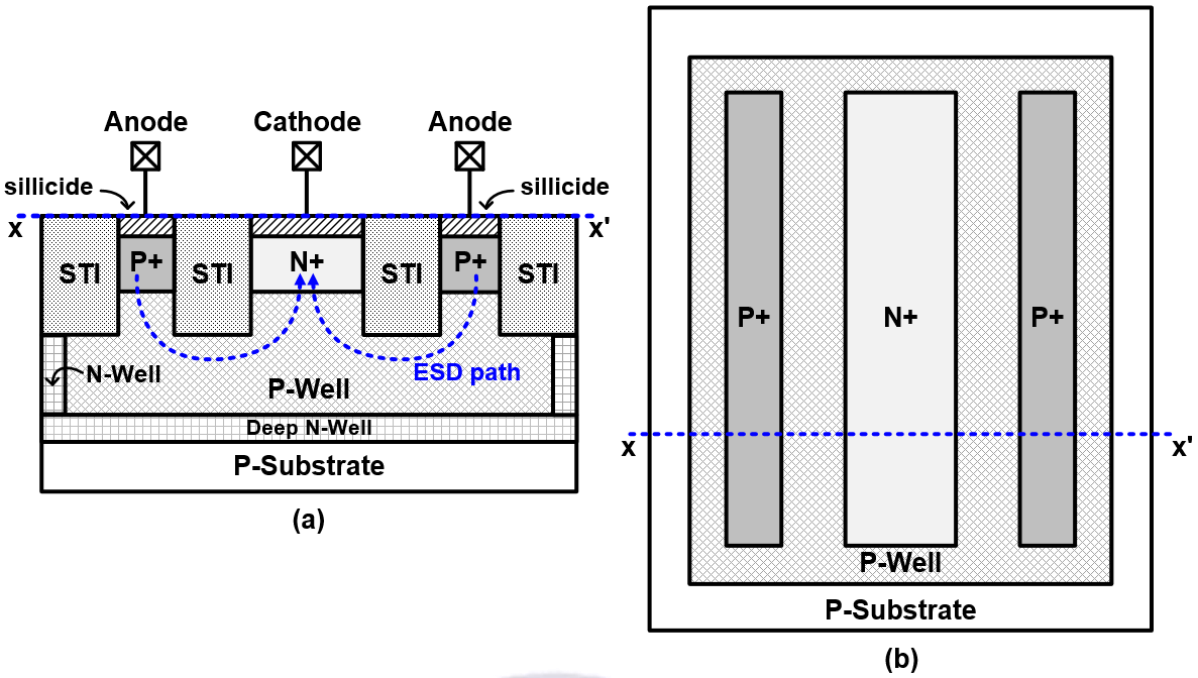


Fig. 2.3. The (a) device cross-sectional view and (b) layout top view of N-type diode (D_N).

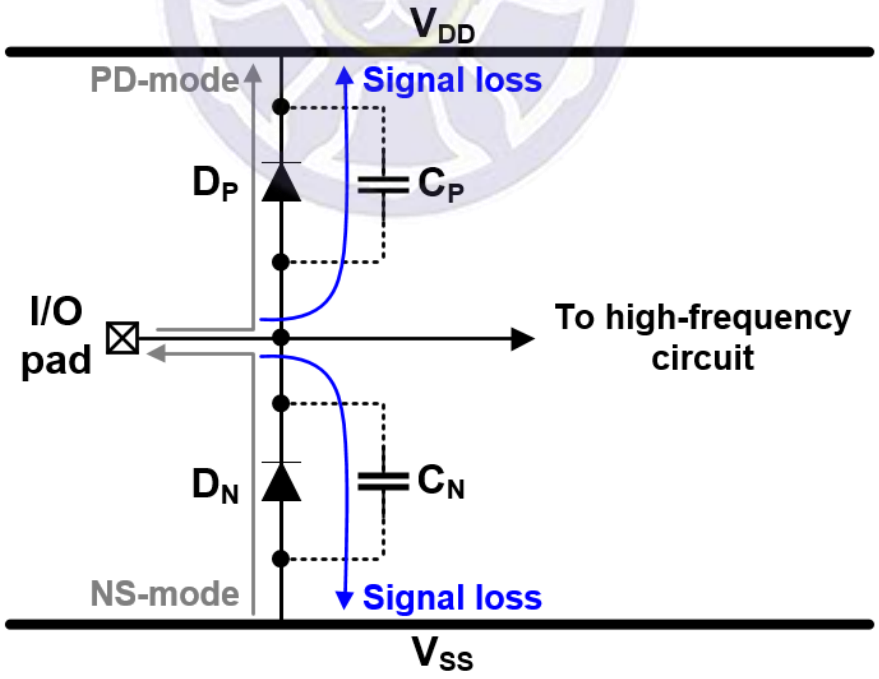


Fig. 2.4. The signal loss caused by ESD protection diodes for high-frequency applications.

2.2 Stacked Diodes

Fig. 2.5 shows the ESD protection design with stacked diodes (SD) at I/O pad. The two D_P are connected in series to P-type stacked diodes (SD_P) between I/O pad and V_{DD}. Similarly, the two D_N are connected in series to N-type stacked diodes (SD_N) between I/O pad and V_{SS}. The device cross-sectional and layout top views of SD_P are shown in Figs. 2.6 (a) and (b). The device cross-sectional and layout top views of SD_N are shown in Figs. 2.7 (a) and (b). For the high-frequency applications, the parasitic capacitance of stacked diodes is proportionally to the number of diodes. Due to the series connection of diodes, the parasitic capacitances are also reduced in series. The total parasitic capacitance seen from I/O pad changes from ($C_P + C_N$) to ($C_P/2 + C_N/2$). Therefore, the problem of parasitic capacitance can be reduced by 50% for high-frequency circuits [24]. However, the diodes cannot be continuously stacked because the parasitic resistance of diode will increase in series to cause a larger turn-on resistance (R_{on}). In addition, the trigger voltage (V_{t1}) will increase proportionally with the number of diodes [25].

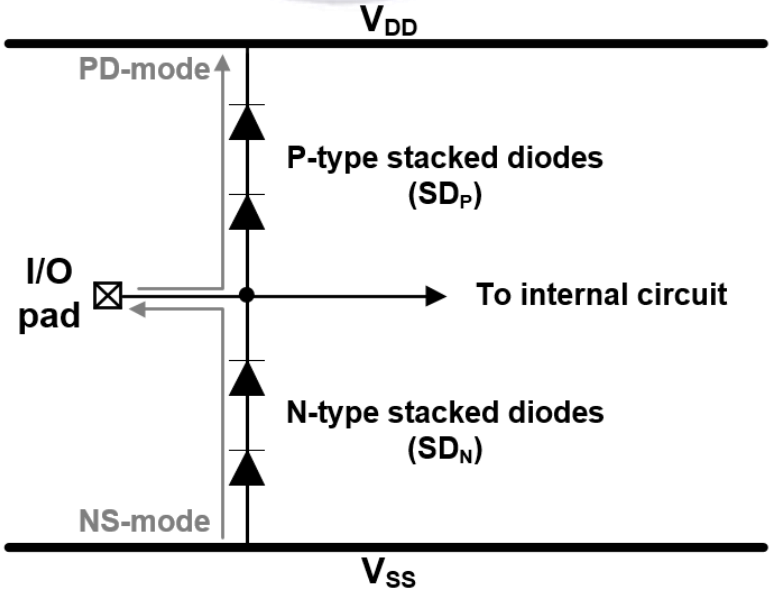
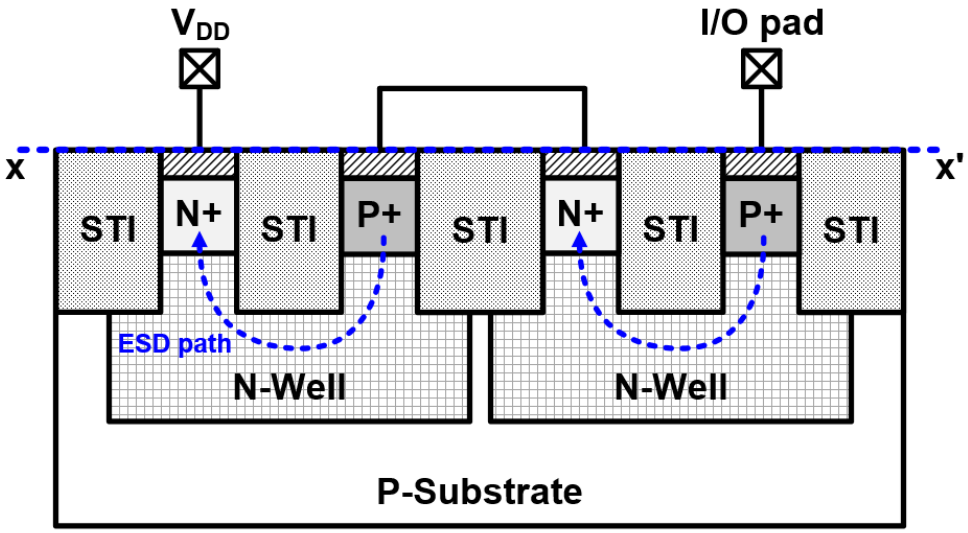
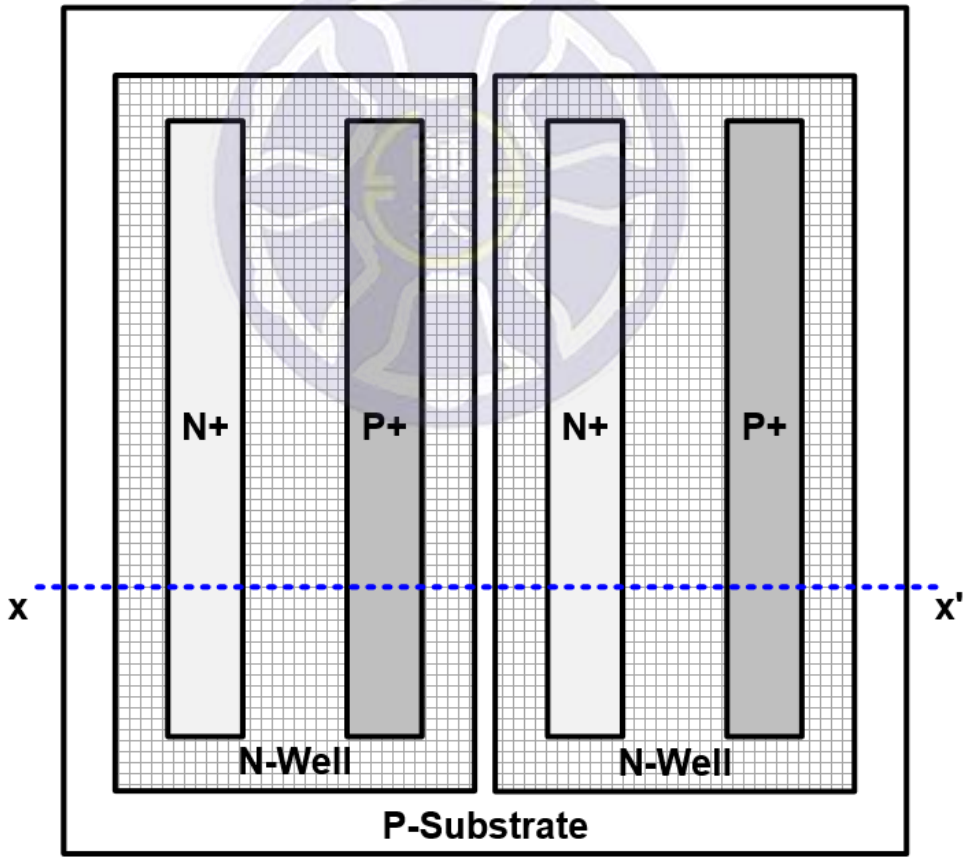


Fig. 2.5. The ESD protection design with stacked diodes (SD) at I/O pad.

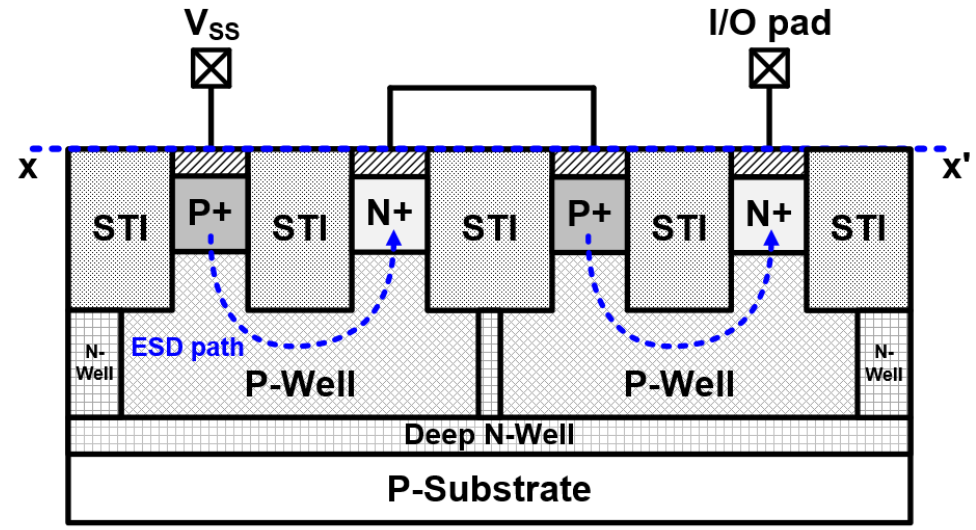


(a)

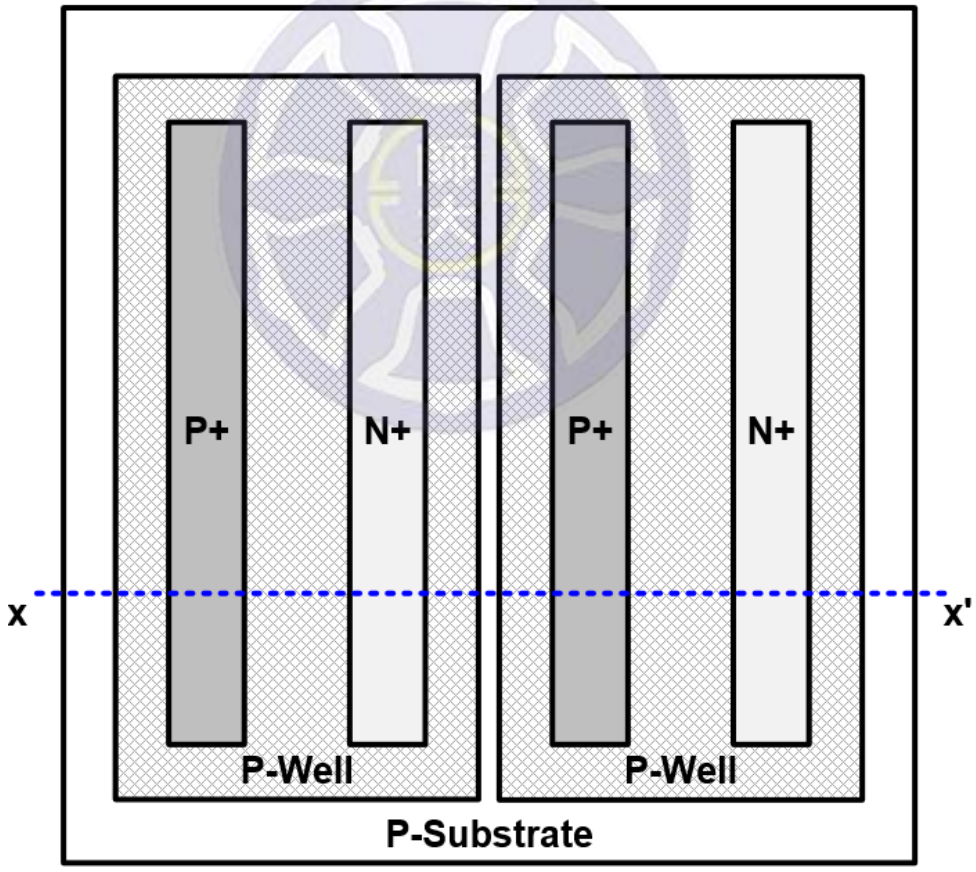


(b)

Fig. 2.6. The (a) device cross-sectional view and (b) layout top view of P-type stacked diode (SD_P).



(a)



(b)

Fig. 2.7. The (a) device cross-sectional view and (b) layout top view of N-type stacked diode (SD_N).

2.3 ESD Protection Diode with Local I/O Clamp

In order to improve the ESD protection of I/O pad, the stacked diode with local I/O clamp was proposed in previous literature [26]. Fig. 2.8 shows the local I/O clamp implemented with stacked diodes. In the blue dashed area, three P-type diodes are stacked between the I/O pad and V_{DD}. Similarly, three N-type diodes are stacked between the I/O pad and V_{SS}. It should be noted that these stacked diodes are forward biased under normal operation. In order to ensure that the local I/O clamp will not be triggered under normal operation, the number of diodes is the key. For example, the 0.18μm CMOS process has a V_{DD} of 1.8V and a V_{SS} of -1.8V. Suppose a diode has a forward voltage (V_D) of 0.7V and three of them have a bias of 2.1V. Therefore, the local I/O clamp will not be turned on under normal operation. When the ESD events occur, the local I/O clamp can provide two ESD paths from V_{DD} to I/O pad (ND-mode) and I/O pad to V_{SS} (PS-mode).

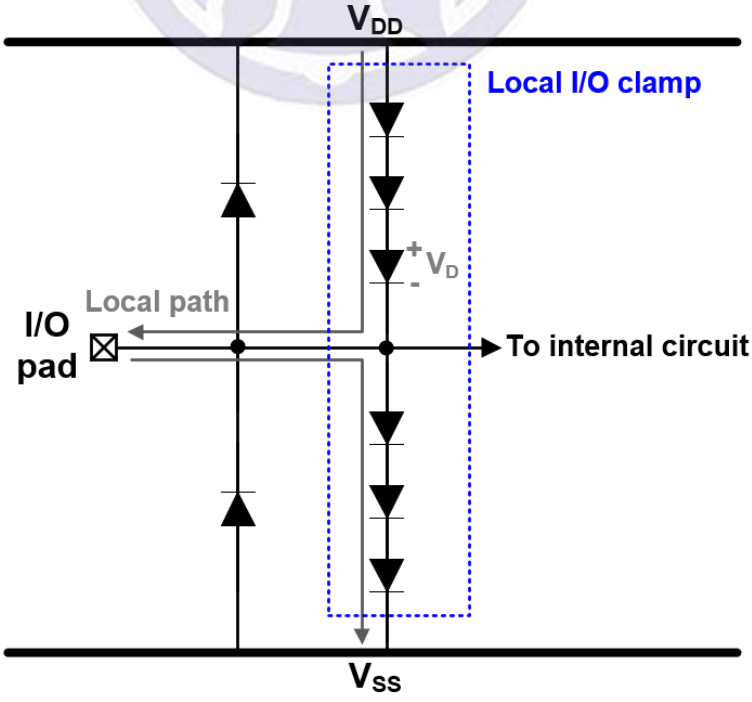


Fig. 2.8. The ESD protection diode with local I/O clamp.

2.4 Whole-Chip ESD Protection Circuit Design

Although the diode can effectively prevent ESD events from the I/O pad, it does not provide ESD protection between the power lines (V_{DD} to V_{SS}). To solve this problem, a power-rail ESD clamp circuit is added between the positive and negative power lines of the circuit [27], as shown in Fig. 2.9. When the ESD event occurs in the power lines, it will discharge through the clamp. In addition, this power clamp also provides two ESD paths (PS-mode and ND-mode) of I/O pad. The methods for implementing power-rail ESD clamp have been proposed in previous literature [28]. Fig. 2.10 shows the typical power clamp circuit consists of a RC inverter with a large size of NMOS (M_{Clamp}). The rise time of the power-supply voltage is approximately milliseconds during normal operation. Therefore, the potential on the transistor capacitor (C) is high and the gate potential of M_{Clamp} is low. The rise time of ESD event is about nanoseconds. When an ESD event occurs between power lines, the capacitance cannot be charged to a high potential due to the RC time-constant. At this time, the gate potential of M_{Clamp} is high

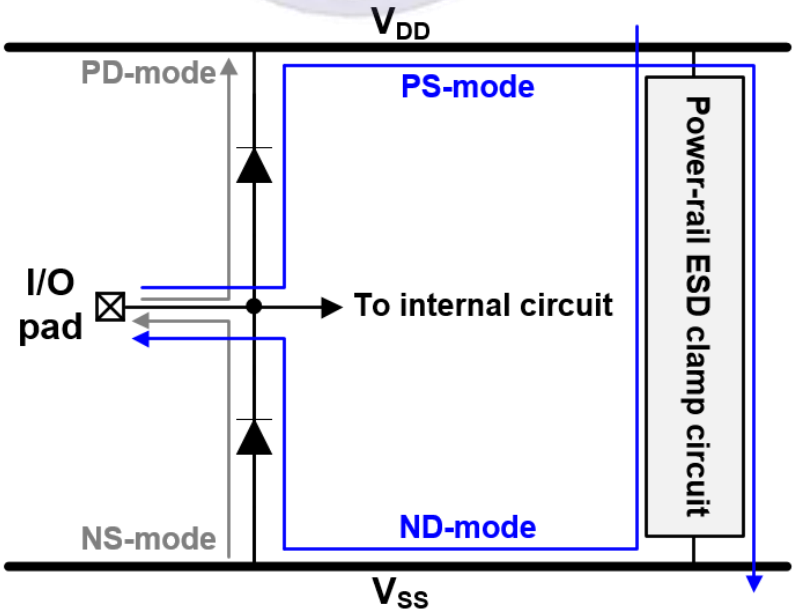


Fig. 2.9. The whole-chip ESD protection design.

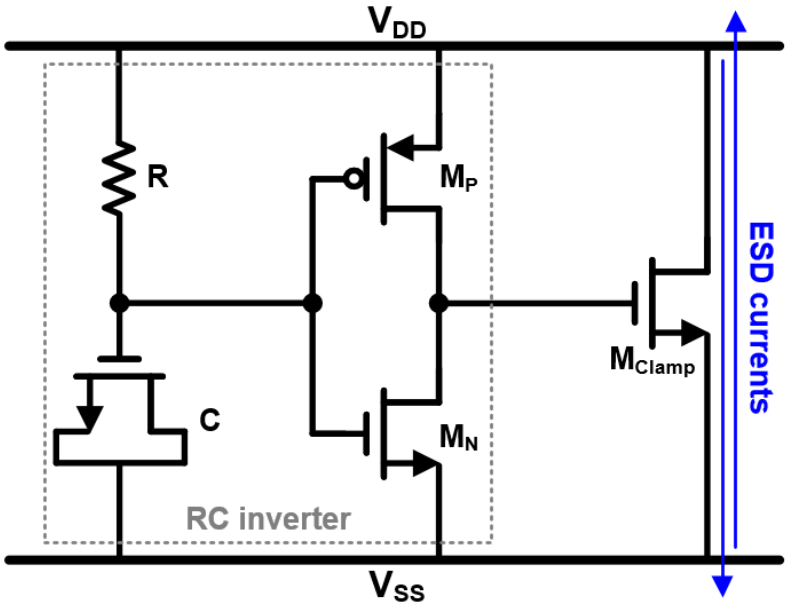


Fig. 2.10. The typical power-rail ESD clamp circuit.

level and the ESD current can be discharged through M_{Clamp}. RC inverter is the circuit that triggers M_{Clamp}. The main discharge capacity of power clamp depends on the M_{Clamp}, so the dimension of M_{Clamp} must be large enough (follow the process specification). In order to truly avoid the ESD damage of internal circuit, designers must pay attention on the whole-chip ESD protection.

2.5 I/O Cell Library

In general, the I/O cells surround the periphery of the integrated circuit, as shown in Fig. 2.11. There are some established devices in the I/O cell library that provide complete ESD protection for the integrated circuit. The I/O cell library contains the ESD protection circuits for input, output, and power lines [29]. In addition, there is an output driver responsible for driving the output stage in the I/O cell library. The choice of ESD protection device in I/O cell includes diode, SCR, MOS, etc. In this thesis, a diode with simple structure and high ESD robustness is selected. There are some implementations

of power cell, the common one is a RC inverter with a large size of NMOS. The output driver is a buffer composed of PMOS and NMOS [30]. The output driver has two parasitic PN paths to provide ESD protection at the output. However, this thesis focuses on the design of I/O cell while the power cell and output driver are for reference only. According to the different conditions of process, designer should select an appropriate I/O cell to connect the integrated circuit with external. In addition, the design of I/O cell should take into account different circuit applications.

For the high-frequency applications, the parasitic effects of traditional I/O cell will result in signal loss. Although the traditional I/O cell provides ESD protection of integrated circuit, it will cause the distortion of the circuit characteristics. Based on this problem, this thesis proposed a deformed I/O cell with low-loss I/O pad and ESD protection device. The deformed I/O cell can effectively prevent the signal loss generated by ESD protection device at high frequencies. In addition, the integrated circuit with the deformed I/O cell can save a lot of chip area, as shown in Fig. 2.12. The

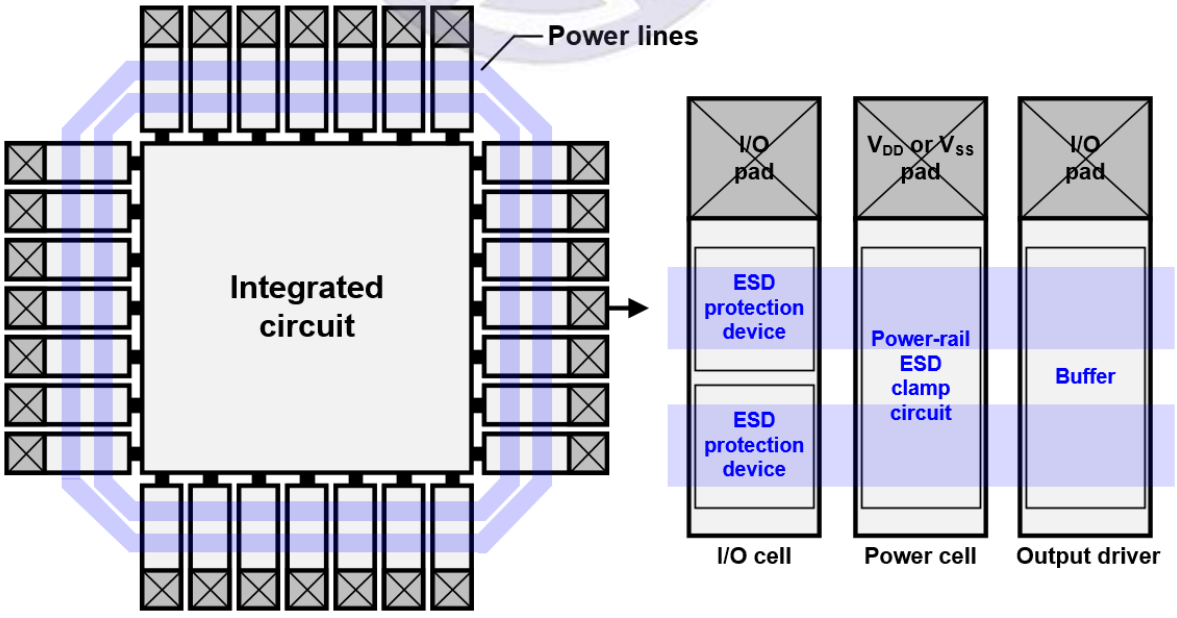


Fig. 2.11. The integrated circuit with traditional I/O cells.

design principle of this deformed I/O cell will be introduced in the next chapter, which contains the structure of low-loss I/O pad with dual-diode ESD protection and its high-frequency characteristics.

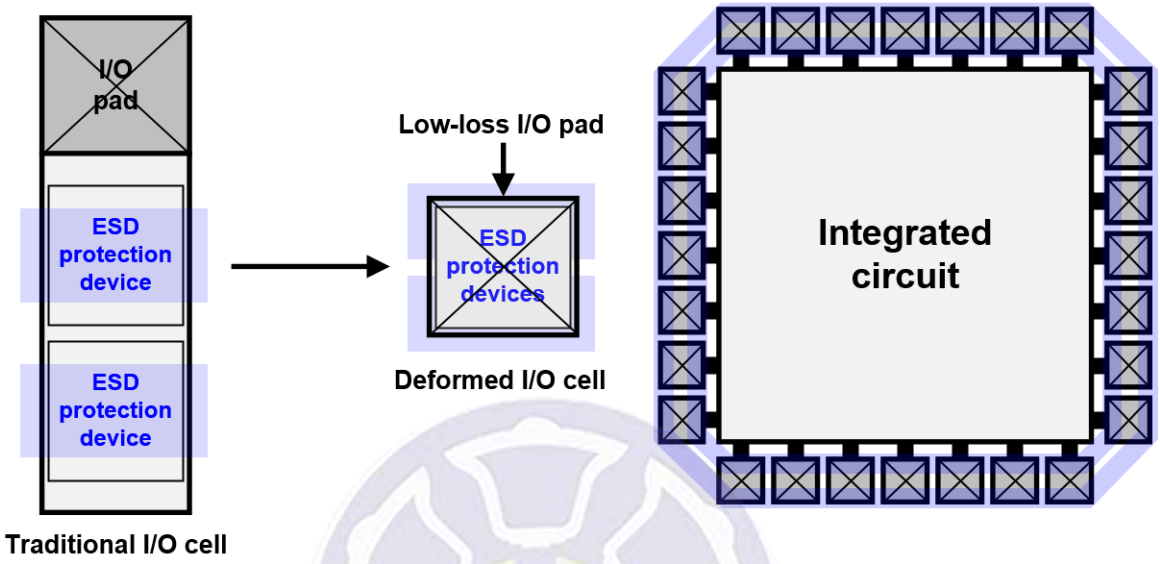


Fig. 2.12. The integrated circuit with deformed I/O cells.

2.6 Summary of This Chapter

In this chapter, the ESD protection circuit of I/O pad has been introduced. The diode has a simple structure and high discharge capacity, so it is suitable as an ESD protection device for I/O pad. The structure of stacked diodes has also been proposed. The stacked diode not only has an advantage of low parasitic capacitance, but also can be used as a local I/O clamp. In addition, the power-rail ESD clamp should be added to the circuit to provide more comprehensive protection. Finally, the integrated circuit with traditional I/O cell can have complete ESD protection but it still has some shortcomings for high-frequency applications. Based on this, this thesis proposed a concept of deformed I/O cell and the details will be introduced in the next chapter.

Chapter 3

Low-Loss I/O Pad with ESD Protection for High-Frequency Circuits

In this chapter, the ESD protection design applied in high-frequency of K/Ka-bands will be introduced. The traditional ESD protection diode has a problem of parasitic capacitance that cause the signal loss at high-frequency operation. Therefore, this chapter will introduce a low-loss I/O pad with dual-diode ESD protection. This design can significantly eliminate the effect of parasitic capacitance in K/Ka-bands.

3.1 Layout Design of Dual-Diode ESD Protection

Fig. 3.1 shows the device cross-sectional view of dual diodes (DD). For the P-type diode (D_P), the I/O pad is connected to P+ diffusion and the V_{DD} is connected to N+ diffusion. The ESD current is bi-directionally discharged from I/O pad to V_{DD} when the ESD events occur. For the N-type diode (D_N), the I/O pad is connected to N+ diffusion and the V_{SS} is connected to P+ diffusion. The ESD current is bi-directionally discharged from V_{SS} to I/O pad when the ESD event occurs. The D_P and D_N are combined into dual diodes (DD) to discharge positive current from I/O pad to V_{DD} (PD-mode) and negative current from I/O pad to V_{SS} (NS-mode). In order to compare the ESD robustness and the value of parasitic capacitance between different size of DD, three sizes of DD have been designed in this thesis. The layout top view of DD is shown in Fig. 3.2. The length (L) is fixed to 1.92μm and the width (W) is designed to be 40μm, 80μm, and 120μm.

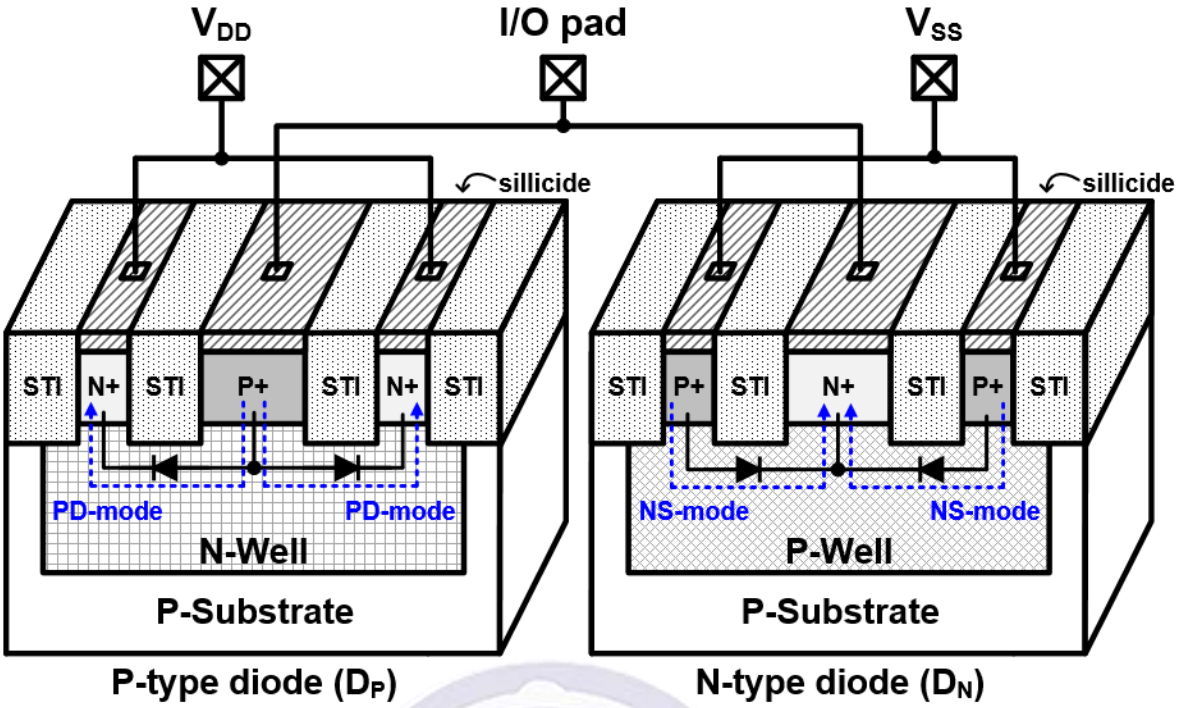


Fig. 3.1. The device cross-sectional view of dual diodes (DD).

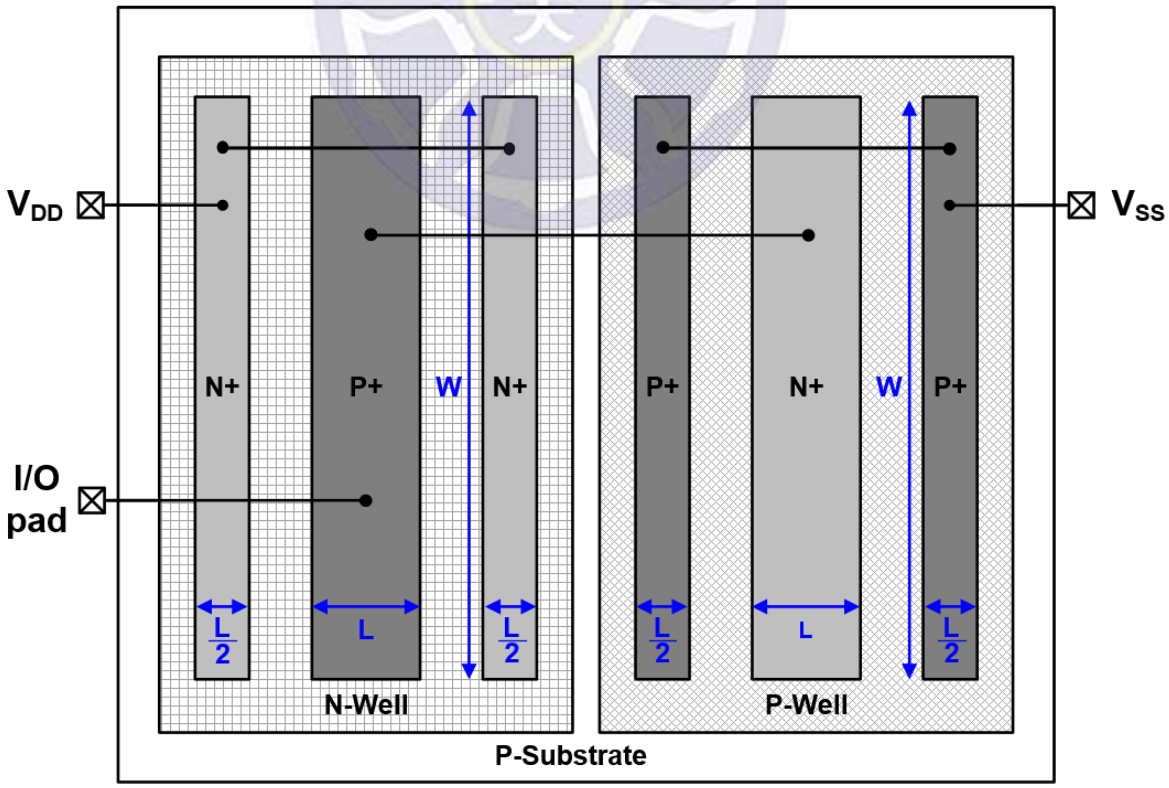


Fig. 3.2. The layout top view of dual diodes (DD).

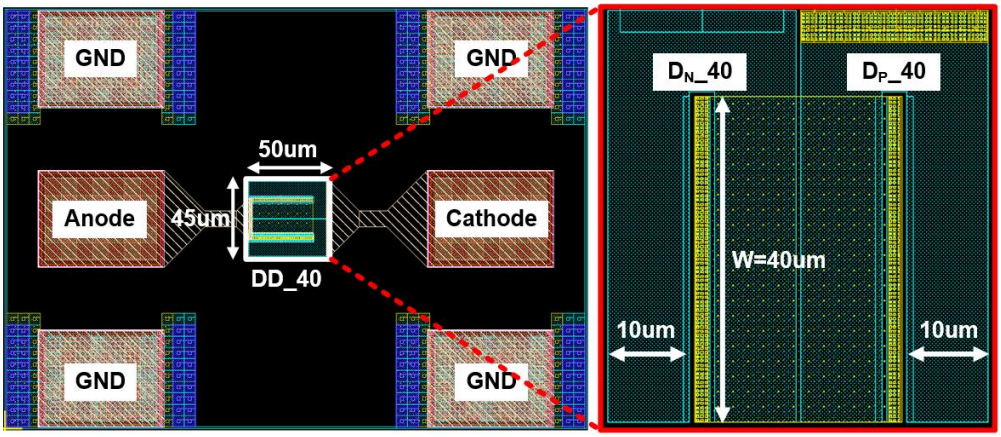
The length of diffusions connected to the I/O pad are two times larger than the diffusions connected to the V_{DD} or V_{SS}. This is for the uniformity of ESD current discharge.

Fig. 3.3 (a) shows the layout top view of DD with the diode width of 40μm (DD_40). The DD_40 contains a P-type diode (D_P_40) and an N-type diode (D_N_40). Fig 3.3 (b) shows the layout top view of DD with the diode width of 80μm (DD_80). The DD_80 is composed of two DD_40 in parallel. Fig 3.3 (c) shows the layout top view of DD with the diode width of 120μm (DD_120). The DD_120 is composed of two P-type diodes (D_P_60) and N-type diodes (D_N_60) with the diode width of 60μm. In order to withstand ESD stress, the metal lines of DD are greater than 10μm. The design parameters of these dual diodes are organized in Table 3.1. The large size of dual diodes provides better ESD robustness, but parasitic capacitance may increase proportionally. The simulation of signal loss caused by the parasitic capacitance of dual diodes will be mentioned in Section 3.5.

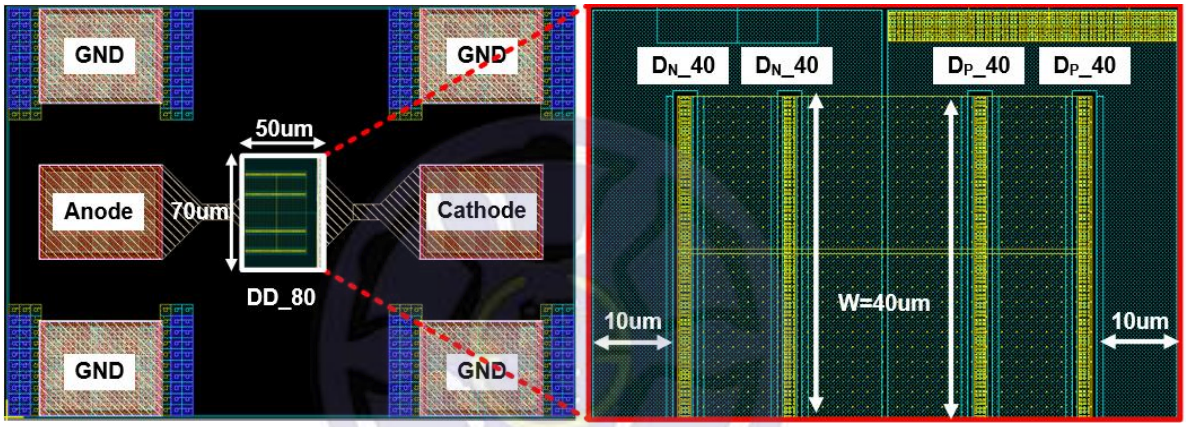
Table 3.1

The design parameters of ESD protection dual diodes.

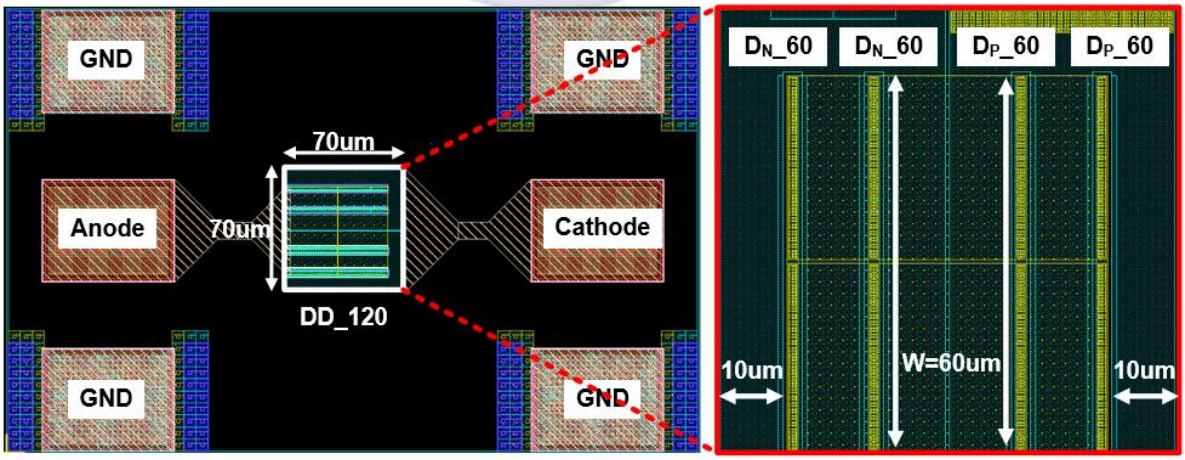
Dual diodes	Diode	Diode length (μm)	Diode width (μm)	Layout area (μm^2)
DD_40	D_P_40	1.92	40	2250
	D_N_40			
DD_80	D_N_40×2	1.92	80	3500
	D_N_40×2			
DD_120	D_P_60×2	1.92	120	4900
	D_P_60×2			



(a)



(b)



(c)

Fig. 3.3. The layout top views of dual diodes (DD) with the diode width of (a) 40μm (DD_40), (b) 80μm (DD_80), and (c) 120μm (DD_120).

3.2 Traditional I/O Pad with Dual-Diode ESD Protection

The ESD protection design of traditional I/O pad with dual diodes (DD) and the structure of traditional I/O pad will be introduced in this section. Fig. 3.4 shows the equivalent circuit of traditional I/O pad with ESD protection dual diodes (DD) for high-frequency circuit. The P-type diode (D_P) and N-type diode (D_N) are combined into dual diodes (DD) at I/O pad to discharge ESD current in the forward-biased condition. Two ESD-current paths are provided for I/O pad, including positive current from I/O to V_{DD} (PD-mode) and negative current from I/O to V_{SS} (NS-mode). The parasitic capacitances of D_P and D_N are C_P and C_N, respectively. The parasitic capacitances are the low impedance paths that causing the input signal continuously loss when the circuit operates at high frequencies. In addition, there are parasitic capacitance (C_{Sub}) and resistance (R_{Sub}) between the I/O pad and substrate [31], which also cause signal loss.

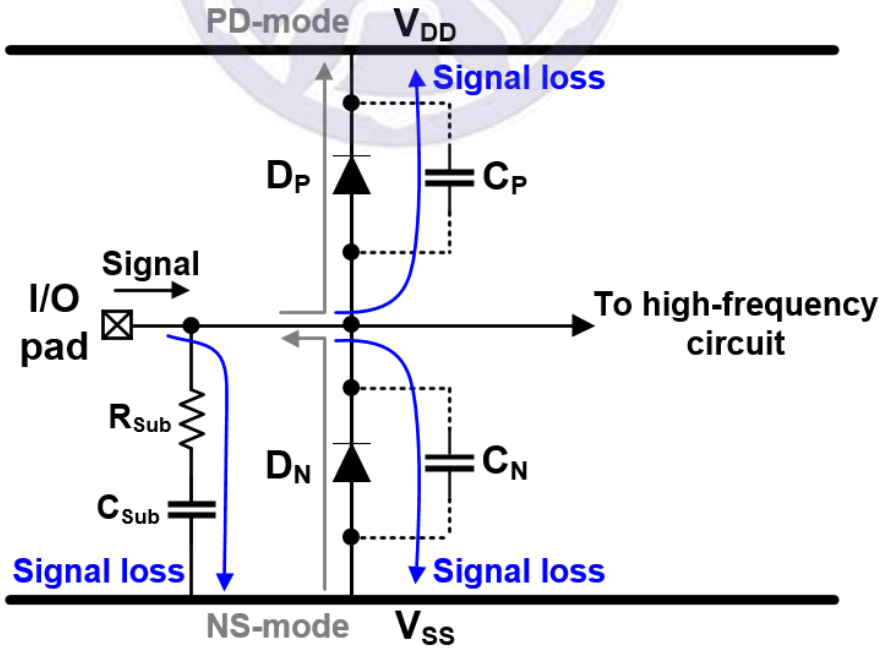


Fig. 3.4. The ESD protection design of traditional I/O pad with dual diodes (DD) for high-frequency circuit.

Fig. 3.5 shows the structure of traditional I/O pad with dual-diode ESD protection (DD) for high-frequency circuit. There are six layers of metal available in CMOS 0.18μm process. The I/O pad is made of the top metal plate (metal-6 and metal-5) and the window is defined as the area where the isolation is removed (the area of blue dotted line). The window area of traditional I/O pad is 50μm×50μm. Due to the specification from foundry, the window area cannot be less than 2500μm. The layout top views of traditional I/O pad with different size of dual diodes (DD) are shown in Figs. 3.6 (a), (b), and (c). Each test device is in the form of ground-signal-ground (GSG) pad. The traditional I/O pad cannot eliminate the effects of parasitic capacitance, so an improved architecture of I/O pad will be introduced in the next section.

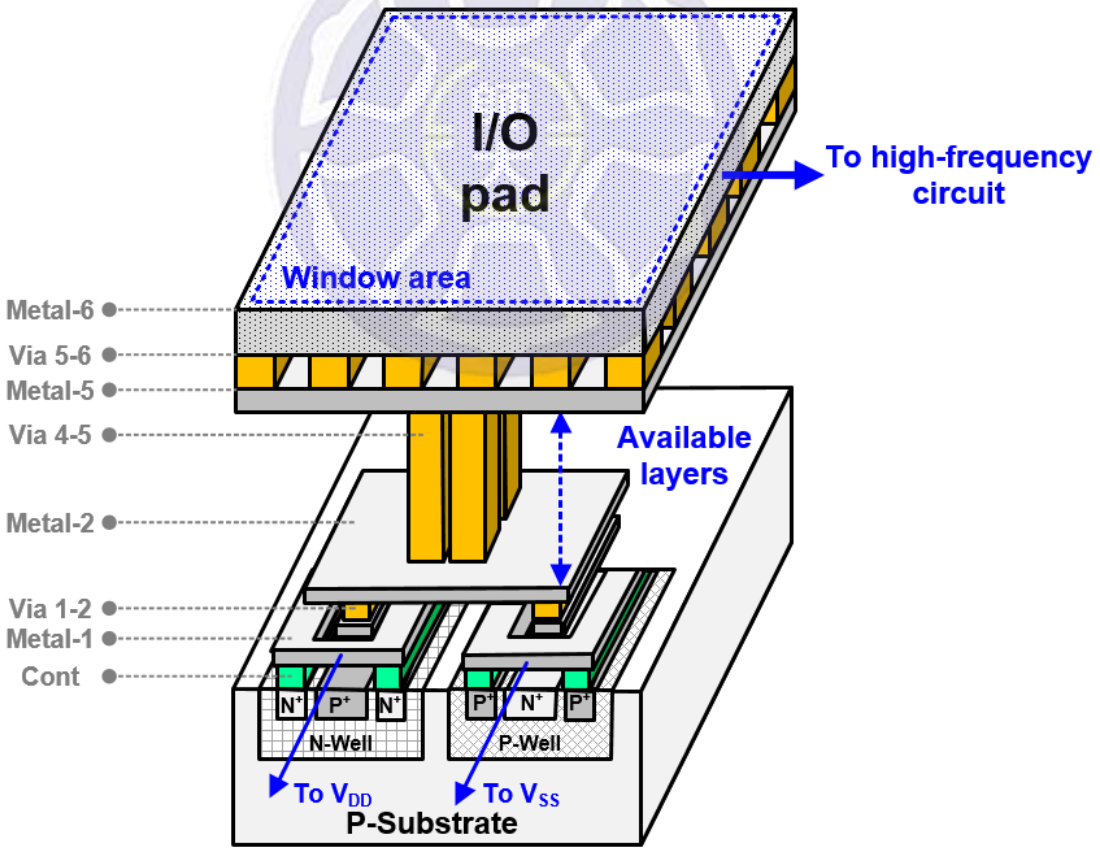
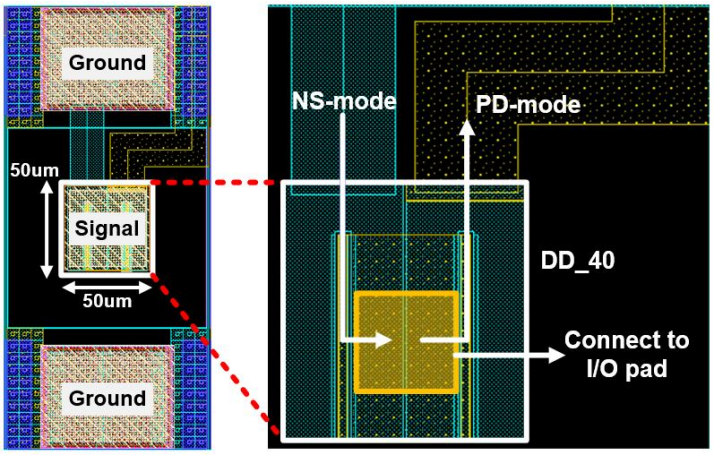
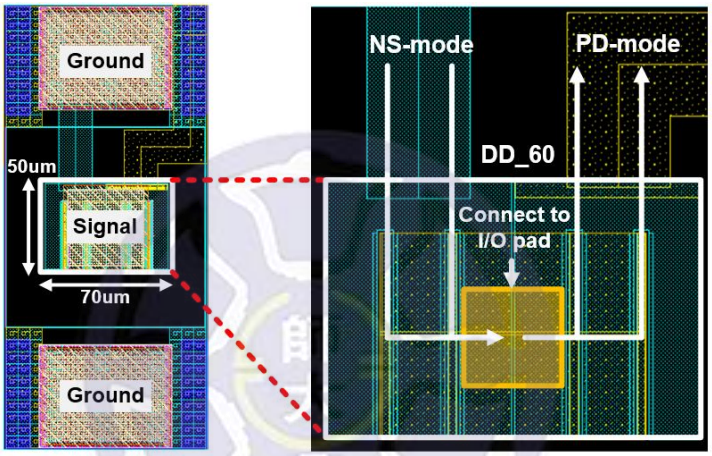


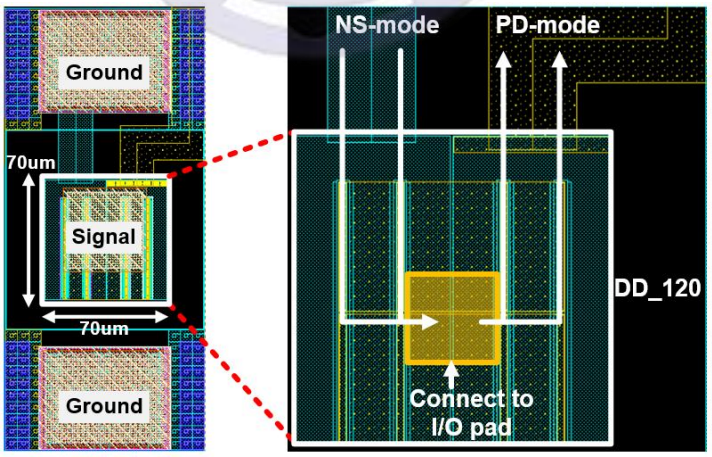
Fig. 3.5. The structure of tradional I/O pad with dual-diode ESD protection (DD) for high-frequency circuit.



(a)



(b)



(c)

Fig. 3.6. The layout top views of tradtional I/O pad with dual diodes (a) W=40μm (DD_40), (b) W=80μm (DD_80), and (c) W=120μm (DD_120).

3.3 Low-Loss I/O Pad with Dual-Diode ESD Protection

An inductive pad that eliminates the effect of parasitic capacitance will be introduced in this section. Fig. 3.7 shows the proposed ESD protection design with stacked inductor and dual diodes at I/O for high-frequency circuit. The proposed I/O pad is designed as a stacked inductor and then connected to the dual-diode ESD protection. The dual diodes are composed of D_P and D_N with the parasitic capacitance C_P and C_N. For the stacked inductor model (the range of blue dotted line), L and R_L are the equivalent inductance and resistance of stacked inductor, respectively. C_L is the parasitic capacitance between the metal layers in the stacked inductor. C_{f1} and C_{f2} are the fringe capacitance between the stacked inductor and substrate. C_{Sub} and R_{Sub} are the parasitic capacitance and resistance of substrate. In order to easily analyze the working principle of this design, the next step is to simplify the circuit of Fig. 3.7.

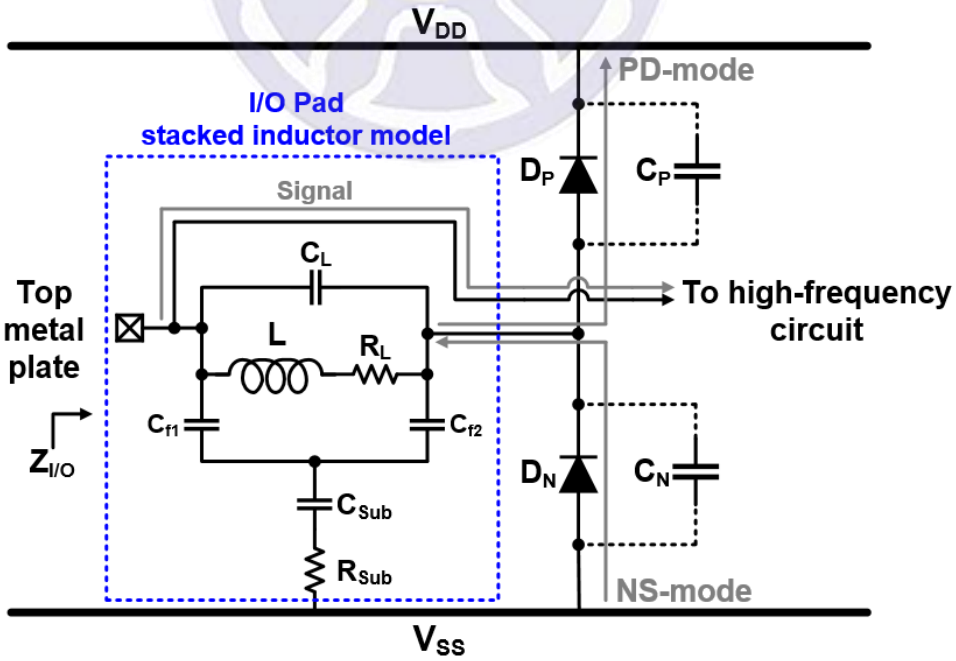


Fig. 3.7. The proposed ESD protection design with stacked inductor and dual diodes at I/O for high-frequency circuit.

As shown in Fig. 3.8 (a), the Z_{f1} and Z_{f2} are the impedance of C_{f1} and C_{f2}, respectively. Z_{Sub} is the equivalent impedance of substrate, such as Eq. (1).

$$Z_{f1} = \frac{1}{j\omega C_{f1}} \;;\; Z_{f2} = \frac{1}{j\omega C_{f2}} \;;\; Z_{Sub} = R_{Sub} + \frac{1}{j\omega C_{Sub}} \tag{1}$$

As shown in Fig. 3.8 (b), the equivalent circuit of the stacked inductor is converted from the Y-model to π-model. The impedanced Z_A, Z_B, and Z_C can be expressed as Eq. (2), where the impedance $Z_M = Z_{f1}Z_{f2} + Z_{f1}Z_{Sub} + Z_{f2}Z_{Sub}$.

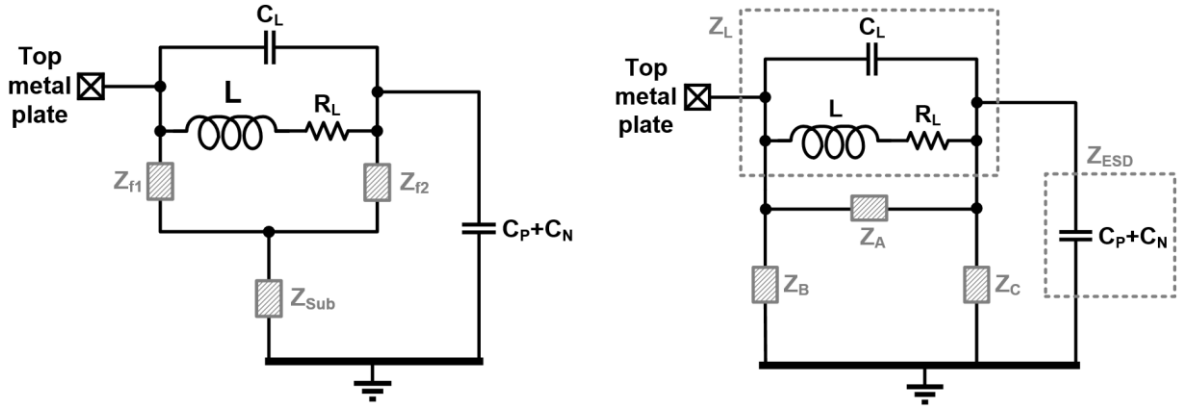
$$Z_A = \frac{Z_M}{Z_{Sub}} \;;\; Z_B = \frac{Z_M}{Z_{f2}} \;;\; Z_C = \frac{Z_M}{Z_{f1}} \tag{2}$$

Therefore, the impedance $Z_{I/O}$ seen from the top metal plate can be expressed as Eq. (3), where the impedance $Z_{ESD} = \frac{1}{j\omega C_P + j\omega C_N}$ and the impedance $Z_L = \frac{1}{\frac{1}{(R_L + j\omega L)} + j\omega C_L}$.

$$Z_{I/O} = Z_B \,//\, [(Z_A // Z_L) + (Z_C // Z_{ESD})] \tag{3}$$

Since the parasitic capacitance and resistance of stacked inductor are weak in K/Ka-bands, the equivalent impedance seen from the top metal plate can be simply expressed as Eq. (4).

$$Z_{I/O} \approx j\omega L + \frac{1}{j\omega(C_P + C_N)} \tag{4}$$



(a) (b)

Fig. 3.8. The equivalent (a) Y-model and (b) π-model of stacked inductor.

According to the principle of resonance, the imaginary components of Eq. (4) will be zero when the circuit is operated at the resonance angular-frequency ($\omega = \omega_o$). The inductance L of stacked inductor model will resonate with the parasitic capacitance of dual-diode ESD protection. The total parasitic capacitance is sum of C_P and C_N. Therefore, the equation of resonance frequency can be expressed as Eq. (5).

$$F_{(resonance)} = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{L\times(C_P+C_N)}} \quad (5)$$

The $Z_{I/O}$ has the lowest impedance when the circuit is operated at the resonance frequency, $F_{(resonance)}$. However, the signal will be continuously lost to ground. Conversely, the $Z_{I/O}$ has the greatest impedance when the operating frequency is far away from $F_{(resonance)}$, so the signal is difficult to lose. In order to have the lowest signal loss in K/Ka-bands, the $F_{(resonance)}$ must be designed to very low frequencies. It can be observed from the Eq. (5), increasing the values of inductance and parasitic capacitance of diode can reduce the value of $F_{(resonance)}$. Different from the previous studies, the method to reduce the signal loss is to use large parasitic capacitance of ESD protection diodes in this thesis. The signal loss will be shift to low frequencies. Therefore, the high-frequency response of circuit is improved.

In order to make the resonant frequency low enough, the value of inductance need to be large, but it will occupy too much area of the chip. However, another effective method is to increase the value of capacitance, a parallel capacitor (C_M) is placed between the stacked inductor of I/O pad and the dual-diode ESD protection. Fig. 3.9 shows the ESD protection scheme with stacked inductor, dual diodes, and parallel capacitor (C_M). The equivalent impedance seen from the I/O pad, which can be described by Eq. (6).

$$Z'_{I/O} \approx j\omega' L + \frac{1}{j\omega'(C_P+C_N+C_M)} \tag{6}$$

When the value of reactance in Eq. (6) is zero, the angular frequency (ω') is defined as the resonant-angular frequency (ω'_o). According to the principle of LC resonance, the stacked inductor of I/O pad will resonate with the equivalent capacitance seen from the I/O pad, the total capacitance is sum of C_P, C_N and C_M, the formula of resonance frequency changes as follows:

$$F'_{(resonance)} = \frac{\omega'_o}{2\pi} = \frac{1}{2\pi\sqrt{L\times(C_P+C_N+C_M)}} \tag{7}$$

Compare (5) with (7), assuming that the L, C_P and C_N are constant, $Freq'_{(resonance)} < Freq_{(resonance)}$ because of the C_M. Therefore, it is possible to ensure a low resonance frequency and a wider bandwidth at high frequencies.

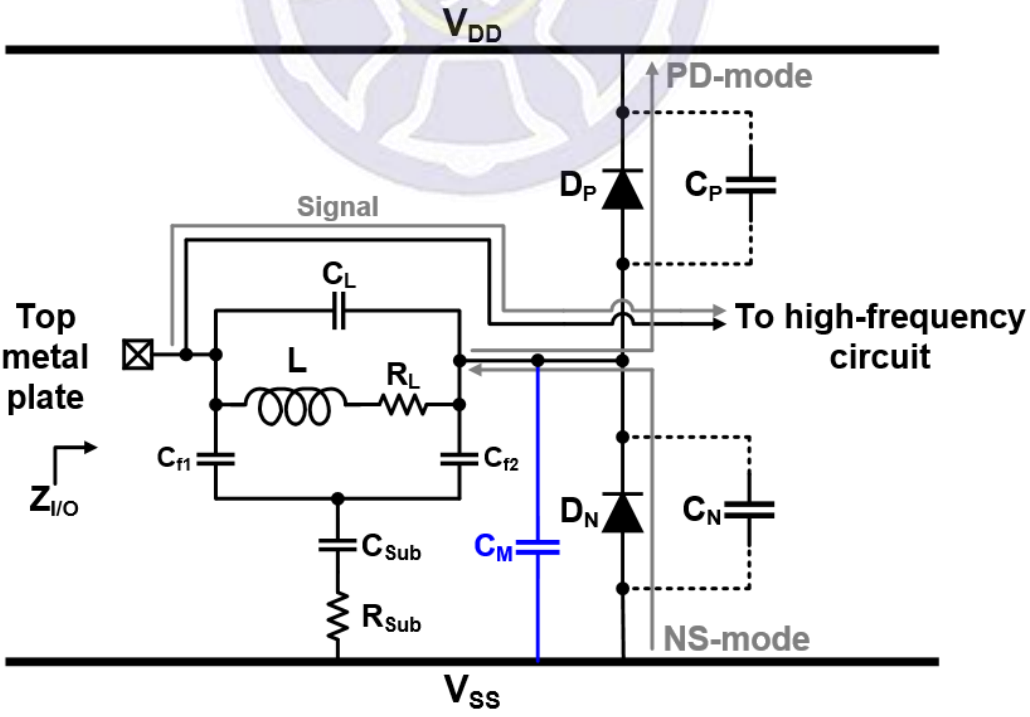


Fig. 3.9. ESD protection scheme with stacked inductor, dual diodes, and parallel capacitor (C_M) at I/O pad for high-frequency circuits.

3.4 Structure Design of Low-Loss I/O Pad

The structure of the inductor in the ESD protection circuit will occupy a large chip area. Therefore, the design of structure will be a challenge. The structure of low-loss I/O pad with stacked inductor and dual-diode ESD protection will be described in detail. This thesis mainly designs two shapes of low-loss I/O pad, which are rectangular and octagonal. Fig. 3.10 shows the structure of rectangular low-loss I/O pad with stacked inductor and dual-diode ESD protection. The top metal plate (metal-6) and stacked inductor (metal-5, metal-4, and, metal-3) are designed as rectangular shapes. The window area is the range in which the insulation of top metal plate is removed (the area of blue dotted line). This window is designed to have a minimum area of 50μm×50μm, which cannot smaller than this due to the process specification. Fig. 3.11 shows the structure of octagonal low-loss I/O pad with stacked inductor and dual-diode ESD protection. The top metal plate (metal-6) and stacked inductor (metal-5, metal-4, and, metal-3) are designed as octagonal shapes. The window area of octagonal low-loss I/O pad is 2737μm^2 (the area of blue dotted line). The stacked inductor of rectangular and octagonal low-loss I/O pads are made of three layers of metal. The purpose of increasing the thickness of stacked inductor is to improve the ESD robustness. In order to save the chip area, the stacked inductor and dual-diode ESD protection are stacked below the top metal plate. In limited area, it is difficult to increase the inductance of stacked inductor. However, it is possible to increase by changing the inductor width, inductor spacing, inner radius, and the number of turns. This thesis designs three different rectangular low-loss I/O pads and an octagonal low-loss I/O pad thorough the modulation of inductance parameters. In order to save chip area, the ESD protection and stacked inductor are designed under the top metal plate.

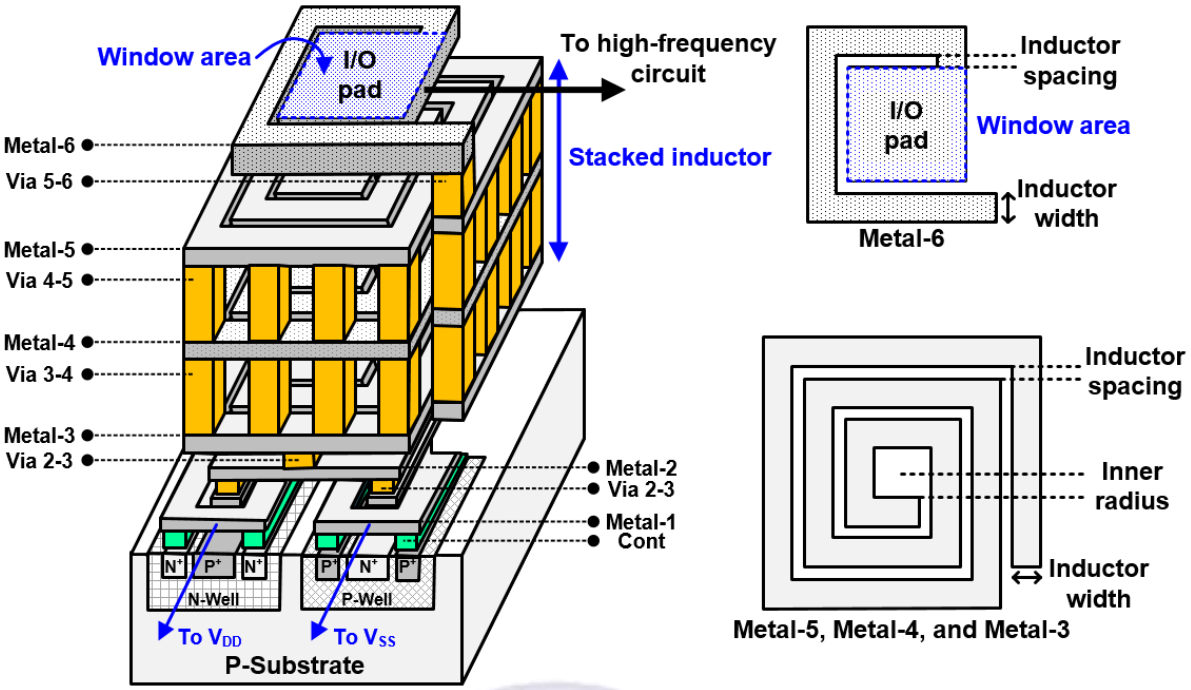


Fig. 3.10. Structure of rectangular low-loss I/O pad with stacked inductor and dual-diode ESD protection.

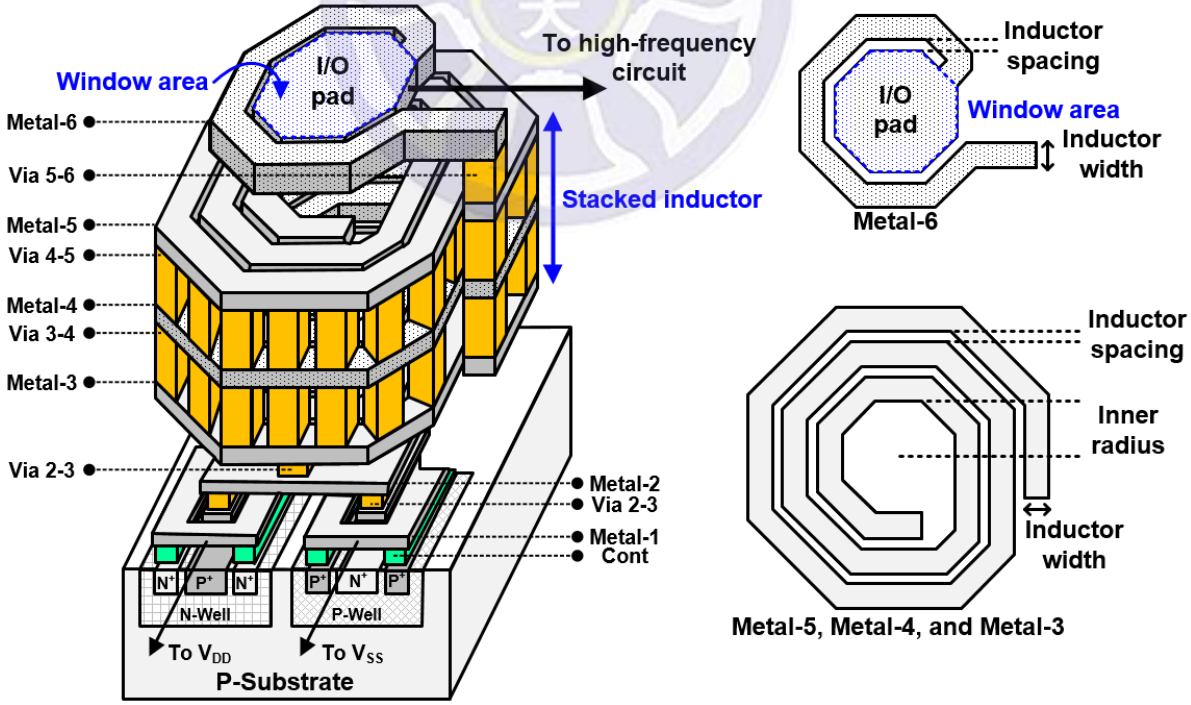


Fig. 3.11. Structure of octagonal low-loss I/O pad with stacked inductor and dual-diode ESD protection.

The layout top views of all low-loss I/O pads are shown in Fig. 3.12. This thesis designs three different forms of rectangular low-loss I/O pad, which are Type I, Type II, and Type III. The stacked inductor (L_1) of Type I has four turns, the inductor width, inductor spacing, and inner radius of L_1 are 6μm, 4μm, and 5μm. The top metal plate (metal-6) of Type I completely overlaps with L_1 and the layout area of Type I is 82μm×82μm, as shown in Fig. 3.12 (a). The stacked inductor (L_2) of Type II has three turns, the inductor width, inductor spacing, and the inner radius of L_2 are 6μm, 4μm, and 19μm. The top metal plate (metal-6) of Type II partially overlaps with L_2 and the layout area of Type II is 90μm×90μm, as shown in Fig. 3.12 (b). The stacked inductor (L_3) of Type III has three turns, the inductor width, inductor spacing, and the inner radius of L_3 are 6μm, 2μm, and 21μm. The top metal plate (metal-6) of Type III non-overlaps with L_3 and the layout area of Type III is 94μm×94μm, as shown in Fig. 3.12 (c). Since the stacked inductors of proposed I/O pads are located below the top metal plate, additional parasitic effect may occur. In order to avoid the additional parasitic effect affecting the high-frequency response of the circuit. Should avoid too much overlap area between the top metal plate and stacked inductor. However, avoiding overlapping area will make the overall area much larger. Base on the considerations of parasitic effect and overall area, partial overlapping (Type II) will be a better choice. Type IV is an octagonal low-loss I/O pad and the top metal plate (metla-6) partially overlaps with the stacked inductor (L_4). The L_4 has three turns, the inductor width, inductor spacing, and the inner radius of L_4 are 6μm, 4μm, and 25μm. The layout area of Type IV is 7457μm^2. The layout top view of Type IV is shown in Fig. 3.12 (d). The design parameters of traditional and proposed I/O pads are shown in Table. 3.2. Although the total area of the proposed I/O pads are ~3 times larger than the traditional I/O pad, the high-frequency response of proposed design will compensate for this disadvantage.

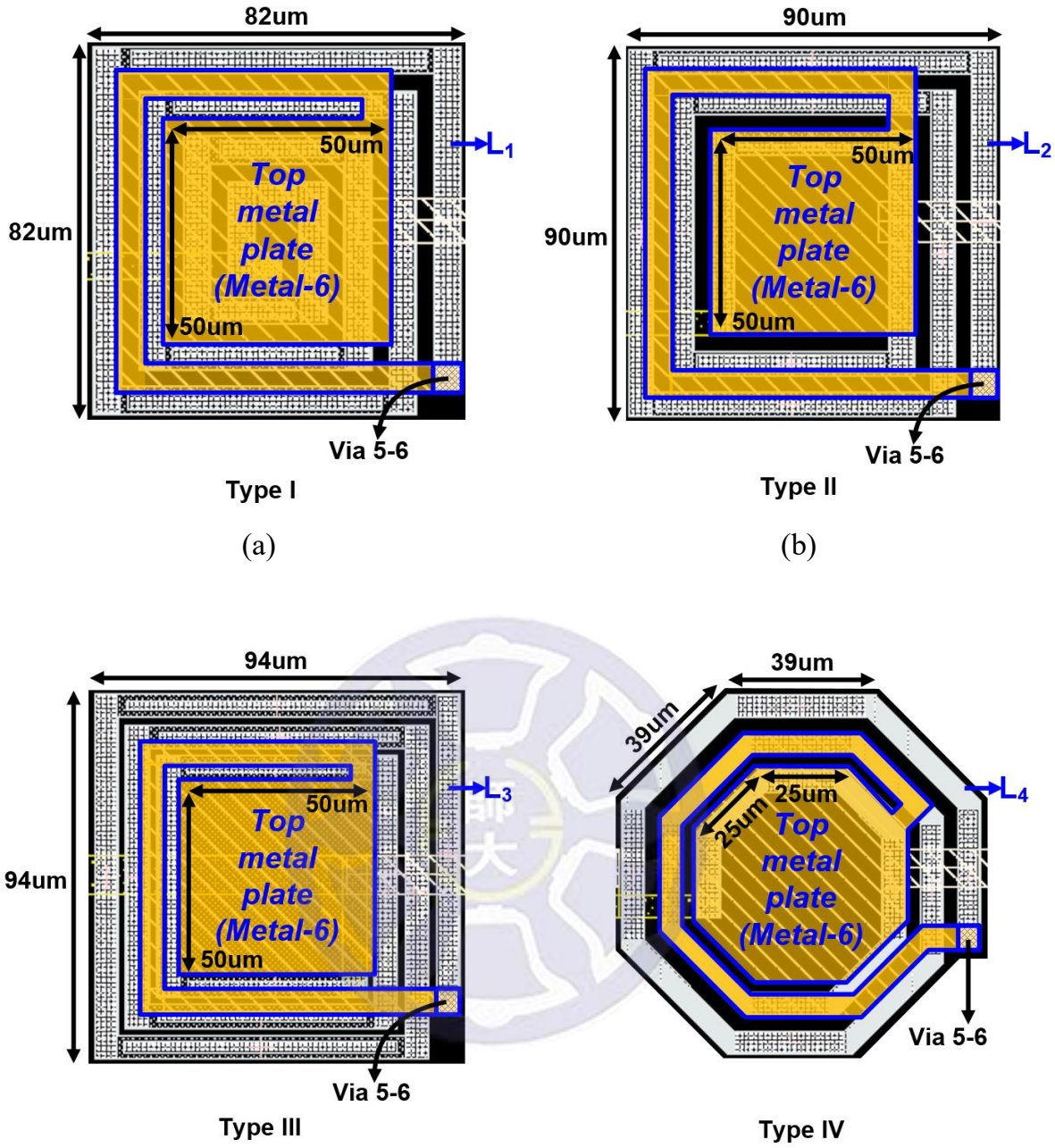


Fig. 3.12. The layout top views of low-loss I/O pads (a) Type I, (b) Type II, (c) Type III, and (d) Type IV.

Table 3.2

The parameters of traditional and proposed I/O pads.

I/O pad	Traditional	Proposed			
		Type I	Type II	Type III	Type IV
Inductor width (μm)	N/A	6	6	6	6
Inductor spacing (μm)	N/A	4	4	2	4
Inner radius (μm)	N/A	5	19	21	25
Number of turns	N/A	4	3	3	3
Window area (μm^2)	2500	2500	2500	2500	2737
Total area (μm^2)	2500	6724	8100	8836	7457

The proposed low-loss I/O pad is used as signal pad and then combines ground pads into ground-signal-ground (G-S-G) pads. The layout top views of Type I with dual-diode ESD protection DD_40, DD_80, and DD_120 are shown in Figs. 3.13 (a), (b), and (c). The Type I with ESD protection has minimal layout area (82μm×82μm) because the top metal plate completely overlaps the stacked inductor L_1. The layout top views of Type II with dual-diode ESD protection DD_40, DD_80, and DD_120 are shown in Figs. 3.14 (a), (b), and (c). Considering the parasitic effect and overall area, the top metal plate of Type II only partially overlaps with the stacked inductor L_2.

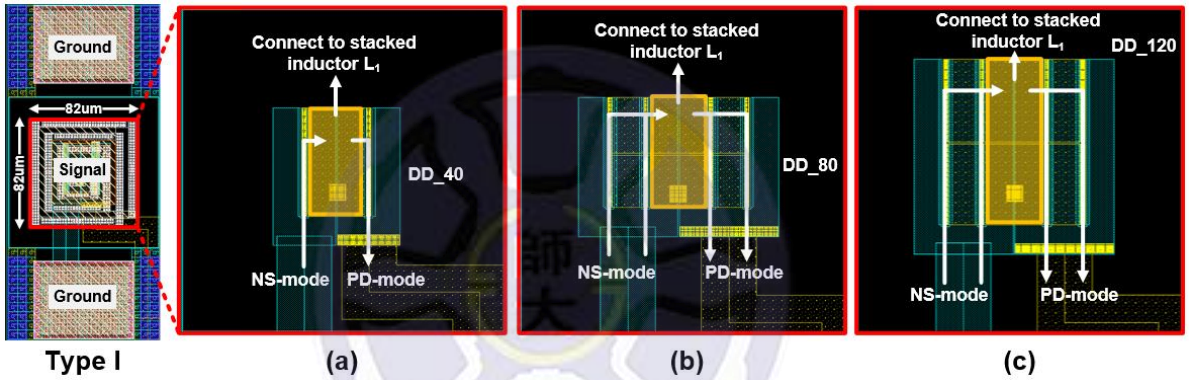


Fig. 3.13. The layout top views of Type I with dual-diode ESD protection (a) DD_40, (b) DD_80, and (c) DD_120.

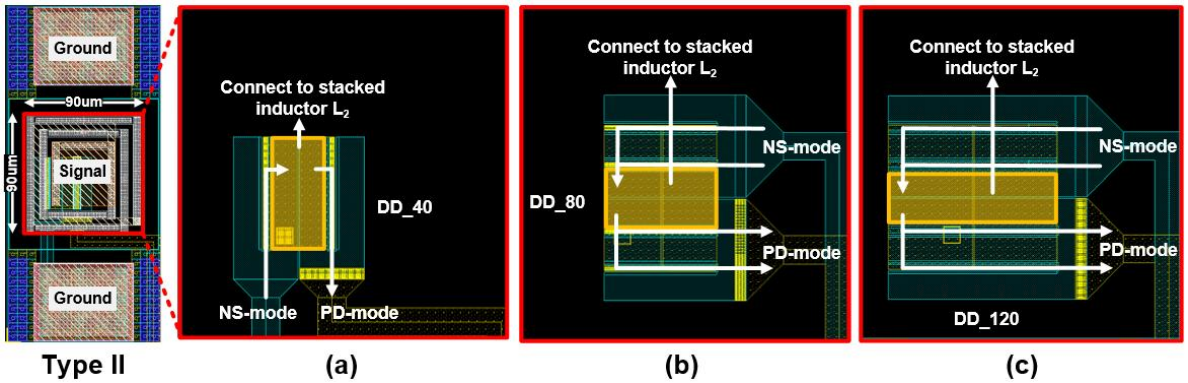


Fig. 3.14. The layout top views of Type II with dual-diode ESD protection (a) DD_40, (b) DD_80, and (c) DD_120.

The layout top views of Type III with dual-diode ESD protection DD_40, DD_80, and DD_120 are shown in Figs 3.15 (a), (b), and (c). The Type II with ESD protection has the largest layout area because the top metal plate non-overlaps with the stacked inductor L_3. The layout top views of Type IV with dual-diode ESD protection DD_40, DD_80, and DD_120 are shown in Figs. 3.16 (a), (b), and (c). The top metal plate partially overlaps with the stacked inductor L_4. All dual diodes are under the proposed low-loss I/O pad, so the total layout areas are unchanged.

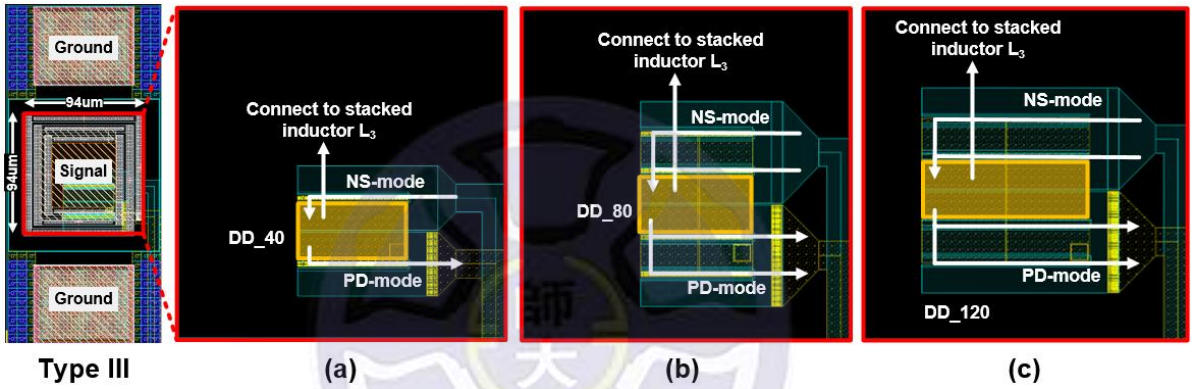


Fig. 3.15. The layout top views of Type III with dual-diode ESD protection (a) DD_40, (b) DD_80, and (c) DD_120.

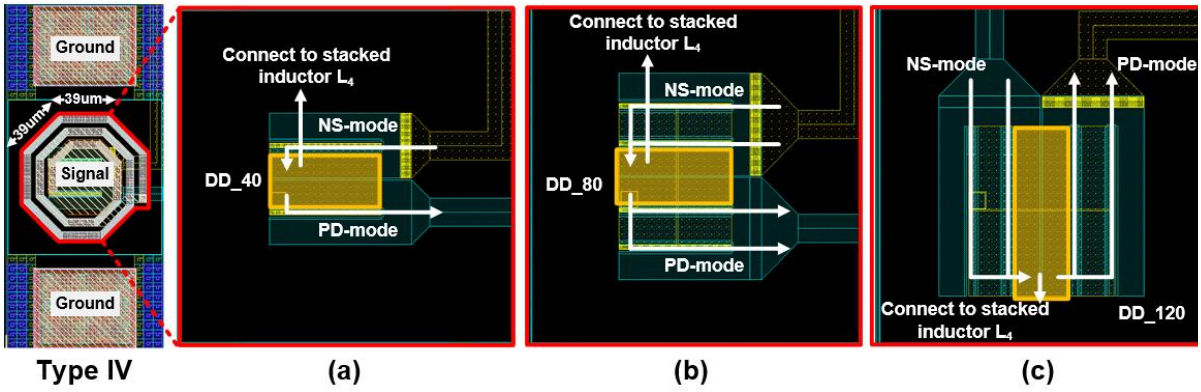
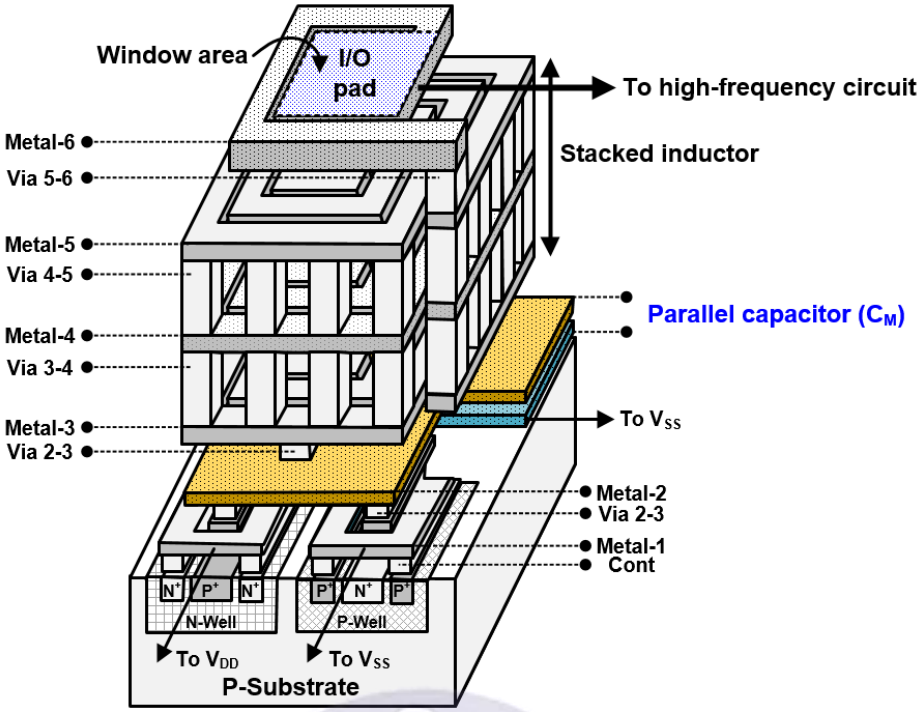


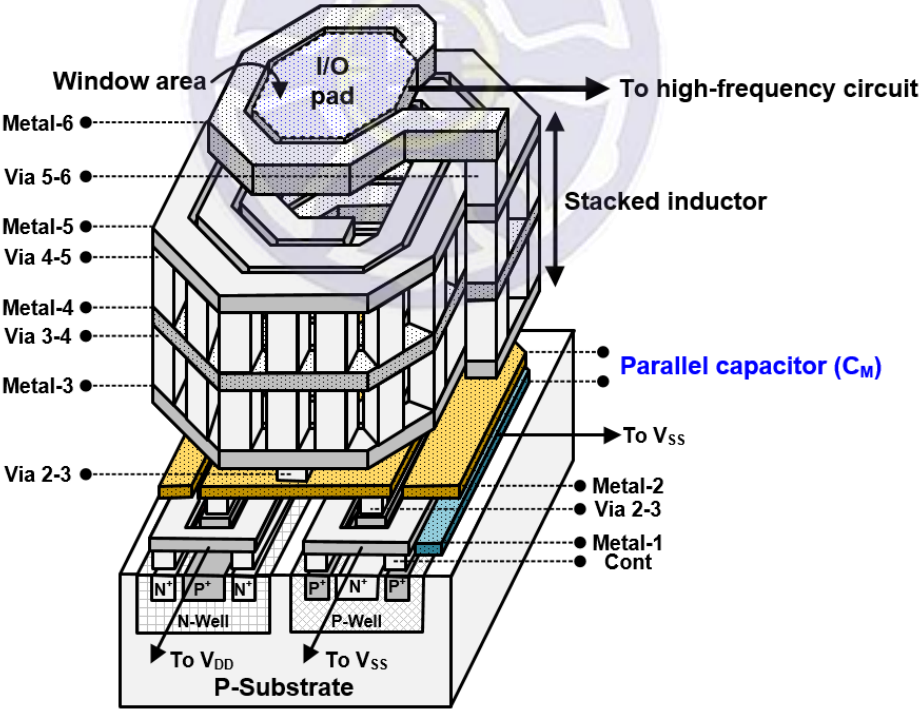
Fig. 3.16. The layout top views of Type IV with dual-diode ESD protection (a) DD_40, (b) DD_80, and (c) DD_120.

To ensure that the resonant frequency of proposed structure is low enough, add a parallel capacitor (C_M) below the stacked inductor. The method is implemented without increasing the chip area. The structure of rectangular and octagonal low-loss I/O pad with parallel capacitor (C_M), stacked inductor, and dual-diode ESD protection are shown in Fig. 3.17 (a) and (b), respectively. The structure of parallel capacitor (C_M) is composed of two parallel metal layers (metal-2 and metal-1). The metal-2 terminal of C_M is connected to the stacked inductor and the metal-1 terminal is connected to V_{SS}. In order to save chip area, the parallel capacitor is designed in the proposed low-loss I/O pad. Fig. 3.17 (a) shows the C_M embedded in the rectangular low-loss I/O pad between the stacked inductor and dual diodes. Fig. 3.17 (b) shows the C_M embedded in the octagonal low-loss I/O pad between the stacked inductor and dual diodes.

Since the dual-diode ESD protection with a diode width of 120μm (DD_120) has a large enough parasitic capacitance, no additional parallel capacitor is needed to compensate. However, the low-loss I/O pads with DD_40 and DD_80 are added to the C_M. The layout top views of low-loss I/O pads with parallel capacitor (C_M) and dual-diode ESD protection (DD_40 and DD_80) are shown in Figs. 3.18 (a), (b), (c), and (d). It can be observed that the form of the parallel capacitor has changed with the different size of dual-diode ESD protection. The low-loss I/O pad with DD_40 is allowed to design a larger C_M in it. However, the low-loss I/O pad with DD_80 can only place C_M in limited space. The layout area of traditional and proposed I/O pads with dual-diode ESD protection are compared in Table 3.3. For the traditional I/O pad, the total layout area with DD_80 and DD_120 will exceed the top metal plate (50μm×50μm). For all proposed I/O pads, the dual-diode ESD protection, stacked inductor, and parallel capacitor are below the top metal plate.

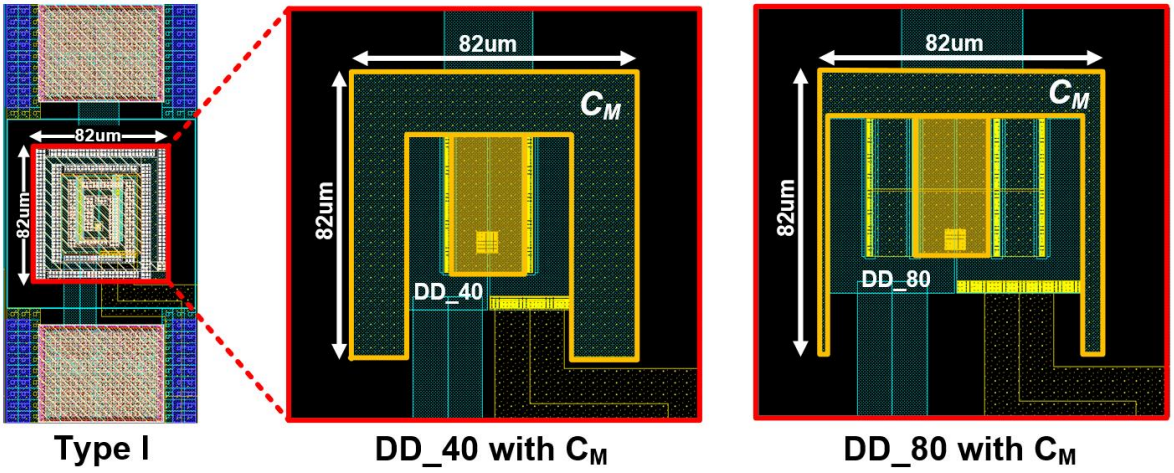


(a)

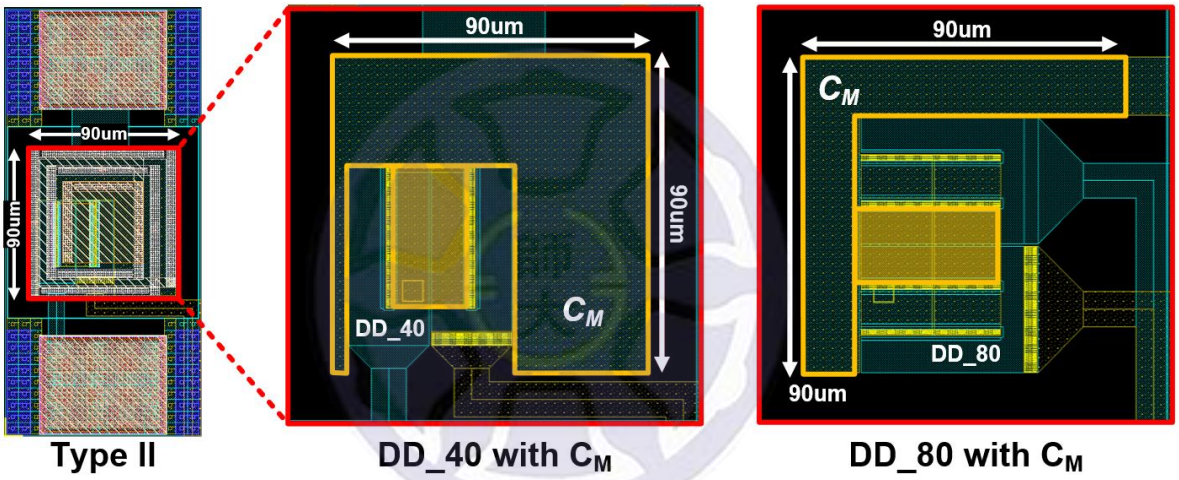


(b)

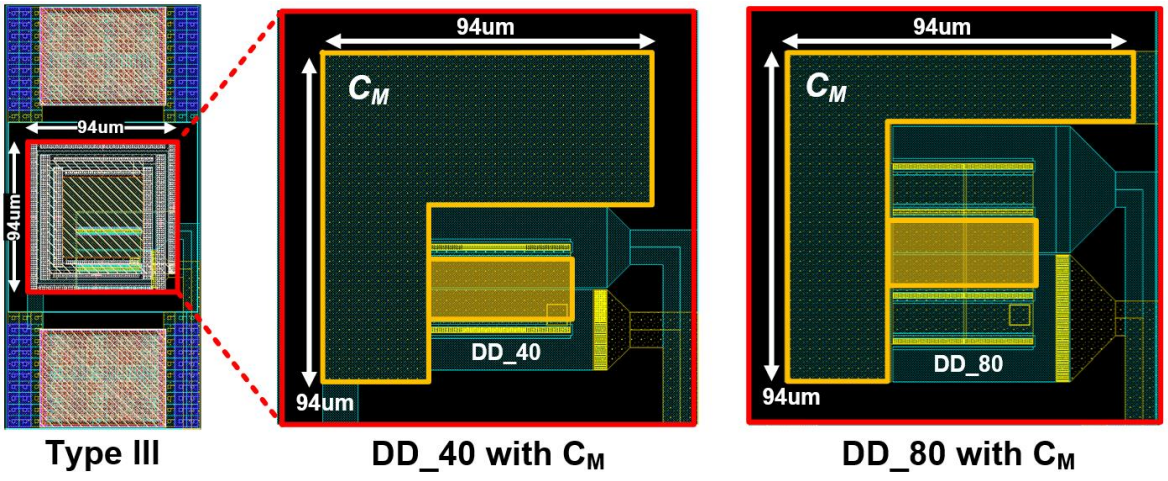
Fig. 3.17. The structrues of (a) rectangular and (b) octagonal low-loss I/O pad with parallel capacitor (C_M), stacked inductor, and dual-diode ESD protection.


82um
82um
82um
82um
C_M
DD_40
82um
82um
C_M
DD_80
Type I
DD_40 with C_M
DD_80 with C_M

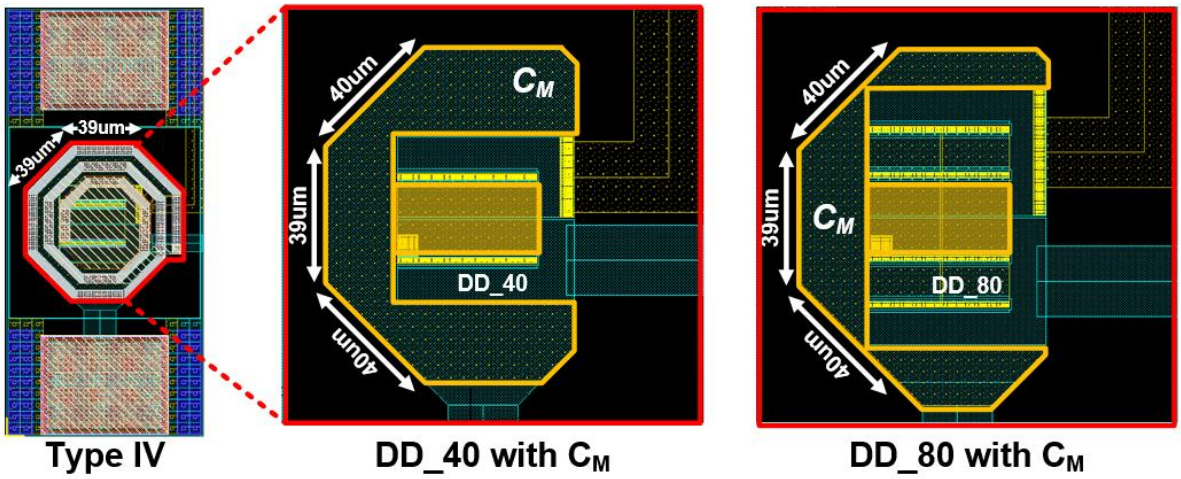
(a)


90um
90um
90um
90um
C_M
DD_40
C_M
90um
90um
C_M
DD_80
90um
Type II
DD_40 with C_M
DD_80 with C_M

(b)


94um
94um
94um
94um
C_M
DD_40
94um
94um
C_M
DD_80
94um
Type III
DD_40 with C_M
DD_80 with C_M

(c)



(d)

Fig. 3.18. The layout top views of low-loss I/O pad (a) Type I, (b) Type II, (c) Type III, and (d) Type IV with parallel capacitor (C_M) and dual-diode ESD protection (DD_40 and DD_80).

Table 3.3

The layout area of traditional and proposed I/O pads with dual-diode ESD protection.

I/O pad	Dual-diode ESD protection	Layout area (μm^2)
Traditional	DD_40	2500
	DD_80	3500
	DD_120	4900
Type I and Type I + C_M	DD_40	6724
	DD_80	
	DD_120	
Type II and Type II + C_M	DD_40	8100
	DD_80	
	DD_120	
Type III and Type III + C_M	DD_40	8836
	DD_80	
	DD_120	
Type IV and Type IV + C_M	DD_40	7457
	DD_80	
	DD_120	

3.5 Simulation Methods and Results

The structures of low-loss I/O pads with stacked inductors have been simulated by Electromagnetic (EM) simulation software to obtain the characteristics of stacked inductors and export the S-parameter files to the Advanced Design System (ADS) software. As shown in Fig. 3.19, the S-parameter model of stacked inductor is converted into the Y-parameter model. The inductance value (L), parasitic resistance (R_L), and quality factor (Q) can be simulated by the Y-parameter model of the stacked inductor. Fig. 3.20 (a) shows the inductance values of stacked inductors L_1, L_2, L_3, and L_4. The inductance values of all stacked inductors are designed around 1nH. The self-resonant frequencies of all stacked inductors are designed around 40GHz. Therefore, the stacked inductors remain inductive in K/Ka-bands. The parasitic resistances and quality factors of stacked inductors are shown in Fig. 3.20 (b) and 3.20 (c), respectively. From the simulation results, it can be confirmed that the octagonal inductor (L_4) has higher quality factor than the rectangular inductors (L_1, L_2, and L_3). The simulation results of stacked inductors at 24GHz are organized in Table 3.4.

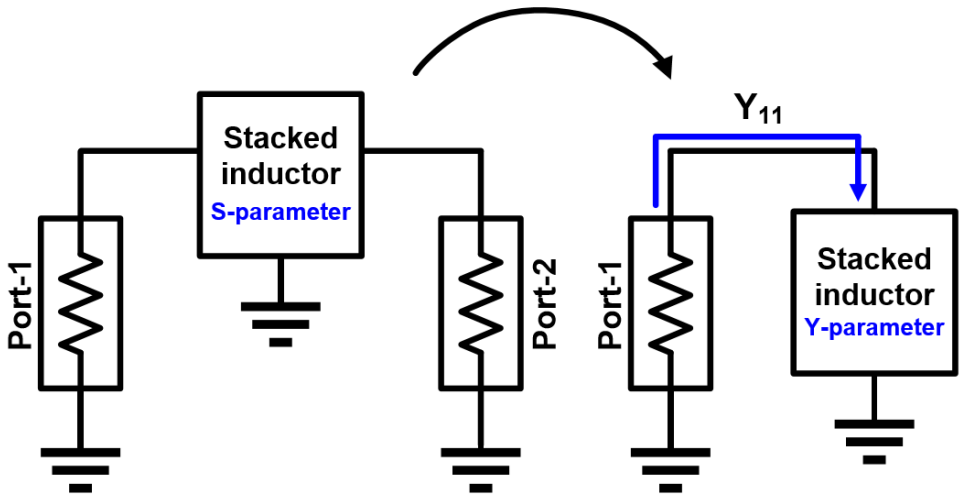
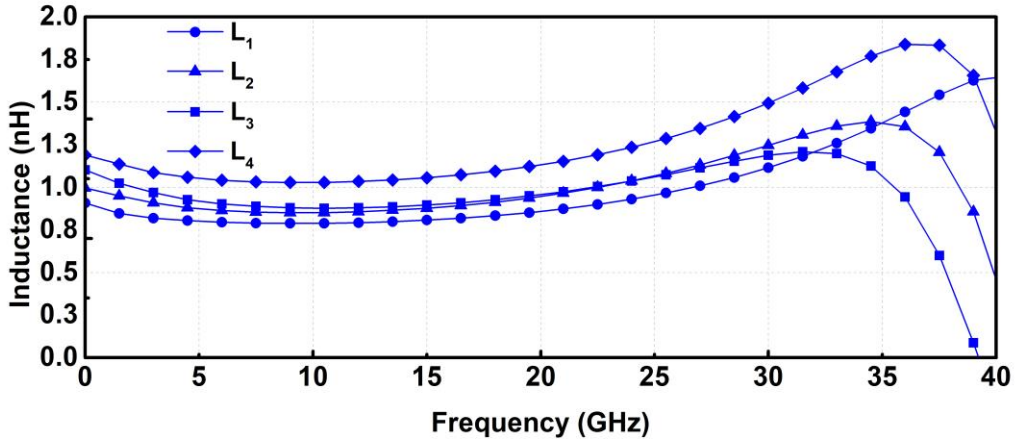
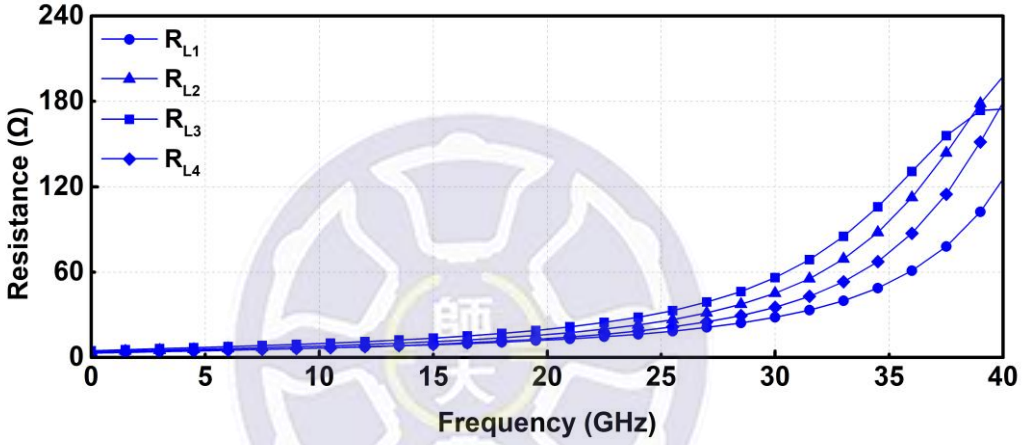


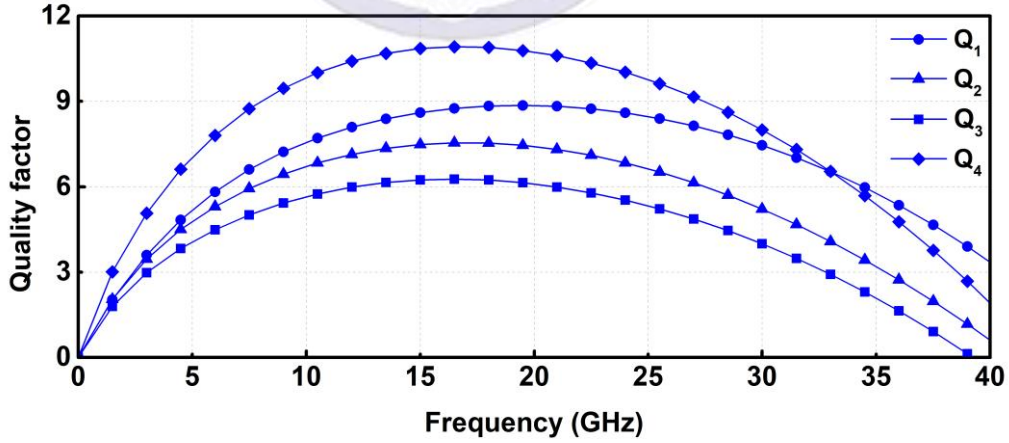
Fig. 3.19. The S-parameter model is converted to the Y-parameter model.



(a)



(b)



(c)

Fig. 3.20. Simulated (a) inductance value (L), (b) parasitic resistance (R_L), and (c) quality factor (Q) of stacked inductors L_1, L_2, L_3, and L_4.

Table 3.4

The simulation results of stacked inductors at 24GHz.

Stacked inductor		Inductance value (nH)	Parasitic resistance (Ω)	Quality factor
Rectangle	L_1	0.95	16.31	8.59
	L_2	1.03	22.86	6.83
	L_3	1.03	28.26	5.52
Octagon	L_4	1.23	18.56	10.02

The structures of traditional and proposed I/O pads have been simulated in EM software. In order to obtain the signal loss of each I/O pad with dual-diode ESD protection, the simulation of two-port network is performed, as shown in Fig. 3.21. The signal losses of traditional and proposed I/O pads with the different size of dual-diode ESD protection are shown in Figs. 3.22 (a), (b), and (c). The largest signal loss of test devices in K/Ka-bands is defined as Loss $_{(max)}$. The resonance frequency is F $_{(resonance)}$, and it should be as far as possible from K/Ka-bands.

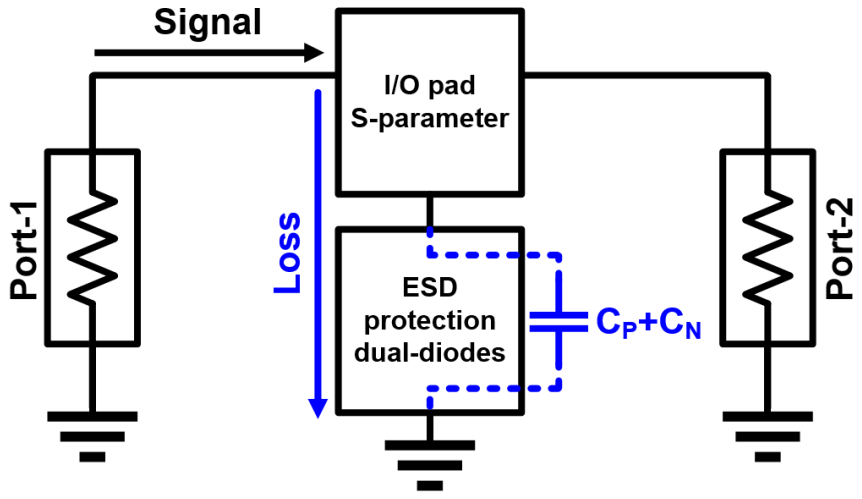
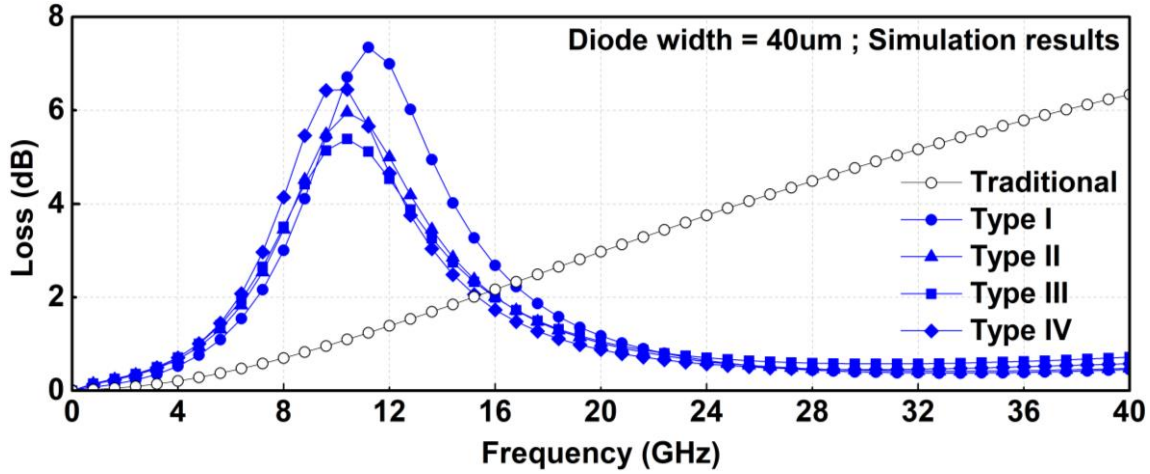


Fig. 3.21. Two-port network.

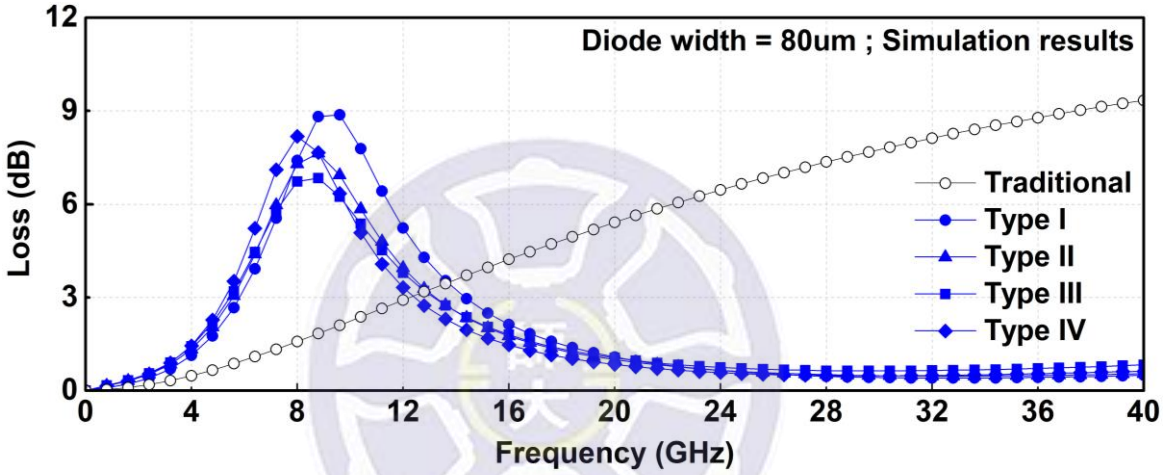
Fig 3.22 (a) shows the signal losses of traditional and proposed I/O pads with the dual-diode ESD protection (W=40μm). It can be clearly observed that the signal loss of traditional I/O pad continues to increase because of the parasitic capacitance of dual-diode ESD protection cannot be eliminated. The Loss $_{(max)}$ of traditional structure reaches 6.33dB. For each proposed I/O pad, the stacked inductor resonates with the parasitic capacitance of dual-diode ESD protection and significantly reduces the signal loss in K/Ka-bands. The Loss $_{(max)}$ of low-loss I/O pads, Type I, Type II, Type III, and Type IV with dual-diode ESD protection (W=40μm) are 1.17dB, 1.01dB, 1.04dB, and 0.87dB.

Fig 3.22 (b) shows the signal losses of traditional and proposed I/O pads with the dual-diode ESD protection (W=80μm). The Loss $_{(max)}$ of traditional structure reaches 9.34dB, which is 1.5 times higher than the Loss $_{(max)}$ of traditional I/O pad with DD_40. It is caused by the larger size of dual diodes. The Loss $_{(max)}$ of low-loss I/O pads, Type I, Type II, Type III, and Type IV with dual-diode ESD protection (W=80μm) are 1.07dB, 0.99dB, 1.04dB, and 0.83dB.

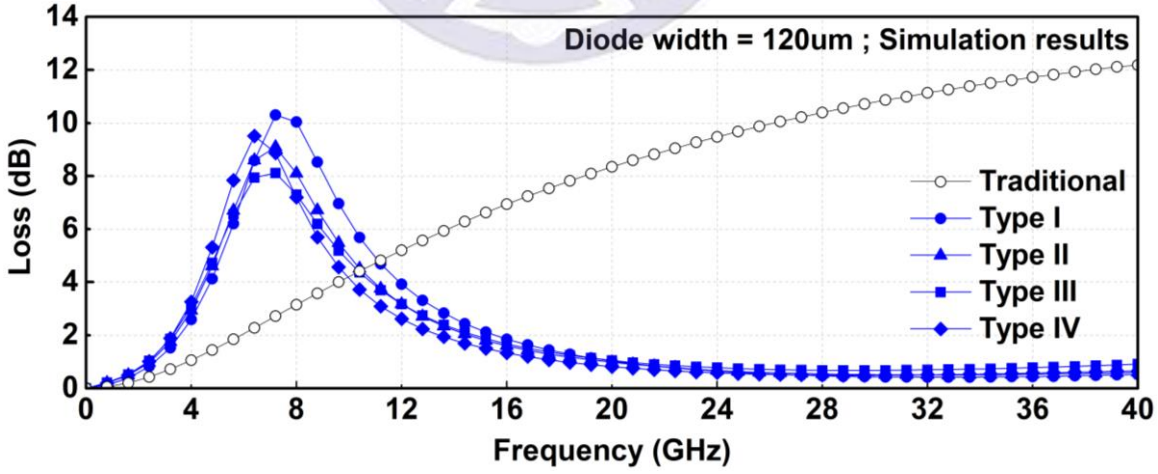
Fig 3.22 (c) shows the signal losses of traditional and proposed I/O pads with the dual-diode ESD protection (W=120μm). The Loss $_{(max)}$ of traditional structure reaches 12.18dB, which is 2 times higher than the Loss $_{(max)}$ of traditional I/O pad with DD_40. It can be observed that the signal loss is proportional to the size of dual-diode ESD protection. The Loss $_{(max)}$ of low-loss I/O pads, Type I, Type II, Type III, and Type IV with dual-diode ESD protection (W=120μm) are 1.02dB, 0.98dB, 0.97dB, and 0.81dB. For each proposed I/O pad, the stacked inductor resonates with the parasitic capacitance of dual-diode ESD protection and significantly reduces the signal loss in K/Ka-bands. The signal losses of the proposed structures are reduced to about 1dB. The simulation results of all test devices are shown in Table 3.5.



(a)



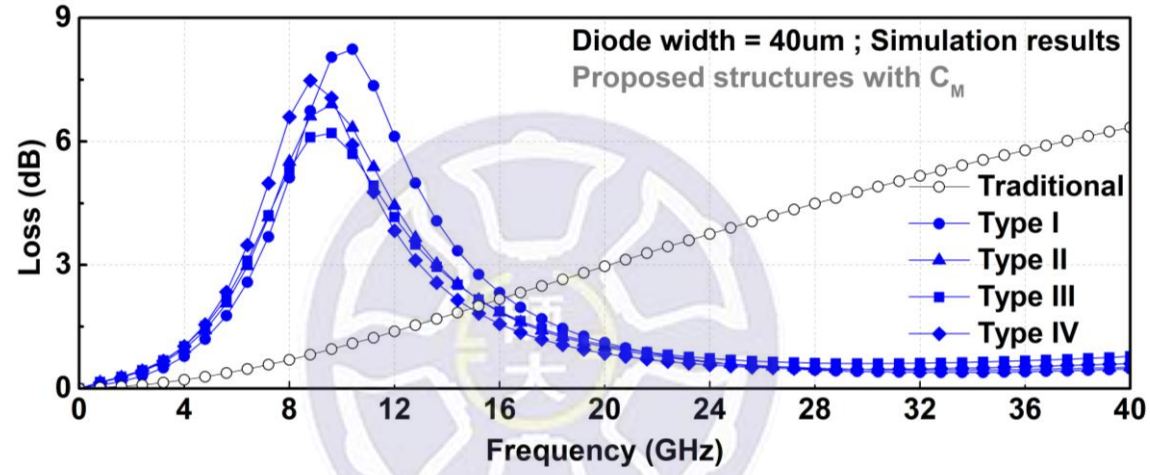
(b)



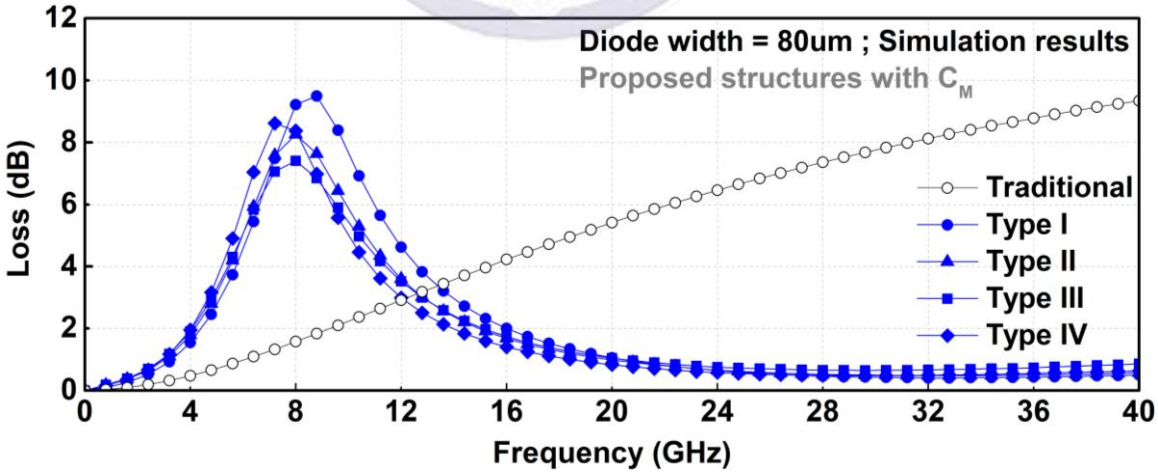
(c)

Fig. 3.22. Simulated signal losses of traditional and proposed I/O pads with the dual-diode ESD protection (a) W=40μm, (b) W=80μm, and (c) W=120μm.

Figs 3.23 (a) and (b) show the signal losses of proposed I/O pads with parallel capacitor (C_M) and dual-diode ESD protection (W=40μm and 80μm). The signal losses of traditional structures have not changed because there are no C_M. The proposed structures with C_M have smaller $F_{(resonance)}$ than without C_M (Figs. 3.22). It is important to ensure that the $F_{(resonance)}$ is far away from K/Ka-bands. Otherwise there will be a large signal loss in the operating bands. The $F_{(resonance)}$ of proposed structures with C_M are about 1 GHz smaller than original structures, as shown in Table 3.5.



(a)



(b)

Fig. 3.23. Simulated signal losses of proposed I/O pads with parallel capacitor (C_M) and dual-diode ESD protection (a) W=40μm and (b) W=80μm.

Table 3.5

The simulation results of traditional and proposed I/O pads with dual-diode ESD protection at high frequency.

I/O pad	Dual diodes	$F_{(resonance)}$ (GHz)	$Loss_{(Max)}$ (dB)
Traditional	DD_40	N/A	6.33
	DD_80	N/A	9.34
	DD_120	N/A	12.18
Type I	DD_40	11.3	1.17
	DD_80	9.2	1.07
	DD_120	7.5	1.02
Type I + C_M	DD_40	10.1	1.11
	DD_80	8.5	1.05
Type II	DD_40	10.5	1.01
	DD_80	8.6	0.99
	DD_120	7.0	0.98
Type II + C_M	DD_40	9.5	1.00
	DD_80	8.0	0.98
Type III	DD_40	10.4	1.04
	DD_80	8.5	1.04
	DD_120	6.9	0.97
Type III + C_M	DD_40	9.3	1.05
	DD_80	7.9	1.04
Type IV	DD_40	10.0	0.87
	DD_80	8.1	0.83
	DD_120	6.6	0.81
Type IV + C_M	DD_40	8.9	0.85
	DD_80	7.5	0.82

3.6 Measurement Methods and Results

The traditional and proposed structures have been fabricated in a 0.18μm CMOS process. All test devices are implemented with ground-signal-ground (G-S-G) pads. The top metal plate (metal-6) is used to route to I/O pad and the lower metals (metal-1 and metal-2) are used to route to V_{SS} and V_{DD}. These test devices are prepared with the one-port S-parameter measurement, two-port S-parameters measurement, TLP measurement, Human-Body Model (HBM) robustness measurement, and Human-Metal Model (HMM) robustness measurement. Fig. 3.24 shows the chip photo of all test devices, including traditional and proposed I/O pads with dual-diode ESD protection. In order to obtain the characteristic of independent stacked inductor and dual-diode ESD protection, the test keys of stacked inductors and dual diodes are also implemented in this chip.

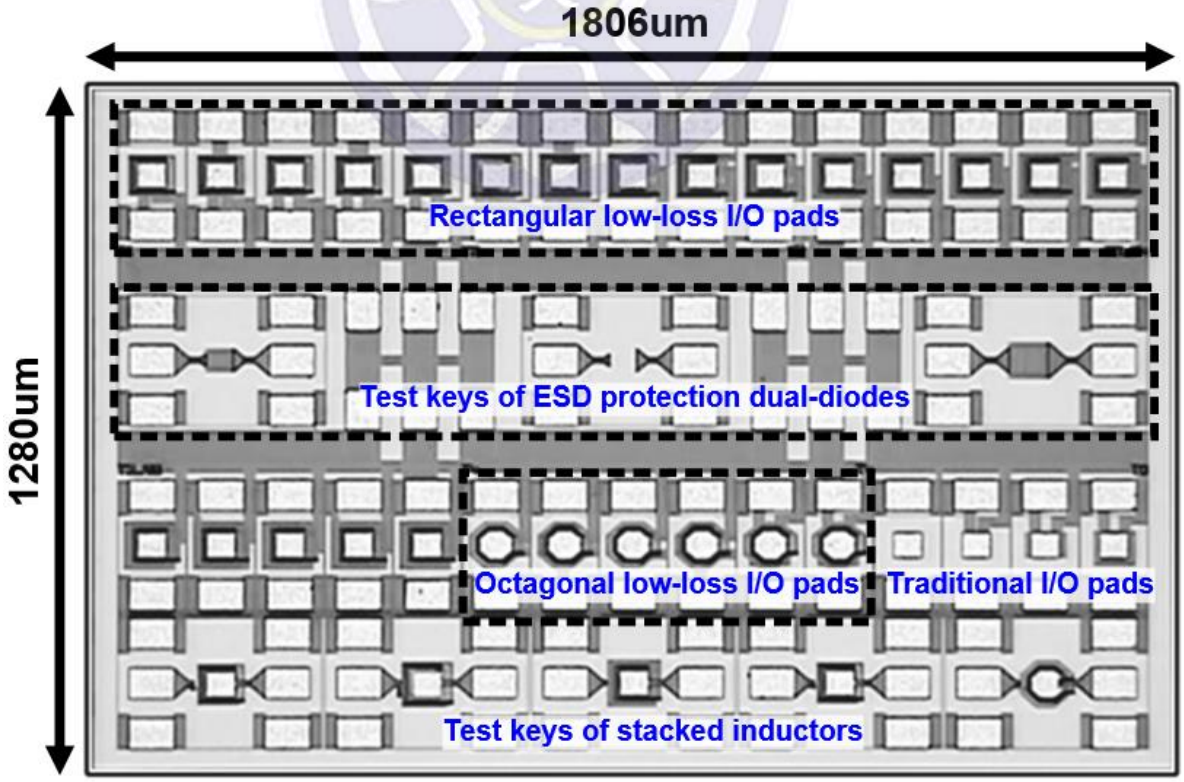


Fig. 3.24. Chip photo of all test devices.

3.6.1 Two-Port S-Parameters Measurement

This thesis has used the 67GHz RFIC Parameter Measurement System to measure the high-frequency characteristics of each device under test (DUT), as shown in Fig. 3.25. The probes are placed on the G-S-G pads in the two-port S-parameters measurement, as shown in Fig. 3.26 (a). In order to obtain the accurate measurement data of DUT, the parasitic effects of G-S-G pads should be de-embedded. Therefore, it is necessary to measure the S-parameters of de-embedded G-S-G pads, as shown in Fig. 3.26 (b). Fig. 3.27 shows the measured S-parameters network which can be represented by a matrix such as Eq. (8). To simplify mathematical operation, the S-parameters matrix is converted to a T-parameters matrix such as Eq. (9). The conversion formula for S-parameters to T-parameters is shown in Eq. (10). The T-parameters of de-embedded G-S-G pads is used to remove the G-S-G pads on the both sides of DUT, as shown in Eq. (11). The measurement results of all test devices are de-embedded in this way to obtain the accurate data of DUT.

$$[S_{Measurement}] = [S_{G\text{-}S\text{-}G}][S_{DUT}][S_{G\text{-}S\text{-}G}] \tag{8}$$

$$[T_{Measurement}] = [T_{G\text{-}S\text{-}G}][T_{DUT}][T_{G\text{-}S\text{-}G}] \tag{9}$$

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} -\dfrac{S_{11}S_{22}-S_{12}S_{21}}{S_{21}} & \dfrac{S_{11}}{S_{21}} \\ -\dfrac{S_{22}}{S_{21}} & \dfrac{1}{S_{21}} \end{bmatrix} \tag{10}$$

$$[T_{DUT}] = [T_{G\text{-}S\text{-}G}]^{-1}[T_{G\text{-}S\text{-}G}][T_{DUT}][T_{G\text{-}S\text{-}G}][T_{G\text{-}S\text{-}G}]^{-1} \tag{11}$$

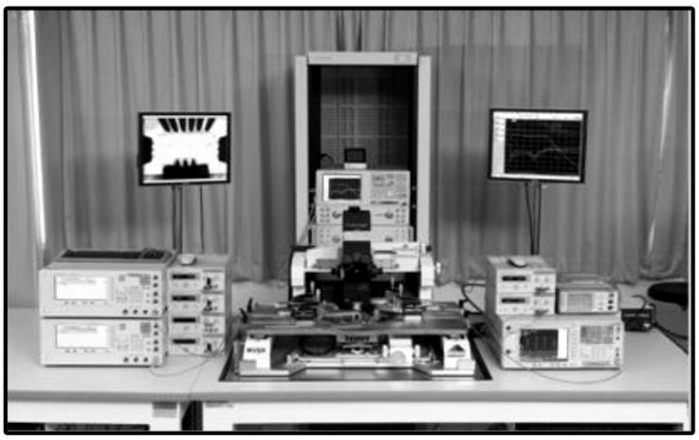


Fig. 3.25. The 67GHz RFIC Parameter Measurement System.

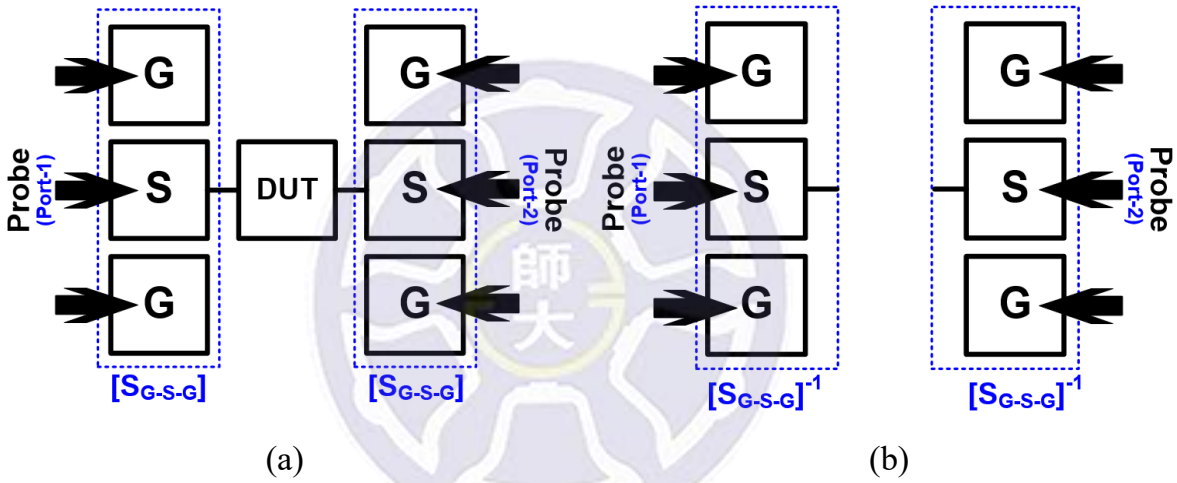


Fig. 3.26. (a) Two-port S-parameters measurement and (b) de-embedded G-S-G pads.

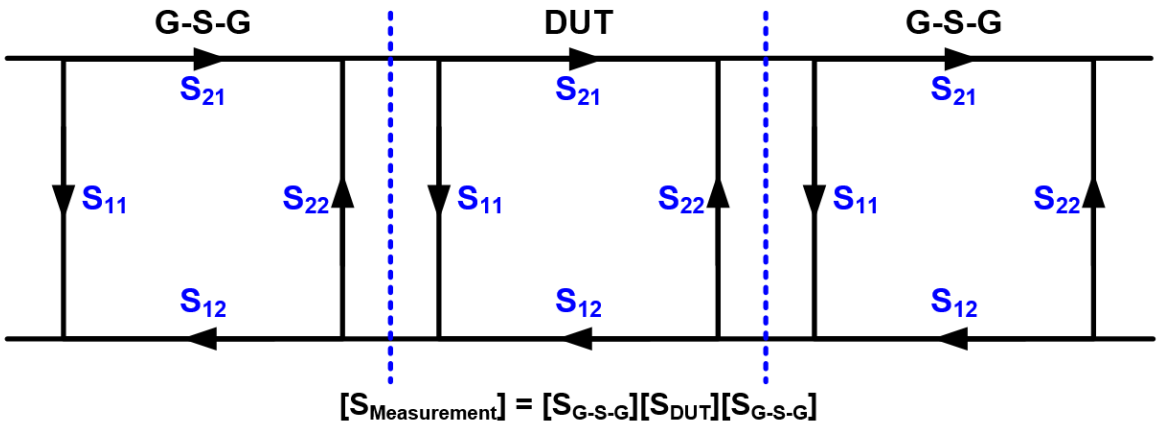


Fig. 3.27. S-parameters network.

The chip photo of independent stacked inductors, L_1, L_2, L_3, and L_4 are shown in Figs. 3.28 (a), (b), (c), and (d). The measured S-parameters are converted into Y-parameters and the Y_{11} can be expressed as Eq. (12). The Z_o is the characteristic impedance of 50Ω. The Y_{11} is used to obtain the inductance value (L), parasitic resistance (R_L), and quality factor (Q) such as Eq. (13).

$$Y_{11}=\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{Z_o(1+S_{11})(1+S_{22})-S_{12}S_{21}} \tag{12}$$

$$L=\frac{\text{imag}(\frac{1}{Y_{11}})}{2\pi f}\ ;\ R_L=\text{real}(\frac{1}{Y_{11}})\ ;\ \text{Quality factor}=\frac{\text{imag}(\frac{1}{Y_{11}})}{\text{real}(\frac{1}{Y_{11}})} \tag{13}$$

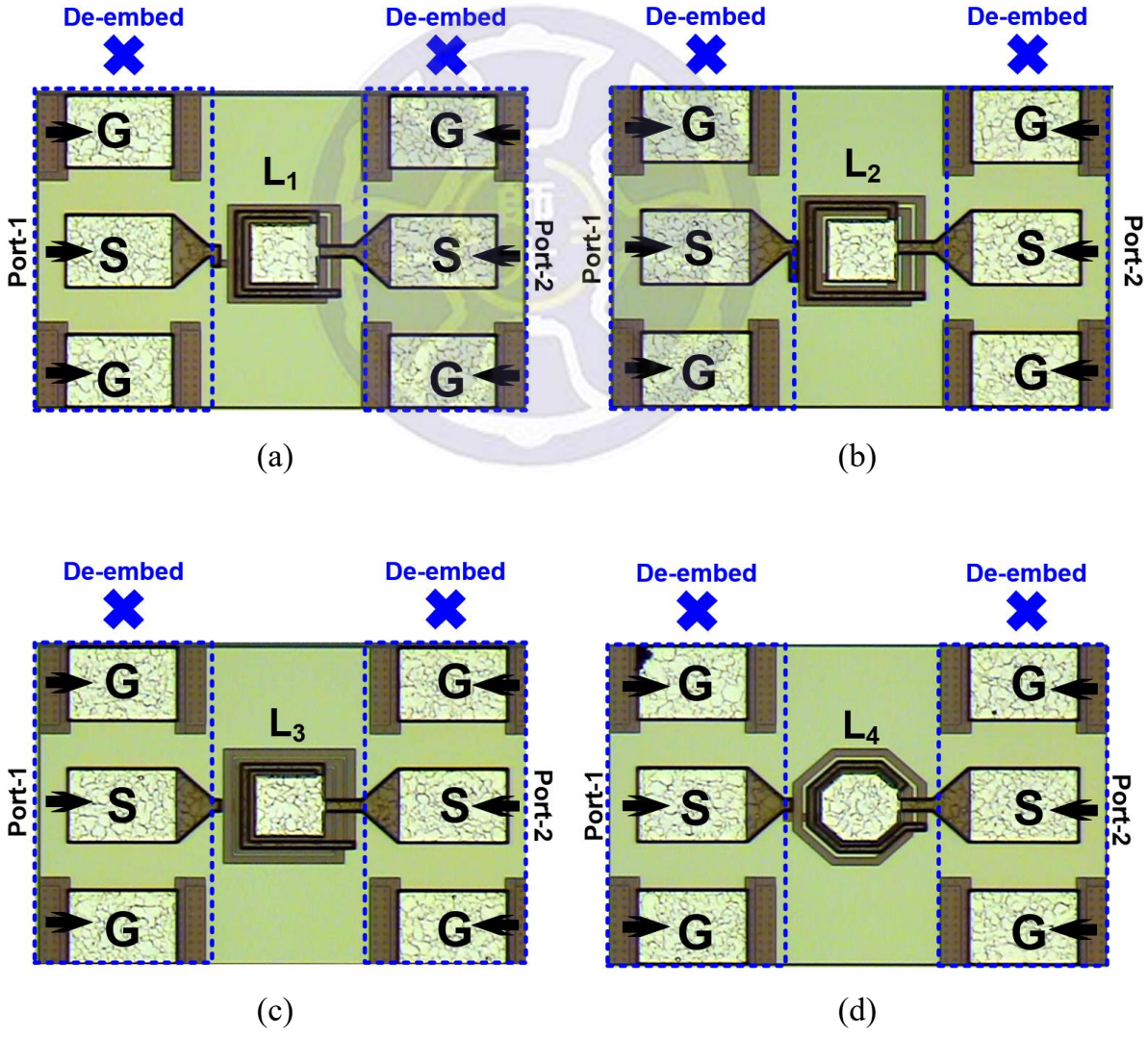


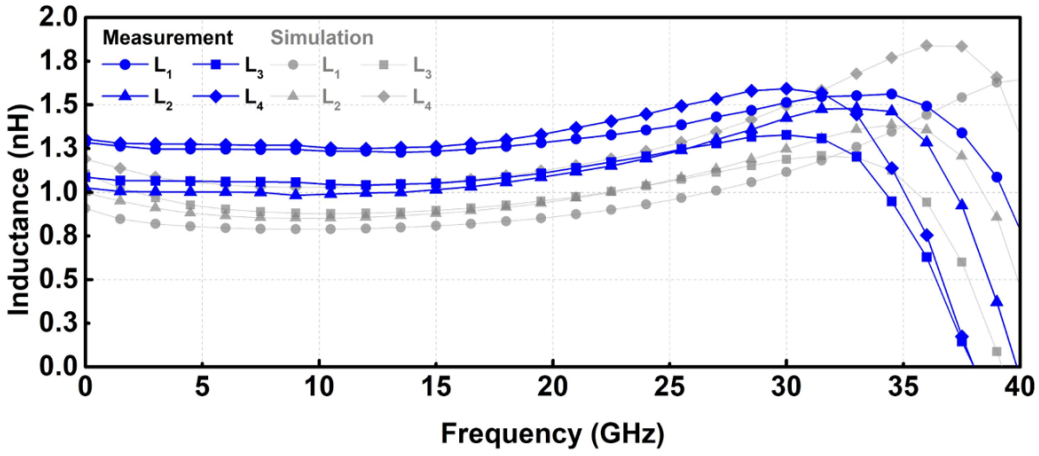
Fig. 3.28. The stacked inductors (a) L_1, (b) L_2, (c) L_3, and (d) L_4 in G-S-G pads.

The measurement results of independent stacked inductors, L_1, L_2, L_3, and L4 are shown in Figs. 3.29. The L_1 and L_4 have higher inductance values than the other two. The measurement results of inductance value are little higher than the simulation results because of the additional parasitic inductance of metal line in the actual chip, as shown in Fig. 3.29 (a). In addition, the self-resonance frequencies of stacked inductors are little lower than the simulation results due to the extra parasitic capacitance in the chip. However, these deviation values are still in the tolerable range. Fig. 3.29 (b) shows the measured parasitic resistance of each stacked inductor and it can be observed that there is extra parasitic resistance in the metal trace. The quality factor of each stacked inductor are shown in Fig. 3.29 (c). The octagonal inductor (L_4) has better quality factor than rectangular inductors (L_1, L_2, and L_3). The measured quality factors have a tendency to change into the capacitive state at high frequency because of the parasitic capacitances of stacked inductors. The two-port measurement results of independent stacked inductors at 24 GHz are organized in Table 3.6.

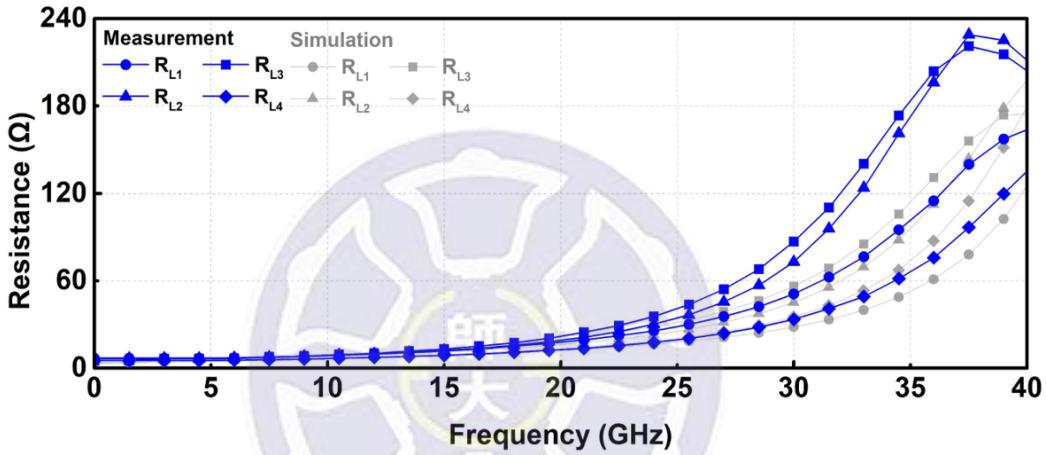
Table 3.6

The measurement results of independent stacked inductors at 24GHz.

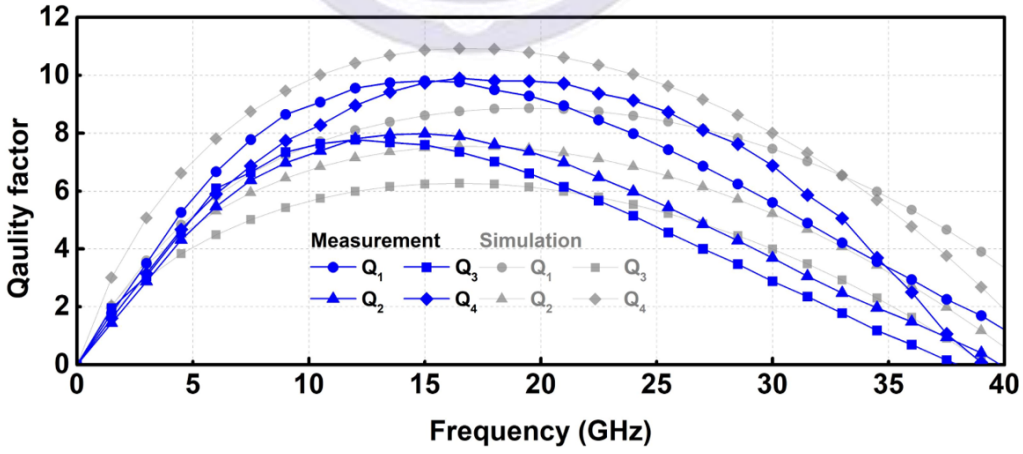
Stacked inductor		Inductance value (nH)	Parasitic resistance (Ω)	Quality factor
Rectangle	L_1	1.35	25.60	7.97
	L_2	1.19	30.10	5.97
	L_3	1.20	35.35	5.14
Octagon	L_4	1.44	17.67	9.12



(a)



(b)



(c)

Fig. 3.29. Measured (a) inductance value (L), (b) parasitic resistance (R_L), and (c) quality factor (Q) of stacked inductors L_1, L_2, L_3, and L_4.

3.6.2 Ono-Port S-Parameter Measurement

The traditional and proposed I/O pads are the signal pads in the ground-signal-ground pads, as shown in Fig. 3.30. The one-port S-parameter measurement is used to obtain the high-frequency response of the traditional and proposed I/O pads with dual-diode ESD protection. Since only a single port is used for measurement, only the S_{11} will be obtained. To obtain the signal loss caused by the test device, the measured S_{11} must be converted to Y_{11} by the Eq. (14). Then the signal loss of test device can be represented by the Eq. (15). The Z_o is the characteristic impedance of 50Ω.

$$Y_{11} = \frac{(1-S_{11})}{Z_o(1+S_{11})} \tag{14}$$

$$\text{Loss} = \left| \frac{2}{2+Y_{11}Z_o} \right| \tag{15}$$

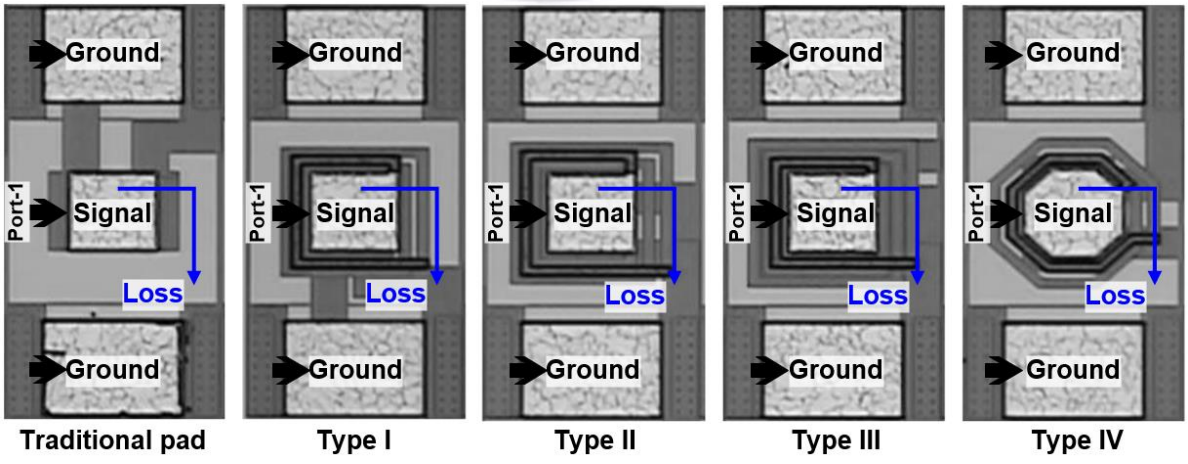
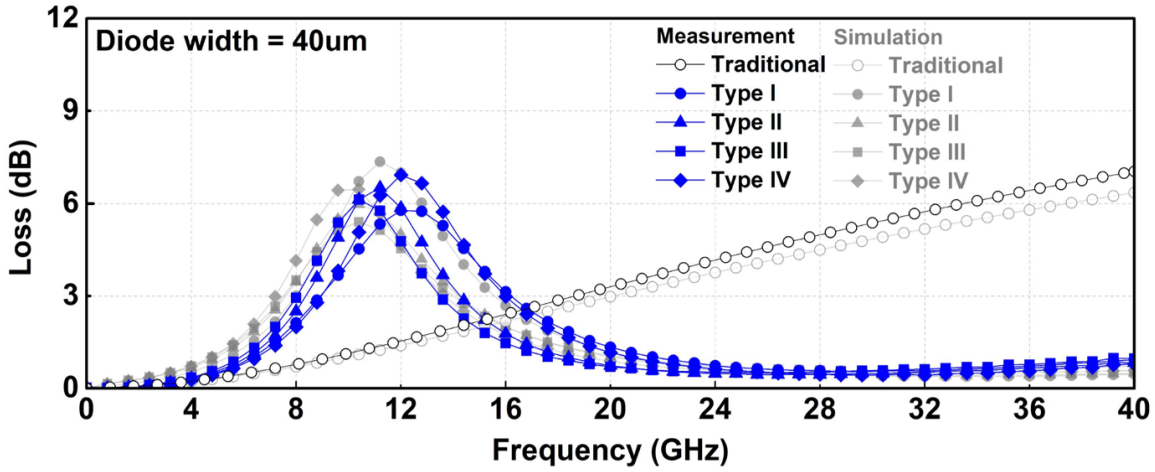


Fig. 3.30. The signal losses caused by the traditional and proposed signal pads with the dual-diode ESD protection.

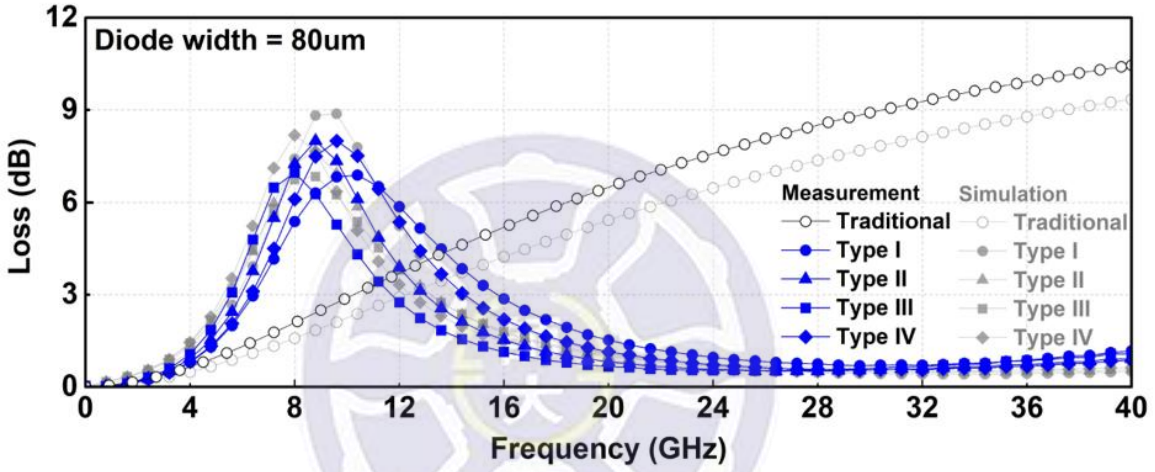
The largest signal loss of test devices in K/Ka-bands is defined as Loss $_{(max)}$. Fig. 3.31 (a) shows the measured signal losses of traditional and proposed I/O pads with the dual-diode ESD protection (W=40μm). It can be clearly observed that the signal loss of traditional structure becomes larger as the frequency increases. The Loss $_{(max)}$ of traditional structure reaches 7.03dB. However, the proposed structures have low signal loss in K/Ka-bands. The Loss $_{(max)}$ of Type I, Type II, Type III, and Type IV are 1.54dB, 0.84dB, 0.78dB, and 1.16dB. The Loss $_{(max)}$ of traditional structure is about 6 times larger than proposed structures.

Fig. 3.31 (b) shows the measured signal losses of traditional and proposed I/O pads with the dual-diode ESD protection (W=80μm). The Loss $_{(max)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 10.45dB, 1.69dB, 0.90dB, 0.71dB, and 1.14dB. The Loss $_{(max)}$ of traditional structure with DD_80 is about 7 times larger than the proposed structures. However, the Loss $_{(max)}$ of proposed structures can be still reduced to about 1dB in K/Ka-bands.

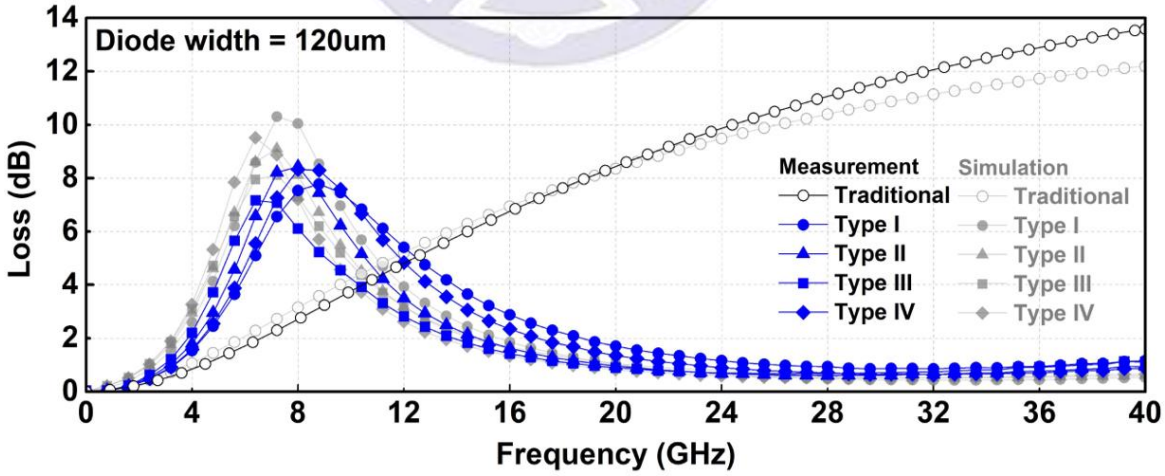
The measured signal losses of traditional and proposed I/O pads with the dual-diode ESD protection (W=120μm) are shown in Fig. 3.31 (c). The Loss $_{(max)}$ of proposed structures, Type I, Type II, Type III, and Type IV are 1.86dB, 1.05dB, 0.96dB, and 1.35dB. However, the Loss $_{(max)}$ of traditional structure reaches 13.58dB, which is ~10 times higher than the proposed structures. Base on the above measurement results, the proposed structure with the fully overlapping inductor (Type I) has a larger signal loss. The proposed structure with non-overlapping inductor (Type III) can reduce the signal loss even lower. The fully overlapping inductor has smaller layout area but it has more parasitic effects. However, the structure with non-overlapping inductor can effectively avoid the parasitic effects between metals. The measurement results of all test structures are organized in Table 3.7.



(a)



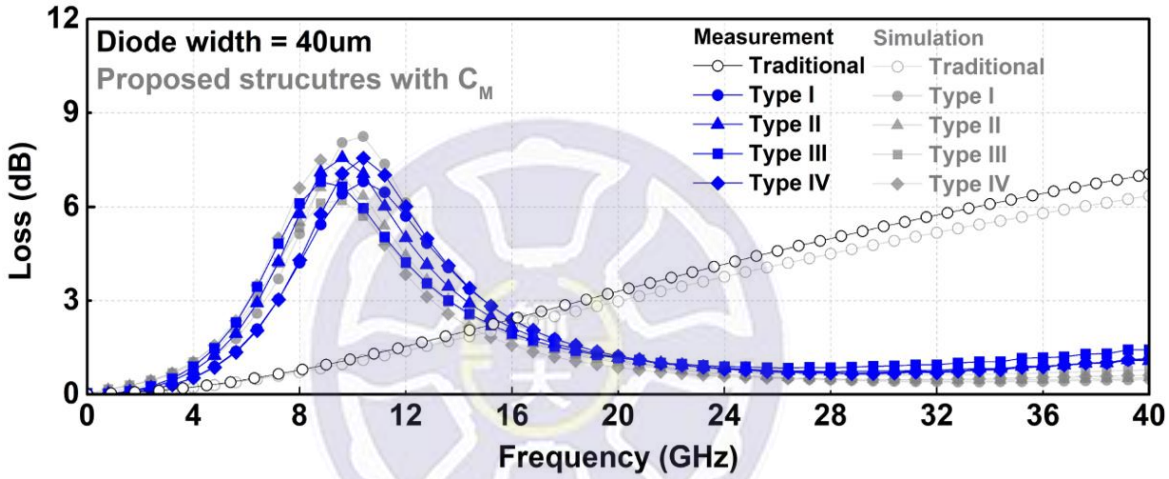
(b)



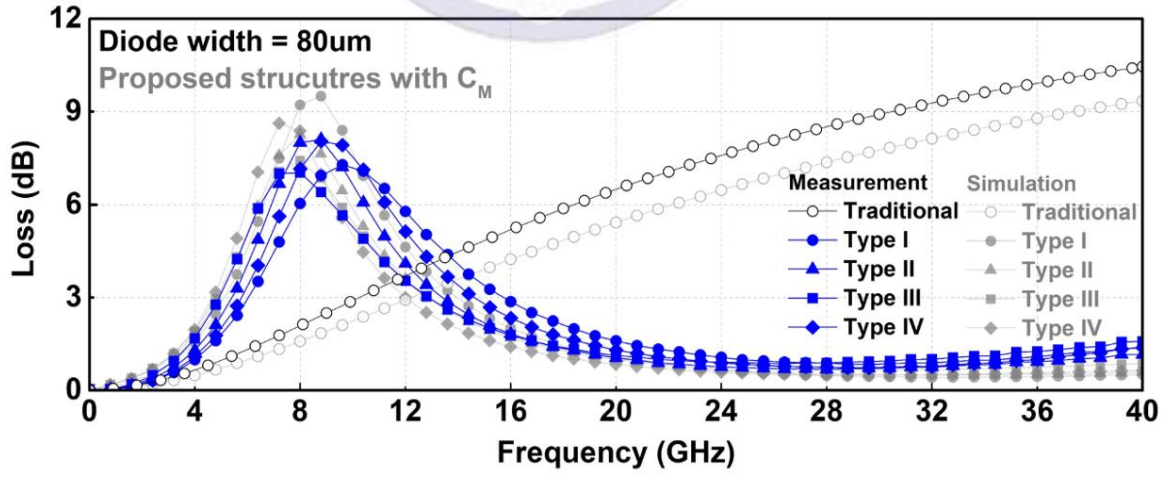
(c)

Fig. 3.31. Measured signal losses of traditional and proposed I/O pads with the dual-diode ESD protection (a) W=40μm, (b) W=80μm, and (c) W=120μm.

Figs 3.32 (a) and (b) show the measured signal losses of proposed I/O pads with parallel capacitor (C_M) and dual-diode ESD protection (W=40μm and 80μm). The signal losses of traditional structure have not changed because there is no combination with C_M. The proposed structures with C_M have smaller $F_{(resonance)}$ than the proposed structures without C_M (Figs. 3.31). Base one this, the structures with C_M have smaller $Loss_{(max)}$ in K/Ka-bands because of the $F_{(resonance)}$ are far away from the operating frequencies.



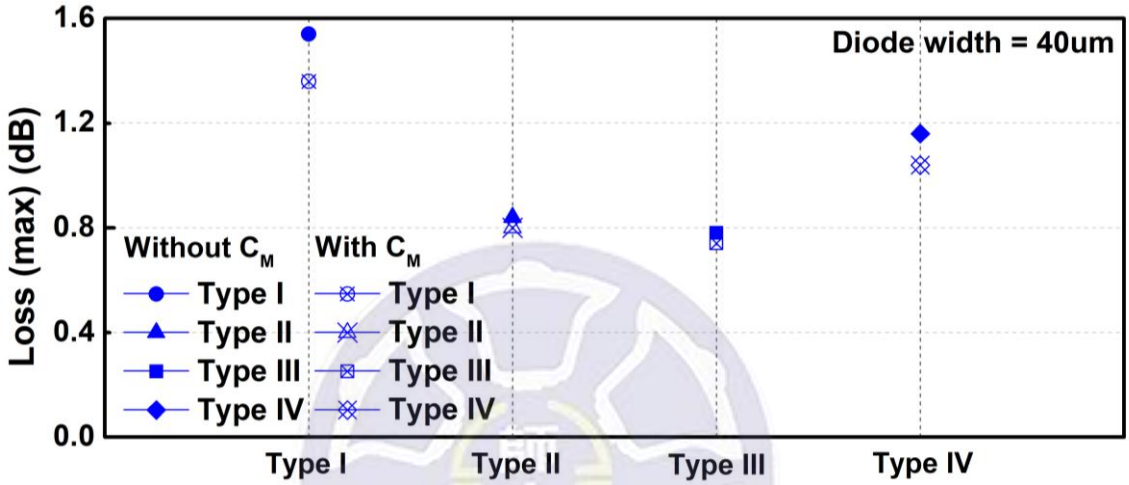
(a)



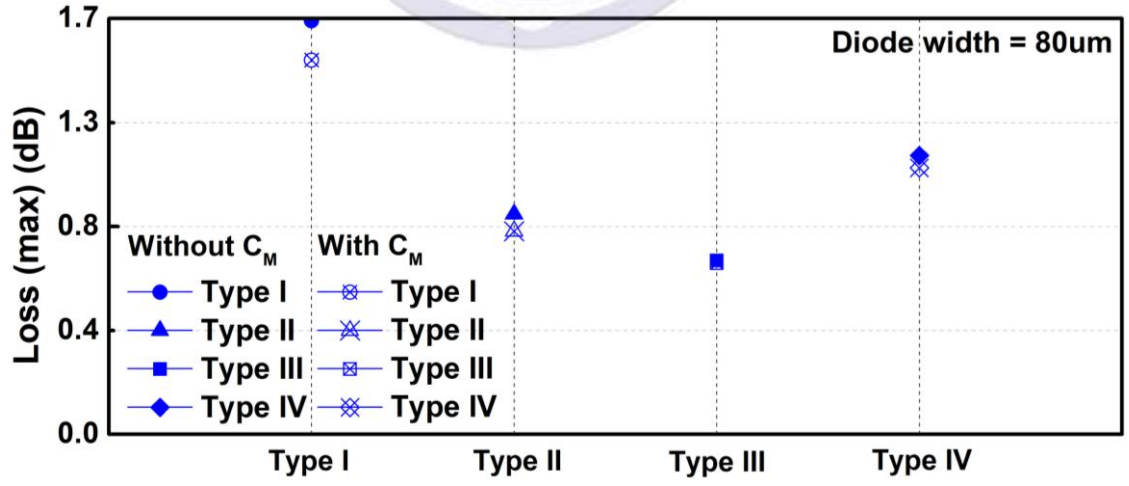
(b)

Fig. 3.32. Measured signal losses of traditional and proposed I/O pads with parallel capacitor and dual-diode ESD protection (a) W=40μm and (b) W=80μm.

In order to compare the signal loss between the proposed structures with or without C_M. The Loss $_{(max)}$ of proposed structures with or without C_M are compared in Figs. 3.33 (a) and (b). It can be observed that the Loss $_{(max)}$ of proposed structures with C_M are lower than the proposed structures without C_M. The improvement is limited because the size of parallel capacitor is limited by the area of I/O pad.



(a)



(b)

Fig. 3.33. The Loss $_{(max)}$ of proposed structures with or without parallel capacitor (C_M) and dual-diode ESD protection (a) W=40μm and (b) W=80μm.

For the proposed structure, the sharper resonance curve indicates better high-frequency characteristics. In order to determine the sharpness of a curve, the full width at half maximum (FWHM) is defined as the distance between two frequencies (F_L and F_H) of the half of $Loss_{peak}$ in the curve. As shown in Fig. 3.34, the FWHM is the value of (F_H-F_L) and the smaller FWHM represents a proposed structure with less signal loss in the operating frequencies. The FWHM of all proposed structures are organized in Table 3.7. It can be observed that the proposed structure of Type III has the lowest FWHM value. Conversely, the proposed structure of Type I has the highest FWHM value. Since the structure of Type I is completely overlapping, the parasitic effects between metals affect the characteristics of stacked inductor. However, the structure of Type III is non-overlapping and the effects between metals can be minimized. In order to ensure that the region of resonant frequency does not affect the operating band, not only the $F_{(resonance)}$ should be low enough and the value of FWHM should be small enough.

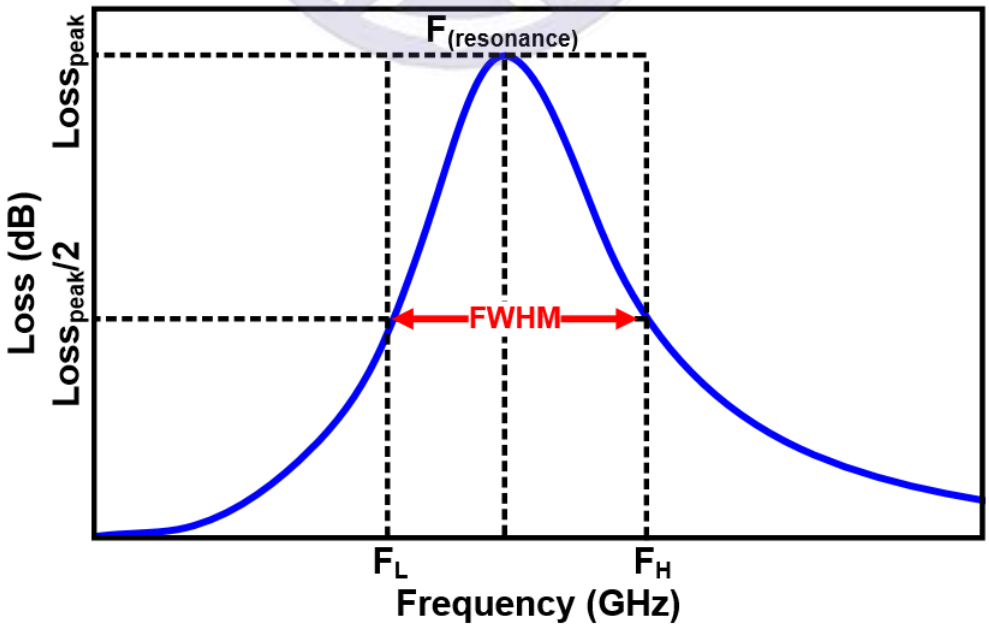


Fig. 3.34. The full width at half maximum (FWHM) of curve.

Table 3.7

The high-frequency measurement results of all test devices.

I/O pad	Dual-diode	$F_{(resonance)}$ (GHz)	Loss $_{(Max)}$ (dB)	FWHM (GHz)
Traditional	DD_40	N/A	7.03	N/A
	DD_80	N/A	10.45	N/A
	DD_120	N/A	13.58	N/A
Type I	DD_40	12.0	1.54	7.7
	DD_80	10.4	1.69	8.4
	DD_120	8.8	1.86	8.8
Type I + C_M	DD_40	10.4	1.36	7.8
	DD_80	9.6	1.53	8.3
Type II	DD_40	11.2	0.84	5.6
	DD_80	8.8	0.90	5.7
	DD_120	7.2	1.05	5.8
Type II + C_M	DD_40	9.6	0.80	5.4
	DD_80	8.0	0.83	5.5
Type III	DD_40	10.4	0.78	4.9
	DD_80	8.0	0.71	5.2
	DD_120	7.1	0.96	5.4
Type III + C_M	DD_40	8.8	0.74	4.7
	DD_80	7.2	0.70	5.2
Type IV	DD_40	12.0	1.16	5.1
	DD_80	9.6	1.14	5.7
	DD_120	8.0	1.35	5.9
Type IV + C_M	DD_40	10.4	1.04	5.1
	DD_80	8.8	1.09	5.5

3.6.3 TLP Measurement

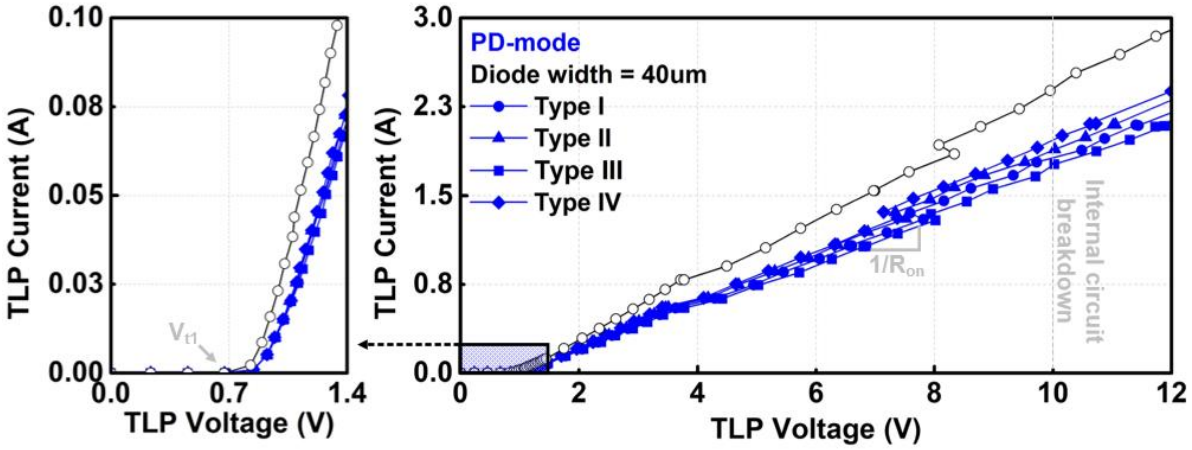
The transmission line pulsing (TLP) generator with a pulse width of 100ns and a rise time of 10ns is used to investigate the I-V characteristics of each test device during high ESD current stress, as shown in Fig. 3.35. There are several important data in the TLP measurement that should be recorded, including the trigger voltage (V_{t1}), turn-on resistance (R_{on}), and breakdown current (I_{BD}). The trigger voltage is defined as the value of TLP voltage when the TLP current starts to exceed 1mA. The value of trigger voltage determines whether the ESD protection device can be turn-on in time when facing the ESD stress. The turn-on resistance is the reciprocal of the slope of TLP I-V curve. The value of turn-on resistance determines the power dissipation that will be generated when the ESD protection is turned on to discharge. The TLP current of the breakdown voltage of 10V in 0.18μm CMOS process is defined as I_{BD}. The I_{BD} indicates the ESD protection level of ESD protection device before the internal circuit breakdown. Therefore, the value of IBD should be as high as possible.

Fig. 3.35. Picture of TLP system.

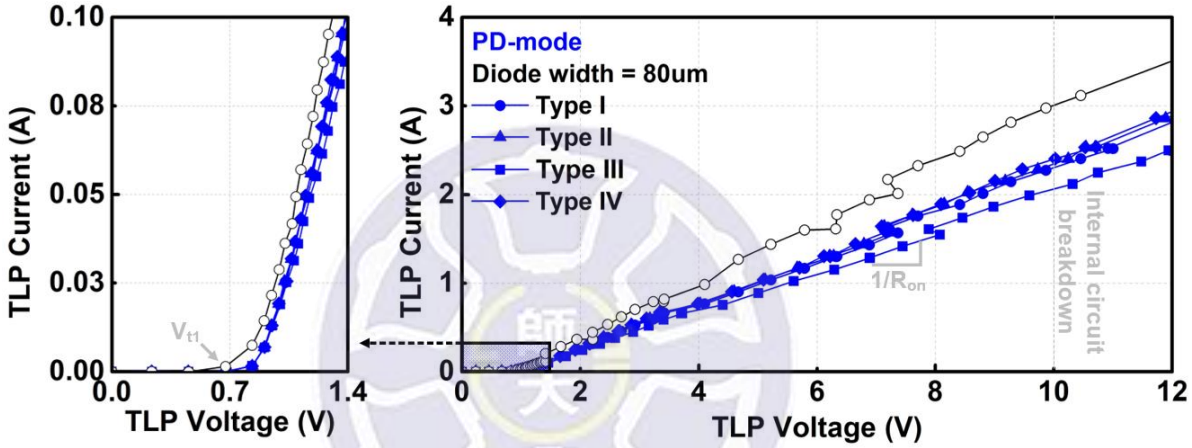
The TLP-measurement results TLP of traditional and proposed I/O pads with the different sizes of dual-diode ESD protection during the stress from I/O pad to V_{DD} (PD-mode) are shown in Figs. 3.36. It can be observed that all test devices have a low enough $V_{t1\ (PD\text{-}mode)}$ of about 0.8V. The traditional and proposed structures have the same dual-diode ESD protection. However, the difference is that the proposed structures contain stacked inductor and the ESD current needs to flow through the stacked inductor to discharge. Therefore, the $R_{on\ (PD\text{-}mode)}$ of proposed structures are slight larger than the traditional structure. The smaller slope of TLP I-V curve will also result in the proposed structures having a smaller I_{BD} than the traditional structure.

Fig. 3.36 (a) shows the TLP I-V curves of traditional and proposed I/O pads with the diode width (W) of 40μm. The $I_{BD\ (PD\text{-}mode)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 2.53A, 1.98A, 1.99A, 1.87A, and 2.10A, respectively. Fig. 3.36 (b) shows the TLP I-V curves of traditional and proposed I/O pads with the diode width (W) of 80μm. The $I_{BD\ (PD\text{-}mode)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 3.11A, 2.40A, 2.53A, 2.24A, and 2.53A, respectively. Fig. 3.36 (c) shows the TLP I-V curves of traditional and proposed I/O pads with the diode width (W) of 120μm. The $I_{BD\ (PD\text{-}mode)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 4.29A, 2.93A, 2.94A, 2.57A, and 2.94A, respectively.

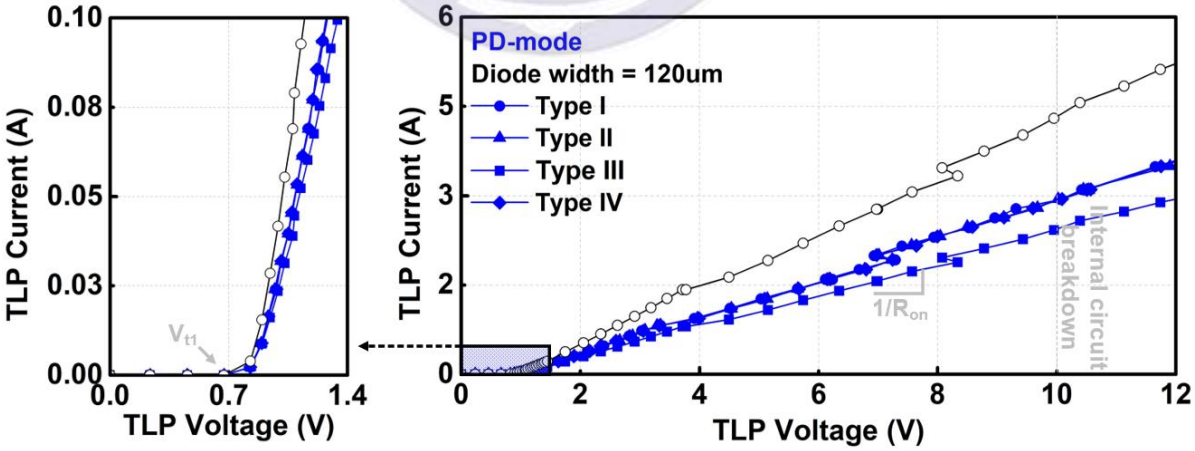
According to the measurement results, the traditional structure has better ESD protection level than proposed structures because it does not contain the stacked inductor. Although the $I_{BD\ (PD\text{-}mode)}$ of traditional structure are about 1.5 times larger than the proposed structures, the signal losses of proposed structures can be more than 6 times lower than the traditional structure. The performance of traditional and proposed structures in PD-mode will be compared in the Section 3.7.



(a)



(b)



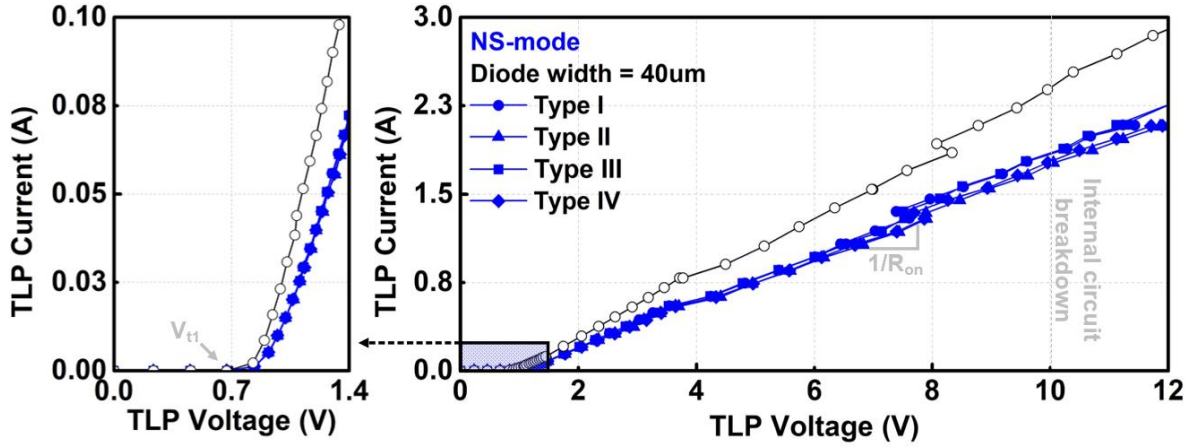
(c)

Fig. 3.36. The TLP I-V curves of tradtional and proposed I/O pads with dual-diode ESD protection (a) W=40μm, (b) W=80μm, and (c) W=120μm in PD-mode.

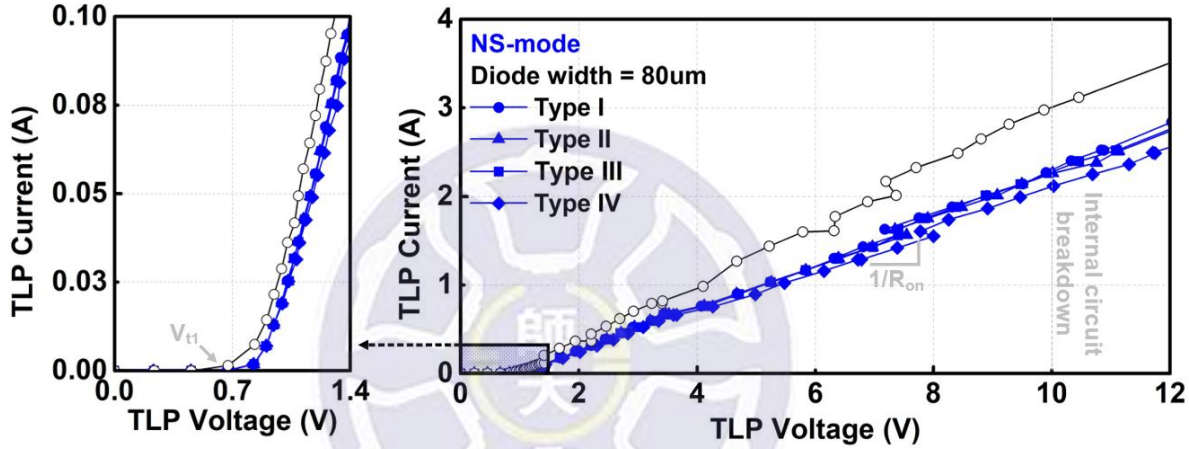
The TLP-measurement results TLP of traditional and proposed I/O pads with the different sizes of dual-diode ESD protection during the stress from V_{SS} to I/O pad (NS-mode) are shown in Figs. 3.37. All test devices have an approximate $V_{t1\ (NS\text{-}mode)}$ of about 0.8V. Both the traditional and proposed structures are using the same dual-diode ESD protection. Therefore, the traditional and proposed structures have approximate I-V curves. However, the proposed structures lead to a larger turn-on resistance than traditional structure due to the additional stacked inductor.

Fig. 3.37 (a) shows the TLP I-V curves of traditional and proposed I/O pads with the diode width (W) of 40μm. The $I_{BD\ (NS\text{-}mode)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 2.68A, 1.99A, 1.87A, 1.88A, and 2.07A, respectively. Fig. 3.37 (b) shows the TLP I-V curves of traditional and proposed I/O pads with the diode width (W) of 80μm. The $I_{BD\ (NS\text{-}mode)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 2.97A, 2.52A, 2.38A, 2.39A, and 2.24A, respectively. Fig. 3.37 (c) shows the TLP I-V curves of traditional and proposed I/O pads with the diode width (W) of 120μm. The $I_{BD\ (NS\text{-}mode)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 4.56A, 3.09A, 3.09A, 2.93A, and 3.10A, respectively.

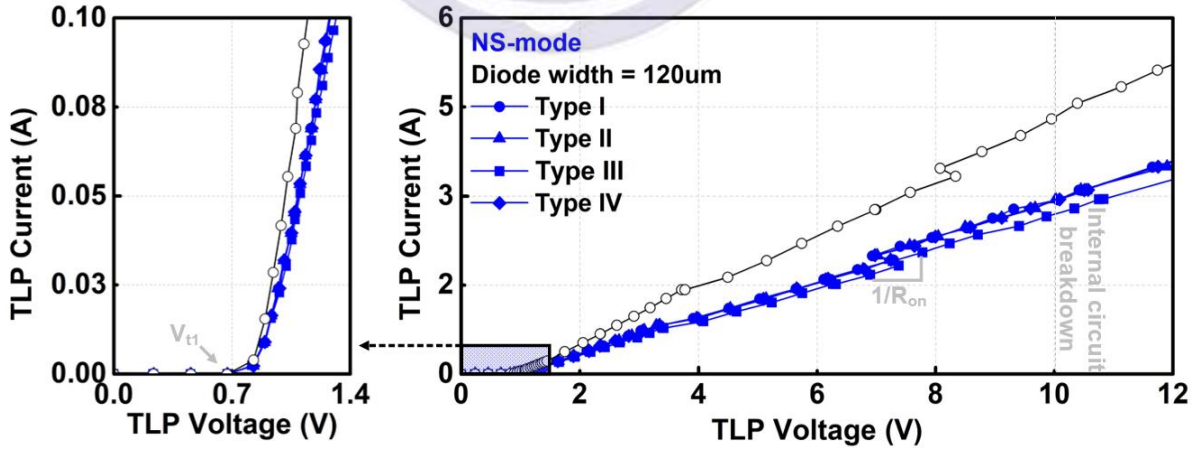
The measurement results of NS-mode are similar to PD-mode because the structures of P-type diode (D_P) is similar to the N-type diode (D_N) and the same size. The $I_{BD\ (NS\text{-}mode)}$ of traditional structure is higher than the proposed structures because there is no stacked inductor on the ESD path of the traditional structure. Although the $I_{BD\ (NS\text{-}mode)}$ of traditional structure are about 1.5 times larger than the proposed structures, the signal losses of proposed structures can be more than 6 times lower than the traditional structure. The performance of traditional and proposed structures in NS-mode will be compared in the Section 3.7.



(a)



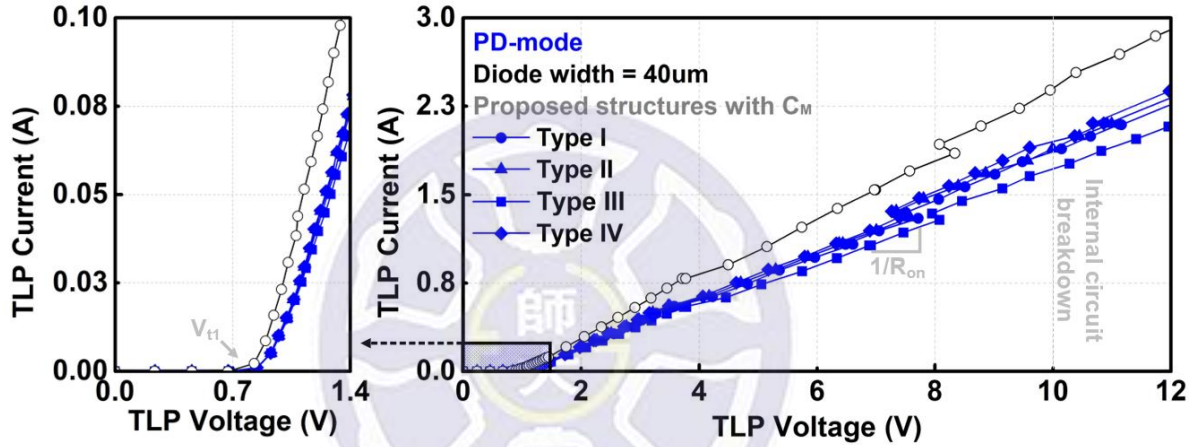
(b)



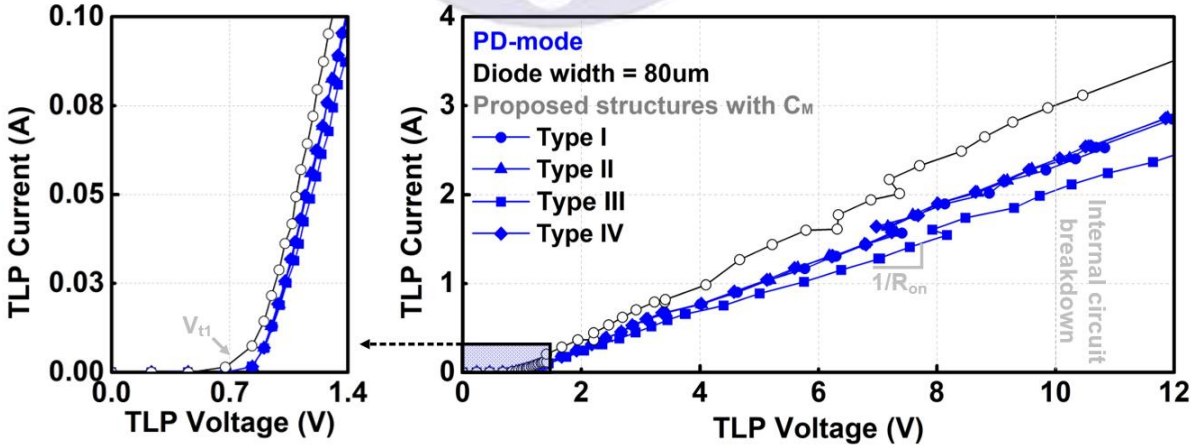
(c)

Fig. 3.37. The TLP I-V curves of tradtional and proposed I/O pads with dual-diode ESD protection (a) W=40μm, (b) W=80μm, and (c) W=120μm in NS-mode.

Figs. 3.38. (a) and (b) show the measured TLP I-V curves of traditional and proposed I/O pads with parallel capacitor (C_M) and dual-diode ESD protection (40μm and 80μm) during stress from I/O pad to V_{DD} (PD-mode). For the diode width of 40μm, the $I_{BD\ (PD\text{-}mode)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 2.53A, 1.99A, 2.09A, 1.97A, and 2.16A. For the diode width of 80μm, the $I_{BD\ (PD\text{-}mode)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 3.11A, 2.40A, 2.40A, 2.38A, and 2.54A.



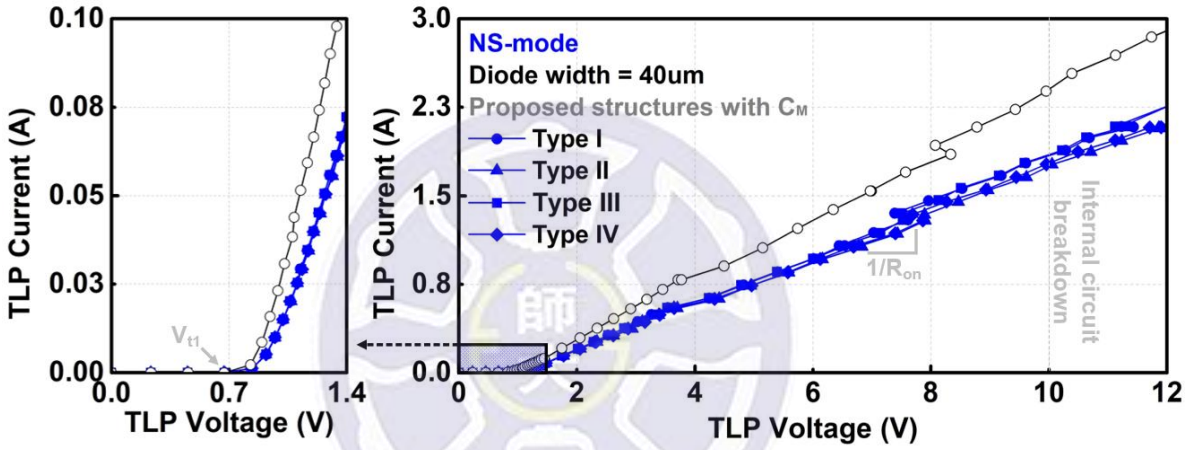
(a)



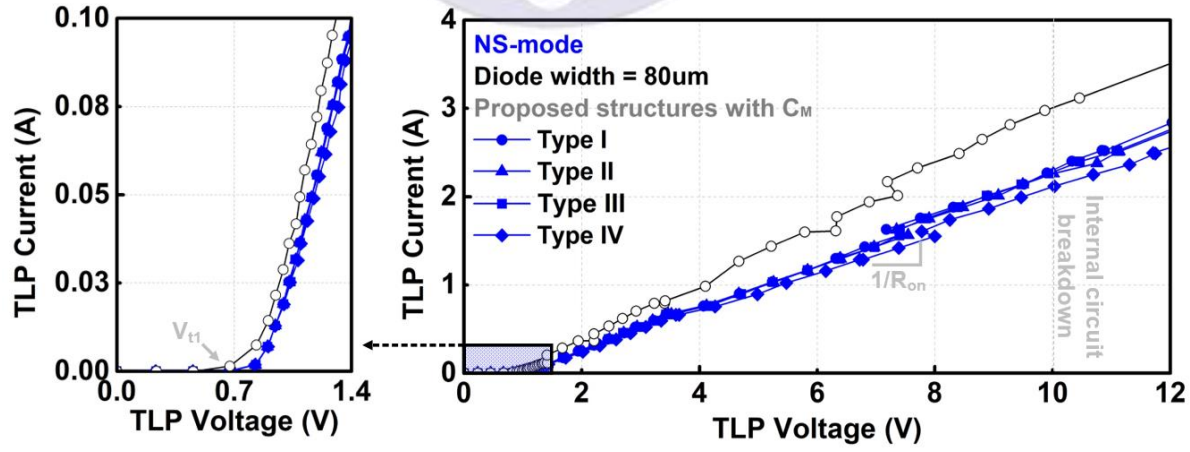
(b)

Fig. 3.38. Measured TLP I-V curves of the proposed structures with paralle capacitor (C_M) and dual-diode ESD protection (a) W=40μm and (b) W=80μm in PD-mode.

Figs. 3.39. (a) and (b) show the measured TLP I-V curves of traditional and proposed I/O pads with parallel capacitor (C_M) and dual-diode ESD protection (40μm and 80μm) during stress from V_{SS} to I/O pad (NS-mode). For the diode width of 40μm, the $I_{BD\ (NS\text{-}mode)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 2.68A, 1.99A, 1.87A, 1.99A, and 1.96A. For the diode width of 80μm, the $I_{BD\ (NS\text{-}mode)}$ of traditional structure, Type I, Type II, Type III, and Type IV are 2.97A, 2.26A, 2.38A, 2.51A, and 2.36A.



(a)



(b)

Fig. 3.39. Measured TLP I-V curves of the proposed structures with paralle capacitor (C_M) and dual-diode ESD protection (a) W=40μm and (b) W=80μm in NS-mode.

Table 3.8

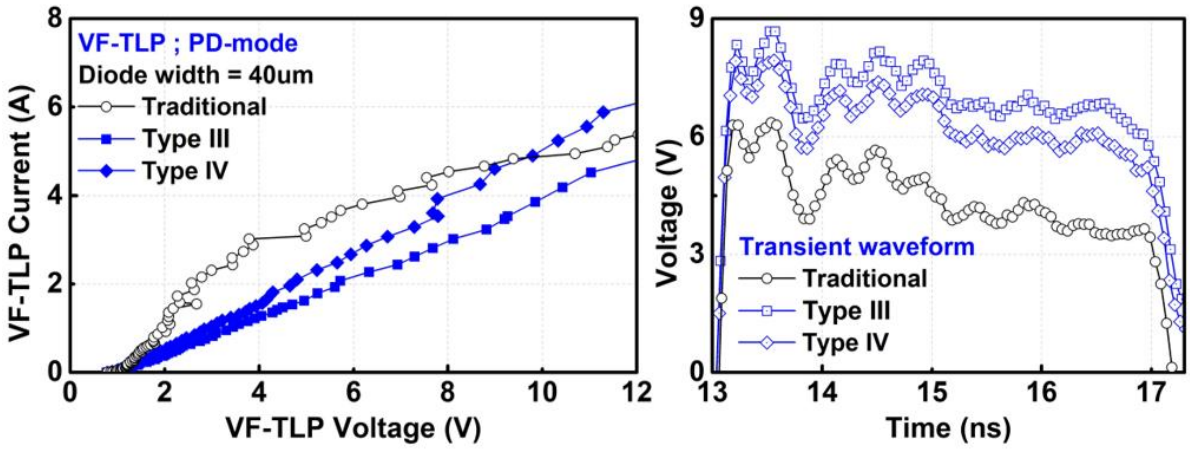
The TLP-measurement results of traditional and proposed structures.

I/O pad	Dual-diode	V_{t1} (PD-mode) (V)	R_{on} (PD-mode) (Ω)	I_{BD} (PD-mode) (A)	V_{t1} (NS-mode) (V)	R_{on} (NS-mode) (Ω)	I_{BD} (NS-mode) (A)
Traditional	DD_40	0.82	4.59	2.53	0.82	4.18	2.68
	DD_80	0.82	3.31	3.11	0.82	3.32	2.97
	DD_120	0.82	2.27	4.29	0.82	2.25	4.56
Type I	DD_40	0.84	5.66	1.98	0.84	5.42	1.99
	DD_80	0.83	4.35	2.40	0.83	4.38	2.52
	DD_120	0.82	3.43	2.93	0.82	3.36	3.09
Type I + C_M	DD_40	0.84	5.39	1.99	0.84	5.46	1.99
	DD_80	0.83	4.30	2.40	0.83	4.38	2.26
Type II	DD_40	0.84	5.38	1.99	0.84	5.52	1.87
	DD_80	0.83	4.16	2.53	0.83	4.51	2.38
	DD_120	0.82	3.40	2.94	0.82	3.40	3.09
Type II + C_M	DD_40	0.84	5.23	2.09	0.84	5.71	1.87
	DD_80	0.83	4.26	2.40	0.83	4.45	2.38
Type III	DD_40	0.84	6.41	1.87	0.84	5.51	1.88
	DD_80	0.83	4.79	2.24	0.83	4.37	2.39
	DD_120	0.82	4.03	2.57	0.82	3.65	2.93
Type III + C_M	DD_40	0.84	5.83	1.97	0.84	5.43	1.99
	DD_80	0.83	4.77	2.38	0.83	4.44	2.51
Type IV	DD_40	0.84	5.09	2.10	0.84	5.65	2.07
	DD_80	0.83	4.23	2.53	0.83	4.57	2.24
	DD_120	0.82	3.42	2.94	0.82	3.40	3.10
Type IV + C_M	DD_40	0.84	5.01	2.16	0.84	5.68	1.96
	DD_80	0.83	3.95	2.54	0.83	4.77	2.36

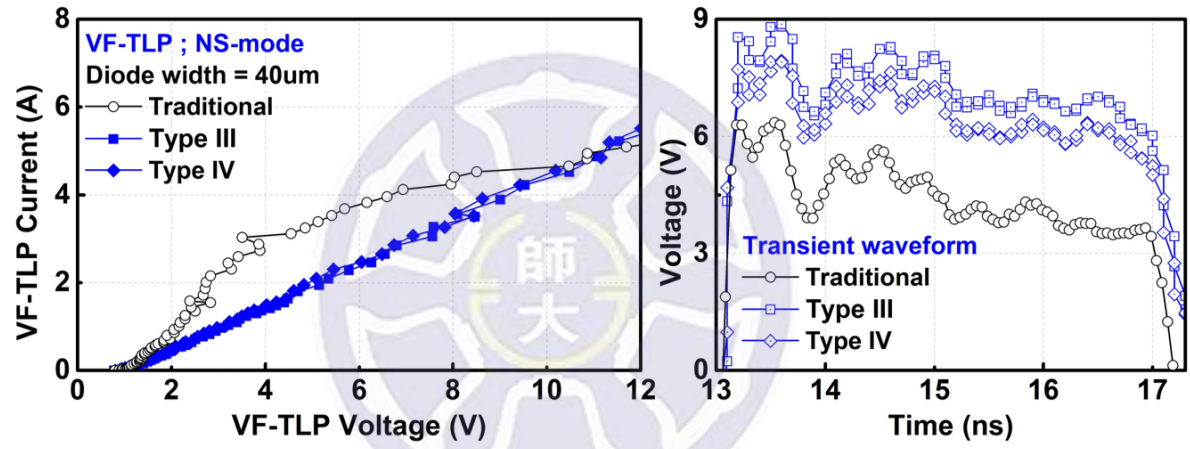
3.6.4 VF-TLP Measurement

In the fast ESD event, the proposed structure may have a higher transient voltage due to the stacked inductor. This problem may cause the high potential of the I/O terminal to impact the internal circuit. A very-fast-TLP (VF-TLP) system is used to simulated the charge-device-model (CDM) ESD stresses. The pulse width and rise time of VF-TLP are 5ns and 200ps, respectively. The VF-TLP I-V characteristics of traditional structure, Type III, and Type IV are measured. Besides, to observe the turn-on behavior during the high ESD current of fast transient, the transient waveform has been measured and recorded. Since the proposed structures have similar characteristics, only the best performing Type III and Type IV are measured here.

Figs. 3.40 (a) and (b) show the VF-TLP I-V curves and the transient waveform at 1A of traditional, Type III, and Type IV with DD_40 in PD-mode and NS-mode, respectively. The current at VF-TLP voltage of 10V is defined as I_{BD}. The test devices under VF-TLP test have smaller Ron and higher I_{BD} than the TLP measurement results. The Ron of traditional structure gradually increases after 8V, so the I_{BD} of proposed structures are similar to traditional structure. In order to compare the transient voltage of each test device, the transient voltage at 15ns is defined as $V_{transient}$. Although the $V_{transient}$ of proposed structures are slightly higher than that of traditional structure due to the inductor, the signal loss of proposed design can be greatly improved. The VF-TLP-measurement results of traditional structure, Type III and Type IV are organized in Table 3.9.



(a)



(b)

Fig. 3.40. Measured VF-TLP I-V characteristics and transient waveform at 1A of traditional structure, Type III, and Type IV with DD_40 during stress from (a) I/O pad to V_{DD} (PD-mode) and (b) V_{SS} to I/O pad (NS-mode).

Table 3.9

The VF-TLP-measurement results of traditional structure, Type III, and Type IV with DD_40 in PD-mode and NS-mode.

I/O pad	Dual-diode	R_{on} (PD-mode) (Ω)	I_{BD} (PD-mode) (A)	$V_{transient}$ (PD-mode) (V)	R_{on} (NS-mode) (Ω)	I_{BD} (NS-mode) (A)	$V_{transient}$ (NS-mode) (V)
Traditional	DD_40	1.78	4.94	4.65	1.66	4.65	4.95
Type III		2.79	4.18	7.61	2.55	4.52	8.06
Type IV		2.28	5.23	7.06	2.23	4.55	7.15

3.6.5 ESD Robustness

In order to measure the ESD robustness of each test device, the die must be packaged and wired, as shown in Fig. 3.41. This thesis uses the Compact ESD simulator HCE-5000 to perform the HBM ESD robustness test of traditional and proposed structures, as shown in Fig. 3.42. The human body model (HBM) is a commonly used model for testing the sensitivity of a device to ESD. The HBM ESD robustness of these fabricated devices have been test. The measurement of HBM is set to apply stress from 1kV to 8kV (one step per 0.5kV). In each step, three stresses are applied to the device within 0.3 seconds. The failure criterion is defined as the voltage shifting more than 30% at 1μA of I-V characteristics after HBM ESD stressed. The HBM-measurement results of traditional and proposed structures are organized in Table 3.10. The $HBM_{(PD\text{-}mode)}$ and $HBM_{(NS\text{-}mode)}$ ESD robustness of all test structures are larger than 8kV. It means that all test structures have a sufficiently high HBM level. To further compare ESD robustness of each test structure, the HMM ESD robustness of these fabricated devices have been test with ESD gun.

This thesis uses the ESD simulator ESS-B3011 to perform human metal model (HMM) ESD robustness test of traditional and proposed structures, as shown in Fig 3.43. The HMM measurement is another stronger ESD test and the energy of HMM test is much higher than HBM test. The HMM test applied on the component level to predict the ESD performance at the system level. The HMM test is measured from 1kV (one step per 0.1kV). In each step, one stress is applied to the device within 0.05 seconds. The definition of HMM's failure criterion is the same as HBM test. The $HMM_{(PD\text{-}mode)}$ and $HMM_{(NS\text{-}mode)}$ ESD robustness of traditional structure, Type I, Type II, Type III, and Type IV with dual diodes (W=40μm) are 2.6kV, 2.5kV, 2.6kV, 2.5kV, and 2.7kV,

respectively. The HMM $_{(PD\text{-}mode)}$ and HMM $_{(NS\text{-}mode)}$ ESD robustness of traditional structure, Type I, Type II, Type III, and Type IV with dual diodes (W=80μm) are 4.0kV, 3.6kV, 3.7kV, 3.7kV, and 4.2kV, respectively. The HMM $_{(PD\text{-}mode)}$ and HMM $_{(NS\text{-}mode)}$ ESD robustness of traditional structure, Type I, Type II, Type III, and Type IV with dual diodes (W=120μm) are 4.6kV, 3.9kV, 4.0kV, 3.9kV, and 4.8kV, respectively. It can be observed that the structures with diode width of 120μm have no significantly higher HMM level than the structures with diode width of 80μm. The reason for this result is that the metal traces have melted before the dual diodes burned. The HMM-measurement results of all test structures are listed in Table 3.10.

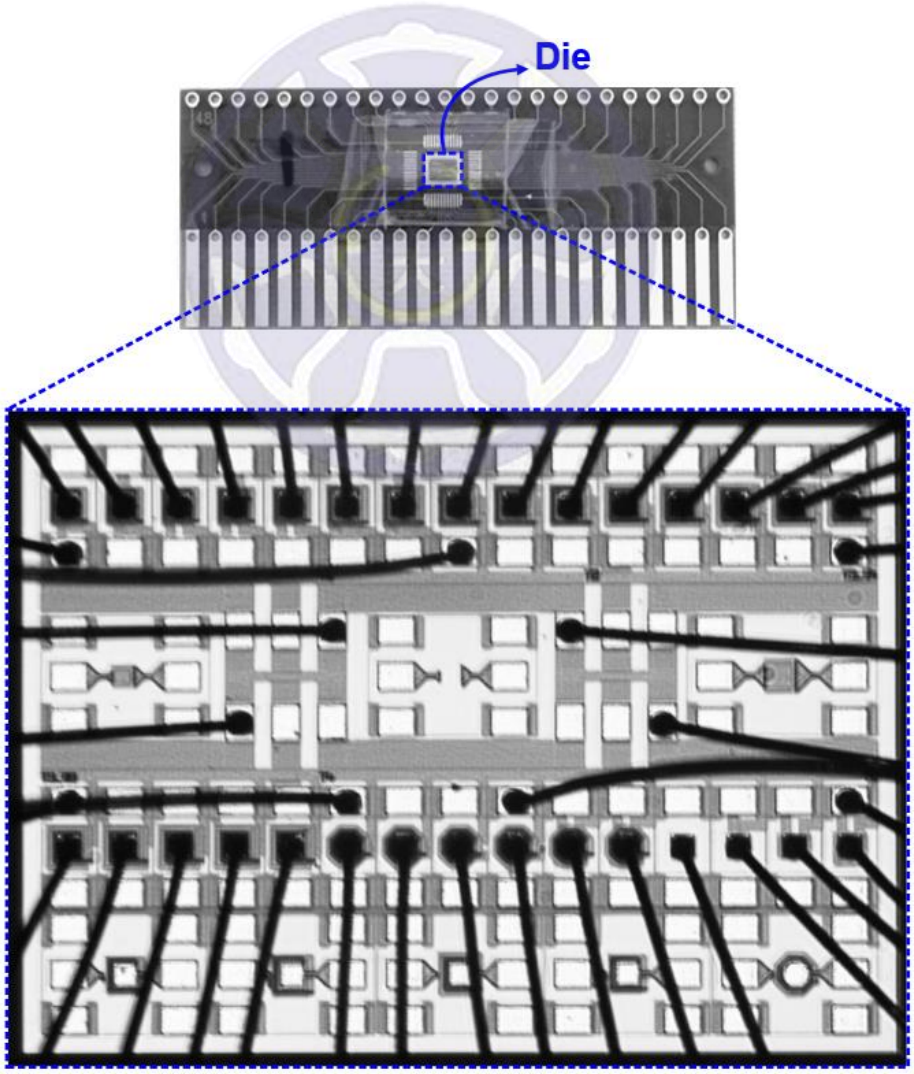


Fig. 3.41 Picture of the packaged die.

Fig. 3.42. Compact ESD simulator HCE-5000.

Fig. 3.43. ESD simulator ESS-B3011.

Table 3.10

The ESD robustness of all test devices.

I/O pad	Dual-diode	HBM (PD-mode)	HBM (NS-mode)	HMM (PD-mode)	HMM (NS-mode)
Traditional	DD_40	>8kV	>8kV	2.6kV	2.6kV
	DD_80	>8kV	>8kV	4.0kV	4.0kV
	DD_120	>8kV	>8kV	4.6kV	4.6kV
Type I	DD_40	>8kV	>8kV	2.5kV	2.5kV
	DD_80	>8kV	>8kV	3.6kV	3.6kV
	DD_120	>8kV	>8kV	3.9kV	3.9kV
Type I + C_M	DD_40	>8kV	>8kV	2.5kV	2.5kV
	DD_80	>8kV	>8kV	3.6kV	3.6kV
Type II	DD_40	>8kV	>8kV	2.6kV	2.6kV
	DD_80	>8kV	>8kV	3.7kV	3.7kV
	DD_120	>8kV	>8kV	4.0kV	4.0kV
Type II + C_M	DD_40	>8kV	>8kV	2.6kV	2.6kV
	DD_80	>8kV	>8kV	3.7kV	3.7kV
Type III	DD_40	>8kV	>8kV	2.5kV	2.5kV
	DD_80	>8kV	>8kV	3.7kV	3.7kV
	DD_120	>8kV	>8kV	3.9kV	3.9kV
Type III + C_M	DD_40	>8kV	>8kV	2.5kV	2.5kV
	DD_80	>8kV	>8kV	3.7kV	3.7kV
Type IV	DD_40	>8kV	>8kV	2.7kV	2.7kV
	DD_80	>8kV	>8kV	4.2kV	4.2kV
	DD_120	>8kV	>8kV	4.8kV	4.8kV
Type IV + C_M	DD_40	>8kV	>8kV	2.7kV	2.7kV
	DD_80	>8kV	>8kV	4.2kV	4.2kV

3.6.5 Failure Analysis

The chip pictures of proposed structures after HMM test are shown in Figs. 3.44. It can be observed that most of the burnt place is the top metal plate of stacked inductor. The connection of stacked inductor (Via 5-6) cannot withstand large ESD stress, so the discharge capacity of proposed structure is dominated by the stacked inductor. Therefore, the design of stacked inductor should be further improved. Some improved solution for stacked inductors will be mentioned in the Section 3.10.

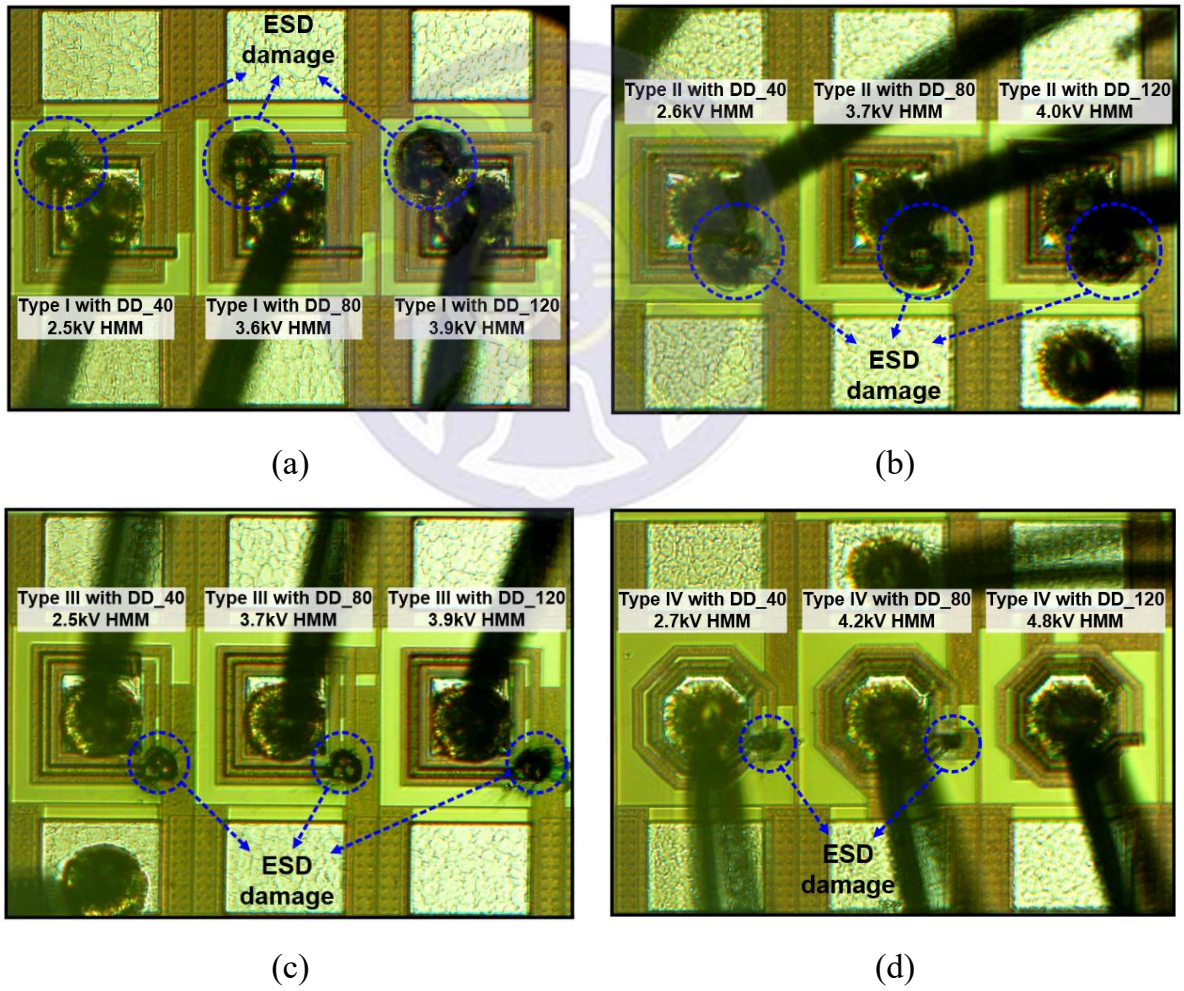


Fig. 3.44. The chip micrographs of the low-loss I/O pads (a) Type I, (b) Type II, (c) Type III, and (d) Type IV with the dual-diode ESD protection after the HMM test.

3.7 Comparison of Traditional and Proposed Structures

The figures of merit (FOMs) of all test structures are compared in Table 3.11. The low signal loss and the high ESD protection level are necessary for high-frequency applications. The I_{BD} is expressed as a breakdown current that the internal circuit can withstand a maximum voltage of 10V in the 0.18μm CMOS process. A higher value of I_{BD} indicates a higher ESD protection level of device. The $Loss_{(max)}$ is defined as the maximum signal loss at K/Ka-bands and the value of $Loss_{(max)}$ should be as small as possible. The HMM means the maximum voltage level that a device can withstand under the component-level test with ESD gun. The values of $I_{BD\ (PD\text{-}mode)}/Loss_{(max)}$ and $I_{BD\ (NS\text{-}mode)}/Loss_{(max)}$ indicate the breakdown current per unit the maximum signal loss of the device in PD-mode and NS-mode, respectively. The value of $HMM/Loss_{(max)}$ indicate the robustness of per unit maximum signal loss of a device under the ESD test in PD-mode and NS-mode. The value of $Area*Loss_{(max)}$ indicate the layout area multiplied by the maximum signal loss of a device.

Table 3.11 shows the proposed structures have higher $I_{BD\ (PD\text{-}mode)}/Loss_{(max)}$, $I_{BD\ (NS\text{-}mode)}/Loss_{(max)}$, $HMM/Loss_{(max)}$ and $HMM/Area*Loss_{(max)}$ than traditional structure. Although the I_{BD} of traditional structure are about 1.5 times larger than proposed structures, the $Loss_{(max)}$ of proposed structures are much lower than traditional structure. Similarly, the HMM level of traditional structure are slightly larger than proposed structures, but there is a problem of excessive signal loss of traditional structure. Based on these results, both the $I_{BD}/Loss_{(max)}$ and the $HMM/\ Loss_{(max)}$ of proposed structures are much higher than the traditional structure, whether in PD-mode or NS-mode. The proposed structures will be further compared with the previous literatures in the next section.

Table 3.11

The comparison results of all test devices.

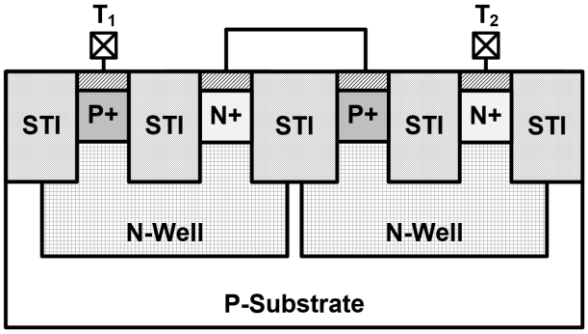
I/O pad	Dual-diode	$I_{BD\ (PD\text{-}mode)}$/ $Loss_{(max)}$ (A/dB)	$I_{BD\ (NS\text{-}mode)}$/ $Loss_{(max)}$ (A/dB)	HMM/ $Loss_{(max)}$ (kV/dB)	HMM/ $Area*Loss_{(max)}$ ($V/\mu m^2*dB$)
Traditional	DD_40	0.39	0.42	0.41	0.16
	DD_80	0.29	0.28	0.38	0.10
	DD_120	0.31	0.33	0.33	0.07
Type I	DD_40	1.28	1.29	1.62	0.24
	DD_80	1.49	1.63	2.13	0.32
	DD_120	1.57	1.66	2.09	0.31
Type I + C_M	DD_40	1.46	1.46	1.83	0.27
	DD_80	1.56	1.47	2.35	0.36
Type II	DD_40	2.36	2.22	3.09	0.38
	DD_80	2.81	2.64	4.10	0.51
	DD_120	2.80	2.94	3.80	0.47
Type II + C_M	DD_40	2.61	2.33	3.25	0.40
	DD_80	2.89	2.86	4.45	0.55
Type III	DD_40	2.39	2.41	3.20	0.36
	DD_80	3.15	3.36	5.21	0.58
	DD_120	2.67	3.05	4.06	0.46
Type III + C_M	DD_40	2.66	2.68	3.37	0.38
	DD_80	3.40	3.58	5.28	0.60
Type IV	DD_40	1.81	1.78	2.32	0.31
	DD_80	2.21	1.96	3.68	0.50
	DD_120	2.17	2.29	3.55	0.48
Type IV + C_M	DD_40	2.07	1.88	2.59	0.35
	DD_80	2.33	2.16	3.85	0.52

3.8 Comparison of Literature

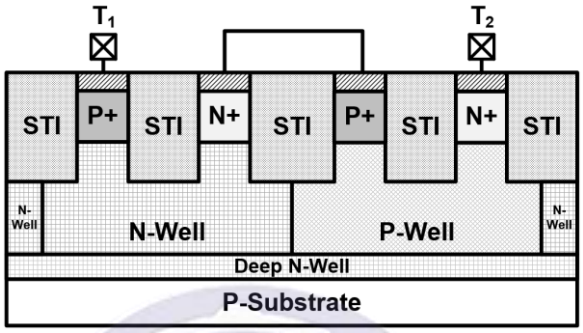
In order to reduce the parasitic capacitance of ESD protection diode, some improved methods have been proposed in the previous literatures. The structure of the stacked diodes can effectively reduce the parasitic capacitance. Assuming that the number of diodes is N, the parasitic capacitance will be reduced by N times. In addition, the silicon controlled rectifier (SCR) has the advantages of high ESD robustness and low parasitic capacitance in a small layout area. Therefore, the SCR is also often used as ESD protection device for high-frequency applications.

Reference [32] proposed a variety of dual diodes with embedded SCRs (DD-SCRs) for high-speed applications. Figs. 3.45 (a), (b), (c), and (d) show the cross-sectional views of P+/NW stacked diode, STI-bounded DD-SCR, metal-bounded DD-SCR, and junction-bounded DD-SCR., respectively. For the P+/NW stacked diodes and the DD-SCRs, two diodes are connected in series between T_1 and T_2. These structures can reduce the turn-on resistance, parasitic capacitance, and increase ESD rubustness by adjusting the STI, metal, and junction.

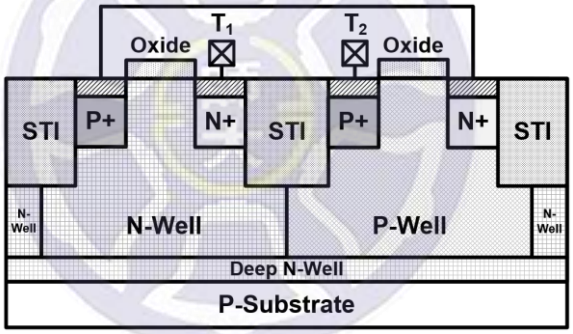
Reference [33] proposed two improved structures of stacked diodes with embedded SCR. Figs. 3.46 (a), (b), and (c) show the cross-sectional views of P-type stacked diode (SD_P), traditional P-type stacked diodes with embedded SCR (T_SDSCR_P), and proposed P-type stacked diodes with embedded SCR (P_SDSCR_P), respectively. These structures can reduce the turn-on resistance and improve ESD robustness by shorting the parasitic path of SCR, docking P+ and N+ junctions, and using silicide to short P-Well and N-Well.



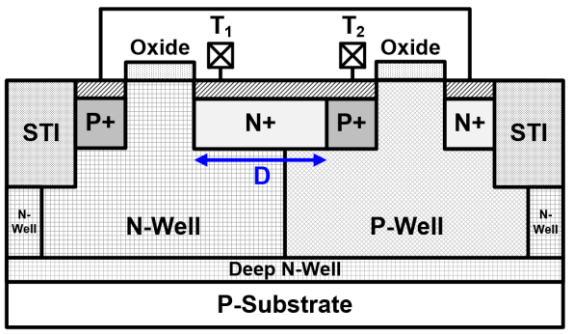
(a)



(b)

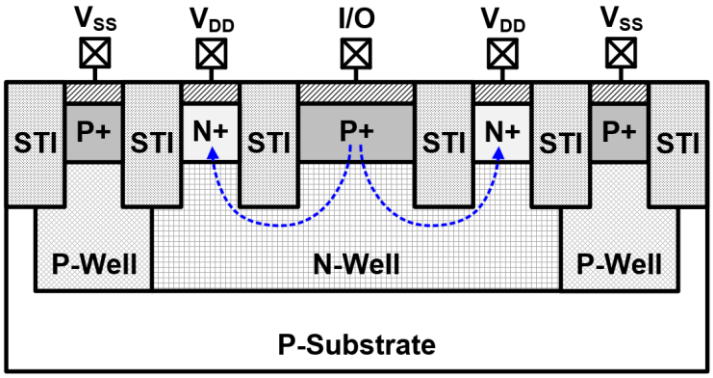


(c)

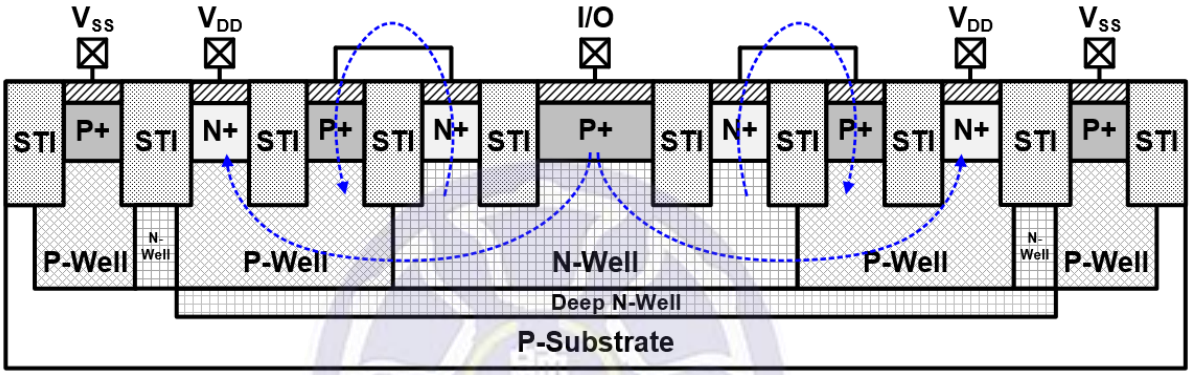


(d)

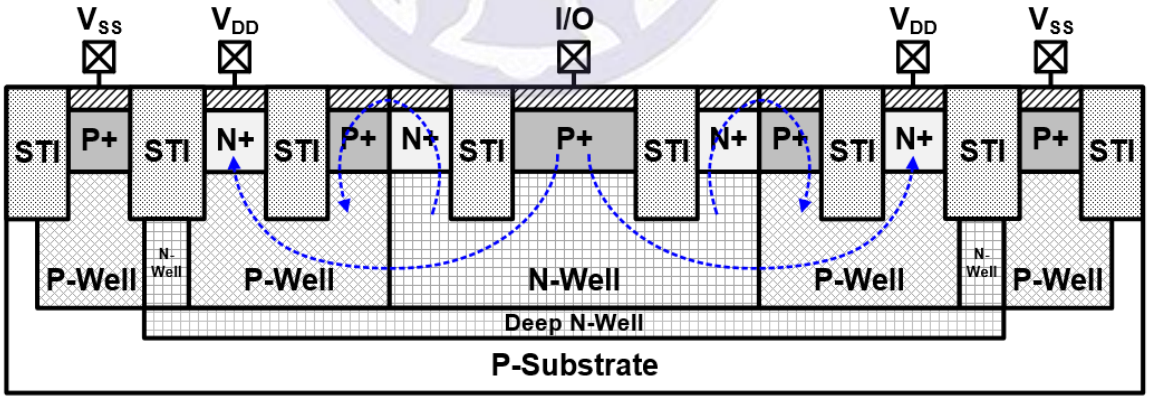
Fig. 3.45. In the Reference [32], the cross-sectional views of (a) P+/NW stacked diodes, (b) STI-bounded DD-SCR, (c) metal-bounded DD-SCR, and (d) junction-bounded DD-SCR.



(a)



(b)



(c)

Fig. 3.46. In the Reference [33], the cross-sectional views of (a) P-type stacked diode (SD_P), (b) traditional P-type stacked diodes with embedded SCR (T_SDSCR_P), and (c) proposed P-type stacked diodes with enbedded SCR (P_SDSCR_P).

In order to compare the performance of ESD protection scheme between this thesis, reference [32], and reference [33], the figures of merit (FOMs) are defined as HBM/$C_{Parasitic}$ and HMM/$C_{Parasitic}$. The $C_{Parasitic}$ is the equivalent parasitic capacitance of the ESD protection device in the operating band. The comparison results of all ESD protection schemes are organized in Table 3.12. It can be observed that the HBM/$C_{Parasitic}$ and HMM/$C_{Parasitic}$ of the proposed structures in this thesis are higher than the previous literatures. Although the equivalent parasitic capacitances of the ESD protection schemes are low enough in the previous literatures, these do not have enough ESD robustness.

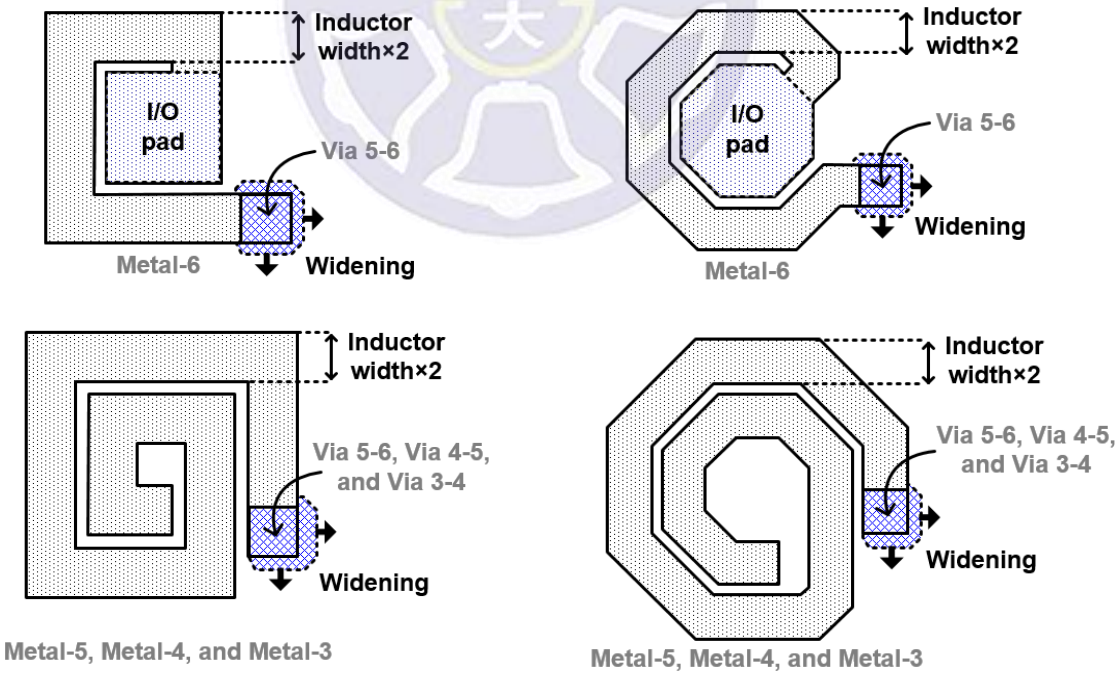
Table 3.12

The comparison of proposed and previous designs.

Device		Width (μm)	$C_{Parasitic}$ (fF)	HBM/$C_{Parasitic}$ (V/fF)	HMM/$C_{Parasitic}$ (V/fF)
This thesis	Traditional	40	207.9	38	12
	Type I		19.4	412	128
	Type I + C_M		22.3	358	112
	Type II		17.6	454	147
	Type II + C_M		20.4	392	127
	Type III		15.8	506	158
	Type III + C_M		19.2	416	130
	Type IV		14.9	536	181
	Type IV + C_M		22.1	361	122
Reference [32]	P+/NW stacked diode	40	14.3	130	N/A
	STI-bounded DD-SCR		12.1	147	
	metal-bounded DD-SCR		22.2	96	
	junction-bounded DD-SCR		20.6	100	
Reference [33]	SD_P	30	42.2	99	26
	T_SDSCR_P		34.0	132	41
	P_SDSCR_P		33.7	18	50

3.9 Discussion of This Chapter

The proposed structures have a problem of higher turn-on resistance due to the stacked inductor. According to the failure analysis, it can be known that the metal of stacked inductor will melt first before the ESD protection diode burns out. In order to improve these shortcomings of the proposed structure, some methods are proposed. As shown in Figs. 3.47 (a) and (b), widening the inductor width can effectively reduce the parasitic resistance of the stacked inductor. In addition, widening the connection (Via 5-6, Via 4-5, and Via 3-4) of the stacked inductor can improve ESD robustness. However, widening the inductor width will reduce the inductance value under the limited area. As shown in Fig. 3.48, the structure of inter-digitized capacitor has higher capacitance to compensate the problem of insufficient inductance [34].



(a) (b)

Fig. 3.47. The (a) rectangular inductor and (b) octagonal inductor with wider inductor width and metal connection (Via) to reduce the parasitic resistance of stacked inductor.

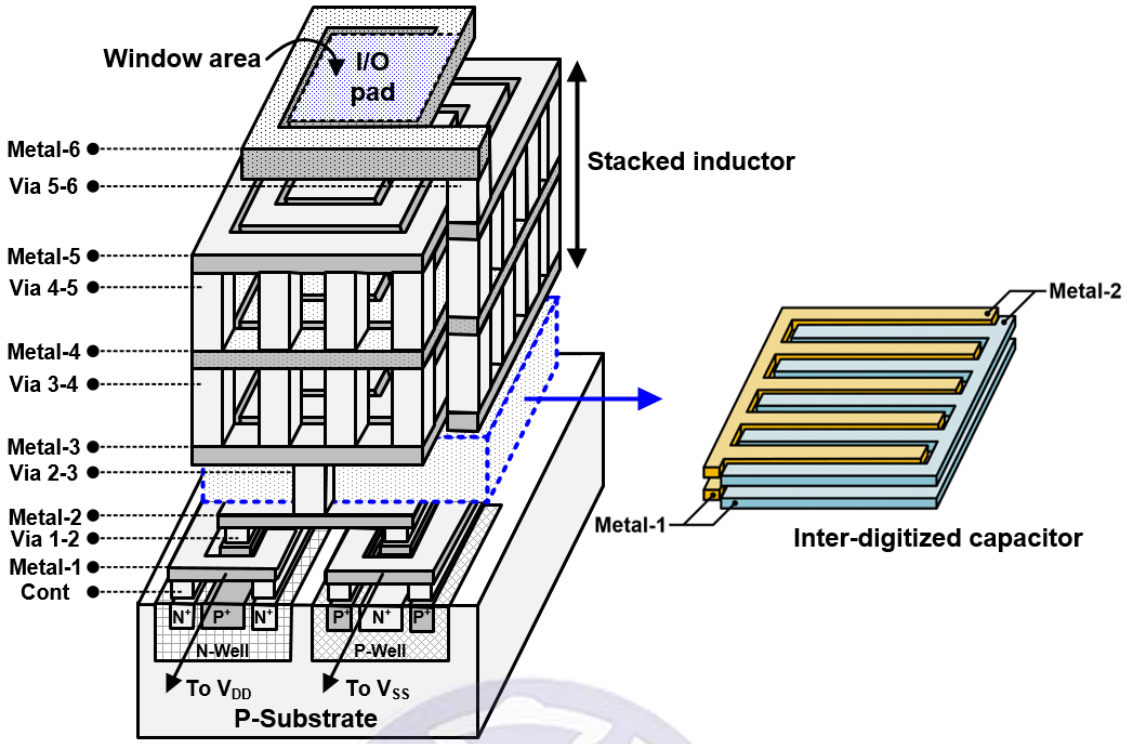


Fig. 3.48. The structure of inter-digitized capacitor.

3.10 Summary of This Chapter

The traditional I/O pad and the proposed low-loss I/O pads have been implemented in the 0.18μm CMOS process for K/Ka-bands applications. The ESD protection design in I/O pad is an important consideration to have sufficient ESD robustness without losing the original characteristics of high-frequency. Although the traditional I/O pad with dual-diode ESD protection can provide effective protection, the signal is continuously lost. The proposed structures solve this problem of signal loss in K/Ka-bands by the LC-resonance effect between the stacked inductor and the parasitic capacitance of dual-diode ESD protection. The measurement results confirm that the proposed structures have high capability of ESD protection and lower signal loss than the traditional structure. Besides, the stacked inductor and dual diodes of proposed structure are designed under the top metal plate to save chip area.

Chapter 4

Depletion Diodes for High-Voltage Applications

4.1 Traditional P-type Diode

The traditional P-type diode (T_DP) is a two-terminal device with the single conduction path from anode to cathode. Fig. 4.1 shows the cross-sectional view of traditional P-type diode. The anode terminal is connected to P+ diffusion and the cathode terminal is connected to N+ diffusion. Fig. 4.2 shows the layout top view of T_DP and the distance parameters of A, B, and C are designed to be 10μm, 20μm, and 4.5μm, respectively. This thesis designed a traditional P-type diode with the diode widths of 20μm. The P-type traditional diode can only provide a positive voltage from anode to cathode. However, a novel structure of bidirectional diode for high-voltage applications is proposed in the next section.

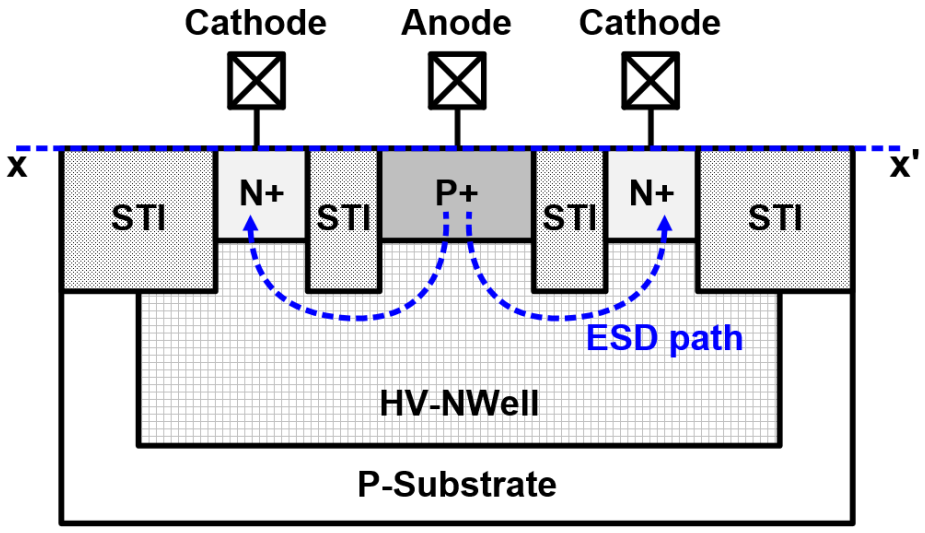


Fig. 4.1. The cross-sectional view of tradtional P-type diode (T_DP).

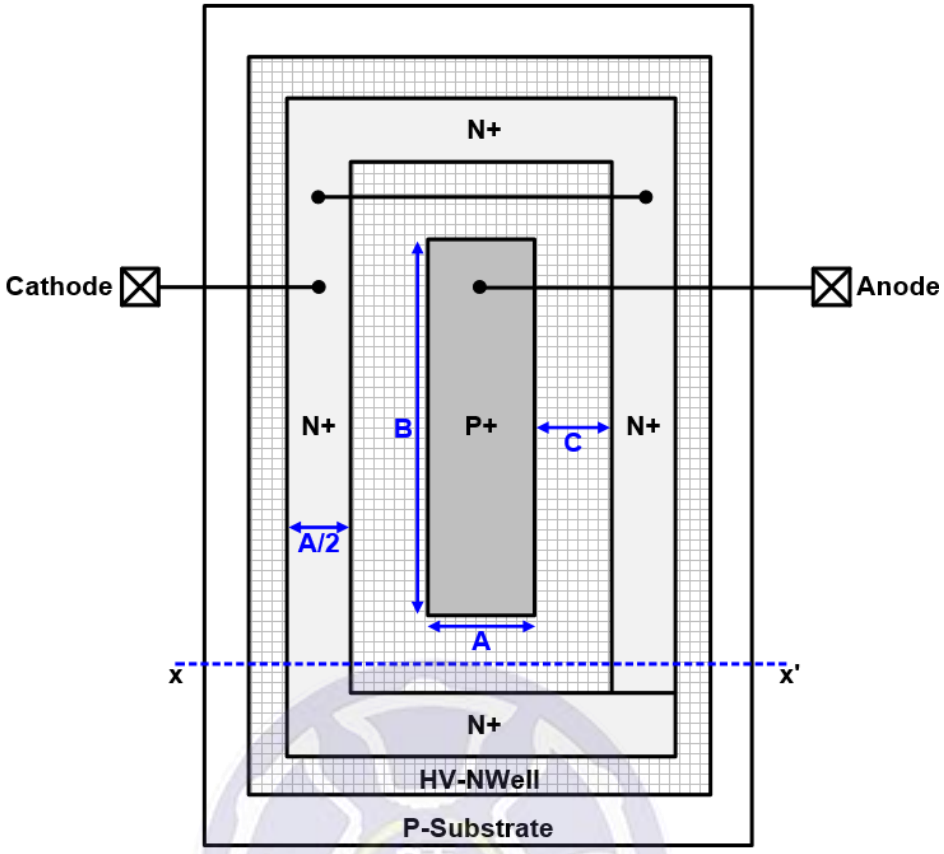


Fig. 4.2. The layout top view of the traditional P-type diode (T_D$_P$).

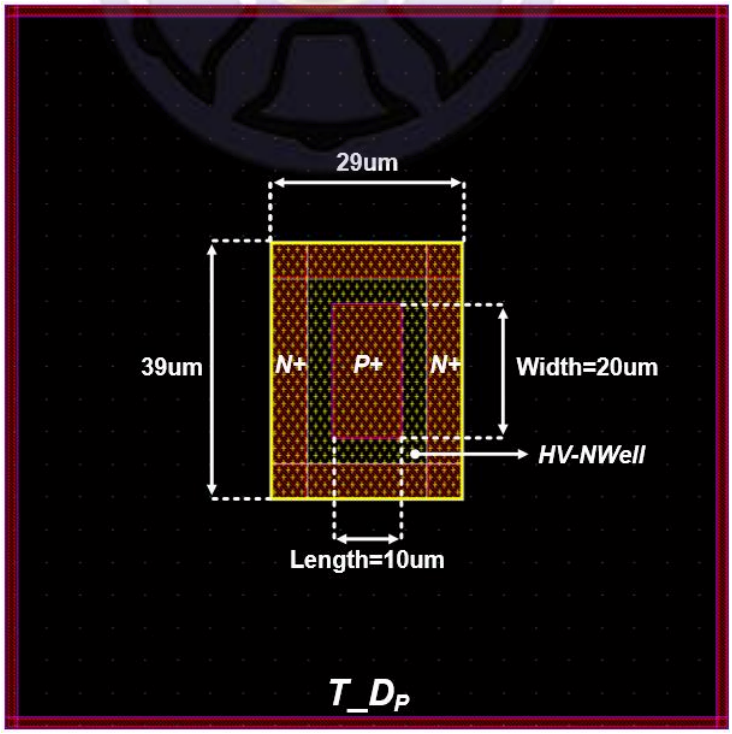


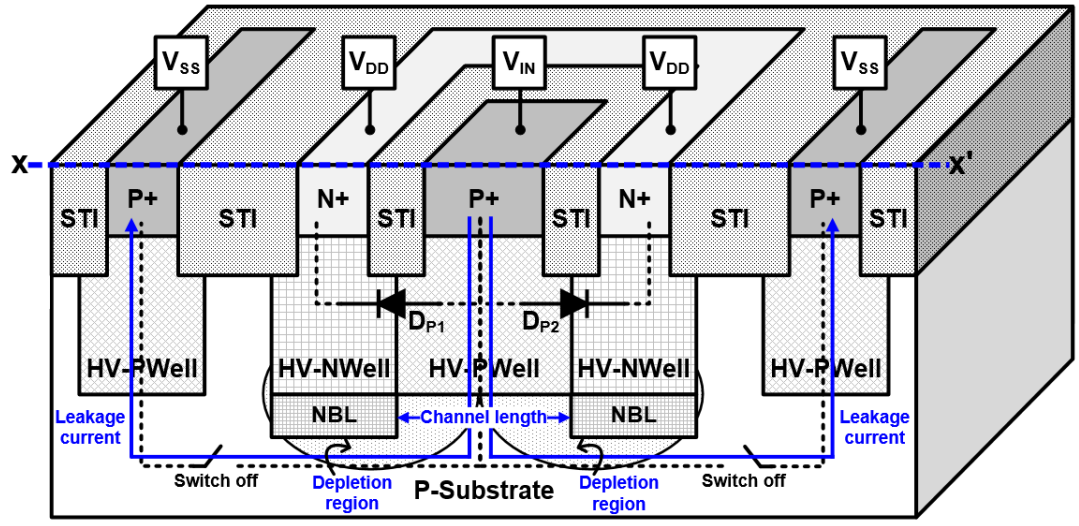
Fig. 4.3. The layout top view of the traditional P-type diode (T_D$_P$).

4.2 P-type Depletion Diodes

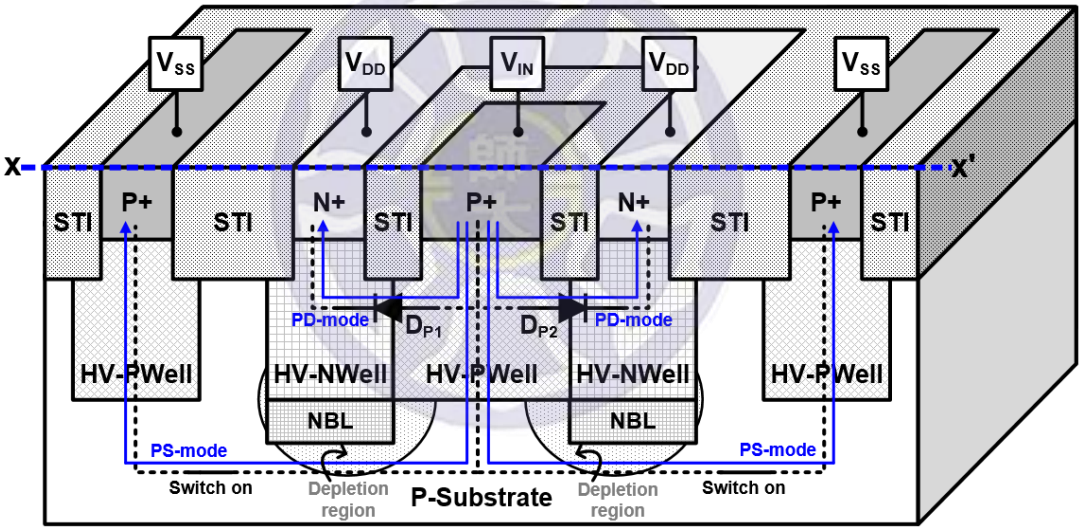
Compared to the traditional diode is a two-terminal device, the proposed depletion diodes are the three-terminal device with two conduction paths from V_{IN} to V_{DD} and V_{IN} to V_{SS}. Fig. 4.4 (a) shows the cross-sectional view of P-type depletion diodes (D_D_P) under the normal operating condition (V_{DD}>V_{IN}>V_{SS}). The V_{IN} and V_{SS} are connected to P+/HV-PWell and the V_{DD} is connected to N+/HV-NWell. The distance between N-type buried layer (NBL) is defined as the channel length and this channel is controlled by the depletion region of PN-junction. The depletion region controls the cut-off and turn-on of this channel like a switch.

In the normal operation, the D_{P1} and D_{P2} are turned off due to the reverse bias. The PN-junction near the channel will form a large area of depletion region and the channel is closed (switch off). In order to ensure a sufficiently low leakage current, the depletion region must completely cover the channel. The distance between NBL and the bias between V_{IN} and V_{DD} are the important factors to determine the depletion region of the channel.

Fig. 4.4 (b) shows the cross-sectional view of P-type depletion diodes (D_D_P) under ESD stress (V_{IN}>V_{DD}>V_{SS}). When a positive voltage occurs at V_{IN}, the D_{P1} and D_{P2} are turned on and the depletion region near the channel disappears (switch on). The ESD current will discharge to V_{DD} through D_{P1} and D_{P2} (PD-mode) and discharge to V_{SS} through P-Substrate (PS-mode).



(a)



(b)

Fig. 4.4. The cross-sectional view of P-type depletion diodes (D_D_P) under the (a) normal operating condition (V_{DD}>V_{IN}>V_{SS}) and (b) ESD stress.

Fig. 4.5 shows the layout top view of P-type depletion diodes (D_DP), the most important parameter of A is defined as the distance between NBL (channel length). In order to investigate the effect of channel length for discharge capacity and the magnitude of leakage current, there are four channel length are designed as 3μm, 6μm, 12μm, and 24μm in this thesis. The distances B and C are the diode length and diode width of P-type depletion diodes, respectively. The distance D is expressed as the width of HV-NWell and NBL. The N+/HV-NWell and NBL at the terminal of V_{DD} are designed to completely surround the P+/HV-PWell at the terminal of V_{IN}. It is to ensure that the depletion region can actually close the channel during normal operation.

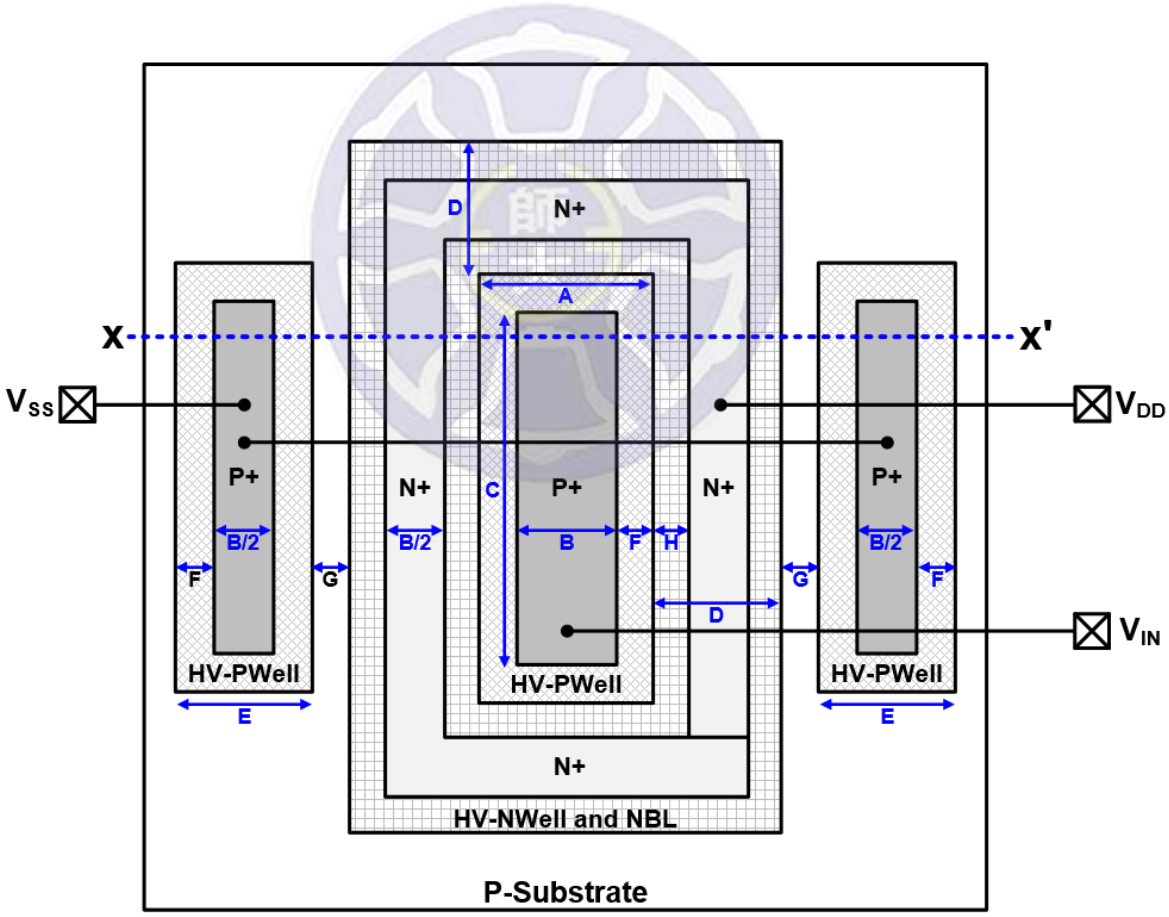
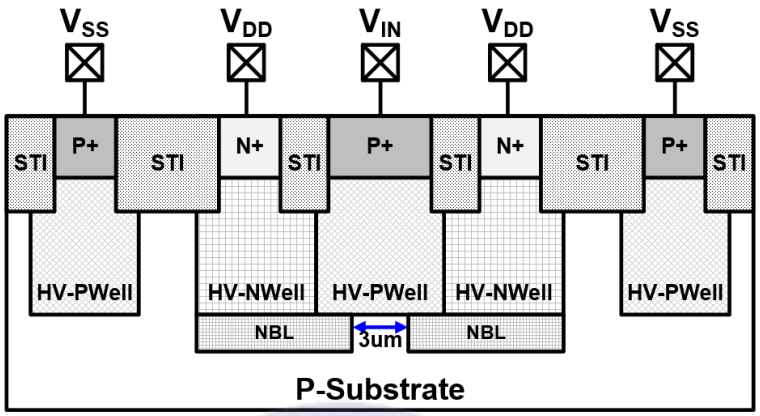
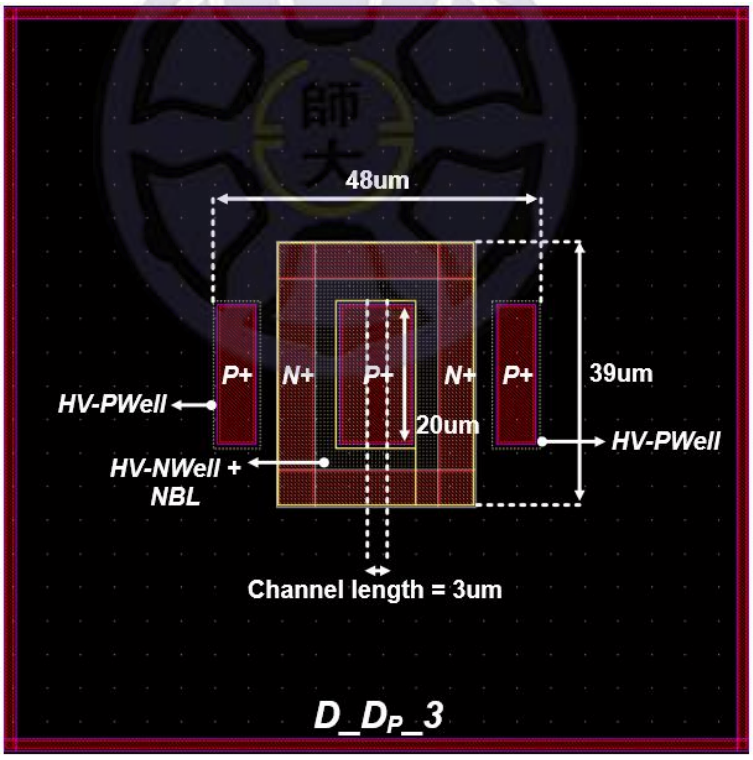


Fig. 4.5. The layout top view of P-type depletion diodes (D_DP).

Figs. 4.6 (a) and (b) show the cross-sectional view and layout top view of P-type depletion diodes (D_DP) with the diode width of 20μm and with the channel length of 3μm (D_DP_3). The design parameters of D_DP_3 are shown in Table 4.1.



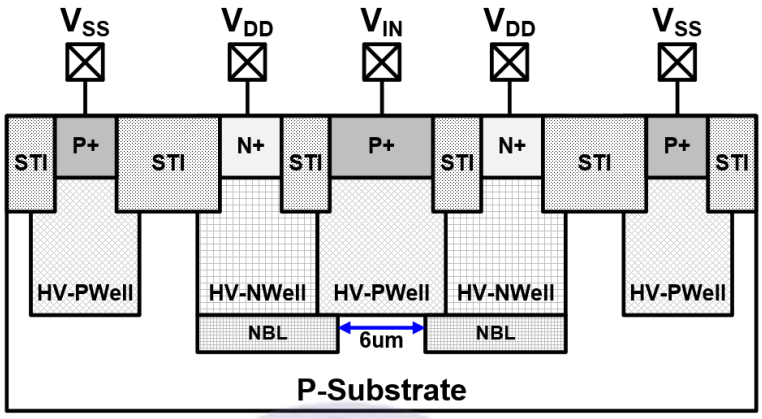
(a)



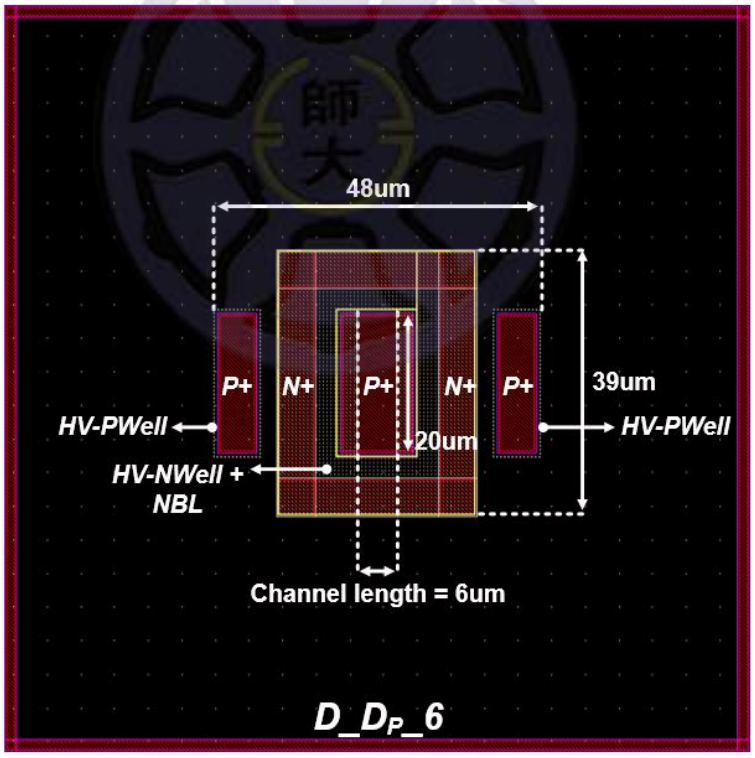
(b)

Fig. 4.6 (a) The cross-sectional view and (b) the layout top view of P-type depletion diodes (D_DP) with the diode width of 20μm and with the channel length of 3μm (D_DP_3).

Figs. 4.7 (a) and (b) show the cross-sectional view and layout top view of P-type depletion diodes (D_DP) with the diode width of 20μm and with the channel length of 6μm (D_DP_6). The design parameters of D_DP_6 are shown in Table 4.1.



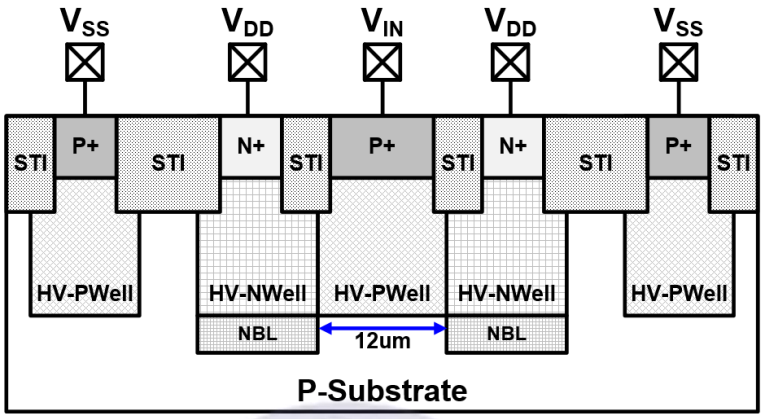
(a)



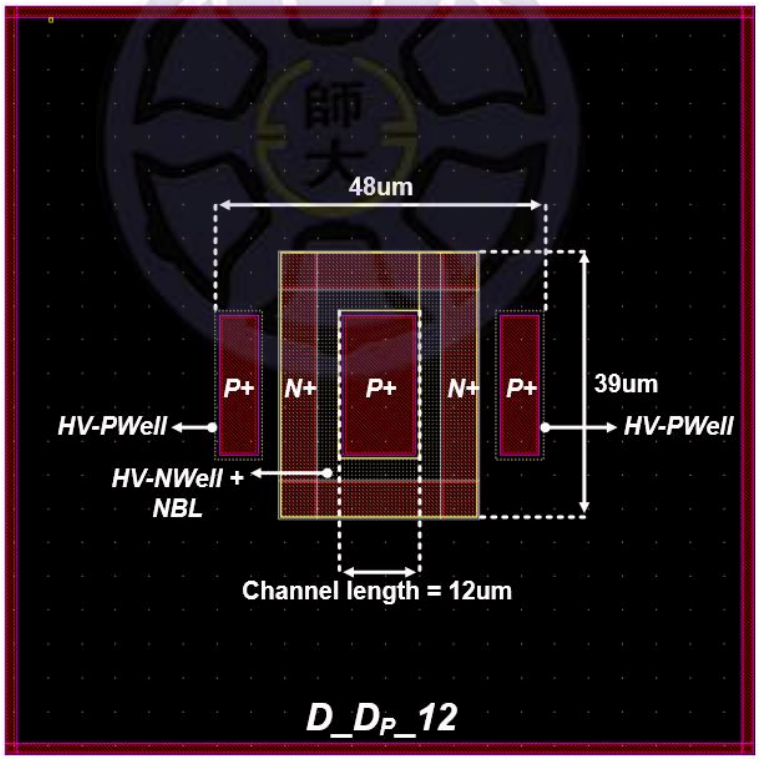
(b)

Fig. 4.7. (a) The cross-sectional view and (b) the layout top view of P-type depletion diodes (D_DP) with the diode width of 20μm and with the channel length of 6μm (D_DP_6).

Figs. 4.8 (a) and (b) show the cross-sectional view and layout top view of P-type depletion diodes (D_DP) with the diode width of 20μm and with the channel length of 12μm (D_DP_12). The design parameters of D_DP_12 are shown in Table 4.1.



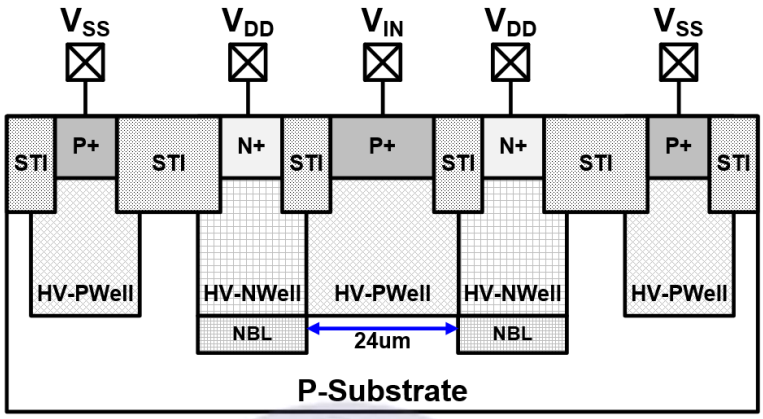
(a)



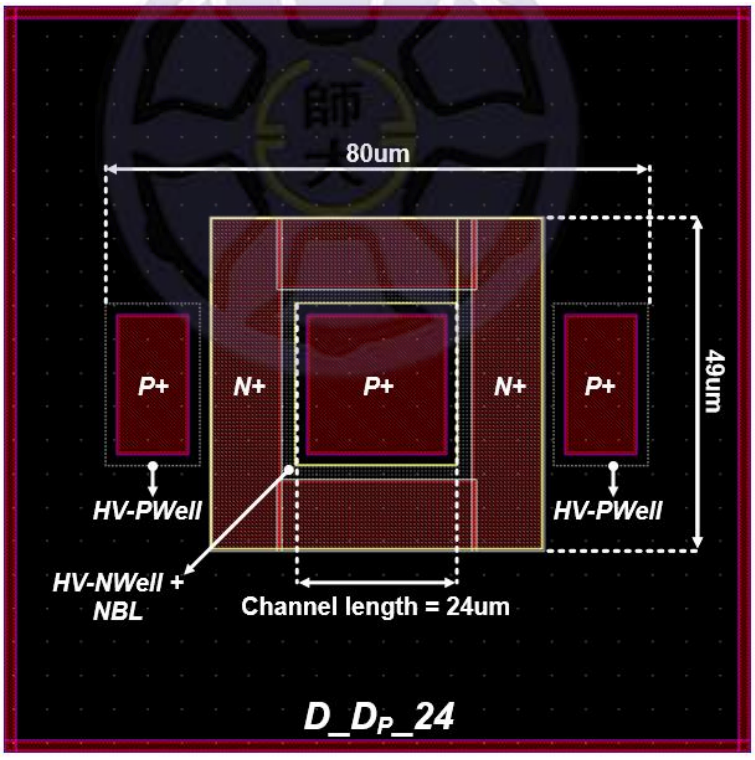
(b)

Fig. 4.8. (a) The cross-sectional view and (b) the layout top view of P-type depletion diodes (D_DP) with the diode width of 20μm and with the channel length of 12μm (D_DP_12).

Figs. 4.9 (a) and (b) show the cross-sectional view and layout top view of P-type depletion diodes (D_DP) with the diode width of 20μm and with the channel length of 24μm (D_DP_24). The design parameters of D_DP_24 are shown in Table 4.1.



(a)



(b)

Fig. 4.9. (a) The cross-sectional view and (b) the layout top view of P-type depletion diodes (D_DP) with the diode width of 20μm and with the channel length of 24μm (D_DP_24).

Table 4.1

The design parameters of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 3μm (D_D_P_3), 6μm (D_D_P_6), 12μm (D_D_P_12), and 24μm (D_D_P_24).

Device	A (μm)	B (μm)	C (μm)	D (μm)	E (μm)	F (μm)	G (μm)	H (μm)
D_D_P_3	3	10	20	8.85	7	0.95	2.75	3.45
D_D_P_6	6	10	20	8.85	7	0.95	2.75	3.45
D_D_P_12	12	10	20	8.85	7	0.95	2.75	3.45
D_D_P_24	24	20	20	8.85	14	1.95	1.75	3.45

4.3 Measurement Methods and Results

The P-type depletion diodes (D_DP) have been fabricated in a 0.50μm CMOS process. Fig. 4.14 shows the chip photo of all test devices. The top metal plate (metal-3) is used to route to V_{IN} and the lower metals (metal-1 and metal-2) are used to route to V_{SS} and V_{DD}. These test devices are prepared with the DC measurement, TLP measurement, Human-Body Model (HBM) robustness measurement, and Human-Metal Model (HMM) robustness measurement.

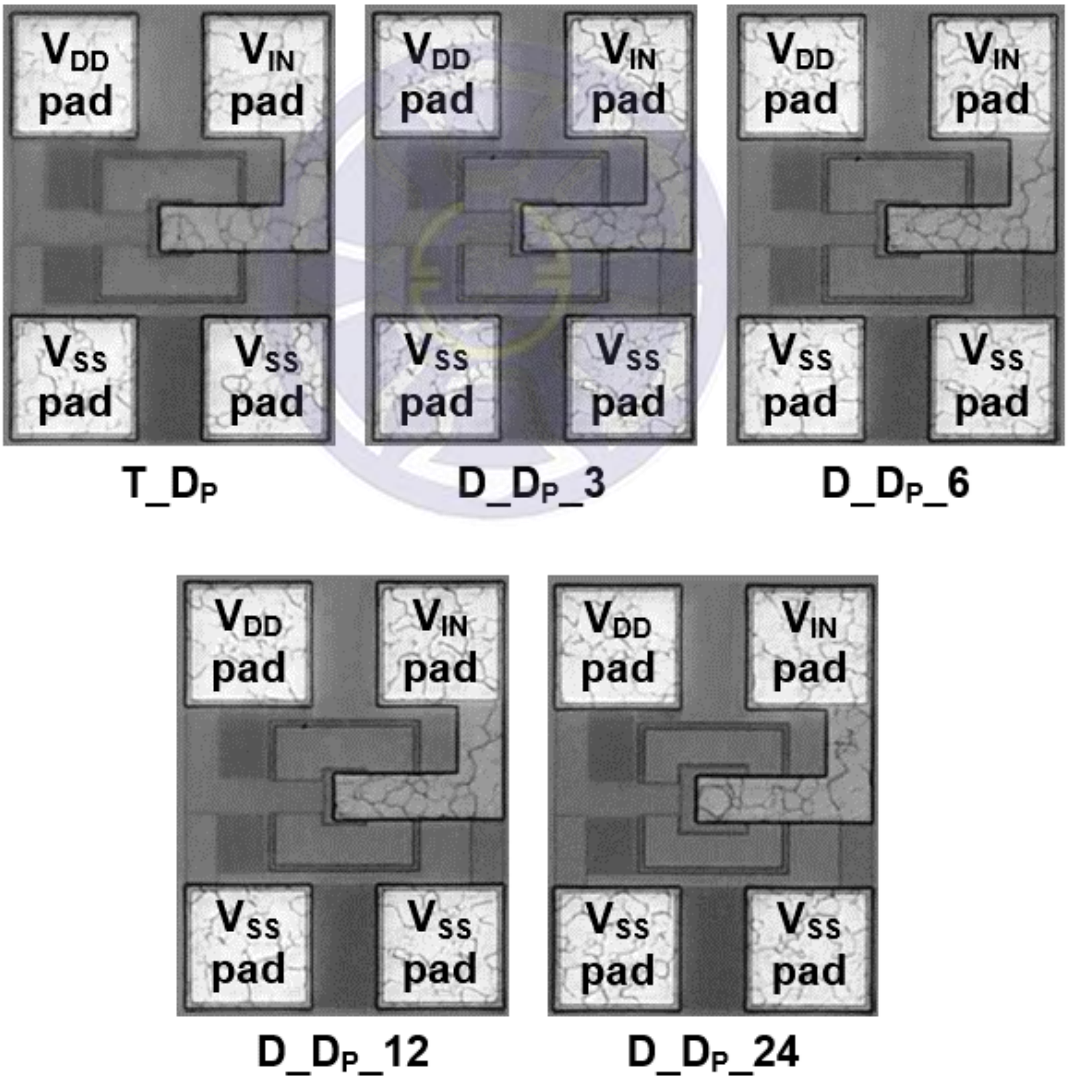


Fig. 4.10. Chip photo of all test devices.

4.3.1 DC Measurement

In order to obtain the leakage current of P-type depletion diodes under normal operation, this thesis uses Semiconductor Characterization System (SCS) to measure all test devices, as shown in Fig. 4.11. In order to observe the characteristics of each device under different bias voltages, the V_{DD} is set to 5V, 10V, and 15V and the V_{SS} is the lowest potential of 0V. The V_{IN} is swept from 0V to (V_{DD} + 1V). Fig. 4.12 shows the DC bias setting of P-type depletion diodes. The distance between NBL is defined as the channel length. The current of channel from V_{IN} to V_{SS} is defined as the leakage current. In order to clearly compare the DC characteristics of each device, the V_{IN} with a 50% increase in leakage current is defined as the $V_{Turn\text{-}on}$. When the input voltage is greater than $V_{Turn\text{-}on}$, it means that the channel cannot be effectively pinched off by the depletion region. Therefore, $V_{Turn\text{-}on}$ should be as high as possible for the P-type depletion diodes. In order to compare the leakage current of each test device under the normal operation, the $I_{Leakage}$ is defined as the leakage current when V_{IN} is equal to V_{DD}. The channel should be pinched off by the depletion region under normal operation, so the $I_{Leakage}$ should be as low as possible.

Fig. 4.11. Picture of Semiconductor Characterization System (SCS).

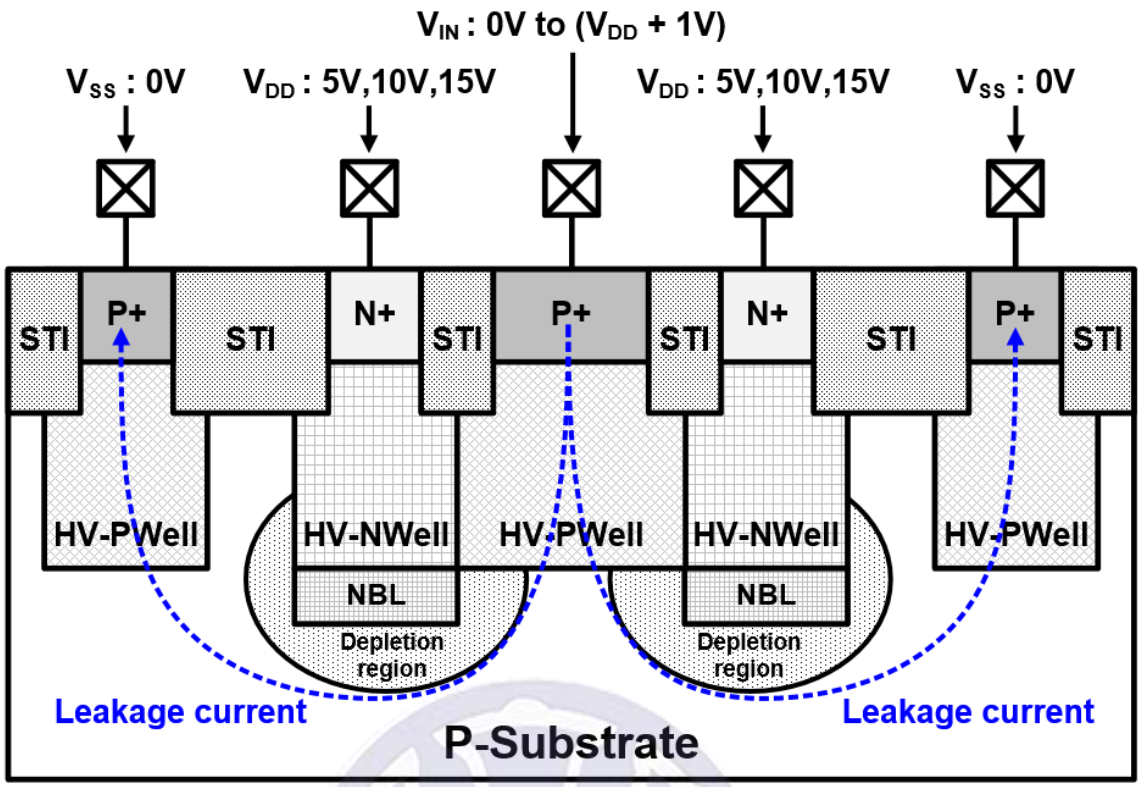


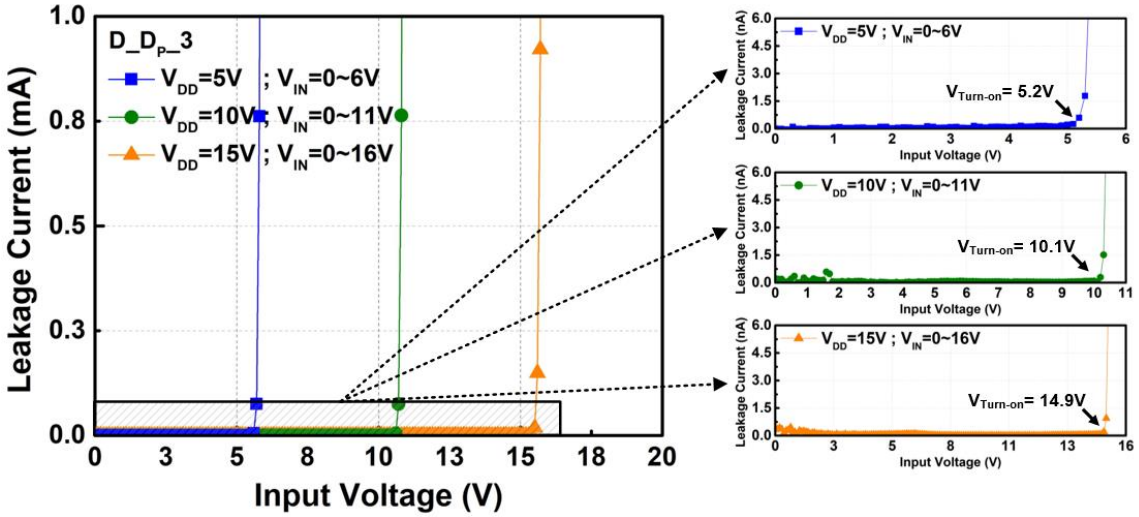
Fig. 4.12. The DC-bias setting of P-type depletion diodes.

Fig. 4.13 (a) shows the DC-measurement results of P-type depletion diodes (D_D_P) with the diode width of 20μm and with the channel length of 3μm (D_D_P_3). From the measurement result of, it can be observed that the leakage currents of D_D_P_3 is low enough under the normal operation (V_{SS}<V_{IN}<V_{DD}). Due to the small channel length of 3μm, the channel can be completely turned off. Then, increasing the V_{IN} to (V_{DD} + 1V) causes the depletion region to disappear and induces large leakage current from V_{IN} to V_{SS}. The leakage currents of D_D_P_3 under the V_{DD} of 5V, 10V, and 15V are shown in Table 4.6. It can be confirmed that D_D_P_3 has sufficiently low leakage current (~pA) under the normal operation. In addition, the D_D_P_3 also have high $V_{Turn\text{-}on}$ of ~ (V_{DD} ± 0.2V).

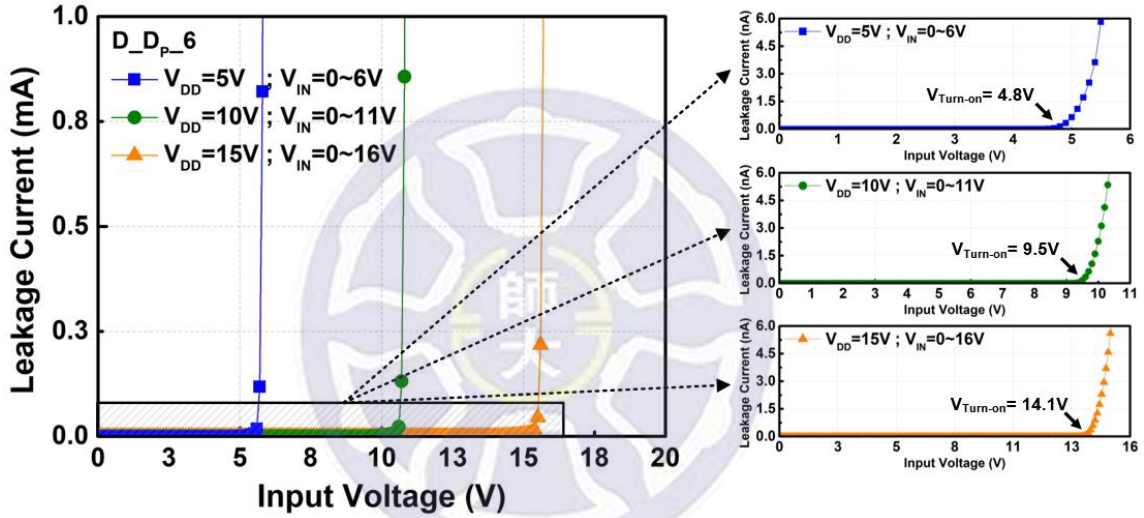
Fig. 4.13 (b) shows the DC-measurement results of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 6μm (D_D_P_6). From the measurement results, the depletion diodes with channel length of 6μm still have low enough leakage current under the normal operation ($V_{SS}<V_{IN}<V_{DD}$). When the V_{IN} is increased to near V_{DD}, the leakage current rises slightly. The leakage currents of D_D_P_6 under the V_{DD} of 5V, 10V, and 15V are shown in Table 4.2. The leakage currents of D_D_P_6 are ~10 times larger than the leakage currents of D_D_P_3.

Fig. 4.13 (c) shows the DC-measurement results of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 12μm (D_D_P_12). From the measurement results, it can be observed that the leakage current increases linearly under the normal operation ($V_{IN} \geqq V_{DD}$). The $V_{Turn\text{-}on}$ of D_D_P_12 is within the range of operation voltage, which means that the channel cannot be pinched off by the depletion region. Table 4.2 shows the leakage currents of D_D_P_12 under the V_{DD} of 5V, 10V, and 15V. The leakage currents with the channel length of 12μm are ~100 times larger than the leakage currents of D_D_P_3.

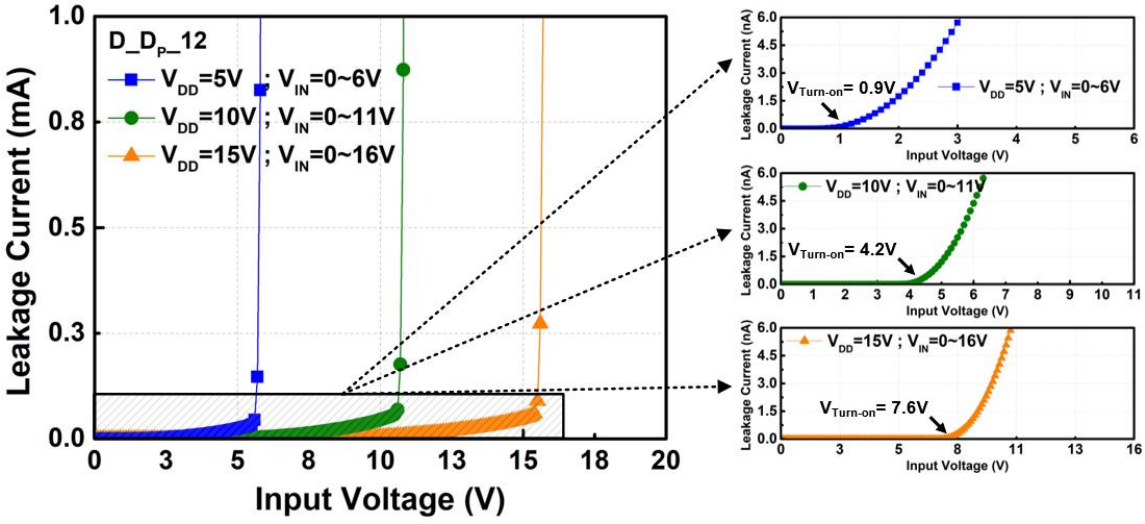
Fig. 4.13. shows the DC-measurement results of the P-type depletion diodes (D_D_P) with the diode width of 20μm and with the channel length of 24μm (D_D_P_24). From measurement results, the problem of leakage current becomes more serious when the channel length is 24μm. The values of $V_{Turn\text{-}on}$ are about 0.1V~0.6V, which means that the channel cannot be pinched off by the depletion region under the normal operation. The leakage currents of D_D_P_24 under the V_{DD} of 5V, 10V, and 15V are shown in Table 4.2. The leakage currents with the channel length of 24μm are ~200 times larger than the leakage currents of D_D_P_3.


D_D_P_3
V_DD=5V ; V_IN=0~6V
V_DD=10V ; V_IN=0~11V
V_DD=15V ; V_IN=0~16V
Leakage Current (mA)
Input Voltage (V)
V_DD=5V ; V_IN=0~6V
V_Turn-on= 5.2V
V_DD=10V ; V_IN=0~11V
V_Turn-on= 10.1V
V_DD=15V ; V_IN=0~16V
V_Turn-on= 14.9V
Leakage Current (nA)
Input Voltage (V)

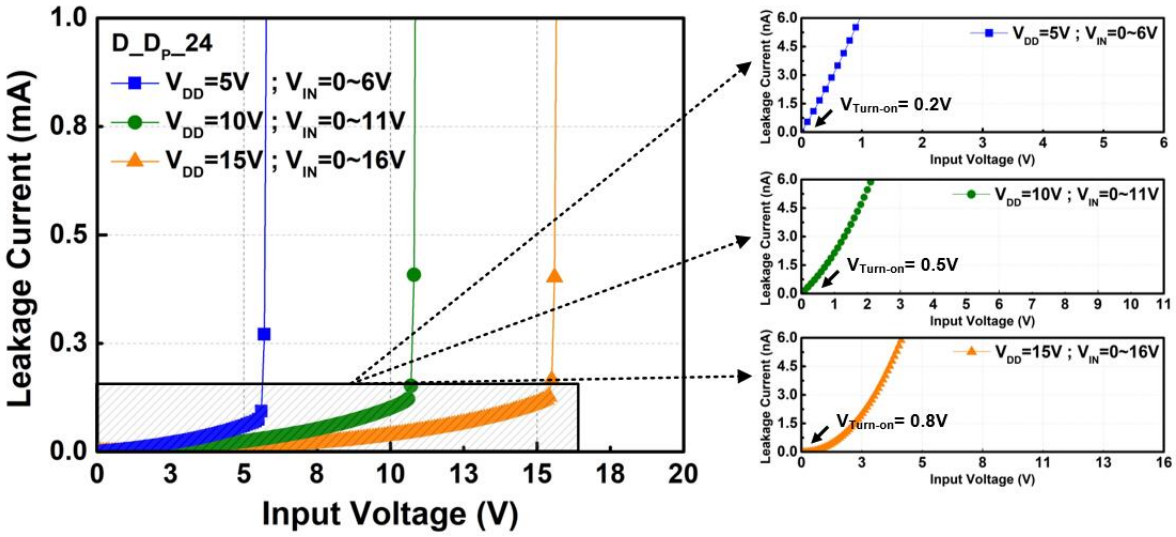
(a)


D_D_P_6
V_DD=5V ; V_IN=0~6V
V_DD=10V ; V_IN=0~11V
V_DD=15V ; V_IN=0~16V
Leakage Current (mA)
Input Voltage (V)
V_DD=5V ; V_IN=0~6V
V_Turn-on= 4.8V
V_DD=10V ; V_IN=0~11V
V_Turn-on= 9.5V
V_DD=15V ; V_IN=0~16V
V_Turn-on= 14.1V
Leakage Current (nA)
Input Voltage (V)

(b)


D_D_P_12
V_DD=5V ; V_IN=0~6V
V_DD=10V ; V_IN=0~11V
V_DD=15V ; V_IN=0~16V
Leakage Current (mA)
Input Voltage (V)
V_Turn-on= 0.9V
V_DD=5V ; V_IN=0~6V
V_DD=10V ; V_IN=0~11V
V_Turn-on= 4.2V
V_DD=15V ; V_IN=0~16V
V_Turn-on= 7.6V
Leakage Current (nA)
Input Voltage (V)

(c)



(d)

Fig. 4.13. The DC-measurement results of P-type depletion diodes (D_DP) with the diode width of 20μm and the channel length of (a) 3μm (D_DP_3), (b) 6μm (D_DP_6), (c) 12μm (D_DP_12), and (d) 24μm (D_DP_24).

Table 4.2

The DC-measurement results of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 3μm (D_D_P_3), 6μm (D_D_P_6), 12μm (D_D_P_12), and 24μm (D_D_P_24).

Device	V_{DD}	$V_{Turn\text{-}on}$	$I_{Leakage}$ (V_{IN}=V_{DD})
D_D_P_3	5V	5.2V	21pA
	10V	10.1V	92pA
	15V	14.9V	150pA
D_D_P_6	5V	4.8V	0.64μA
	10V	9.5V	2.28μA
	15V	14.1V	4.58μA
D_D_P_12	5V	0.9V	24.01μA
	10V	4.2V	45.28μA
	15V	7.6V	47.80μA
D_D_P_24	5V	0.2V	60.11μA
	10V	0.5V	100.94μA
	15V	0.8V	111.70μA

In order to obtain the channel characteristics of P-type depletion diodes, V_{DD} is floated and the DC current from V_{IN} to V_{SS} is measured. The DC-bias setting with floating V_{DD} is shown in Fig. 4.14. The measurement results of P-type depletion diodes with floating V_{DD} are shown in Fig. 4.15. The small channel current is due to the special layout design of NBL and the current from V_{IN} to V_{SS} is discharged by the breakdown mechanism of PNP. The solution to this problem will be presented in Section 4.6.

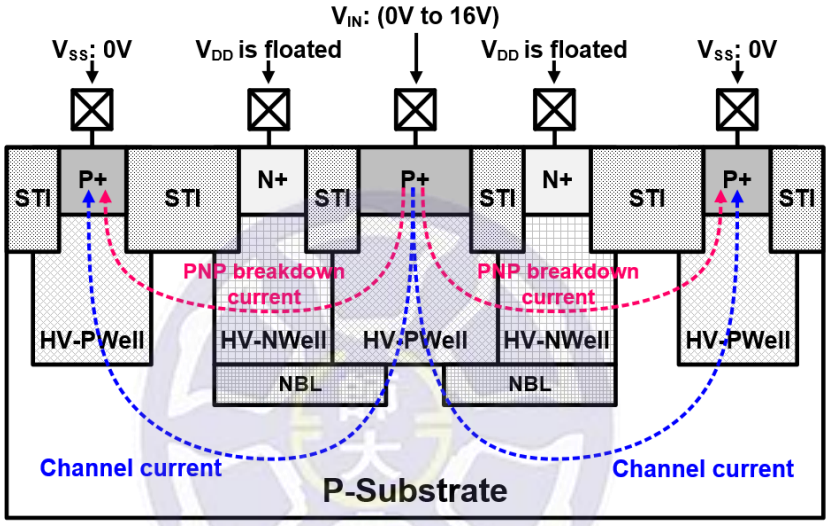


Fig. 4.14. The DC-bias setting of P-type depletion diodes with floating V_{DD}.

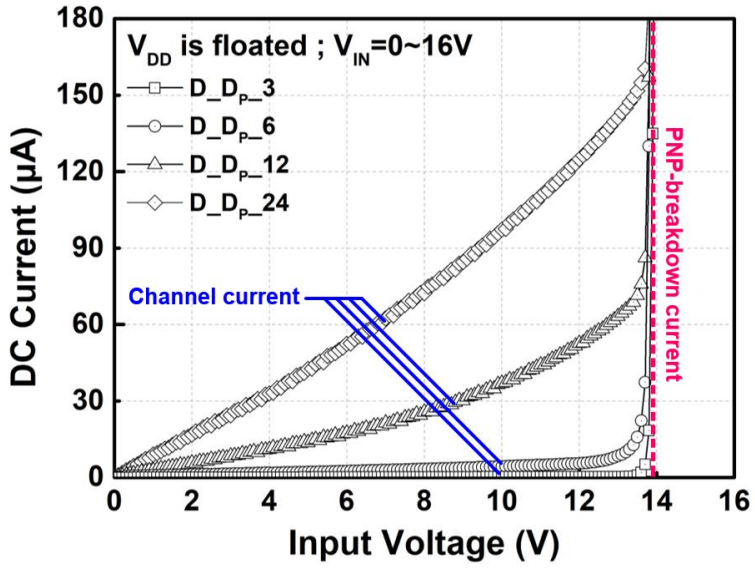
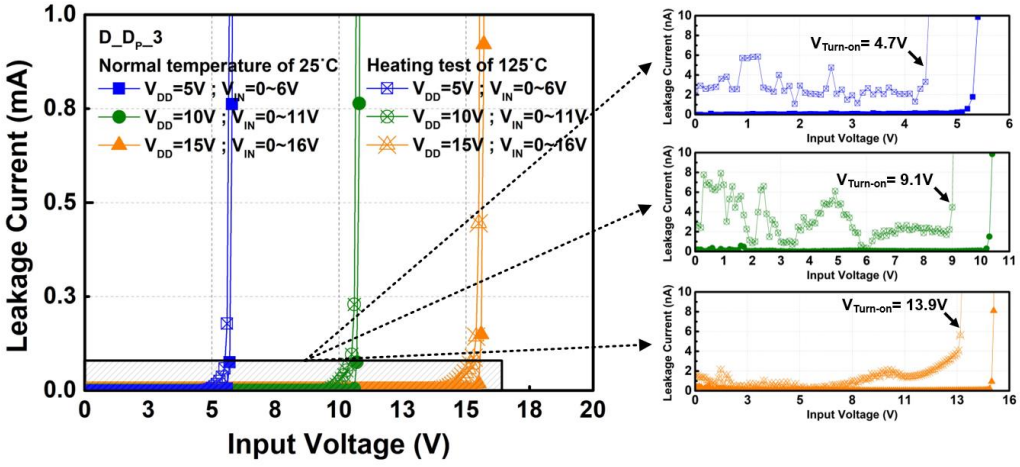


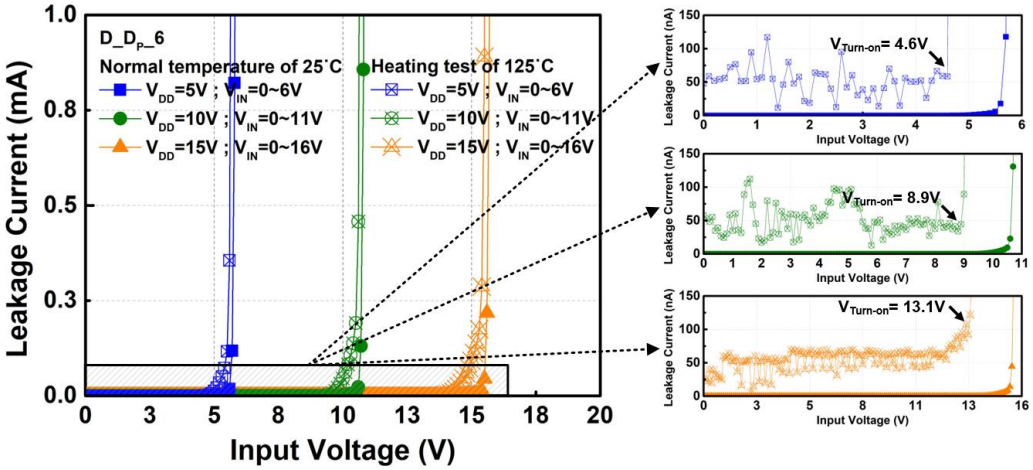
Fig. 4.15. The DC-measurement results of P-type depletion diodes with floating V_{DD}.

4.3.2 Heating Test

In order to observe whether the depletion diodes have a sufficiently low leakage current in a high temperature environment, the heating test is performed and the leakage current at the high temperature is recorded. The measurement method is to place the wafer on an aluminum plate and heat the aluminum plat from the normal temperature of 25°C to 125°C. The leakage currents of depletion diodes at 25°C and 125°C are recorded independently. Since the leakage currents of D_DP_12 and D_DP_24 are too large at normal temperature, these are not included in the heating test. Fig. 4.16 (a) and (b) show the DC-measurement results of D_DP_3 and D_DP_6 at the normal temperature of 25°C and the high temperature of 125°C. It can be observed that the leakage currents of D_DP_3 and D_DP_6 have a significant increase at high temperature. The DC comparison results of D_DP_3 and D_DP_6 at 25°C and 125°C are arranged in Table 4.3. The $I_{Leakage}$ of D_DP_3 and D_DP_6 at 125°C increased by about 1000 times and the $V_{Turn\text{-}on}$ has a tendency to shrink. For the D_DP_3. From the heating test results, D_DP_3 and D_DP_6 still have a sufficiently low leakage current under the normal operation. However, it must be noted that the $V_{Turn\text{-}on}$ becomes small.



(a)



(b)

Fig. 4.16. The DC-measurement results of P-type depletion diodes (D_DP) with the diode width of 20μm and the channel length of (a) 3μm (D_DP_3) and (b) 6μm (D_DP_6) at the normal temperature of 25°C and the high temperature of 125°C.

Table 4.3

The DC-measurement results of D_DP_3 and D_DP_6) at the normal temperature of 25°C and the high temperature of 125°C

Device	V_{DD}	Normal temperature of 25°C		High temperature of 125°C	
		$V_{Turn-on}$	$I_{Leakage}$ (V_{IN}=V_{DD})	$V_{Turn-on}$	$I_{Leakage}$ (V_{IN}=V_{DD})
D_DP_3	5V	5.2V	21pA	4.7V	87nA
	10V	10.1V	92pA	9.1V	96nA
	15V	14.9V	150pA	13.9V	98nA
D_DP_6	5V	4.8V	0.64μA	4.6V	128μA
	10V	9.5V	2.28μA	8.9V	456μA
	15V	14.1V	4.58μA	13.1V	916μA

4.3.3 TLP Measurement

In order to investigate the test device behavior during high ESD current stress, transmission line pulsing (TLP) generator with a pulse width of 100ns and a rise time of 10ns is used to measure the trigger voltage (V_{t1}), turn-on resistance (R_{on}), and second breakdown current (I_{t2}) of the test device. The V_{t1} is defined as a TLP voltage in which TLP current is increased over 10^3 times. The I_{t2} is defined as the TLP current with the leakage current shifting over 30%.

Fig. 4.17 shows the measured TLP I-V curve of traditional P-type diode with the diode width of 20μm (T_D_P) during the stress from input to V_{DD} (PD-mode). The trigger voltage (V_{t1}) and turn-on resistance (R_{on}) of T_D_P are 0.82V and 3.65Ω. The second breakdown current (I_{t2}) of T_D_P is 9.74A. However, a traditional P-type diode can only provide this single ESD path (PD-mode) at the I/O pad.

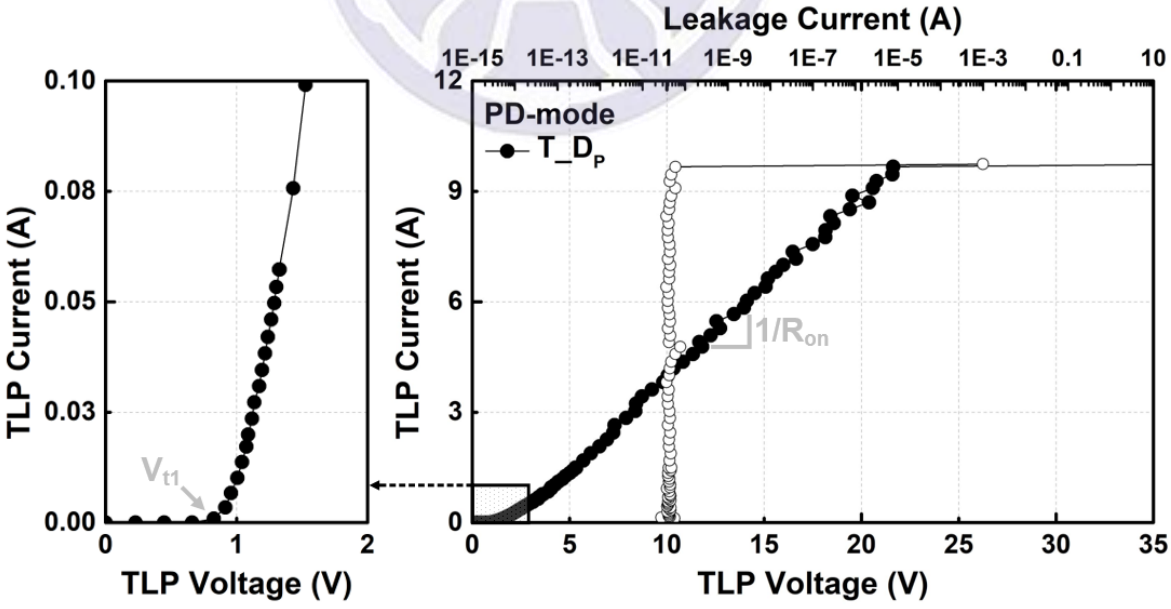


Fig. 4.17. Measured TLP I-V curve of traditional P-type diode with the diode width of 20μm (T_D_P) during the stress from input to V_{DD} (PD-mode).

Fig. 4.18 shows the measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 3μm (D_D_P_3) during the stress from input to V_{DD} (PD-mode). The trigger voltage (V_{t1}) and turn-on resistance (R_{on}) of D_D_P_3 are 0.89V and 3.63Ω. The second breakdown current (I_{t2}) of the D_D_P_3 is 9.45A.

Fig. 4.19 shows the measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 6μm (D_D_P_6) during the stress from input to V_{DD} (PD-mode). The trigger voltage (V_{t1}) and turn-on resistance (R_{on}) of D_D_P_6 are 0.89V and 3.77Ω. The second breakdown current (I_{t2}) of the D_D_P_6 is 9.81A.

Fig. 4.20 shows the measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 12μm (D_D_P_12) during the stress from input to V_{DD} (PD-mode). The trigger voltage (V_{t1}) and turn-on resistance (R_{on}) of D_D_P_12 are 0.89V and 3.77Ω. The second breakdown current (I_{t2}) of the D_D_P_12 is 9.81A.

Fig. 4.21 shows the measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 24μm (D_D_P_24) during the stress from input to V_{DD} (PD-mode). The trigger voltage (V_{t1}) and turn-on resistance (R_{on}) of D_D_P_24 are 0.81V and 2.22Ω. The second breakdown current (I_{t2}) of the D_D_P_24 is 9.92A. The TLP-measurement results of the traditional P-type diode (T_D_P) and the depletion diodes (D_D_P) with the channel length of 3μm (D_D_P_3), 6μm (D_D_P_6), 12μm (D_D_P_12), and 24μm (D_D_P_24) in PD-mode are organized in Table 4.4.

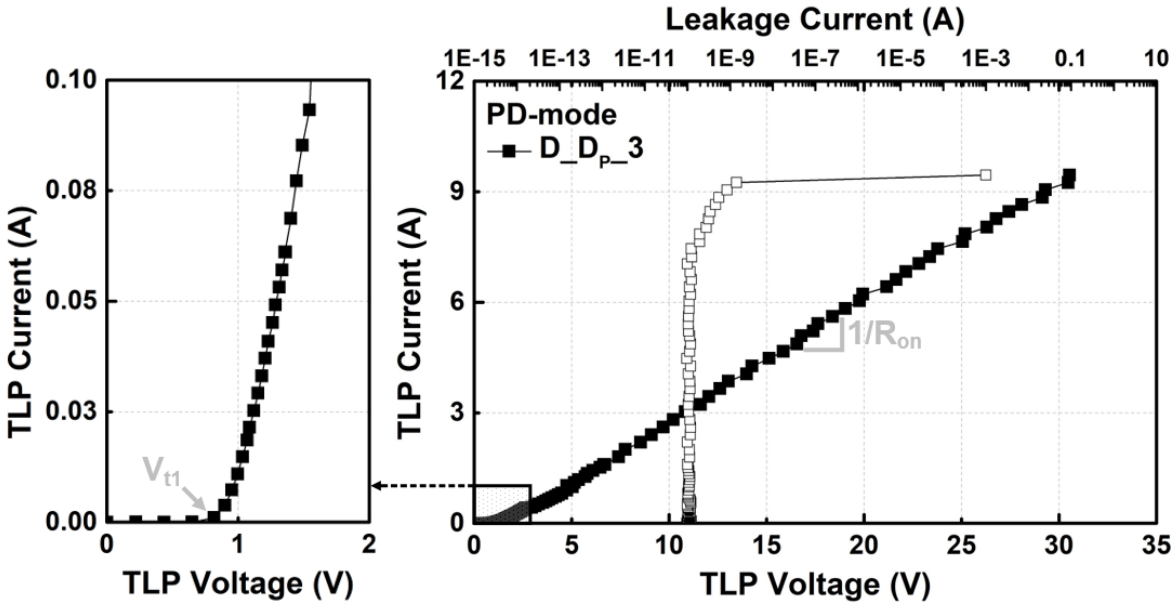


Fig. 4.18. Measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 3μm (D_D_P_3) during the stress from input to V_{DD} (PD-mode).

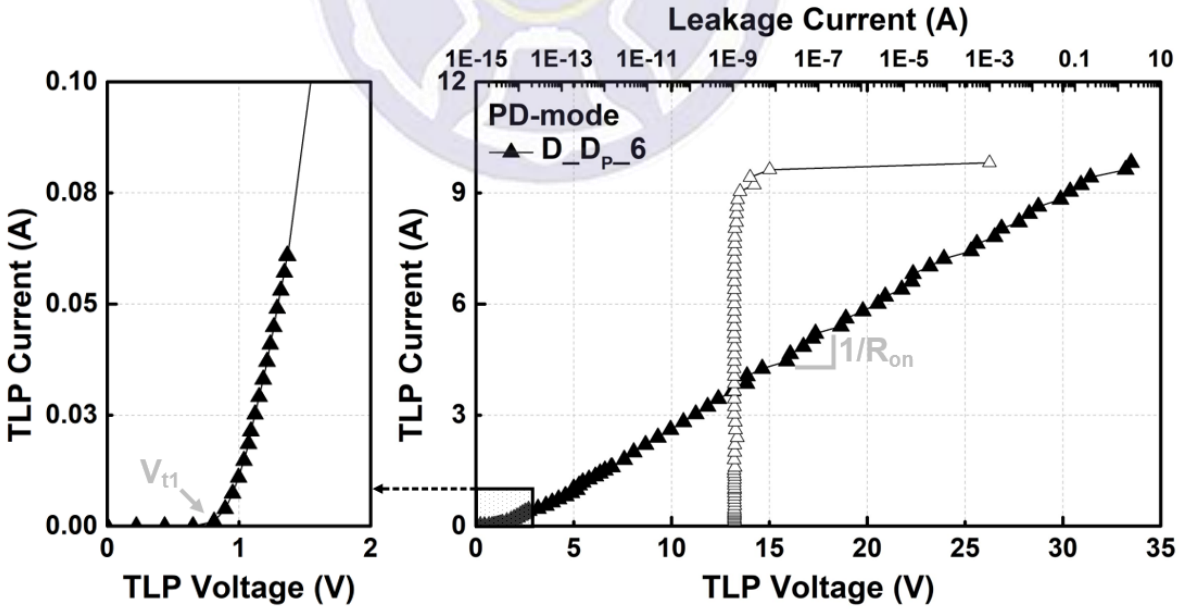


Fig. 4.19. Measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 6μm (D_D_P_6) during the stress from input to V_{DD} (PD-mode).

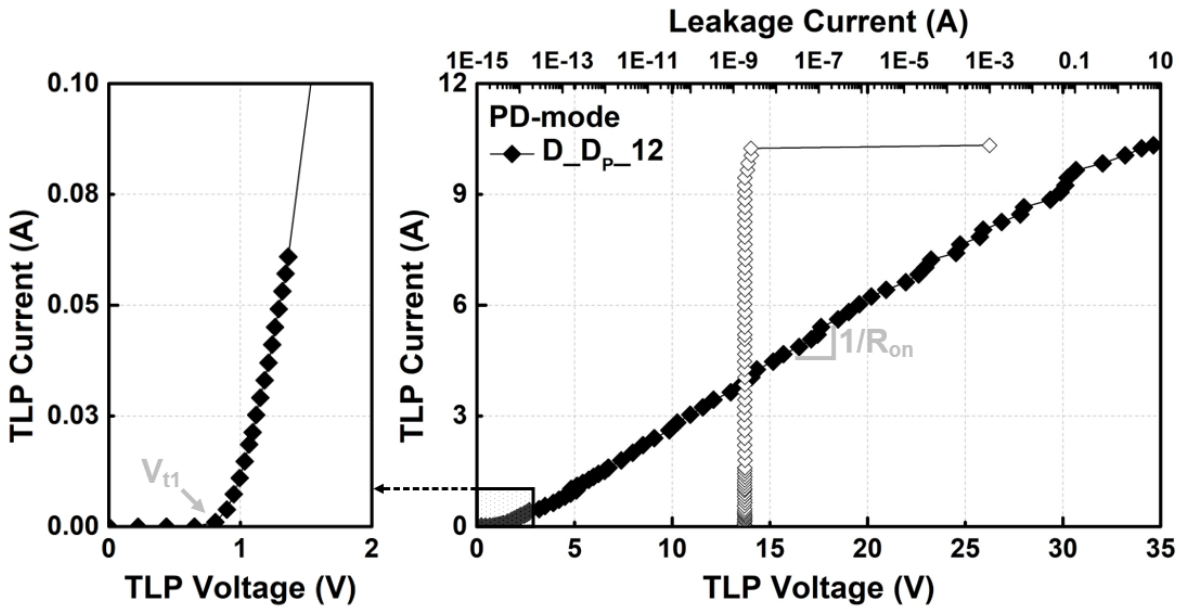


Fig. 4.20. Measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 12μm (D_D_P_12) during the stress from input to V_{DD} (PD-mode).

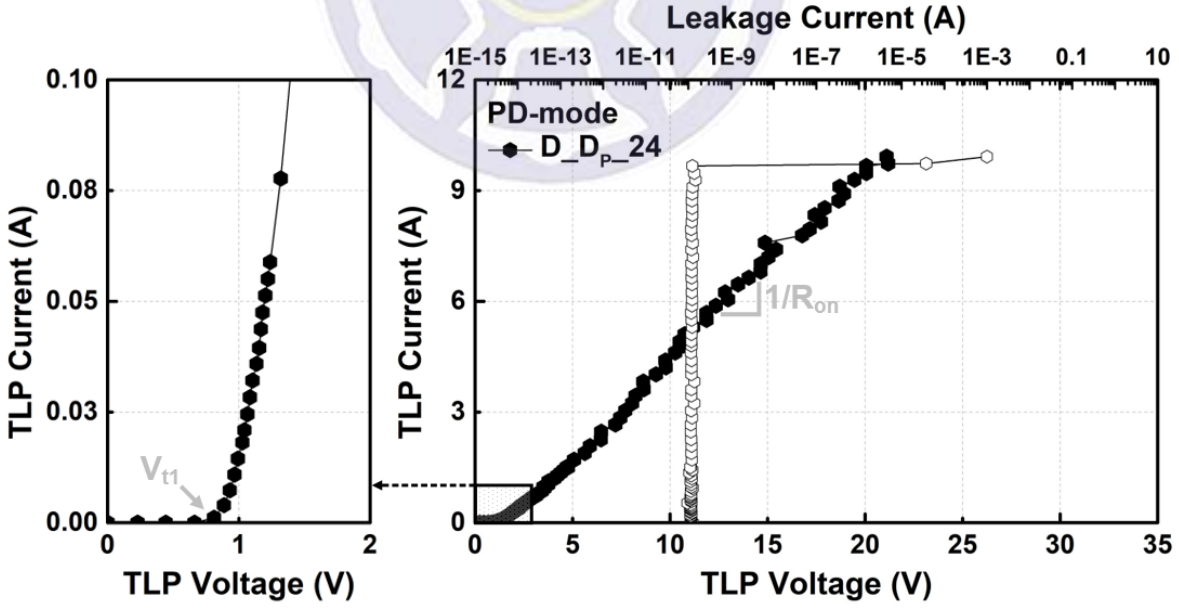


Fig. 4.21. Measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 24μm (D_D_P_24) during the stress from input to V_{DD} (PD-mode).

Table 4.4

The TLP-measurement results of all P-type depletion diodes during the stress from input to V_{DD} (PD-mode).

Device	V_{t1} (PD-mode) (V)	R_{on} (PD-mode) (Ω)	I_{t2} (PD-mode) (A)
T_D_P	0.82	3.65	9.74
D_D_P_3	0.89	3.63	9.45
D_D_P_6	0.89	3.77	9.81
D_D_P_12	0.89	3.65	10.32
D_D_P_24	0.81	2.22	9.92

Fig. 4.22 shows the measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 3μm (D_D_P_3) during the stress from input to V_{SS} (PS-mode). The trigger voltage (V_{t1}) and turn-on resistance (R_{on}) of the D_D_P_3 are 13.82V and 53.81Ω. The second breakdown current (I_{t2}) of the D_D_P_3 is 1.70A.

Fig. 4.23 shows the measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 6μm (D_D_P_6) during the stress from input to V_{SS} (PS-mode). The trigger voltage (V_{t1}) and turn-on resistance (R_{on}) of the D_D_P_6 are 13.82V and 56.35Ω. The second breakdown current (I_{t2}) of the D_D_P_6 is 1.54A.

Fig. 4.24 shows the measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 12μm (D_D_P_12) during the stress from input to V_{SS} (PS-mode). The trigger voltage (V_{t1}) and turn-on resistance (R_{on}) of D_D_P_12 are 13.82V and 59.45Ω. The second breakdown current (I_{t2}) of the D_D_P_12 is 1.47A.

Fig. 4.25 shows the measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 24μm (D_D_P_24) during the stress from input to V_{SS} (PS-mode). The trigger voltage (V_{t1}) and turn-on resistance (R_{on}) of D_D_P_24 are 13.90V and 57.35Ω. The second breakdown current (I_{t2}) of the D_D_P_24 is 1.51A. The TLP-measurement results of the depletion diodes (D_D_P) with the channel length of 3μm (D_D_P_3), 6μm (D_D_P_6), 12μm (D_D_P_12), and 24μm (D_D_P_24) in PS-mode are organized in Table 4.5. It can be observed that the TLP I-V curves of all test devices in PS-mode are different from the expected results. The discussion about PS-mode will be mentioned in the Section 4.6.

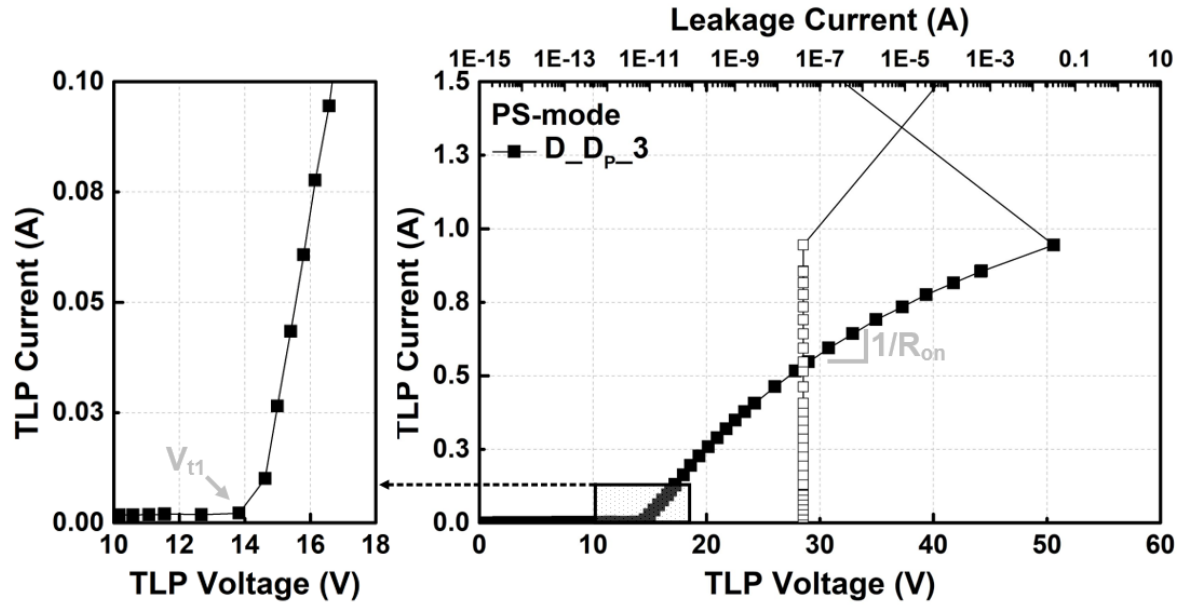


Fig. 4.22. Measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 3μm (D_D_P_3) during the stress from input to V_{SS} (PS-mode).

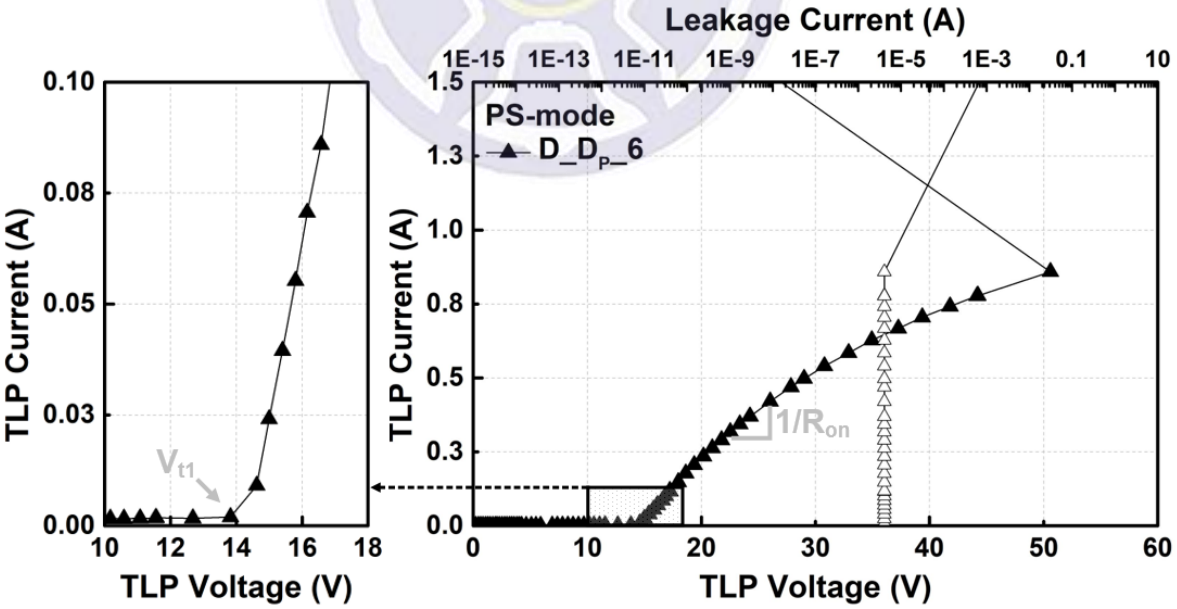


Fig. 4.23. Measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 6μm (D_D_P_6) during the stress from input to V_{SS} (PS-mode).

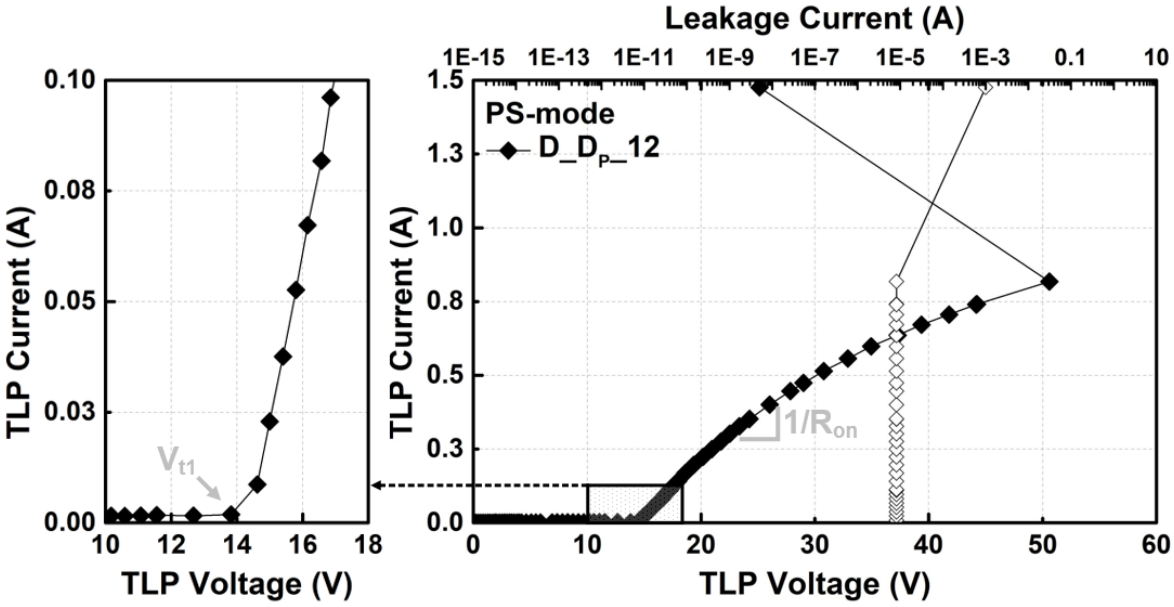


Fig. 4.24. Measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 12μm (D_D_P_12) during the stress from input to V_{SS} (PS-mode).

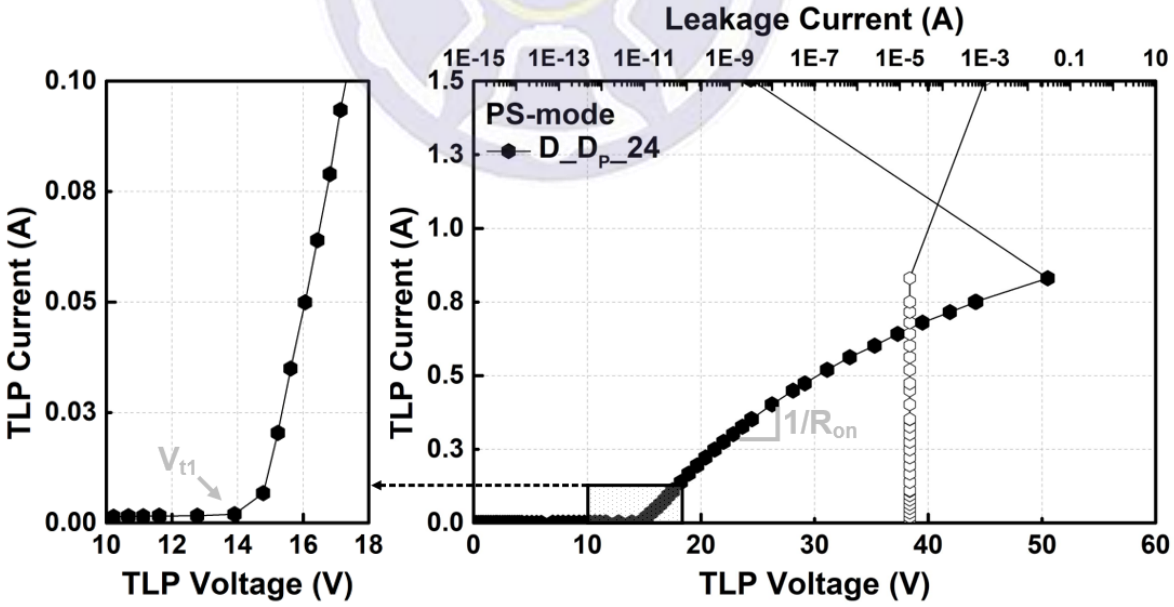


Fig. 4.25. Measured TLP I-V curve of P-type depletion diodes (D_D_P) with the diode width of 20μm and the channel length of 24μm (D_D_P_24) during the stress from input to V_{SS} (PS-mode).

Table 4.5

The TLP measurement results of all P-type depletion diodes during the stress from input to V_{SS} (PS-mode).

Device	$V_{t1\ (PS\text{-}mode)}$ (V)	$R_{on\ (PS\text{-}mode)}$ (Ω)	$I_{t2\ (PS\text{-}mode)}$ (A)
D_D_P_3	13.82	53.81	1.70
D_D_P_6	13.82	56.35	1.54
D_D_P_12	13.82	59.45	1.47
D_D_P_24	13.90	57.35	1.51

4.3.4 ESD Robustness

In order to measure the ESD robustness of each test device, the die must be packaged and wired, as shown in Fig. 4.26. This thesis uses the compact ESD simulator (HCE-5000) to perform the HBM ESD robustness of P-type depletion diodes (D_D_P). The measurement of HBM is set to apply stress from 1kV to 8kV (one step per 0.5kV). In each step, three stresses are applied to the device within 0.3 seconds. The failure criterion is defined as the voltage shifting more than 30% at 1μA of the I-V characteristics after HBM ESD stressed. The value of HBM robustness from input to V_{DD} and input to V_{SS} are $HBM_{(PD\text{-}mode)}$ and $HBM_{(PS\text{-}mode)}$, respectively. The $HBM_{(PD\text{-}mode)}$ and $HBM_{(PS\text{-}mode)}$ ESD robustness of all test devices are greater than 8kV, as show in Table 4.6.

In order to further compare the ESD robustness of each test device, the HMM ESD test has been completed. This thesis uses the ESD simulator (ESS-B3011) to perform HMM ESD robustness test of all test devices. The HMM ESD test is measured from 1kV (one step per 0.5kV). In each step, one stress is applied to the device within 0.05 seconds. The definition of HMM's failure criterion is the same as HBM. The value of HMM robustness from input to V_{DD} and input to V_{SS} are $HMM_{(PD\text{-}mode)}$ and $HMM_{(PS\text{-}mode)}$, respectively. The measurement results of HMM ESD test are shown in Table 4.5. Since there is a structure of diode in the path of PD-mode, the larger size of device has better HMM level. However, there is a P-type channel in the path of PS-mode. The large size of device will not have a better HMM level in PS-mode. It can be observed that the distance of NBL has no significant effect on ESD robustness.

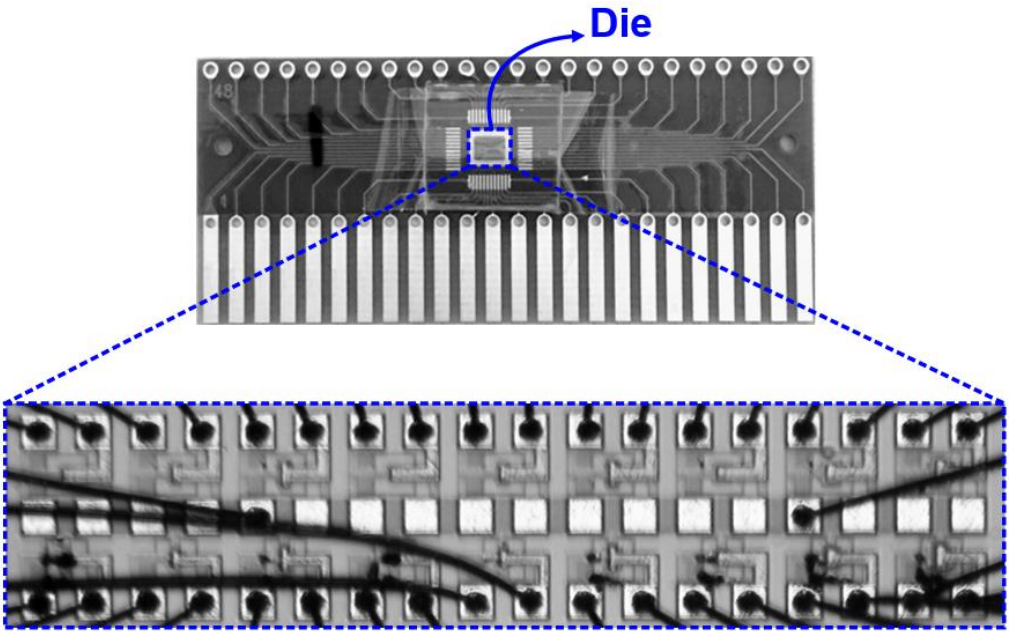


Fig. 4.26. Picture of the packaged die.

Table 4.6

The ESD robustness of P-type depletion diodes during the stress from input to V_{DD} (PD-mode) and input to V_{SS} (PS-mode).

Device	HBM (PD-mode) (kV)	HBM (PS-mode) (kV)	HMM (PD-mode) (kV)	HMM (PS-mode) (kV)
T_D_P	>8	N/A	7	N/A
D_D_P_3	>8	>8	7	2.5
D_D_P_6	>8	>8	7	2.5
D_D_P_12	>8	>8	7	2.5
D_D_P_24	>8	>8	7	2

4.4.4 Failure Analysis

In order to investigate the failure situation of ESD protection device, the chip micrographs of P-type depletion diodes (D_D_P) after the HMM $_{(PD\text{-}mode)}$ test have been taken as shown in Fig. 4.27. It can be observed that the metal connected to the V_{DD} pad will be destroyed first before the ESD protection device burns out. In order to solve this problem, some improvement methods will be mentioned in Section 4.7.

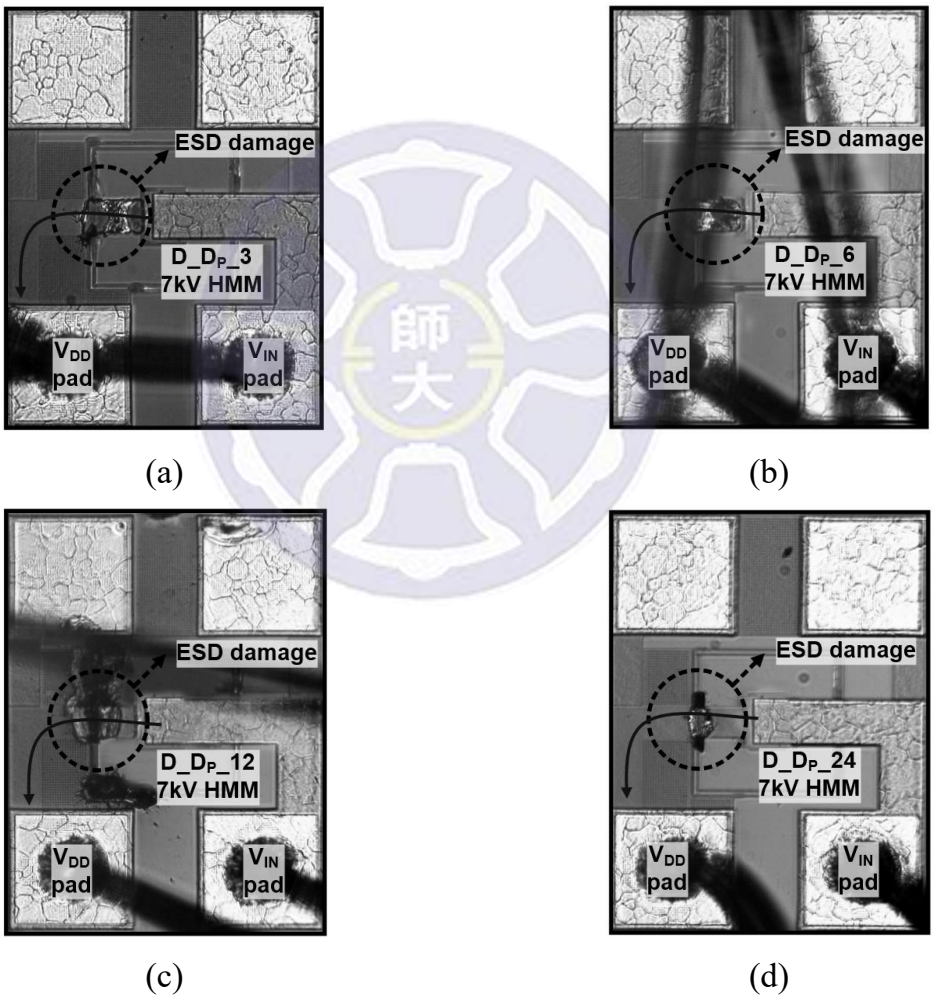
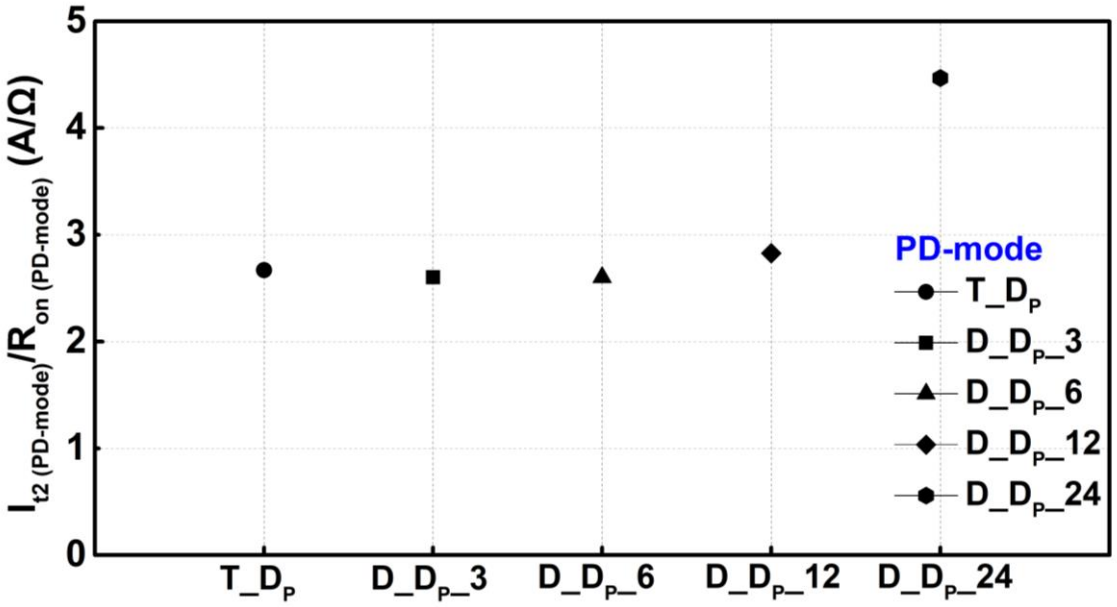


Fig. 4.27. The chip micrographs of the P-type depletion diodes with the channel length of (a) 3μm (D_D_P_3), 6μm (D_D_P_6), 12μm (D_D_P_12), 24μm (D_D_P_24) after the 7kV HMM $_{(PD\text{-}mode)}$ test.

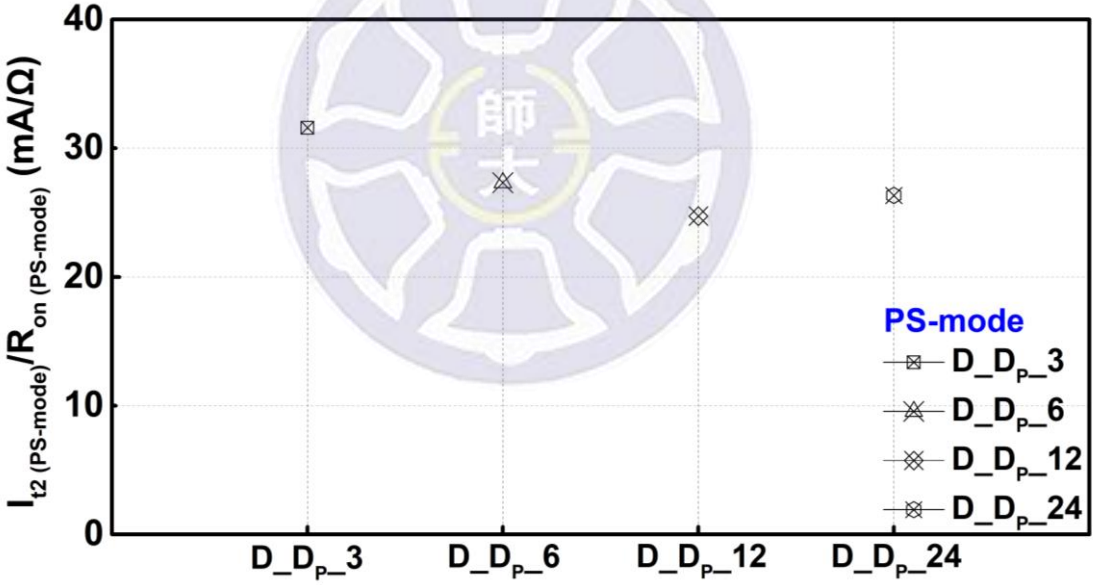
4.4 Comparison of Traditional and Proposed Structures

For the proposed structure, the leakage current of P-type depletion diodes (D_D_P) should be low enough under the normal operation ($V_{SS}<V_{IN}<V_{DD}$). The $I_{Leakage}$ is defined as the leakage current of D_D_P when V_{IN} is equal to V_{DD}. The V_{IN} with a 50% increase in leakage current is defined as the $V_{Turn\text{-}on}$. The leakage current of D_D_P will rise sharply when the V_{IN} exceeds $V_{Turn\text{-}on}$. Therefore, the value of $V_{Turn\text{-}on}$ should be as high as possible. In order to compare the DC characteristics of the P-type depletion diodes with the different channel length of 3μm, 6μm, 12μm, and 24μm, define the figures of merit (FOM) as $V_{Turn\text{-}on}/I_{Leakage}$. Regardless of the V_{DD}, the D_D_P with the channel length of 3μm (D_D_P_3) has the highest FOM because of the low enough leakage current. It can be observed that the value of FOM drops significantly as the channel length increases.

For the TLP measurement, the I_{t2} is the maximum TLP current that the ESD protection device can withstand. The value of I_{t2} should be as large as possible. R_{on} is the equivalent resistance when the ESD protection device is discharged. The value of R_{on} should be as small as possible. The FOM is defined as I_{t2}/R_{on} and the comparison results of all test devices in PD-mode and PS-mode are shown in Figs. 4.28 (a) and (b), respectively. It can be observed that the D_D_P_24 has better performance in PD-mode because wider channel length can provide better discharge capacity. However, the performance of each device in PS-mode is not much different because the discharge path is P-Substrate. All the comparison results are organized in the Table 4.7.



(a)



(b)

Fig. 4.28. The comparison results of the P-type depletion diodes (D_DP) with the channel length of 3μm (D_DP_3), 6μm (D_DP_6), 12μm (D_DP_12), and 24μm (D_DP_24) under the TLP measurement of (a) PD-mode and (b) PS-mode.

Table 4.7

The comparison results of traditional and proposed structure under the DC measurement and the TLP measurement.

Device	$V_{Turn-on}/I_{Leakage}$ (V/pA)			$I_{t2\ (PD-mode)}/R_{on\ (PD-mode)}$ (A/Ω)	$I_{t2\ (PS-mode)}/R_{on\ (PS-mode)}$ (mA/Ω)
	V_{DD}=5V	V_{DD}=10V	V_{DD}=15V		
T_D_P_20	N/A	N/A	N/A	2.66	N/A
D_D_P_3_20	0.25	0.11	0.10	2.60	31.59
D_D_P_6_20	7.5E-6	4.16E-6	3.07E-6	2.60	27.32
D_D_P_12_20	3.74E-8	9.27E-8	1.58E-7	2.82	24.72
D_D_P_24_20	3.32E-9	4.95E-9	7.16E-9	4.46	26.32

4.5 Comparison of Literature

Some ESD protection devices have a phenomenon of snapback such as silicon controlled rectifier (SCR) and NPN bipolar junction transistor (BJT), etc. However, the snapback effect of ESD protection devices may cause a problem of latch-up [35]. Therefore, the Reference [36] proposed a non-snapback structure of PNP transistor for the ESD protection of high-voltage I/O. Fig. 4.29 shows the cross-sectional view of lateral PNP transistor coupled to a vertical diode. Reference [36] investigates the characteristics of proposed device by modulating the collector width (L_C) and the lateral distance (D). Increasing collector width can effectively improve the problem of large R_{on} of the vertical diode and then improve the I_{t2}. The modulation of lateral distance does not affect the ESD robustness but will dominate the breakdown voltage of PNP transistor. The layout area of ESD protection device is defined as A. In order to compare the capability of ESD protection per unit layout area, the FOMs are defined as I_{t2}/A and HBM/A. The comparison results of all test devices are organized in Table 4.8. The proposed devices in this thesis have better FOMs than the devices in Reference [36].

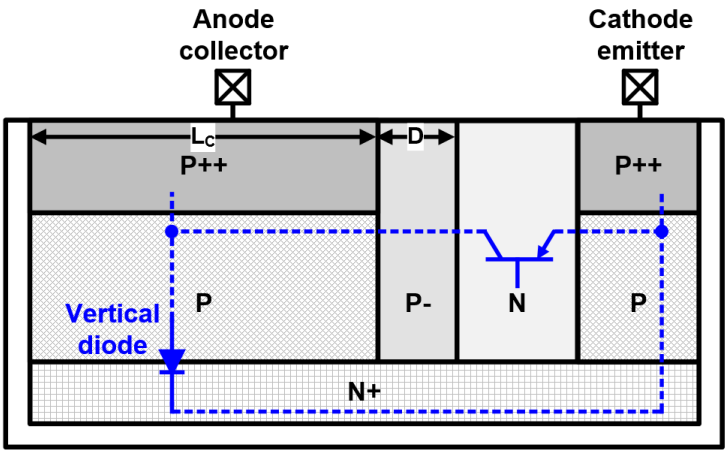


Fig. 4.29. In the Reference [36], the cross-sectional view of lateral PNP transistor coupled to a vertical diode.

Table 4.8

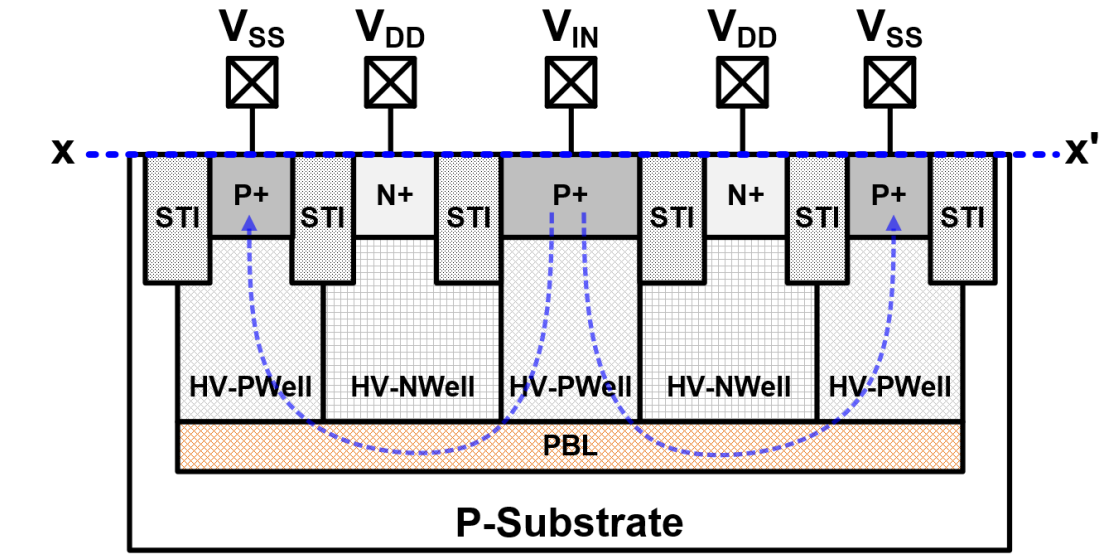
The comparison of proposed and previous designs.

Device			A (μm^2)	I_{t2} (A)	HBM (kV)	I_{t2}/S ($mA/\mu m^2$)	HBM/A ($V/\mu m^2$)
This thesis	T_D_P		1131	9.74	>8	8.61	7.07
	D_D_P_3		1872	9.45	>8	5.04	4.27
	D_D_P_6		1872	9.81	>8	4.24	4.27
	D_D_P_12		1872	10.32	>8	5.51	4.27
	D_D_P_24		3920	9.92	>8	2.53	2.04
Reference [36]	DUT_1		10000	4.2	9.5	0.42	0.95
	DUT_2		10752	4.5	>10	0.41	0.93
	DUT_3		13157	4.6	>10	0.34	0.76
	DUT_4 D=1.57μm	L_C= 7.87μm	N/A	2.5	N/A	N/A	N/A
		L_C= 14.8μm	N/A	3.4	N/A	N/A	N/A
		L_C= 21.73μm	N/A	3.9	N/A	N/A	N/A
	DUT_5 L_C=18.3μm	D= 7.03μm	11764	5.7	8	0.48	0.68
		D= 8.50μm	12280	5.7	7	0.46	0.57
		D= 9.97μm	12837	5.7	9.5	0.44	0.74

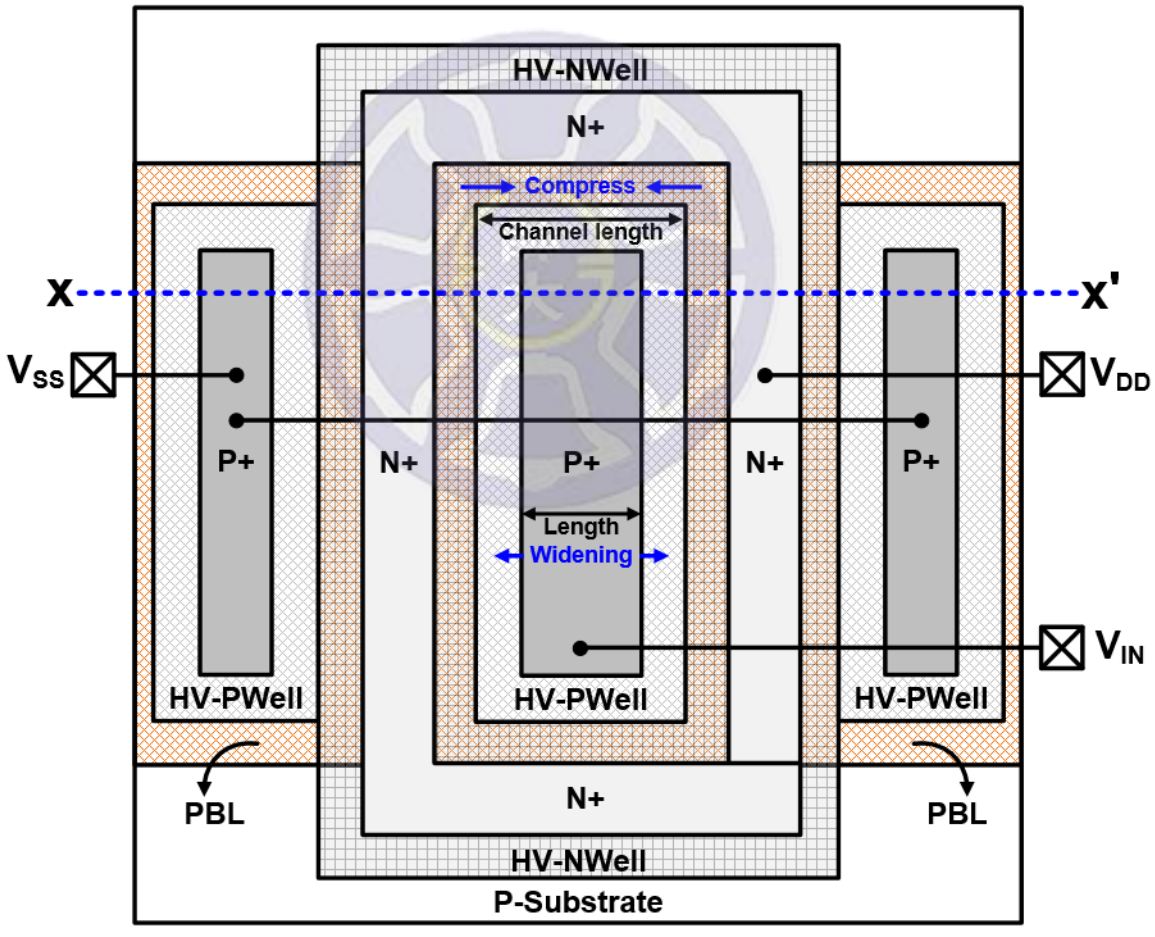
4.6 Discussion of This Chapter

From the TLP-measurement results, the depletion diodes have sufficiently high ESD robustness in PD-mode. However, the discharge phenomenon in PS-mode is not as expected. The current does not discharge from V_{IN} to V_{SS} through P-substrate. However, the current is discharged through the parasitic PNP transistor until the TLP voltage increases beyond the breakdown voltage ~14V. The reason for this problem is that the special layout design of NBL conflicts with the process specification. In order to avoid the current path of P-substrate being blocked by the layer of NBL, the improved structure of P-type depletion diodes are proposed.

As shown in Fig. 4.30 (a), the original layer of NBL is replaced with PBL and the PBL is connected to the V_{IN} and V_{SS}. The channel length is redefined as the distance between HV-NWell. The structure of P-type depletion diodes with PBL can effectively improve the discharge situation of PS-mode. From the TLP-measurement result of D_D_P_24 can be confirmed that the size of length significantly affects the discharge capacity. The length of D_D_P_24 is two times larger than D_D_P_3, D_D_P_6, and D_D_P_12, resulting in a lower turn-on resistance. Based on this result, the length of D_D_P should be wide enough and the distance of HV-NWell should be small enough to achieve better discharge capability and low leakage current, as shown in Fig. 4.28 (b). From the failure analysis, it can be known that the metal layer will be melted first after the HMM ESD test. Therefore, the width of metal needs to be widened to withstand the high-energy ESD test.



(a)



(b)

Fig. 4.30. (a) The cross-sectional view and (b) the layout top view of P-type depletion diodes with PBL.

4.7 Summary of This Chapter

The traditional P-type diode (T_D_P) and the proposed P-type depletion diodes (D_D_P) have been implemented in the 0.50μm CMOS process for high-voltage applications. In general, a diode can only provide a current path in single direction. This means that multiple diodes are needed to implement a complete ESD protection circuit. Therefore, this thesis has designed a new structure of diode which can provide two current paths. The working principle is to control the current channel through the depletion region of the PN-junction. The important thing is that the channel must be kept off during the normal operation to make the leakage current low enough. From the DC-measurement results, it can be confirmed that the leakage current can be low enough when the channel length of depletion diodes is 3μm. In addition, the proposed depletion diodes have sufficiently high ESD robustness in PD-mode that can be confirmed from the TLP, HBM, and HMM measurement. However, the structure of depletion diodes needs to be further improved to solve the problem of PS-mode.

Chapter 5

Conclusions and Future Works

5.1 Conclusions

The I/O pad of integrated circuit must incorporate ESD protection device to increase tolerance and improve the product yield. The diode is a widely used ESD protection device with the advantages of simple structure and great capability of discharge. However, the diode still has some problems that need to be improved.

For the high-frequency applications, the parasitic capacitance of diode will cause signal loss and severely affect circuit performance. In the previous literatures, a common improvement is to reduce the parasitic capacitance of ESD protection diode as much as possible. However, the parasitic capacitance of diode can only be reduced by a limited amount. Base on this, this thesis has proposed a low-loss I/O pad with the dual-diode ESD protection in the Chapter 3. The principle is to eliminate the signal loss through the resonance phenomenon of stacked inductor and parasitic capacitance. All test structures are implemented in 0.18μm CMOS process. The measurement results of high-frequency confirmed that the signal losses of proposed structures are more than 6 times smaller than that of the traditional structure in K/Ka-bands. It is confirmed from TLP measurement that the proposed structures have sufficiently high ESD robustness. However, the R_{on} of proposed structures are slightly larger than the traditional structure due to the stacked inductor. Even so, the proposed structures have the higher values of FOM than traditional structure because of a significant reduction in signal loss.

For the high-voltage applications, the structure of ESD protection device is complex in order to withstand high operating voltage. The structure of traditional P-type diode (T_D_P) is simple but the disadvantage is that there is only a single current path. Base on this, this thesis has proposed a bidirectional P-type depletion diodes (D_D_P) and implemented it in high-voltage process. The D_D_P has two current paths that contain V_{IN} to V_{DD} (PD-mode) and V_{IN} to V_{SS} (PS-mode). An equivalent diode is between V_{IN} and V_{DD}, a channel controlled by depletion region is between V_{IN} and V_{SS}. The traditional P-type diode and the P-type depletion diodes have been implemented in 0.50μm CMOS process. The measurement results confirm that the P-type depletion diodes have low leakage current under the normal operation and high ESD robustness in PD-mode. Although the discharge phenomenon of proposed device in PS-mode is not as expected, it is still operational. The solution to this problem has been proposed in discussion and it will be planned for future work.

5.2 Future Works

This thesis has presented some different ideas for the future work of low-loss I/O pad. Figs. 5.1 (a), (b), and (c) show the ESD protection schemes of C-LC, C-L-C, and C-L-C-L circuits with the stacked inductor and the two-stages dual diodes. Compared with the original design, an additional stage of dual diodes (stage-1) is added between the top metal plate and the stacked inductor. The purpose of the additional stage-1 is to share the ESD stress of the stacked inductor and stage-2. The sum of the diode width (W) of stage-1 and stage-2 is 120μm. According to different circuits, the ratio of the diode width of stage-1 and stage-2 is different. Figs. 5.2 (a), (b), and (c) show the structures of low-loss I/O pads with the C-LC, C-L-C, and C-L-C-L circuits.

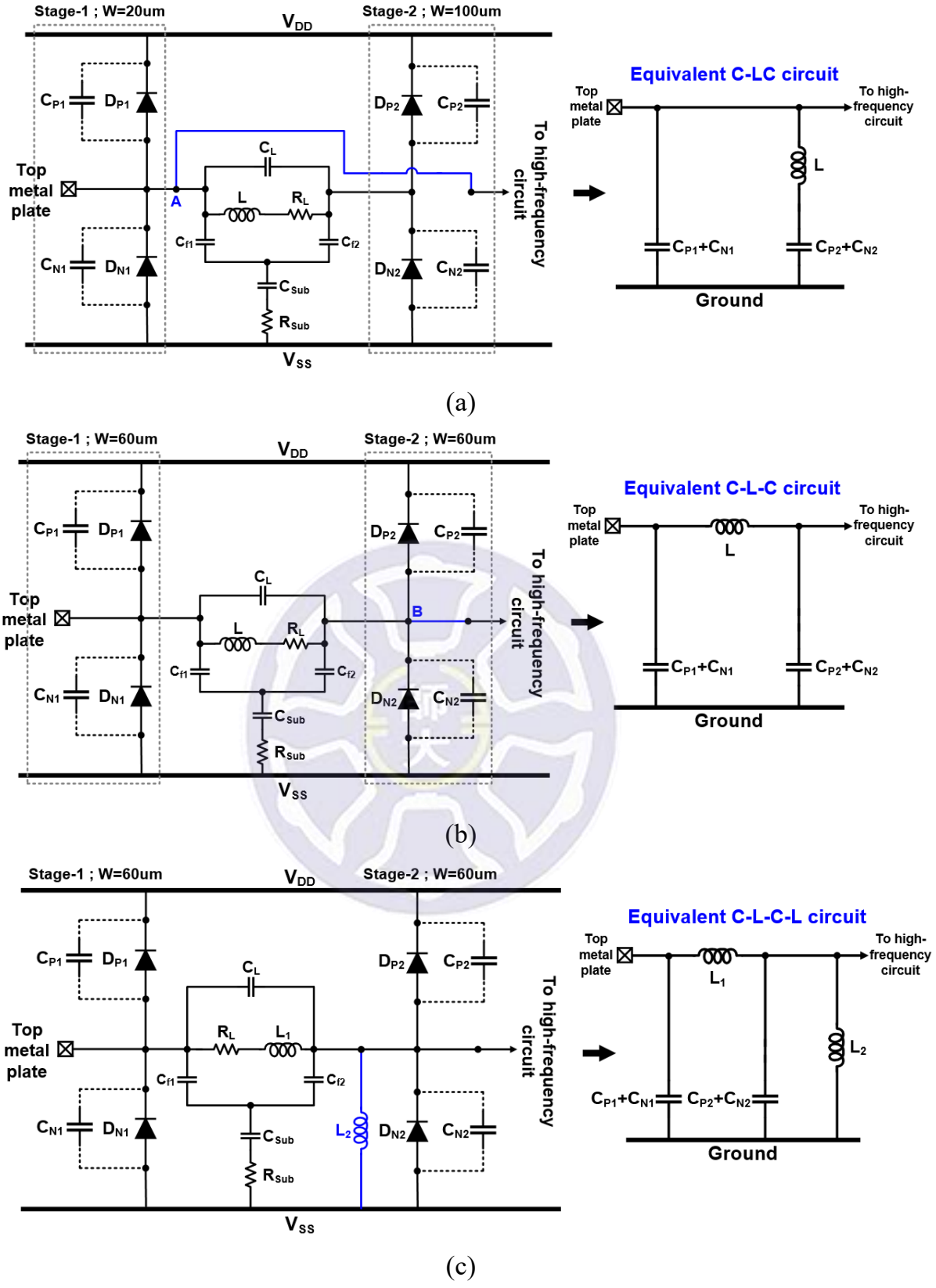
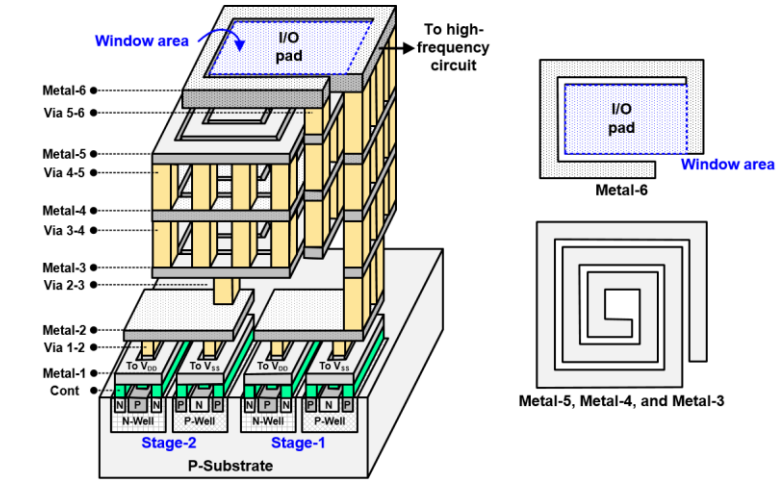
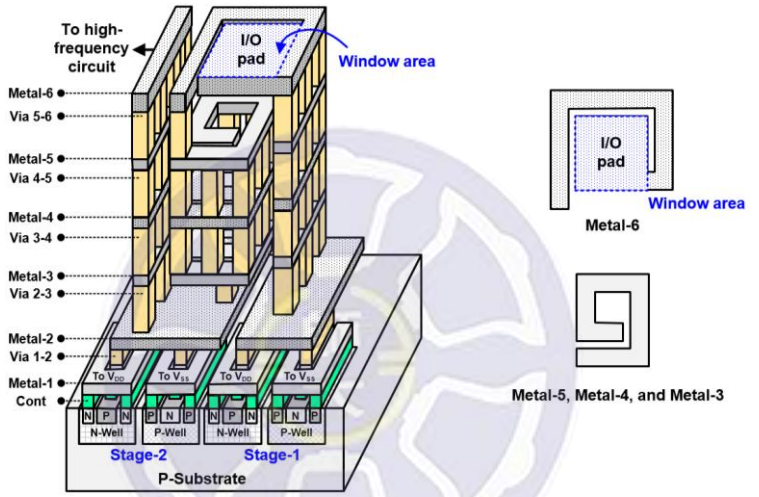


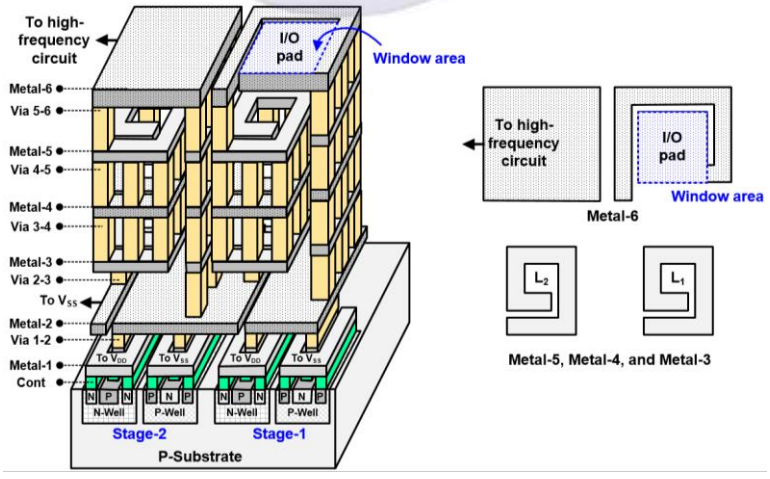
Fig. 5.1. The ESD protection schemes of (a) C-LC, (b) C-L-C, and (c) C-L-C-L circuits with the stacked inductor and the two-stages dual diodes.



(a)



(b)



(c)

Fig. 5.2. The structures of low-loss I/O pads with the (a) C-LC, (b) C-L-C, and (c) C-L-C-L circuits for high-frequency circuit.

Fig. 5.3 shows the simulated signal losses of traditional, C-LC, C-L-C, and C-L-C-L structures. It can be observed from the preliminary simulation results that the signal loss of the C-LC structure gradually increases after 25GHz. The signal loss of the C-LC structure is dominated by the parasitic capacitance of stage-1. Therefore, the diode width of stage-1 cannot be too large for C-LC structure. The inductance required for the C-LC structure is about 1nH. For the C-L-C structure, it only has the lowest signal loss at the high resonance frequency, $F_{H\ (resonance)}$. However, the advantage of C-L-C structure is that it only requires only a very low inductance value of 0.1nH. This means that the layout area of C-L-C structure can be greatly reduced. Based on this advantage, an additional small inductor (L_2) can be added to form the C-L-C-L structure. The values of L_1 and L_2 are 0.1nH and 0.15nH. There are two resonance frequencies in the C-L-C-L structure for $F_{L\ (resonance)}$ and $F_{H\ (resonance)}$. However, the challenge of C-L-C-L structure is the drift of resonance frequency. The inductance value must be designed very accurately. Finally, these different circuit designs will be incorporated into future work.

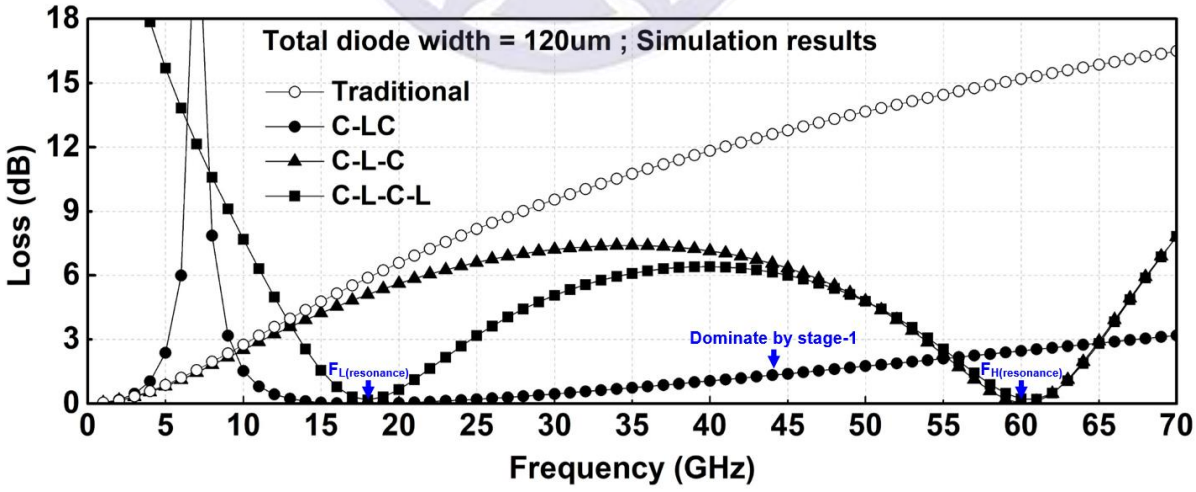
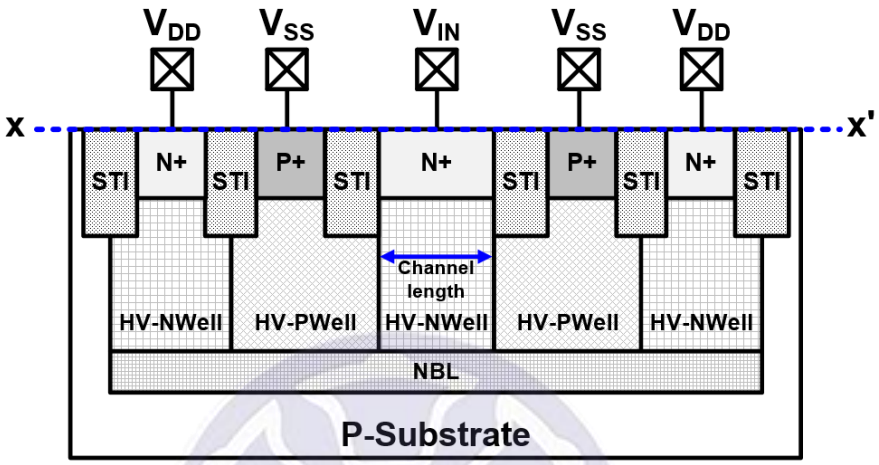
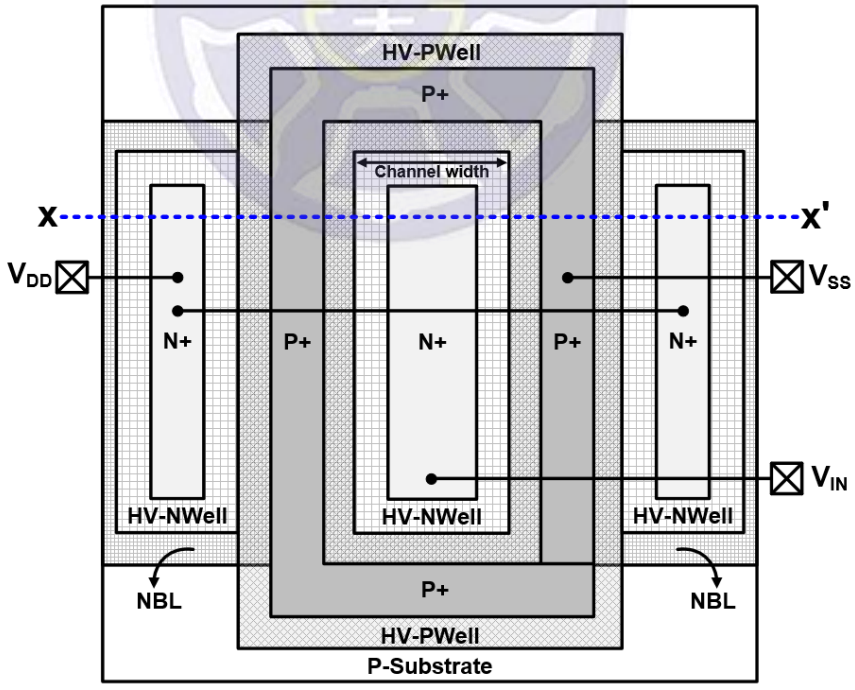


Fig. 5.3. Simulated signal losses of traditional, C-LC, C-L-C, and C-L-C-L structures.

This thesis has prepared some future works for the depletion diodes in high-voltage applications. Based on the implementation of P-type depletion diodes (D_D_P), the next step is to implement the N-type depletion diodes (D_D_N). Figs. 5.4 (a) and (b) show the cross-sectional and layout top views of N-type depletion diodes.



(a)



(b)

Fig. 5.4. The (a) cross-sectional and (b) layout top views of N-type depletion diodes (D_D_N).

In addition, the P-type and N-type depletion diodes are also planned to be implemented as a power-rail ESD clamp circuit. Fig. 5.5 shows the whole-chip ESD protection design composed of the P-type and N-type depletion diodes. The power clamp is composed of a detection circuit and a depletion diodes clamp. The cross-sectional view of depletion diodes clamp is shown in Fig. 5.6. Under the normal operation, the point A is high voltage level and the channel of depletion diodes clamp is closed. Conversely, the point A is low voltage level and the depletion diodes clamp is turned on to discharge when the ESD events occur between the power lines.

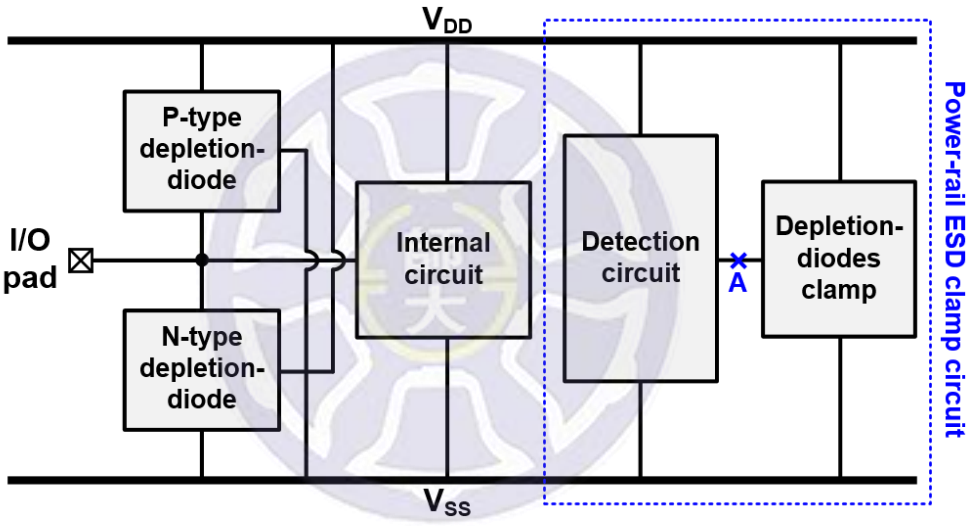


Fig. 5.5. Whole-chip ESD protection design with P-type and N-type depletion diodes.

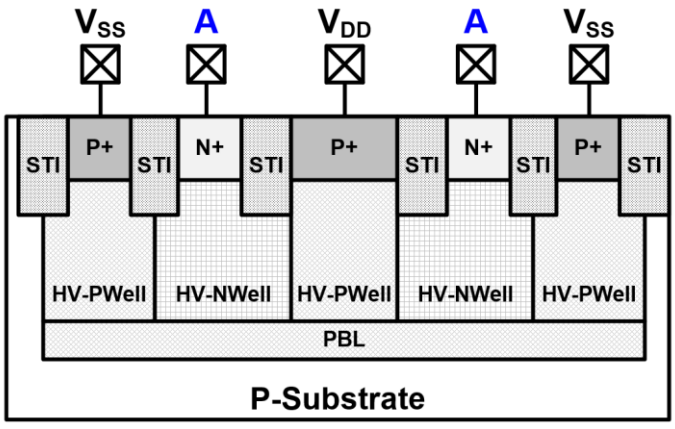


Fig. 5.6. The cross-sectional view of the depletion diodes clamp.

Reference

[1] J. Vinson and J. Liou, "Electrostatic discharge in semiconductor devices: Protection techniques," in *Proc. IEEE Int. Conf. in Micro-electronics*, vol. 88, no. 12, pp. 1878-1902, Dec. 2000.

[2] ESD association standard test method for electrostatic discharge sensitivity testing—human body model (HBM) component level, ANSI/ESD STM5.1-2007, 2007.

[3] M. Kelly, G. Servais, T. Diep, D. Lin, S. Twerefour, and G. Shah, "A comparison of electrostatic discharge models and failure signatures for CMOS integrated circuit devices," in *Proc. EOS/ESD Symp*., 1995, pp. 175-185.

[4] K. Verhaege, G. Groeseneken, H. Maes, P. Egger, and H. Gieser, "Influence of tester, test method, and device type on CDM ESD testing," in *Proc. EOS/ESD-Symp.*, 1994, pp. 49-62.

[5] K. Muhonen, N. Peachey, and A. Testin, "Human metal model (HMM) testing challenges to using ESD guns" in *Proc. EOS/ESD Symp*., 2009, pp. 1-9.

[6] ESD association standard test method for electrostatic discharge sensitivity testing—machine model (MM) component level, STM5.3.1-2009, 2009.

[7] ESD association standard test method for electrostatic discharge sensitivity testing—human body model (HBM) component level, STM5.1-2007, 2007.

[8] ESD association standard test method for electrostatic discharge sensitivity testing—charged device model (CDM) component level, STM5.3.1-2009, 2009.

[9] M.-D. Ker and C.-Y. Lin "ESD protection consideration in nanoscale CMOS technology" in *Proc. IEEE Int. Conf. on Nanotechnology*, 2011, pp. 720-723.

[10] F. Roger, W. Reinprecht, and R. Minixhofer, "Process variation aware ESD design window considerations on a 0.18 μm analog, mixed-signal high voltage

technology," in *Proc. EOS/ESD Symp.*, 2011, pp. 1-7.

[11] S. Sharma, E. Lagunas, S. Maleki, S. Chatzinotas, J. Grotz, J. Krause, and B. Ottersten, "Resource allocation for cognitive satellite communications in Ka-band (17.7–19.7GHz)," in *Proc. IEEE Int. Conf. Communication Workshop*, 2015, pp. 1646-1651.

[12] M. Nishikawa, K. Nakamura, H. Minda, K. Nakagawa, H. Hanado, S. Kawamura, S. Sugitani, and S. Shimizu, "Precipitation measurement using a dual Ka-band radar system for GPM/DPR algorithm development," in *Proc. IEEE Int. Geoscience and Remote Sensing Symp.*, 2012, pp. 1928-1931.

[13] R. Glogowski, J. Zurcher, C. Peixeiro, and J. Mosig, "A low-loss planar Ka-band antenna subarray for space applications," *IEEE Trans. Antennas Propag.*, vol. 61, no. 9, pp. 4549-4557, Sep. 2013.

[14] S. Cao, J. Chun, S. Beebe, and R. Dutton, "ESD design strategies for high-speed digital and RF circuits in deeply scaled silicon technologies," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2301-2311, Sep. 2010.

[15] K. Gong, H. Feng, R. Zhan, and A. Wang, "A study of parasitic effects of ESD protection on RF ICs" *IEEE Trans. Microwave Theory Tech*., vol. 50, no. 1, pp. 393-402, Jan. 2002.

[16] M.-D. Ker, C.-Y. Lin, and Y.-W. Hsiao, "Overview on ESD protection designs of low parasitic capacitance for RF ICs in CMOS technologies," *IEEE Trans. Device Mater. Reliab.*, vol. 11, no. 2, pp. 207-218, Jun. 2011.

[17] M.-D. Ker and Y.-W. Hsiao, "ESD protection design with low capacitance consideration for high-speed/high-frequency I/O interfaces in integrated circuits," *Recent Patents on Engineering*, vol. 1, no. 2, pp. 131-145, Jun. 2007.

[18] M. Mergens, M. Mayerhofer, J. Willemen, and M. Stecher, "ESD protection

considerations in advanced high-voltage technologies for automotive," in *Proc. EOS/ESD*, 2006, pp. 54-63.

[19] J.-S. Kim and W.-H. Lee "Offset-compensated operational amplifier for gray voltage generation of 262144 color QVGA LCD driver IC," in *Proc. IEEE Asian Solid-State Circuits Conf.*, pp. 368-371, Nov. 2007.

[20] Y.-C. Huang, C.-T. Dai, and M.-D. Ker, "Self-protected LDMOS output device with embedded SCR to improve ESD robustness in 0.25-μm 60-V BCD process," in *Proc. IEEE Int. Symp. on Next-Generation Electronics*, 2013, pp.116-119.

[21] F. Ma, B. Zhang, Y. Han, J. Zheng, B. Song, S. Dong, and H. Liang, "High holding voltage SCR-LDMOS stacking structure with ring-resistance-triggered technique," *IEEE Electron Device Letters*, vol. 34, no. 9, pp.1178-1180, 2013.

[22] V. DeHeyn, G. Groesenken, B. Keppens, M. Natarajan, L. Vacaresse, and G. Gallopyn, "Design and analysis of new protection structures for Smart Power Technology with controlled trigger and holding voltage," in *Proc. Int. Reliab. Physics Symp.*, 2001, pp. 253-258.

[23] Y. Li, J. Liou, J. Vinson, and L. Zhang, "Investigation of LOCOS- and polysilicon-bound diodes for robust electrostatic discharge (ESD) applications," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 814-819, Apr. 2010.

[24] C.-Y. Lin, M.-L. Fan, M.-D. Ker, L.-W. Chu, J.-C. Tseng, and M.-H. Song "Improving ESD robustness of stacked diodes with embedded SCR for RF applications in 65-nm CMOS," in *Proc. Int. Reliab. Physics Symp.*, Jun. 2014, pp. EL.1.1-EL.1.4.

[25] M.-D. Ker and C.-Y. Chang, "ESD protection design for CMOS RF integrated circuits using polysilicon diodes," *Microelectron. Reliab.*, vol. 42, no. 6, pp. 863-

872, Jun. 2002.

[26] S. Thijs, M. Okushima, J. Borremans, P. Jansen, D. Linten, M. Scholz, P. Wambacq, and G. Groeseneken, “Inductor-based ESD protection under CDM-like ESD stress conditions for RF applications,” in *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 49-52, 2008.

[27] C.-Y Chang and M.-D. Ker, “On-chip ESD protection design for GHz RF integrated circuits by using polysilicon diodes in sub-quarter-micron CMOS process,” in *Proc. IEEE Int. Symp. on VLSI Tech., Syst., and Applications*, pp. 240-243, 2001.

[28] M.-D. Ker and T.-Y. Chen, “Design on the turn-on efficient power-rail ESD clamp circuit with stacked polysilicon diodes,” in *Proc. IEEE Int. Symp. on Circuits and Syst.*, 2001, pp. 758-761.

[29] S. Maeda, M. Tanaka , Y. Otsuk, M. Tsukuda , and Y. Morishita, “Area-efficient ESD design using power clamps distributed outside I/O cell ring,” in *Proc. EOS/ESD Symp*, 2016.

[30] Y. Koo, K. Lee, J. Kwack, J. Won, and K. Kim, “The design of Bi-CMOS LVDS output buffer with ESD protection circuit using 90nm CMOS technology,” in *Proc. Int. Conf. on Advances in Electronics and Micro-elevtronics*, Oct. 2008, pp. 54-58.

[31] S. Aloui, E. Kerherve, J. Begueret, R. Plana, and D. Belot, “Optimized pad design for millimeter-wave applications with a 65 nm CMOS RF technology,” in *Proc. Eur. Microw. Conf.*, Sep. 2009, pp. 1187-1190.

[32] A. Dong, J. Salcedo, S. Parthasarathy, Y. Zhou, S. Luo, J. Hajjar, and J. Liou, “ESD protection structure with reduced capacitance and overshoot voltage for

high speed interface application," *Microelectronics Reliab.*, vol. 79, pp. 201-205, Mar. 2017.

[33] J.-T. Chen and M.-D. Ker, "On-chip ESD protection devices for high-speed I/O applications in CMOS technology," *IEEE Trans. Electron Devices,* vol. 64, no. 10, pp. 3979-3985, Oct. 2017.

[34] L. Zhu and K. Wu, "Accurate circuit model of interdigital capacitor and its application to design of new quasi-lumped miniaturized filters with suppression of harmonic resonance," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 347-356, Mar. 2000.

[35] J.-C. Tseng, C.-T. Hsu, C.-K. Tsai, Y.-C. Liao, and M.-D. Ker, "ESD protection design for low trigger voltage and high latch-up immunity," in *Proc. IEEE Int. Physical and Failure Analysis of Integrated Circuits Symp.*, 2010, pp. 32-35.

[36] P. Renaud, A. Gendron, M. Bafleur, and N. Nolhier, "High robustness PNP-based structure for the ESD protection of high voltage I/Os in an advanced smart power technology," in *Proc. IEEE Bipolar/BiCMOS Circuits Tech. Meeting*, 2007, pp. 226-229.

Vita

姓名: 彭柏維 (Bo-Wei Peng)

性別: 男

出生日期: 中華民國 83 年 02 月 27 日

學歷: 高雄市立高雄高級工業職業學校 (98 年 9 月－101 年 6 月)

國立雲林科技大學 電子工程學系學士班 (101 年 9 月－105 年 6 月)

國立臺灣師範大學 電機工程學系碩士班 (105 年 9 月－107 年◯月)

碩士班修習課程

積體電路可靠度	林群祐 教授
積體電路與靜電放電防護設計實務	林群祐 教授
射頻與微波積體電路	蔡政翰 教授
工程機率與統計	黃政吉 教授
高等計算機網路	戴建耘 教授
超大型積體電路設計導論	賴以威 教授
半導體物理	李敏鴻 教授
半導體物理導論 (二)	駱芳鈺 教授
人工智慧	戴建耘 教授
多媒體網路	戴建耘 教授
書報討論(一), (二)	葉家宏 教授 王嘉斌 教授 陳瑄易 教授 王偉彥 教授

E-mail: showmymusic@gmail.com

Publish List

[1] B.-W. Peng and C.-Y. Lin, “Low-Loss I/O pad with ESD protection devices for gigahertz applications,” in *Proc. International Electron Device and Materials Symp.*, 2017.

[2] B.-W. Peng and C.-Y. Lin, “Low-Loss I/O Pad with ESD protection for K/Ka-Bands applications in the nanoscale CMOS process,” *IEEE Trans. Circuit Syst. II*, vol. 65, no. 10, pp. 1475-1479, Oct. 2018.