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Master's Thesis

應用於高速電路之靜電放電防護設計

ESD Protection Design of High-Speed Circuit

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戴子鈞 謹誌於師大

中華民國一一零年十月

應用於高速電路之靜電放電防護設計

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摘　　要

本論文旨在研究應用於高速積體電路之全晶片靜電放電防護設計，在 CMOS 製程下實作，以低電容元件搭配分散式電路的設計，並與既有二極體及電晶體元件的設計相比較。

隨著內部電路的操作頻率不斷提升，寄生電容造成的訊號損耗嚴重影響電路高頻性能，本篇論文利用兩級分散式電路架構的方式，將單級的防護元件以小尺寸分散至兩級來設計防護電路，以降低每級的元件寄生電容，並在兩級之間以匹配元件降低訊號通過時的損耗，形成π型架構的設計。傳統的π型架構設計使用的是二極體或電晶體元件，本論文提出利用其他低電容矽控整流器元件如堆疊二極體內嵌矽控整流器 (SDSCR) 及電阻觸發式矽控整流器 (RTSCR) 搭配π型架構，組成π-SDSCR 與π-RTSCR，來與π型連接的傳統元件進行比較。由實驗結果可知，在 20GHz 時，創新設計π-SDSCR 在單位插入損耗 (S_{21}) 下所達到的二次崩潰電流 (I_{t2}) 為傳統設計的 1.76 倍，π-RTSCR 則為傳統設計的 1.62 倍，相較於傳統架構，本文提出的設計具備更高的 ESD 防護能力及更低的寄生電容，更適用於高速電路。

最後，為了驗證與比較防護電路的性能，本論文也設計了一應用於高速的轉阻放大器 (Trans-impedance amplifier, TIA)，分別搭配傳統π型二極體設計與本論

文所提出的防護電路，並進行電路的量測，驗證實際的防護效果及對電路性能的影響。由實驗結果可知，創新設計與傳統設計都能為 TIA 電路提供 4kV 的 HBM ESD 耐受度，且π-SDSCR 在 17GHz 時的插入損耗僅傳統設計的 0.83 倍，π-RTSCR 則為傳統設計的 0.9 倍，顯示創新設計在提供足夠 ESD 耐受度的同時，對電路高頻性能影響更低。

關鍵字：全晶片靜電放電防護、π型架構、轉阻放大器

ESD Protection Design of High-Speed Circuit

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ABSTRACT

This thesis is to study a whole-chip electrostatic discharge (ESD) protection design for high-speed circuits. In CMOS process, the low-capacitance device is designed with distributed circuit in comparison with traditional design by diode and MOS.

As the operating frequency of the internal circuit increases, the signal loss caused by parasitic capacitance seriously affects the high-frequency performance of the circuit. A two-stage distributed circuit architecture is used in this thesis to divide a single-stage protection device into two stages in a small size which can reduce the parasitic capacitance of the device in each stage. The matching element is added between two stages and formed π-structure to reduce the signal loss. Diode or MOS is used in traditional π-model design. This thesis proposes to use other innovative low-capacitance silicon-controlled rectifier (SCR) such as stacked diodes with embedded silicon-controlled rectifier (SDSCR) and resistor-triggered SCR (RTSCR) with the π-model to compare with the π-connected traditional devices. From the experiment result, the secondary breakdown current (I_{t2}) provided by proposed π-SDSCR per unit insertion loss (S_{21}) at 20GHz is 1.76 times higher than that of the traditional design. That value provided by proposed π-RTSCR is 1.62 times higher than that of the traditional design. As compare with traditional structure,

proposed designs have higher ESD protection ability and lower parasitic capacitance which are more suitable for high-speed circuits.

In order to verify and compare the performance of the protection circuits, this thesis designed a high-speed trans-impedance amplifier (TIA), which has added the traditional π-diode and the proposed π-SCR in this paper as ESD protection. The circuits were measured to verify the protection ability and the influence on the circuit performance. From the experiment result, both traditional and proposed designs provide 4kV HBM ESD robustness for the TIA circuit. However, the degradation of insertion loss (ΔS_{21}) of TIA with π-SDSCR at 17GHz is only 0.83 times of that of TIA with traditional design. The value of TIA with π-RTSCR is 0.9 times of that of TIA with traditional design. It shows that as compare with traditional structure, proposed designs have lower impact on the high frequency performance of the circuit, while also providing sufficient ESD tolerance.

Keyword：whole-chip ESD protection, π-structure, TIA

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Chapter 1

Introduction

1.1 Motivation

In recent years, the demand for electronic products continues to increase. As the result, semiconductor industry becomes more and more important. However, electrostatic-discharge (ESD) events may cause great damage to integrated circuits [1]. Gross output value of IC products decreases due to the permanent failures caused by ESD stress. So that it is an effective way to enhance the production value of semiconductor industry to learn how to design ESD protection circuits. With the rapid development of processing technologies, the size of transistor is minimized to increase the operating speed and the gate oxide of transistor becomes thinner at the same time. A thin gate oxide may easily damage by the ESD stress [2]. Therefore, the robustness of electronic circuits decreases. However, there are still strict specifications for commercial IC products. There are more and more severe challenges about the reliability of integrated circuits in current semiconductor industry.

With the development of internet and communication technology, the demand for high-speed transmission products is gradually increasing. As the operating frequency of electronic circuits increases, it is more difficult to protect ICs from ESD damage effectively. The parasitic capacitance existing in protection elements causes signal loss on input signal. The high-frequency signal attenuation occurs when the ESD protection circuits are equipped [3]. In order not to degrade the high-frequency characteristics of internal circuit, the parasitic effect of protection device needs to be considered for different applications.

1.2 Background of ESD

ESD is a phenomenon that the charges transfer between different objects forming the discharging path. ESD current is up to several amperes (A) and can be generated in nanoseconds (ns). Some parts inside the circuit are unable to operate functionally when the large current flows into internal circuit instantly. As the result, IC products must be equipped with ESD protection circuit to ensure the reliability during operation. ESD problems have existed in electronics circuits since the semiconductor industry started to develop. Moreover, different kinds of ESD events are found as the process progresses.

1.3 ESD Test Standards

For commercial IC products, reliability is an important issue. The electronic circuits during manufacturing have to pass related tests. Some associations such as US military standard (MIL-STD), Joint Electron Device Engineering Council (JEDEC), and Electrostatic Discharge Association (ESDA) built the standards for ESD tests. The components are required to take the ESD tests before assembled into the products. The tests for electronic components is defined as component-level test. Component-level tests are classified as human-body model (HBM), machine model (MM), and charged-device model (CDM) based on the cause of ESD and discharging method. However, the specific HBM level can ensure a minimum MM level. There is a reduction of MM test in recent years. The equivalent circuits and test standards of HBM and CDM are introduced in following part.

(1) Human-Body Model (HBM)

The human body will accumulate electric charges due to friction between the feet and the floor when walking. When the IC products are touched by people, the discharging path is formed. ESD current flows into IC instantly and causes damage to the IC. The model of HBM (MIL-STD-883C method 3015.7) is shown in Fig. 1.1. The equivalent capacitance of HBM is 100pF, and the equivalent resistance is 1.5kΩ. The human body is charged as a 100pF capacitor and discharges the charges to ground through IC as a 1.5kΩ resistor [4], [5]. The target level of HBM ESD is shown in Table 1.1 [6]. The components of commercial IC products are required to pass 2kV HBM test.

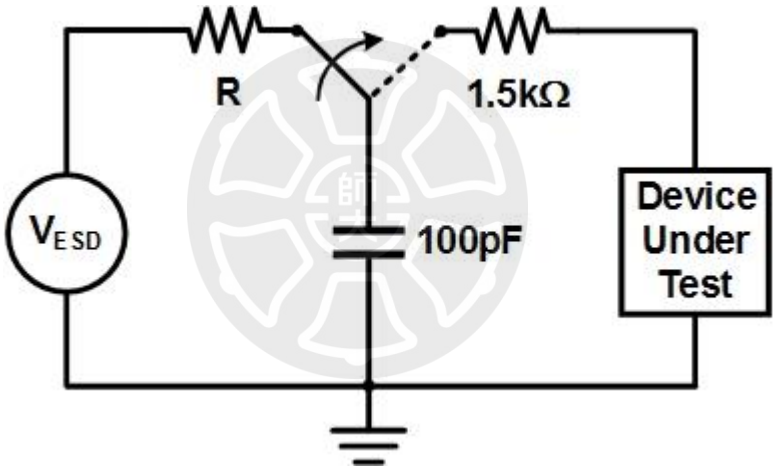


Fig. 1.1. The equivalent circuit of HBM.

Table 1.1. The target level of HBM

HBM Level	Impact on manufacturing environment
100V to <500V	Detailed ESD control method
500V	Basic ESD control methods for safe manufacturing
1kV	
2kV	

(2) Charged-Device Model (CDM)

In the manufacturing process of IC, it may accumulate charges itself. Once the pin of IC contacts with ground, the discharging path is formed. The ESD current flowing from charged device leads to internal damage. The model of CDM is shown in Fig. 1.2 [7], [8]. The discharging time of CDM is much shorter than that of HBM and MM [9]. IC suffers permanent damage more easily. As shown in Table 1.2, the components of commercial IC products are required to pass 250V CDM test [10]. In this thesis, very fast TLP test is used with the pulse width in range of 1~10ns to simulate CDM ESD stress.

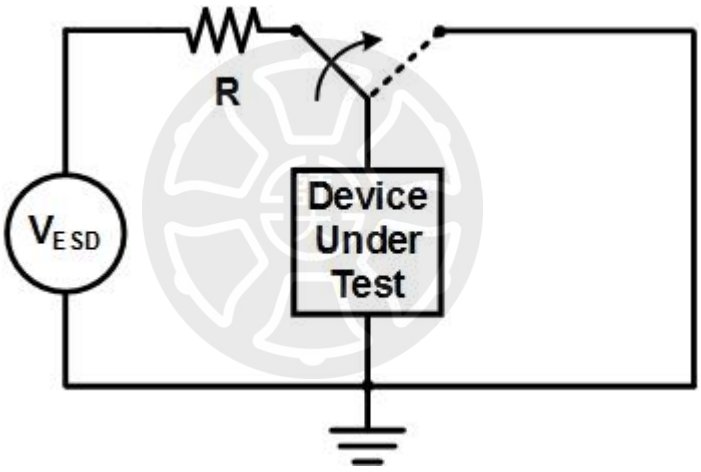


Fig. 1.2. The equivalent circuit of CDM.

Table 1.2. The target level of CDM

CDM Level	ESD Control Requirements
$V_{CDM} < 200V$	Basic ESD control methods, Process specific measures, Charging/discharging measurements at each process step.
$V_{CDM} \geq 200V$	Basic ESD control methods.

1.4 Design Concepts of ESD Protection

ESD event is very common in our daily lives and has serious impact on electronic products. It is necessary to design ESD protection circuits for IC products to prevent the damage of ESD stress. The I/O terminal is the most vulnerable to ESD damage from outside among all the pins in integrated circuits. The gate-oxide is generally controlled by the bias applied to input pad [11]. Therefore, to protect the thin gate-oxide in time before ESD current flows into internal circuit, ESD protection circuits are usually placed near I/O pad to discharge it. The protection circuits are also necessary between the power rails to prevent from ESD damage. The whole-chip ESD protection design is realized with I/O ESD protection circuit and power-rail ESD clamp circuit as shown in Fig. 1.3.

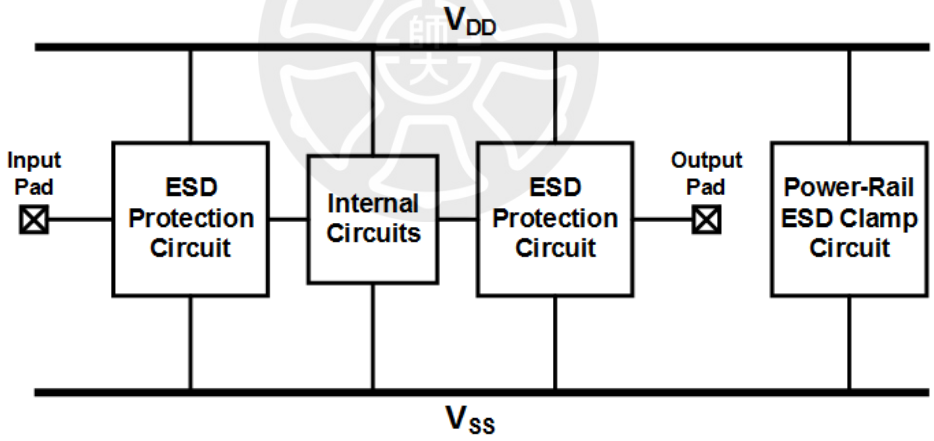


Fig. 1.3. Whole-chip ESD protection design.

Fig. 1.4 shows a general ESD design window. ESD design window is defined as a guideline for designing protection circuits, where X-axis shows the measured voltage of device under test, and Y-axis shows the measured current value. ESD protection device is designed to operate in the range between supply voltage (V_{DD}) which is the maximum voltage value and the internal circuit breakdown voltage (V_{BD}). Generally, the lower

limit is 1.1×V_{DD}, and the upper limit is 0.9×V_{BD}. There are some properties of ESD protection circuit [12]. To reduce the power consumption, protection device must be kept off when internal circuit operates below V_{DD}. In addition, when internal circuit is during normal operation, ESD protection design should not affect circuit functions. ESD protection device has to turn on before the internal circuit breakdown when ESD stress hits. So that the trigger voltage (V_{t1}) must be lower than V_{BD}. There is snapback phenomenon in some protection devices. The voltage cross the protection device drops a lot during conduction. Therefore, the power dissipation can be lower because of the lower holding voltage (V_h) and the device can conduct more ESD current before thermal breakdown. However, V_h must be higher than V_{DD} to prevent latch-up effect. The slope of I-V curve is defined as the reciprocal of on-resistance (R_{on}). The protection device turns on with lower R_{on} can discharge ESD current in lower clamping voltage. Protection device is destroyed permanently when ESD current is higher than the secondary breakdown current (I_{t2}), as the result, the robustness is proportional to I_{t2}.

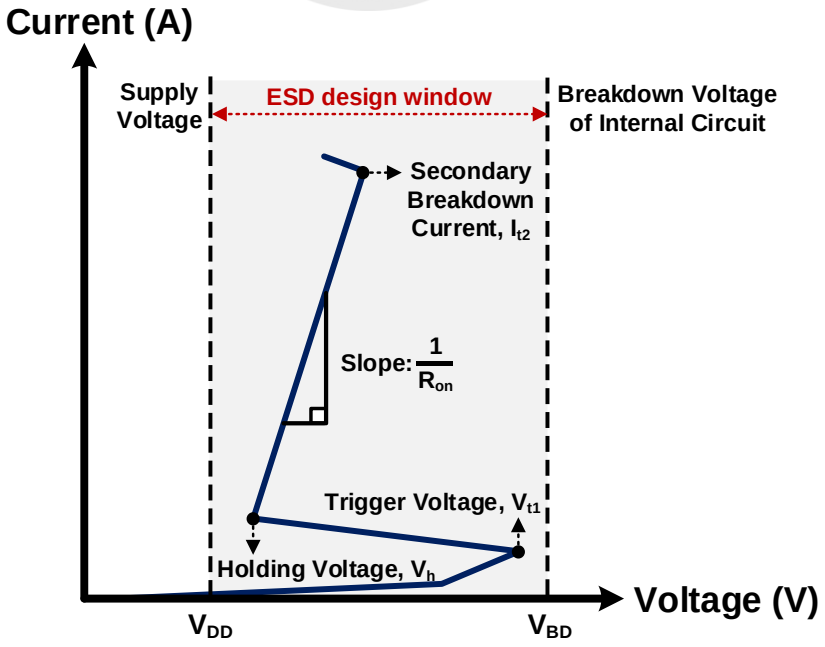


Fig. 1.4. ESD design window.

There are four pin-combinations which are positive I/O-to-V_{SS} (PS mode), positive I/O-to-V_{DD} (PD mode), negative I/O-to-V_{SS} (NS mode), and negative I/O-to-V_{DD} (ND mode). Equipped with power-rail ESD clamp circuit, the discharging path is shown in Fig. 1.5.

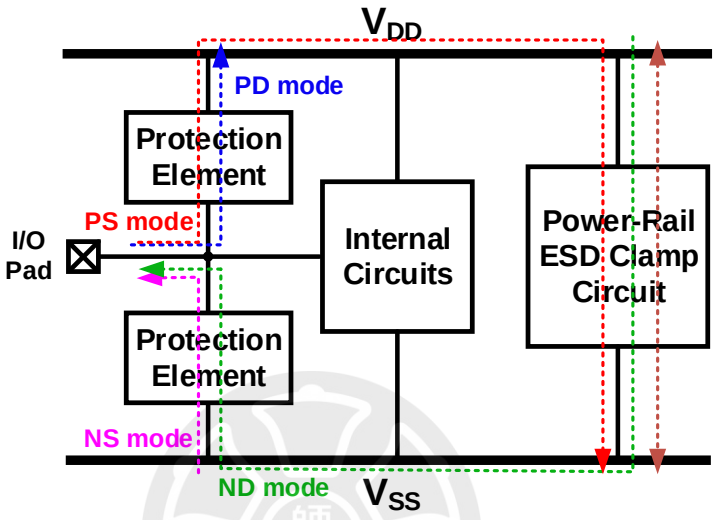


Fig. 1.5. Whole-chip ESD protection design with corresponding path.

1.5 Organization about This Thesis

There are five chapters in this thesis. The motivation of this research and the background of the reliability issue is introduced in chapter 1. Chapter 2 presented some studies of ESD protection designs for high-frequency applications. In chapter 3, the devices which are selected for traditional and proposed design are noted. The simulation data and measurement results are recorded at the end of this chapter. At last, the proposed ESD protection circuit is verified with a trans-impedance amplifier (TIA). There are the simulation and measurement results in chapter 4. Chapter 5 discussed the conclusion and future work.

Chapter 2

Studies of ESD Protection Designs for High-Speed Applications

2.1 Consideration of ESD Protection Design at High-Speed Circuits

As the operating speed of IC increases, ESD protection circuit used for high-speed IC faces more severe challenges. The parasitic capacitance formed by ESD protection circuit at I/O pad is one of important design consideration for high-speed circuit [13]. As shown in Fig. 2.1, the parasitic capacitance of ESD protection circuit will cause the signal loss form I/O pad to ground and the performance of high-speed circuit will degenerate. It has to be considered as ESD protection circuit is applied.

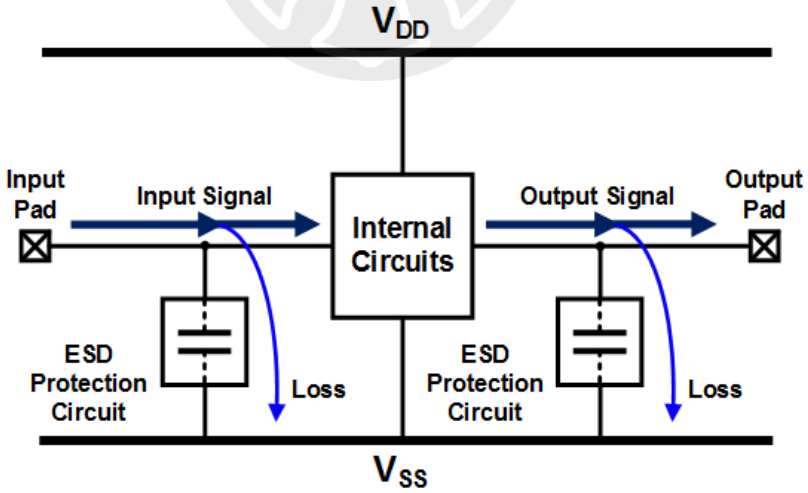


Fig. 2.1. Signal loss at high frequencies.

ESD protection circuit must provide ICs with enough robustness against ESD stress. The ESD level is proportional to the size of protection device. ESD protection device

must be large enough to provide sufficient ESD robustness. However, larger device size leads to higher parasitic capacitance which may cause undesirable signal loss. It is hard to design a ESD protection circuit for high-speed applications without distortion of input signal [14], [15]. There is a trade-off between ESD robustness and high-frequency performance when ESD protection circuit is designed for high-speed applications,

Diode, MOS, and silicon-controlled rectifier (SCR) are commonly used devices for ESD protection in CMOS process [16]. The I-V curve of diode is plotted in Fig. 2.2. Forward biased diode discharges high current and clamps the voltage at a low level. Diode is suitable for ESD protection because of its characteristics. Diode also discharges current when it reversely breaks down. However, the high breakdown voltage makes the heat during discharging is much higher.

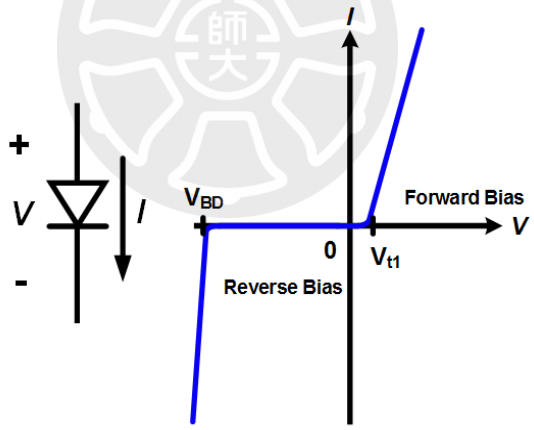


Fig. 2.2. The I-V curve of diode.

MOS is also used as an ESD protection device with the gate of NMOS connected to ground and the gate of PMOS connected to V_{DD}. In order to reduce unnecessary power dissipation, the channel of MOS is kept off with gate connected to ground or V_{DD} under normal operation. The I-V curve of NMOS is plotted in Fig. 2.3. When ESD stress hits, the parasitic NPN inside NMOS turns on to discharge ESD current accompanied by the

slight snapback phenomenon. The trigger voltage of NMOS is higher than that of diode because it is conducted after the breakdown of P-N junction.

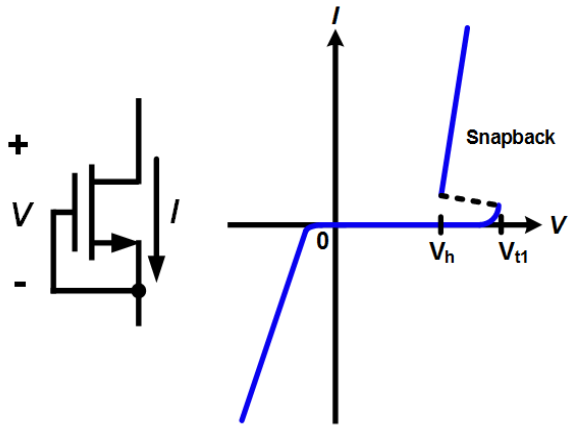


Fig. 2.3. The I-V curve of NMOS.

SCR is a p-n-p-n four-layer device composed of embedded NPN and PNP [17]. It turns on with the leakage current flowing through the resistance between the base and emitter. The I-V curve of SCR is plotted in Fig. 2.4. When SCR is conducted, there is a positive-feedback mechanism formed. As a result, SCR can discharge high current with strong snapback phenomenon [18].

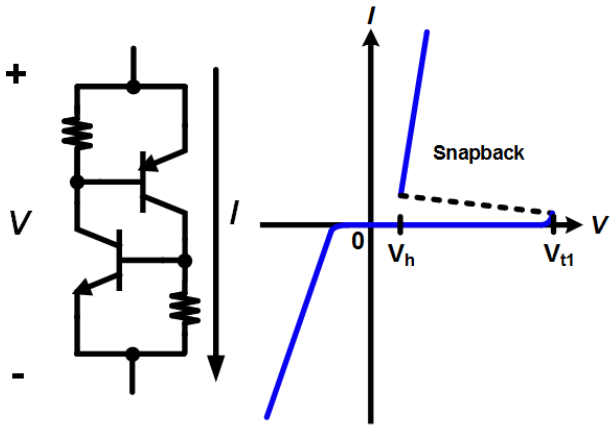


Fig. 2.4. The I-V curve of SCR.

2.2 ESD Protection Designs for High-Speed Application

2.2.1 Capacitive ESD Protection Circuit

(1) Dual Diodes [19]

As shown in Fig. 2.5, a pair of diodes near I/O pad is a commonly used ESD protection circuit. The diode placed from I/O to V_{DD} (D_{P1}) form the path for positive I/O-to-V_{DD} (PD mode) when positive ESD stress hits I/O pad. The diode placed from V_{SS} to I/O pad (D_{N1}) form the path for negative I/O-to-V_{SS} (NS mode) when negative ESD stress hits I/O pad. In assistance with power-rail ESD clamp circuit, the whole-chip ESD protection can be realized. In series with power-rail ESD clamp circuit, the diode (D_{P1}) forms the path of the positive I/O-to-V_{SS} (PS mode). The path of the negative I/O-to-V_{DD} (ND mode) is formed by the diode (D_{N1}) in series with power-rail ESD clamp circuit. To reduce the parasitic effect, the size of diode is cut down to lower the capacitive load. However, the ESD robustness decreases with reducing size.

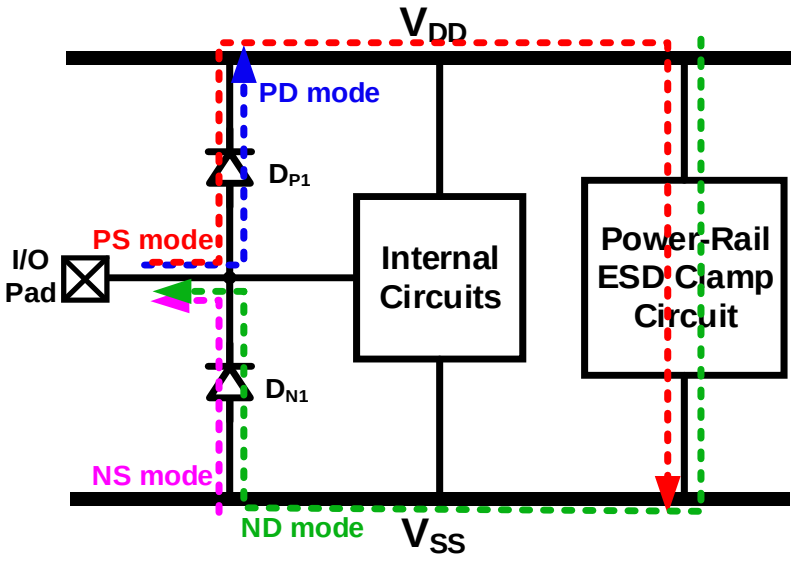


Fig. 2.5. ESD protection design of dual diodes [19].

(2) Dual Stacked Diodes with Embedded SCR (SDSCR) [20]

For the high-speed applications, the parasitic capacitance of protection circuit has to be reduced to lower the signal loss. To solve this problem, there is an improved configuration proposed which is stacking diodes with embedded SCR (SDSCR). SCR is a useful ESD protection device in CMOS process due to high robustness. Moreover, the SCR device can be applied at high frequencies because of its low parasitic capacitance per layout area. With positive-feedback mechanism, the SCR device can discharge high ESD current.

As shown in Fig. 2.6, two stacked diodes with embedded SCR are placed from V_{SS} to I/O pad (D_{N1}, D_{N2}) and I/O pad to V_{DD} (D_{P1}, D_{P2}). The discharging path of dual SDSCR is the same as the dual diodes. With the help of power-rail ESD clamp circuit, whole-chip ESD protection is realized. In this improved structure, the parasitic capacitance is reduced and the stacked diode also act as the trigger device of the embedded SCR to make it fast turn on.

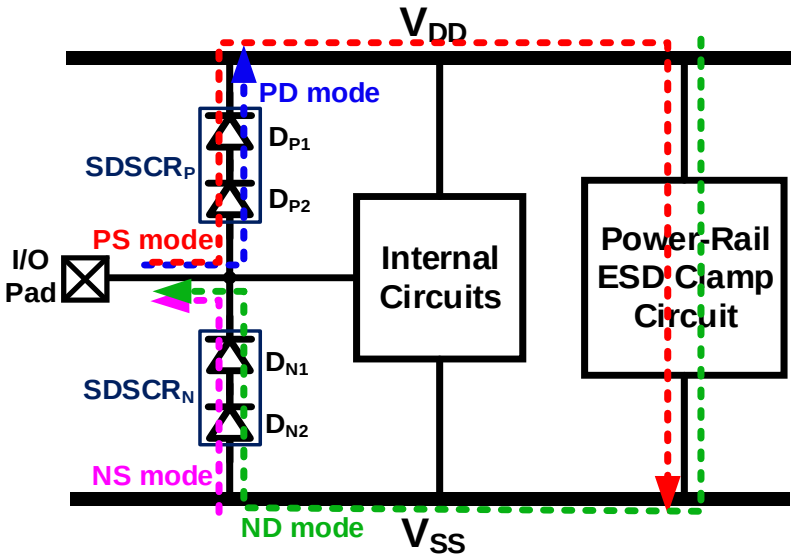


Fig. 2.6. ESD protection design of dual SDSCR [20].

(3) Dual Resistor-Triggered SCR (RTSCR) [21]

By using a small resistor as the trigger element of SDSCR, the resistor-triggered SCR (RTSCR) is present. As shown in Fig. 2.7, the small resistor is inserted between each stacked diodes. Two resistor-trigger SCR are placed from V_{SS} to I/O pad (D_{N1}, D_{N2}) and I/O pad to V_{DD} (D_{P1}, D_{P2}). The discharging path of dual RTSCR is the same as the dual diodes. With the help of power-rail ESD clamp circuit, whole-chip ESD protection is realized. In this structure, the small resistor can limit the large ESD current flowing through the diode path so that the large ESD current can be discharge through the robust SCR path. The small resistor can reduce the overall parasitic capacitance seen at I/O as well.

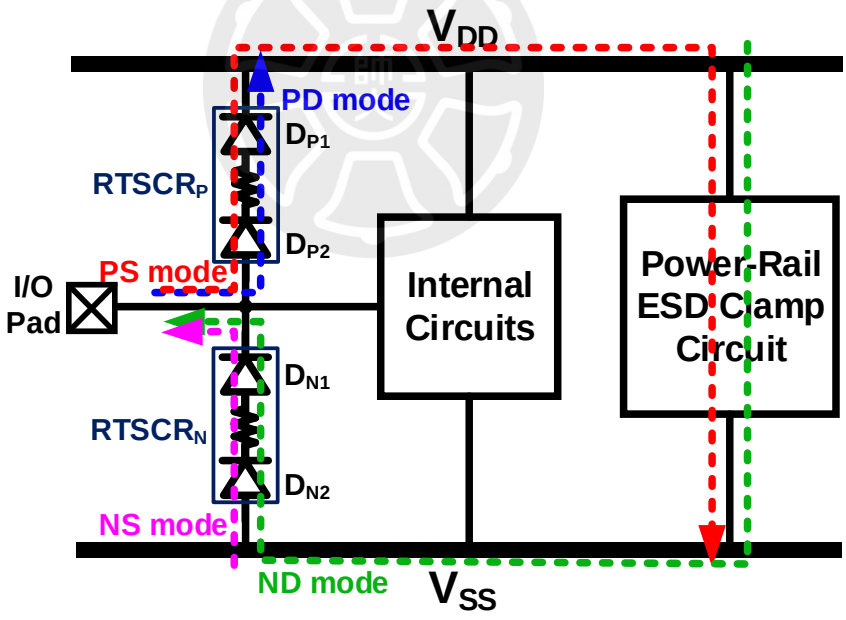


Fig. 2.7. ESD protection design of dual SDSCR [21].

2.2.2 Distributed ESD Protection Circuit (DESD)

The parasitic capacitance of ESD protection circuit near I/O pad will cause high-frequency performance degradation. To solve this problem, the size of protection device must be reduced. However, the size of protection device is proportional to the ESD robustness. Smaller device provides relatively lower ESD level.

Another way to design the ESD protection circuit for high-frequency applications is dividing ESD protection devices into many sections [22]. It is an effective way to maintain the ESD robustness without severe high-frequency degradation. To achieve good high-frequency performance, these parts of protection device are connected with matching elements such as inductor. The inductor can resonate with the parasitic capacitance of protection devices. Therefore, the high-frequency signal can be transmitted with less distorting.

As shown in Fig. 2.8, the distributed ESD protection circuit is composed of two sections (D_{P1}, D_{N1} and D_{P2}, D_{N2}). An inductor (L) is used to sustain the broadband performance as the matching element. The diodes can provide the discharging path under forward bias for PD mode and NS mode. With the help of power-rail ESD clamp circuit, the ESD stress under PS mode and ND mode can also be discharged.

Another way to match the dual diodes is presented in Fig. 2.9. The ESD protection device is divided into three sections (D_{P1}, D_{N1}, D_{P2}, D_{N2}, and D_{P3}, D_{N3}) and with three inductors (L_1, L_2, and L_3). Each part of protection device can be much smaller. However, with more inductors in use, the layout area is also increased. Both two structures can present great ESD robustness and achieve good broadband performance.

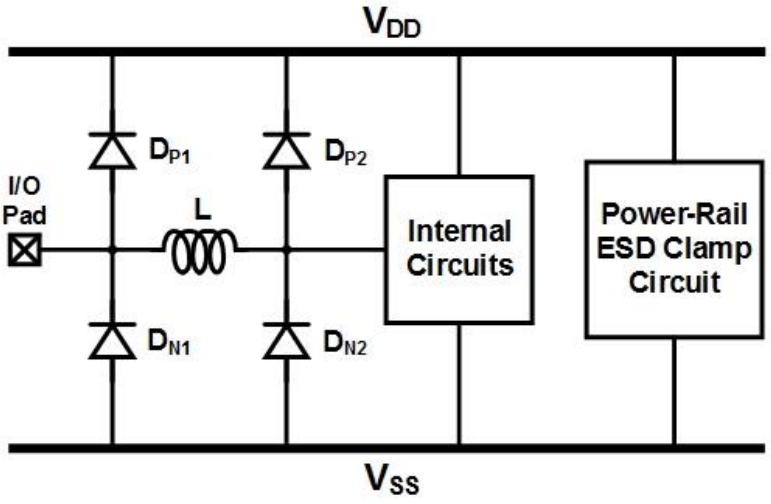


Fig. 2.8. ESD protection design of two-section distributed circuit [22].

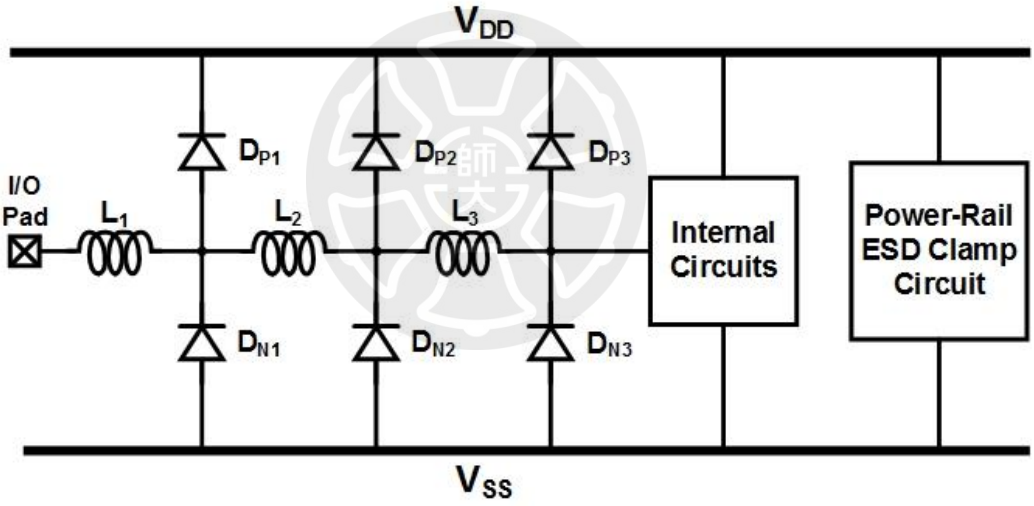


Fig. 2.9. ESD protection design of multi-section distributed circuit [22].

Chapter 3

Design of π-Model SCR (π-SCR)

3.1 Design Concepts of Distributed Circuit

In recent years, wireless communication technology has been flourishing and the demand for high-speed transmission products is gradually increasing. The high transmission rate products need to be equipped a wider bandwidth to enable faster signal changes. As products with high transmission rates become more and more popular, the requirements of broadband integrated circuits for ESD protection are also becoming stricter. The protection components must not affect the high frequency performance of the internal circuit as much as possible, and provide high ESD robustness at the same time. Therefore, traditional ESD protection designs applied to electronic circuits are no longer suitable for high-speed ICs. The parasitic capacitance of protection device near I/O pad may affect the input signal. The impedance of parasitic capacitor decreases as the operating frequency rises. It means that the protection device beside the input terminal causes the signal loss. To achieve high ESD level, the protection device has to be in large size. However, the parasitic capacitance affects the normal operation of internal circuit severely. Some methods are proposed to lower the parasitic effects, such as distributed ESD protection circuit [23], [24].

The protection device is divided into two smaller parts. One part is near the I/O pad, and the other part is close to internal circuits. Two parts of protection devices are connected by a matching element to sustain the high frequency performance. Matching element can resonate with the parasitic capacitance of two stages. Therefore, this distributed circuit can stand high ESD level with less signal loss. The parasitic

capacitance of the devices placed from V_{SS} to I/O and I/O to V_{DD} are parallel when analyzed in the ac state. As shown in Fig. 3.1, the high-frequency equivalent circuit is like a π shape.

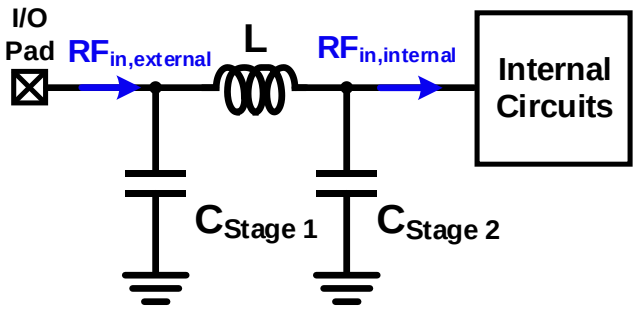
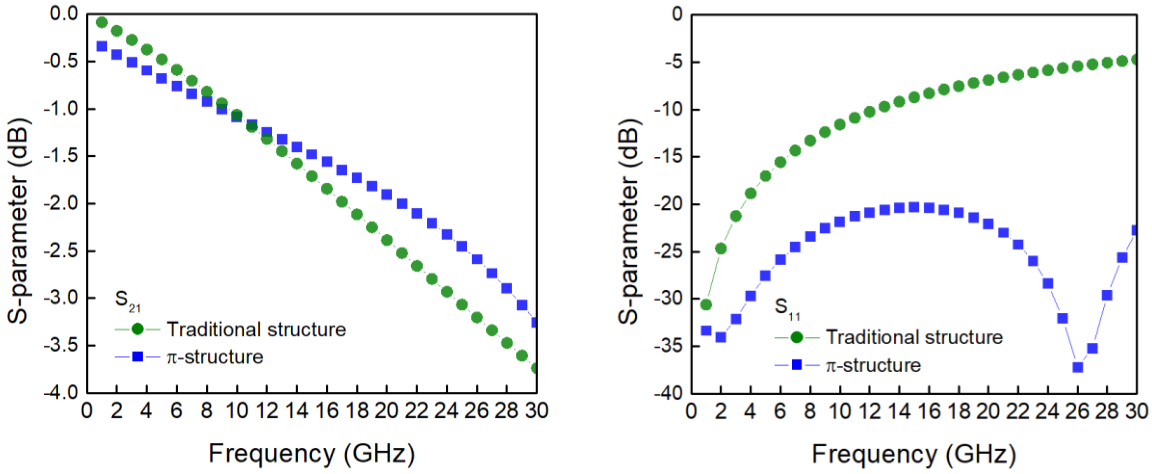


Fig. 3.1. High-frequency equivalent circuit of π-model circuit.

C_{Stage1} and C_{Stage2} are from the protection element in two stages such as SCR and diode. The size of protection device decides the value of parasitic capacitance. According to the expected specification, the selected device is equipped to discharge the ESD current. Therefore, the size of the device has to be large enough. The PN junction and side-wall of protection element lead to parasitic capacitance. The junction capacitance increases with larger layout area. The longer perimeter of PN junction also makes the side-wall capacitance rise. Fig. 3.2 shows the high-frequency simulation results of traditional structure and π-structure. As compared with traditional structure, π-structure can provide lower insertion loss (S_{21}) and return loss (S_{11}).

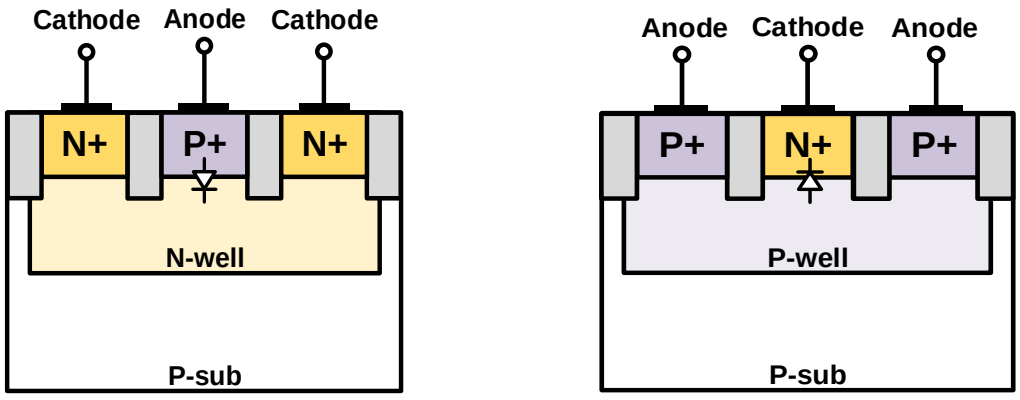


(a) (b)

Fig.3.2. (a) S_{21} (b) S_{11} simulation results of π-structure

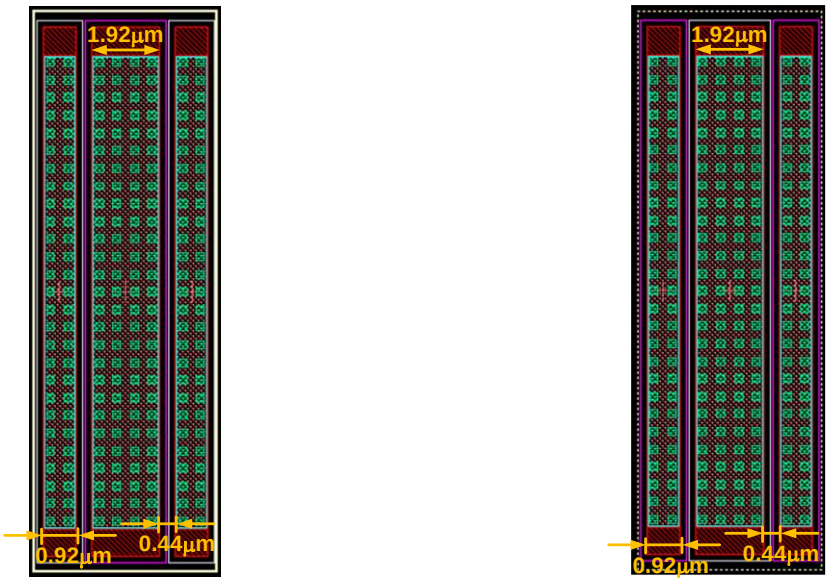
3.2 Traditional π-Model Diode (π-Diode)

In CMOS technology, diode is a common ESD protection device. It consists of P-type and N-type semiconductor. There are two ways to realize p-n junction on chip. As shown in Fig. 3.3 (a), P-type diode has its P+ as anode and its N-well as cathode. As shown in Fig. 3.3 (b), the anode of N-type diode is P-well and the cathode of that is N+. The layout top view of symmetrical P-type and N-type diode is shown in Fig. 3.4.



(a) (b)

Fig. 3.3. Cross-sectional view of symmetrical (a) P-type and (b) N-type diode.



(a) (b)

Fig. 3.4. Layout top view of symmetrical (a) P-type and (b) N-type diode.

When diode is conducted under forward bias, it turns on and discharges current at low voltage. It can also discharge current under reverse bias, but the clamping voltage is higher than that of the forward biased diode. Diode has high ESD robustness because of low power dissipation. The characteristics like a switch make it suitable for ESD protection. Besides, it is also used as trigger device for SCR, MOSFET, and BJT.

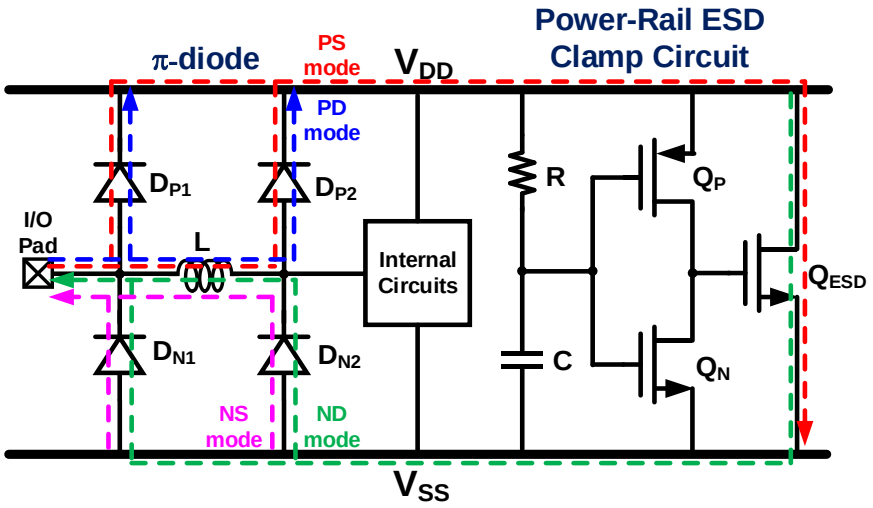


Fig. 3.5. Whole-chip ESD protection circuit with traditional π-diode.

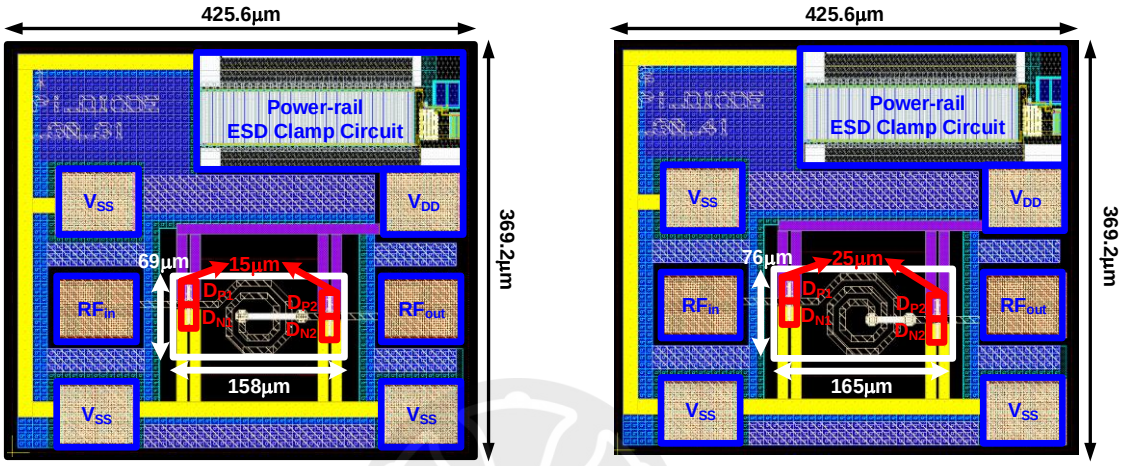
There is a two-section distributed circuit with diodes as device in traditional π-model diode (π-diode). The whole-chip ESD protection circuit with π-diode is shown in Fig. 3.5. Stage 1 is composed of diodes placed from V_{SS} to I/O (D_{N1}) and from I/O to V_{DD} (D_{P1}), and stage 2 is composed of diodes placed from V_{SS} to I/O (D_{N2}) and from I/O to V_{DD} (D_{P2}). The power-rail ESD clamp circuit is equipped to discharge the ESD current between V_{DD} and V_{SS}.

The ESD current under PD mode can be discharged by D_{P1} and D_{P2}. The ESD current under NS mode is discharged by D_{N1} and D_{N2}. The ESD current between V_{DD} and V_{SS} is discharged by the power-rail ESD clamp circuit. The ESD current under ND mode can be discharged by the power-rail ESD clamp circuit in series with D_{N1} and D_{N2}. The ESD current under PS mode is discharged by D_{P1} and D_{P2} in series with the power-rail ESD clamp circuit.

Table 3.1. The test cell of π-diode

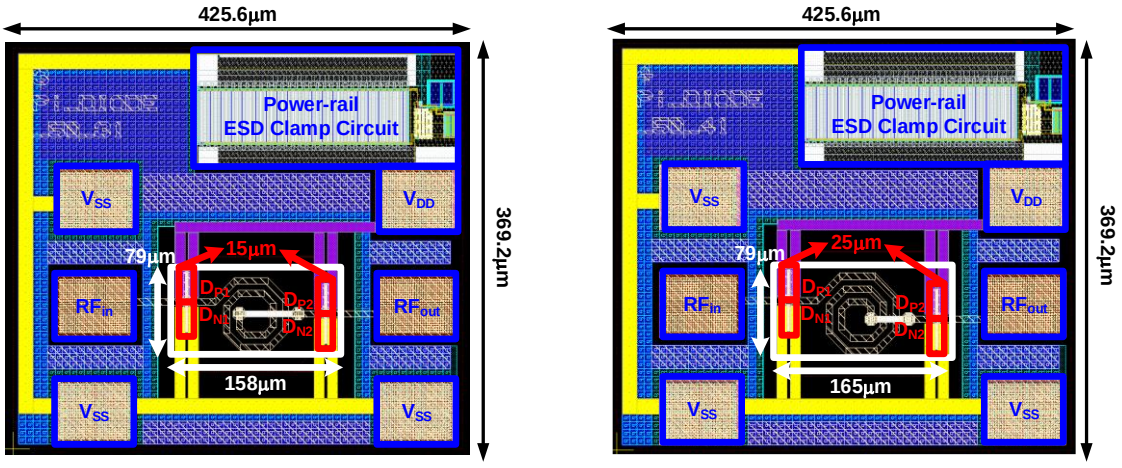
Cell Name	**Stage 1**		**Stage 2**		**Inductor**	
	Device	**Width**	**Device**	**Width**	**Device**	**Inductance**
π-diode_30_31	D_{P1}	15μm	D_{P2}	15μm	L	0.31nH
	D_{N1}	15μm	D_{N2}	15μm		
π-diode_30_41	D_{P1}	15μm	D_{P2}	15μm	L	0.41nH
	D_{N1}	15μm	D_{N2}	15μm		
π-diode_50_31	D_{P1}	25μm	D_{P2}	25μm	L	0.31nH
	D_{N1}	25μm	D_{N2}	25μm		
π-diode_50_41	D_{P1}	25μm	D_{P2}	25μm	L	0.41nH
	D_{N1}	25μm	D_{N2}	25μm		

The test cells of whole-chip ESD protection circuit with π-diode are listed in Table 3.1. The layout top view of each cell is shown below. The width of diode used in π-diode is 15μm (as shown in Fig. 3.6) and 25μm (as shown in Fig. 3.7) respectively and there are two different matching inductor applied in each size.



(a) (b)

Fig. 3.6. Layout top view of (a) π-diode_30_31 (b) π-diode_30_41

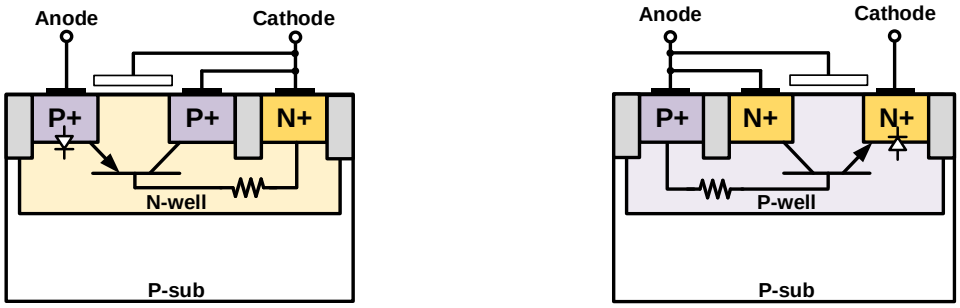


(a) (b)

Fig. 3.7. Layout top view of (a) π-diode_50_31 (b) π-diode_50_41

3.3 Traditional π-Model MOS (π-MOS)

MOS transistor devices are also traditional ESD protection device in CMOS technology [25]. MOS transistors are the most common device in CMOS circuit design so that it is also used widely in ESD protection circuit. When a MOS transistor is connected as GGNMOS (gate-grounded NMOS) and GDPMOS (gate-V_{DD} PMOS), it become a two-terminal device and there is a parasitic BJT formed between anode and cathode. As a result, ESD current can be discharge by the parasitic p-n-p and n-p-n junction. The cross-sectional view of MOS transistors is shown in Fig. 3.8. The anode of GDPMOS is its source terminal and GGNMOS has its source terminal as cathode. The layout top view of GDPMOS and GGNMOS is shown in Fig. 3.9. In order to comply with ESD design rules, the gate length of MOS is design as 0.36μm. The clearance from poly to contact on source of MOS is design as 0.5μm and that on drain side is design as 1.95μm. The silicide blocking is also used on the drain of MOS.

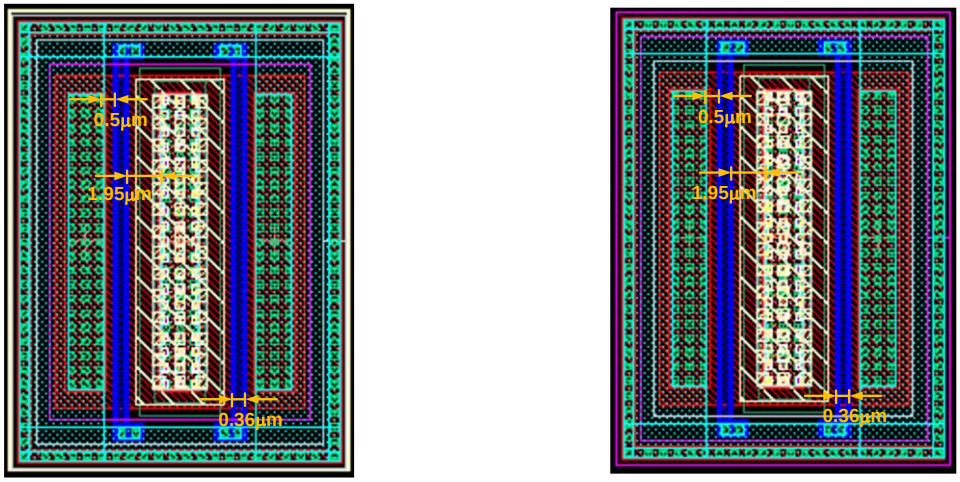


(a) (b)

Fig. 3.8. Cross-sectional view of (a) GDPMOS and (b) GGNMOS .

Traditional π-model MOS (π-MOS) is a two-section distributed circuit with MOS transistors as device. The whole-chip ESD protection circuit with π-MOS is shown in Fig. 3.10. Stage 1 is composed of a GGNMOS placed from V_{SS} to I/O (M_{N1}) and a GDPMOS placed from I/O to V_{DD} (M_{P1}), and stage 2 is composed of a GGNMOS placed

V_{SS} to I/O (M_{N2}) and a GDPMOS placed from I/O to V_{DD} (M_{P2}). The power-rail ESD clamp circuit is equipped to discharge the ESD current between V_{DD} and V_{SS}.



(a) (b)

Fig. 3.9. Layout top view of (a) GDPMOS and (b) GGNMOS.

The ESD current under PD mode can be discharged by M_{P1} and M_{P2}. The ESD current under NS mode is discharged by M_{N1} and M_{N2}. The ESD current between V_{DD} and V_{SS} is discharged by the power-rail ESD clamp circuit. The ESD current under ND mode can be discharged by the power-rail ESD clamp circuit in series with M_{N1} and M_{N2}. The ESD current under PS mode is discharged by M_{P1} and M_{P2} in series with the power-rail ESD clamp circuit.

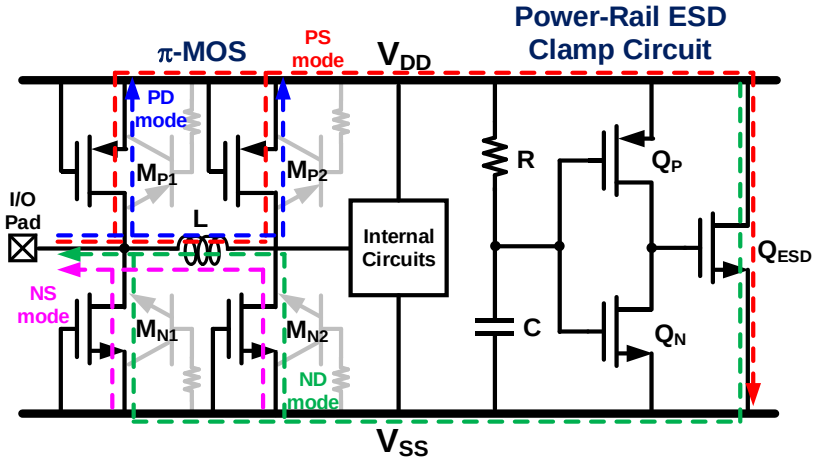


Fig. 3.10. Whole-chip ESD protection circuit with traditional π-MOS.

The test cells of whole-chip ESD protection circuit with π-MOS are listed in Table 3.2. The layout top view of each cell is shown below. The width of MOS transistors used in π-MOS is 100μm (as shown in Fig. 3.11), 22μm (as shown in Fig. 3.12), and 36μm (as shown in Fig. 3.13) respectively. In 22μm and 36μm these two case, there are two inductance of matching inductor are chosen to compare.

Table 3.2. The test cell of π-MOS

Cell Name	Stage 1		Stage 2		Inductor	
	Device	Width	Device	Width	Device	Inductance
π-MOS_44_31	M_{P1}	22μm	M_{P2}	22μm	L	0.31nH
	M_{N1}	22μm	M_{N2}	22μm		
π-MOS_44_41	M_{P1}	22μm	M_{P2}	22μm	L	0.41nH
	M_{N1}	22μm	M_{N2}	22μm		
π-MOS_72_31	M_{P1}	36μm	M_{P2}	36μm	L	0.31nH
	M_{N1}	36μm	M_{N2}	36μm		
π-MOS_72_41	M_{P1}	36μm	M_{P2}	36μm	L	0.41nH
	M_{N1}	36μm	M_{N2}	36μm		
π-MOS_200_31	M_{P1}	100μm	M_{P2}	100μm	L	0.31nH
	M_{N1}	100μm	M_{N2}	100μm		

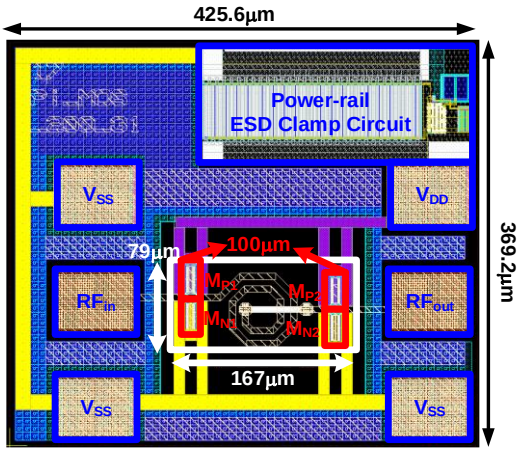
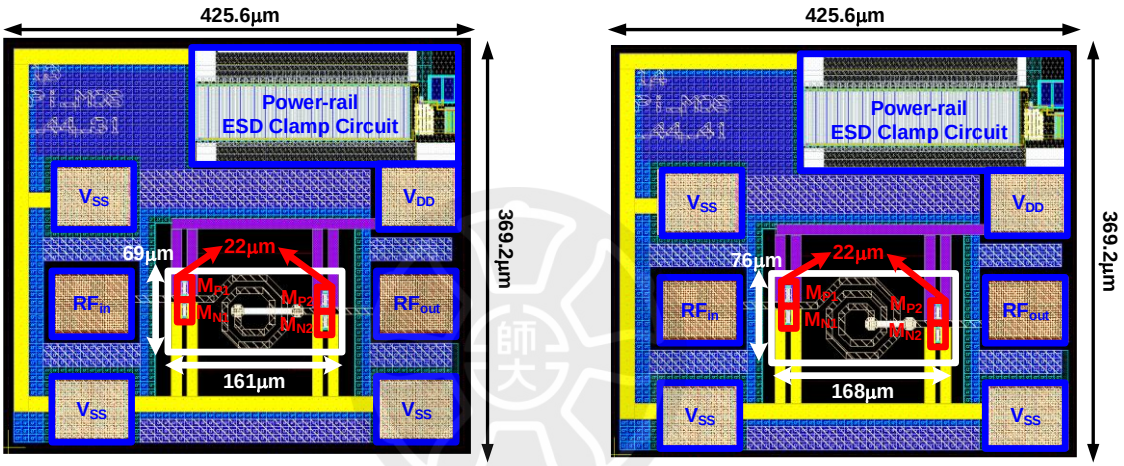
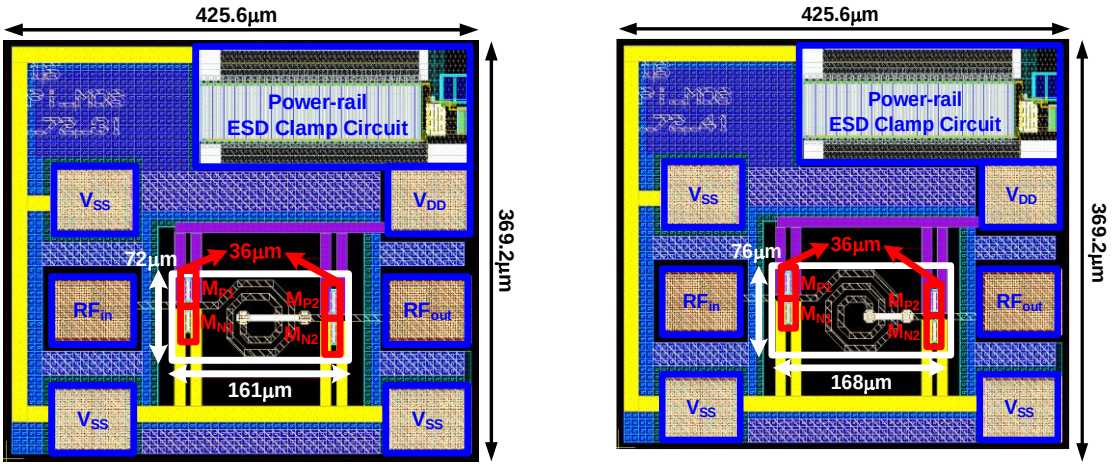


Fig. 3.11. Layout top view of π-MOS_200_31



(a) (b)

Fig. 3.12. Layout top view of (a) π-MOS_44_31 (b) π-MOS_44_41

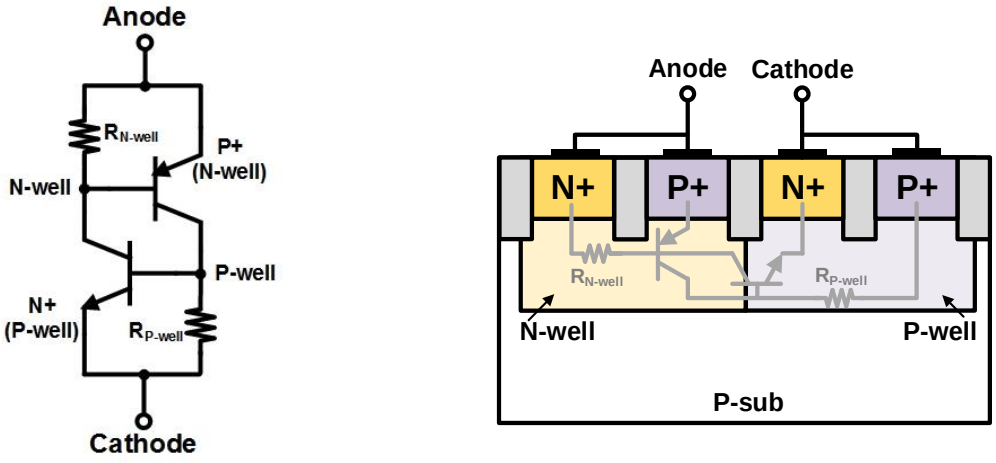


(a) (b)

Fig. 3.13. Layout top view of (a) π-MOS_72_31 (b) π-MOS_72_41

3.4 Proposed π-Model SCR (π-SCR)

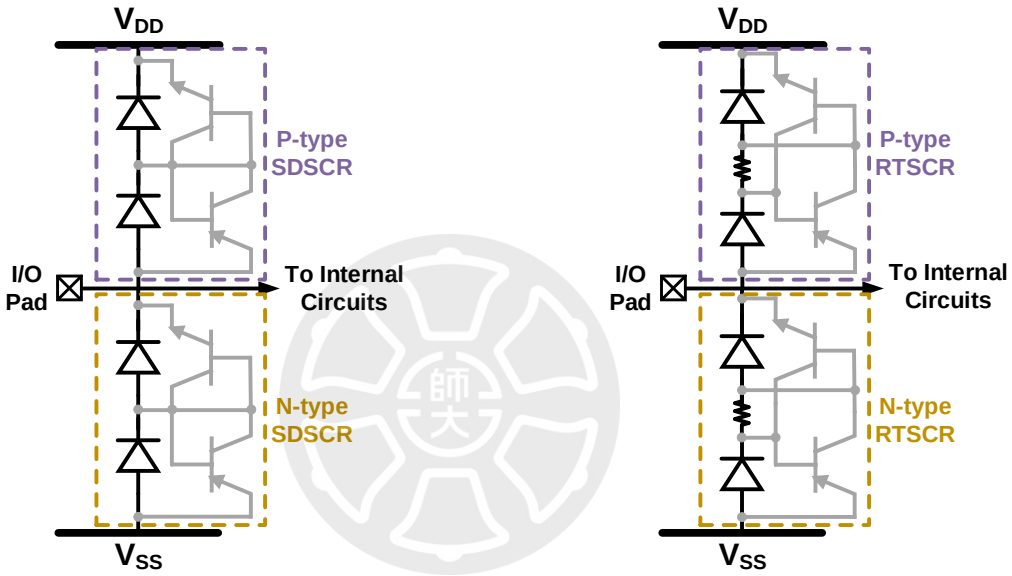
Silicon-controlled rectifier (SCR) is a four-layer semiconductor device which is composed of p-n-p-n (P+/N-well/P-well/N+) in CMOS technology. The equivalent circuit and the cross-sectional view of SCR is shown in Fig. 3.14. The P+/N-well/P-well formed the PNP, and the N-well/P-well/N+ formed the NPN inside SCR. The base of parasitic PNP is connected to the collector of parasitic NPN, and the base of parasitic NPN is connected to the collector of parasitic PNP. When SCR is fully conducted, it can discharge high current due to positive-feedback mechanism [26]. The voltage across SCR decreases rapidly during conduction. The snapback phenomenon of SCR reduces the power dissipation when ESD current flows. Therefore, SCR has high ESD robustness per unit layout area. Because of low clamping voltage, SCR cannot be turned off as internal circuit operates normally. The latch-up problems must be considered when ESD protection circuit is designed with SCR device.



(a) (b)

Fig. 3.14. (a) Equivalent circuit and (b) cross-sectional view of SCR.

The integrated circuits operated in high-speed applications are very sensitive to the parasitic capacitance. In order to effectively protect the high-speed circuit and reduce the parasitic effects, several low-C SCR protection device designs such as stacked diode with embedded SCR (SDSCR) and resistor-triggered SCR (RTSCR) have been presented. As shown as Fig. 3.15, SCR devices are widely used to protect high-speed circuit.

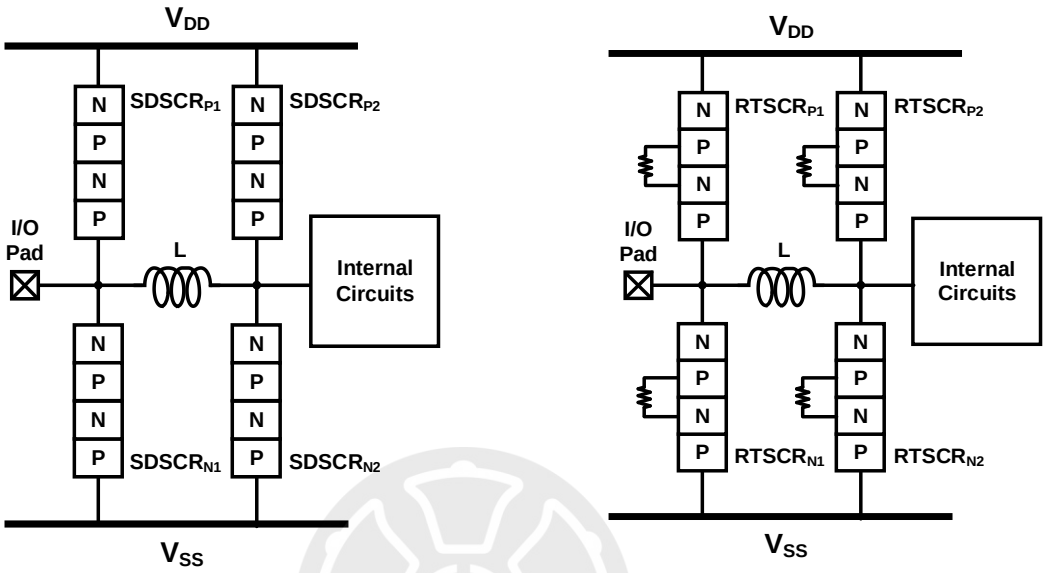


(a) (b)

Fig. 3.15. Equivalent circuit of (a) stacked diode with embedded SCR (SDSCR) (b) resistor-triggered SCR (RTSCR).

To further reduce the signal loss in high-speed applications, proposed π-model SCR (π-SCR) realizes SDSCR and RTSCR with two-section distributed circuit as shown in Fig. 3.16. By the use of matching inductor, the signal loss can be reduced. The octagonal spiral inductor is adopted as the matching element as shown in Fig. 3.17. The metal width of inductor is 6μm. The shape of the conversion between different layers is also octagonal in order not to reduce the cross-sectional area instantaneously. In addition,

three-layer metal (metal 3 to metal 5) is used together to increase the thickness. The structure of proposed matching inductor is shown in Fig. 3.18. In order to enhance the equivalent width, the SCR device can be realized in symmetrical structure.



(a) (b)

Fig. 3.16. Equivalent circuit of proposed (a) π-SDSCR and (b) π-RTSCR.

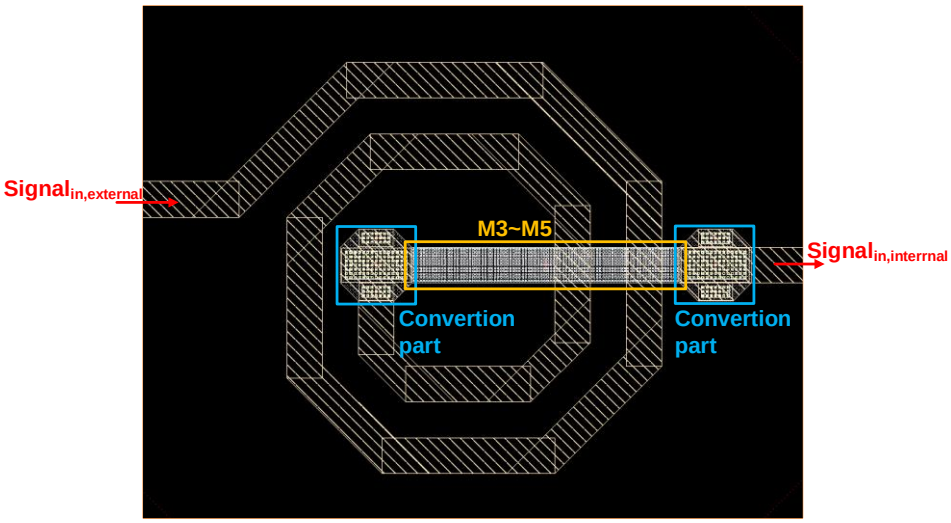


Fig. 3.17. The top view of matching inductor.

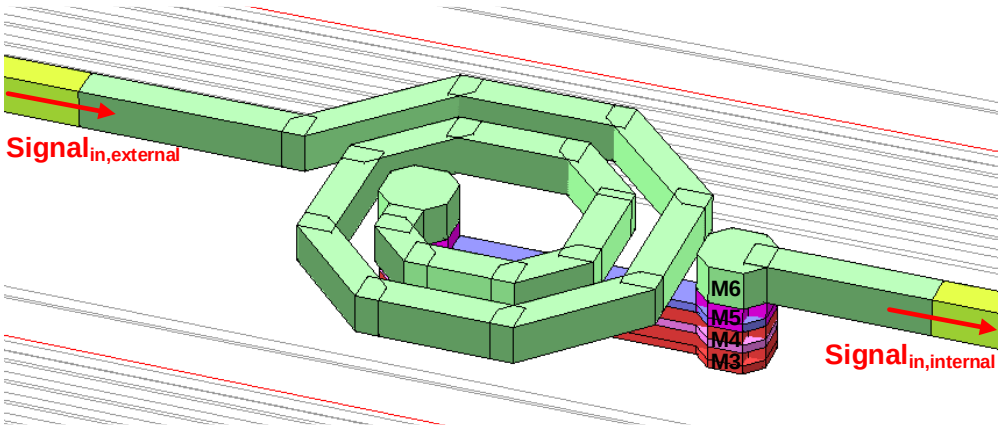
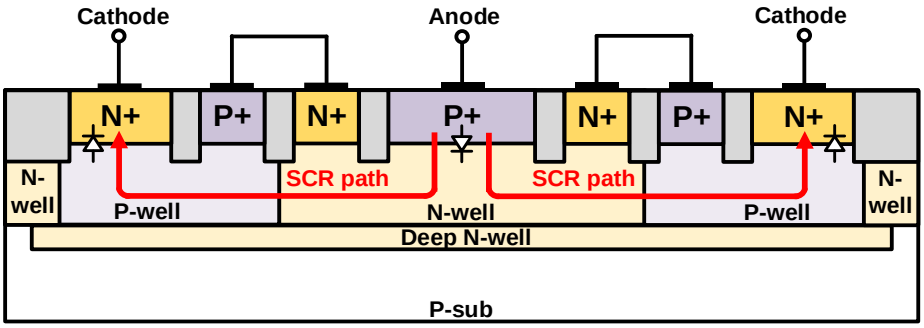


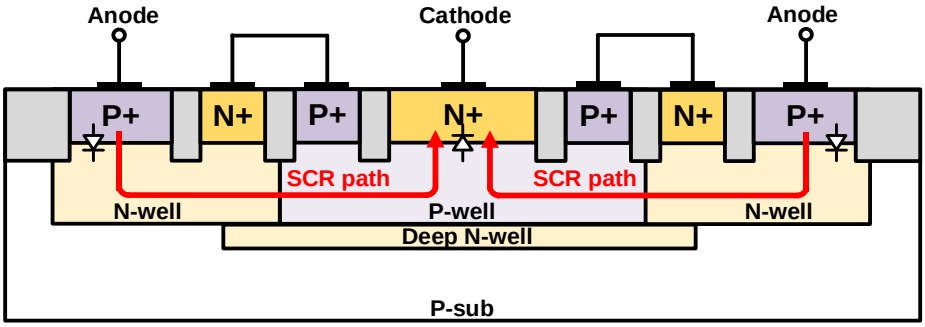
Fig. 3.18. The structure of matching inductor.

3.4.1 π-Model SDSCR (π-SDSCR)

In π-model SDSCR (π-SDSCR), stage 1 near the I/O pad is composed of SDSCRs placed from V_{SS} to I/O ($SDSCR_{N1}$) and from I/O to V_{DD} ($SDSCR_{P1}$), and stage 2 near the internal circuit is composed of SDSCRs placed from V_{SS} to I/O ($SDSCR_{N2}$) and from I/O to V_{DD} ($SDSCR_{P2}$). The cross-sectional view of SDSCR is shown as Fig. 3.19. The layout top view of symmetrical P-type and N-type SDSCR is shown in Fig.3.20. There is a matching inductor between two stages. As shown in Fig. 3.21, π-SDSCR is equipped with power-rail ESD clamp circuit to realize the whole-chip ESD protection.

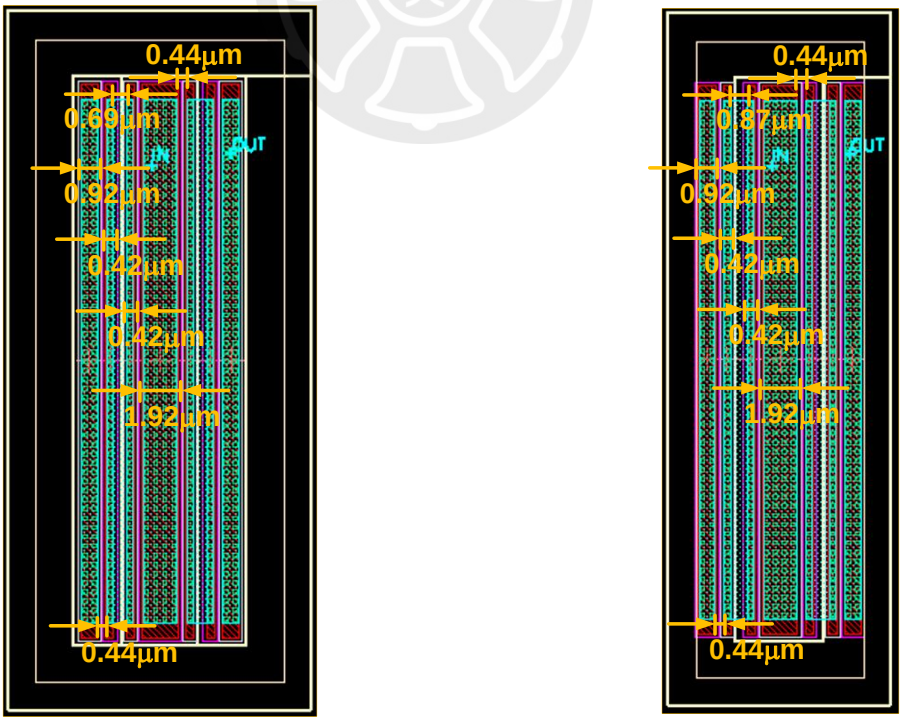


(a)



(b)

Fig. 3.19. Cross-sectional view of (a) P-type SDSCR and (b) N-type SDSCR.



(a) (b)

Fig. 3.20. Layout top view of symmetrical (a) P-type and (b) N-type SDSCR.

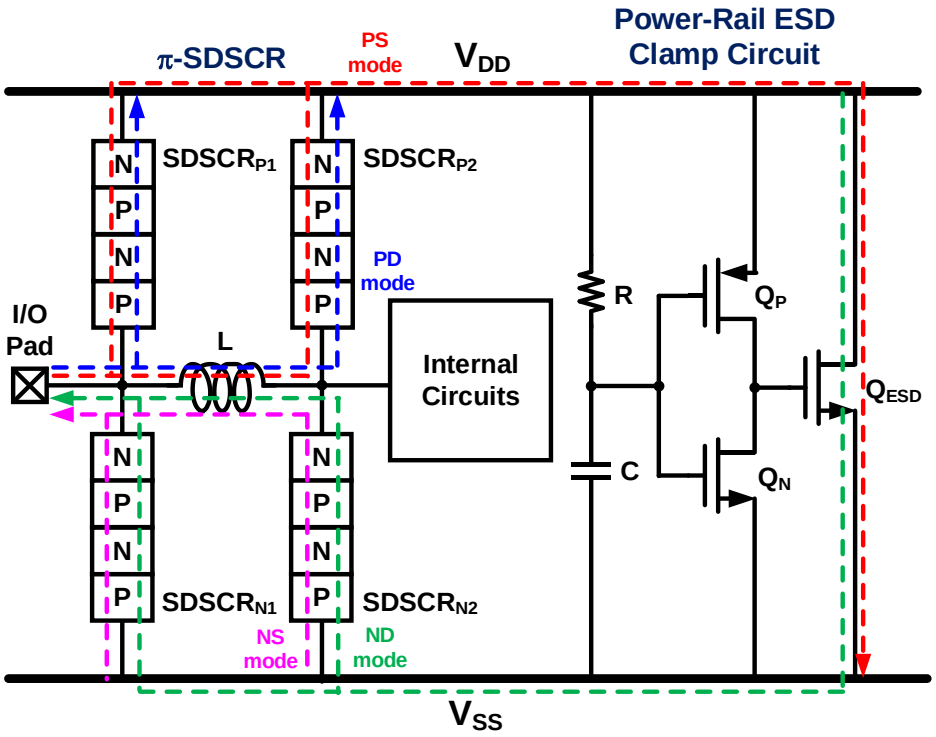


Fig. 3.21. Whole-chip ESD protection circuit with proposed π-SDSCR.

The ESD current under PD mode can be discharged by $SDSCR_{P1}$ and $SDSCR_{P2}$. The ESD current under NS mode is discharged by $SDSCR_{N1}$ and $SDSCR_{N2}$. The ESD current between V_{DD} and V_{SS} is discharged by the power-rail ESD clamp circuit. The ESD current under ND mode can be discharged by the power-rail ESD clamp circuit in series with $SDSCR_{N1}$ and $SDSCR_{N2}$. The ESD current under PS mode is discharged by $SDSCR_{P1}$ and $SDSCR_{P2}$ in series with the power-rail ESD clamp circuit.

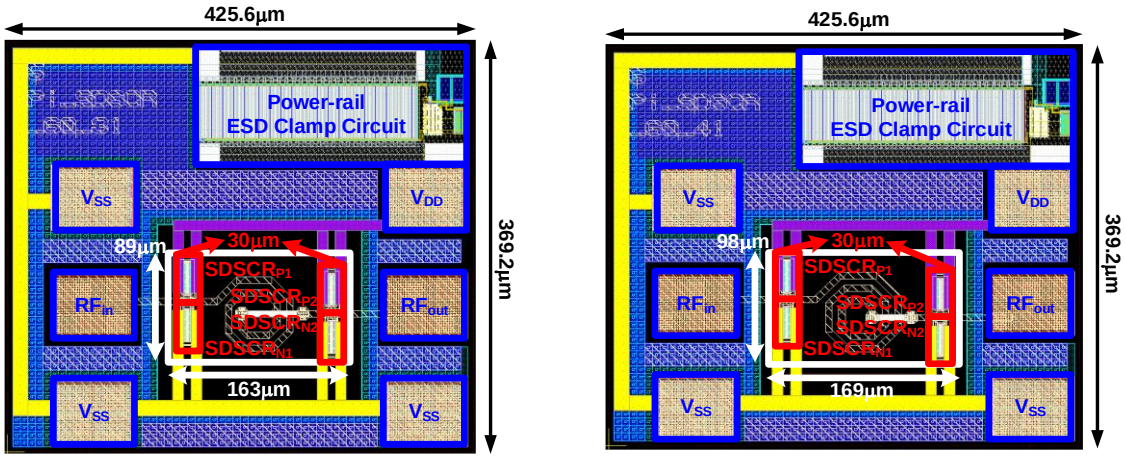
The matching element between stage 1 and stage 2 is realized with an octagonal spiral inductor. It resonates with parasitic capacitance of SDSCRs. The impact of protection device on high-frequency signal can be reduced.

The test devices of π-SDSCR are listed in Table 3.3. The proposed design is fabricated in 0.18μm CMOS process. The width of SDSCR used in π-SDSCR_60_31 and π-SDSCR_60_41 is 30μm in symmetrical structure, the matching inductor is 0.31nH and 0.41nH respectively as shown in Fig. 3.22. The width of SDSCR used in π-

SDSCR_100_31 and π-SDSCR_100_41 is 50μm in symmetrical structure, the matching inductor is 0.31nH and 0.41nH respectively as shown in Fig. 3.23. The area of each test device is 425.6* 369.2μm^2.

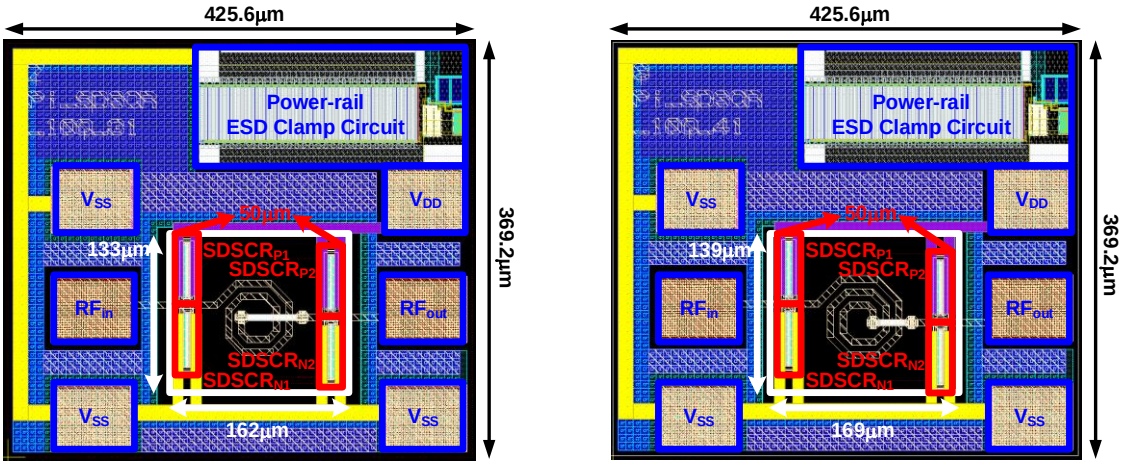
Table 3.3. The test cell of π-SDSCR

Cell Name	Stage 1		Stage 2		Inductor	
	Device	Width	Device	Width	Device	Inductance
π-SDSCR_60_31	$SDSCR_{P1}$	30μm	$SDSCR_{P2}$	30μm	L	0.31nH
	$SDSCR_{N1}$	30μm	$SDSCR_{N2}$	30μm		
π-SDSCR_60_41	$SDSCR_{P1}$	30μm	$SDSCR_{P2}$	30μm	L	0.41nH
	$SDSCR_{N1}$	30μm	$SDSCR_{N2}$	30μm		
π-SDSCR_100_31	$SDSCR_{P1}$	50μm	$SDSCR_{P2}$	50μm	L	0.31nH
	$SDSCR_{N1}$	50μm	$SDSCR_{N2}$	50μm		
π-SDSCR_100_41	$SDSCR_{P1}$	50μm	$SDSCR_{P2}$	50μm	L	0.41nH
	$SDSCR_{N1}$	50μm	$SDSCR_{N2}$	50μm		



(a) (b)

Fig. 3.22. Layout top view of (a) π-SDSCR_60_31 (b) π-SDSCR_60_41.

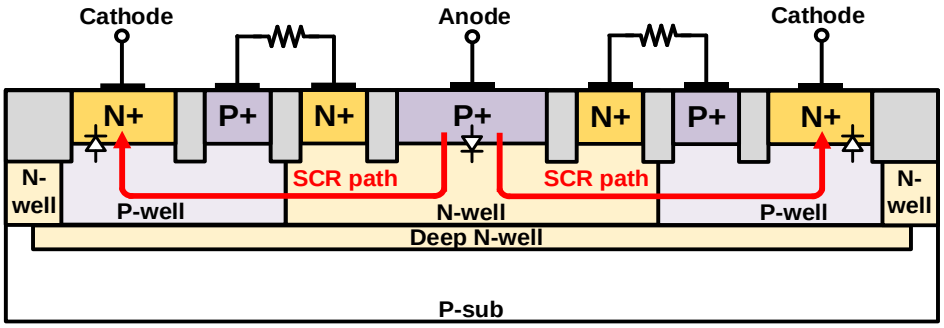


(a) (b)

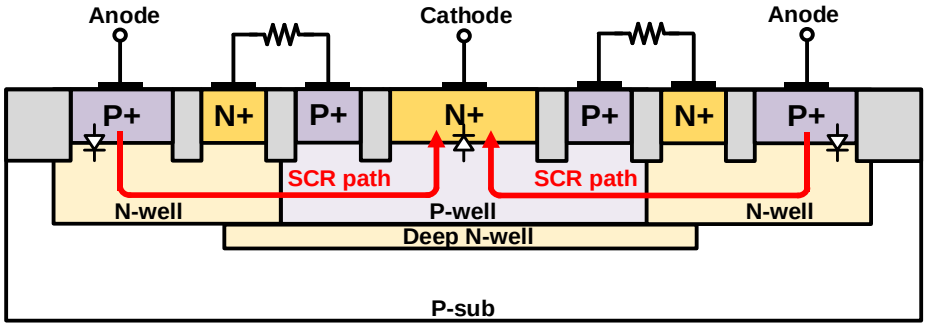
Fig. 3.23. Layout top view of (a) π-SDSCR_100_31 (b) π-SDSCR_100_41.

3.4.2 π-Model RTSCR (π-RTSCR)

In π-model RTSCR (π-RTSCR), stage 1 near the I/O pad is composed of RTSCRs placed from V_{SS} to I/O ($RTSCR_{N1}$) and from I/O to V_{DD} ($RTSCR_{P1}$), and stage 2 near the internal circuit is composed of RTSCRs placed from V_{SS} to I/O ($RTSCR_{N2}$) and from I/O to V_{DD} ($RTSCR_{P2}$). The cross-sectional view of SDSCR is shown as Fig. 3.24. The layout top view of symmetrical P-type and N-type RTSCR is shown in Fig. 3.25. There is a matching inductor between two stages. As shown in Fig. 3.26, π-RTSCR is equipped with power-rail ESD clamp circuit to realize the whole-chip ESD protection.

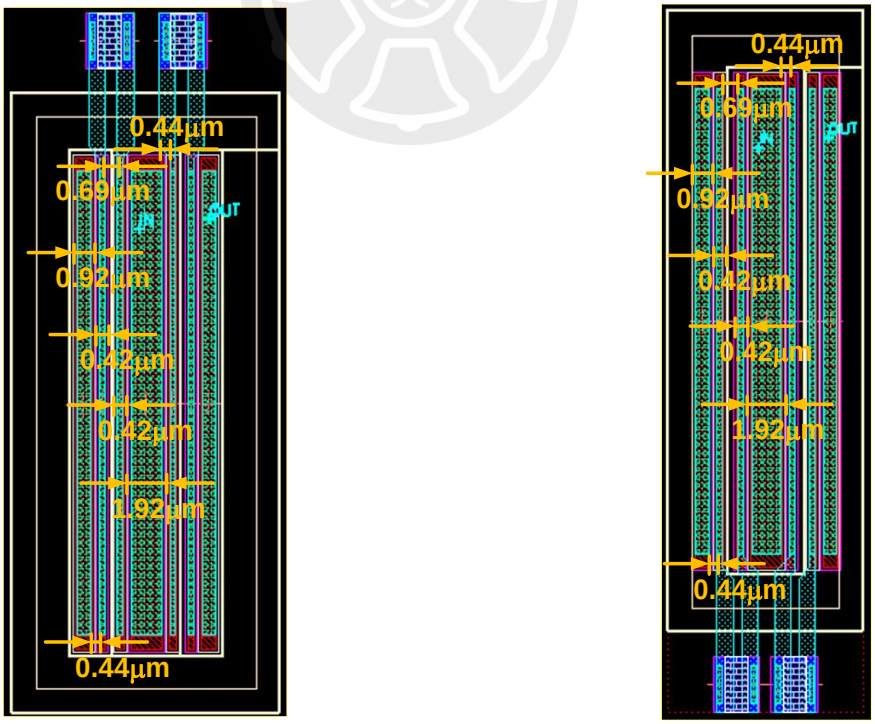


(a)



(b)

Fig. 3.24. Cross-sectional view of (a) P-type RTSCR and (b) N-type RTSCR.



(a) (b)

Fig. 3.25. Layout top view of symmetrical (a) P-type and (b) N-type RTSCR.

The ESD current under PD mode can be discharged by $RTSCR_{P1}$ and $RTSCR_{P2}$. The ESD current under NS mode is discharged by $RTSCR_{N1}$ and $RTSCR_{N2}$. The ESD current between V_{DD} and V_{SS} is discharged by the power-rail ESD clamp circuit. The ESD current under ND mode can be discharged by the power-rail ESD clamp circuit in series with $RTSCR_{N1}$ and $RTSCR_{N2}$. The ESD current under PS mode is discharged by $RTSCR_{P1}$ and $RTSCR_{P2}$ in series with the power-rail ESD clamp circuit.

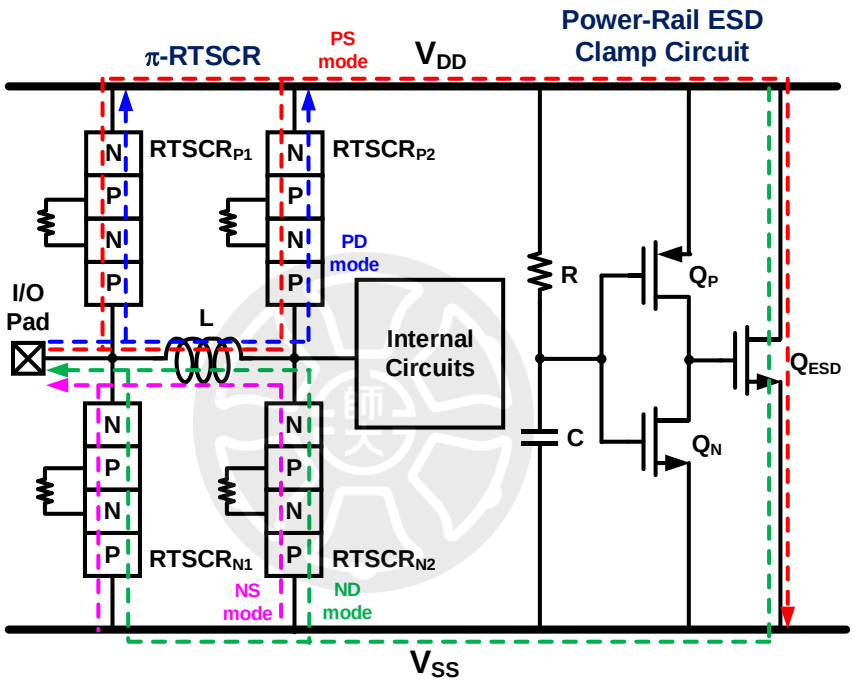


Fig. 3.26. Whole-chip ESD protection circuit with proposed π-RTSCR.

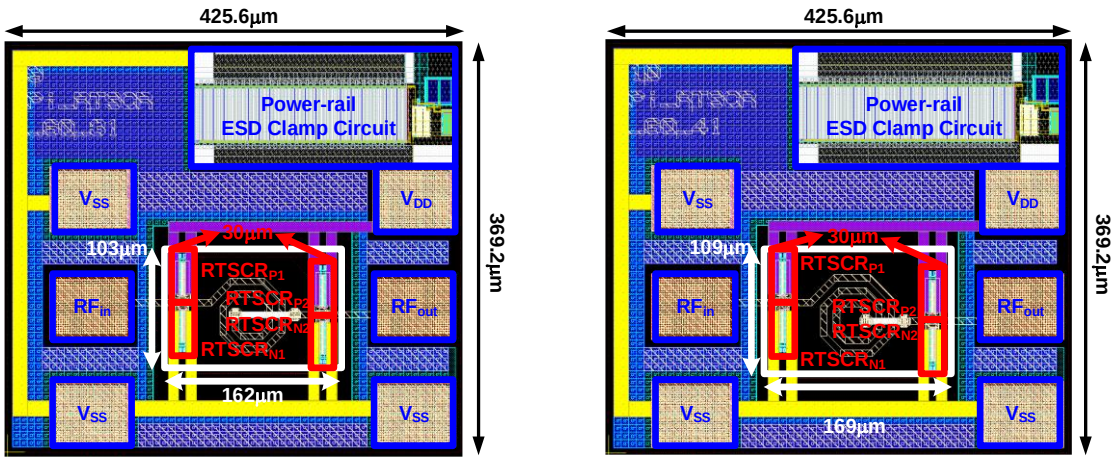
The matching element between stage 1 and stage 2 is realized with an octagonal spiral inductor. It resonates with parasitic capacitance of RTSCRs. The impact of protection device on high-frequency signal can be reduced.

The test devices of π-RTSCR are listed in Table 3.4. The proposed design is fabricated in 0.18μm CMOS process. The width of RTSCR used in π-RTSCR_60_31 and π-RTSCR_60_41 is 30μm in symmetrical structure, the matching inductor is 0.31nH and 0.41nH respectively as shown in Fig. 3.27. The width of RTSCR used in π-

RTSCR_100_31 and π-RTSCR_100_41 is 50μm in symmetrical structure, the matching inductor is 0.31nH and 0.41nH respectively as shown in Fig. 3.28. The area of each test device is 425.6* 369.2μm^2.

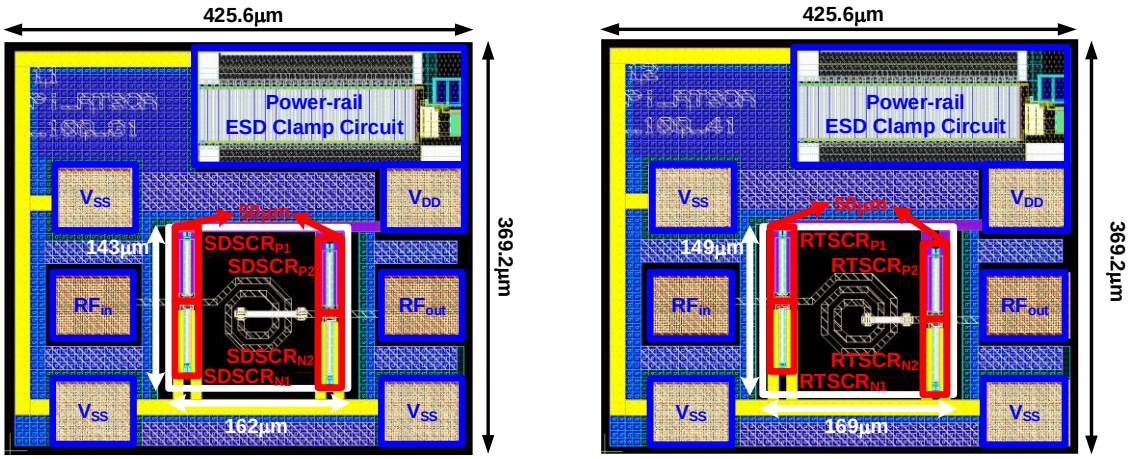
Table 3.4. The test cell of π-RTSCR

Cell Name	Stage 1		Stage 2		Inductor	
	Device	Width	Device	Width	Device	Inductance
π-RTSCR_60_31	$RTSCR_{P1}$	30μm	$RTSCR_{P1}$	30μm	L	0.31nH
	$RTSCR_{N1}$	30μm	$RTSCR_{N1}$	30μm		
π-RTSCR_60_41	$RTSCR_{P1}$	30μm	$RTSCR_{P1}$	30μm	L	0.41nH
	$RTSCR_{N1}$	30μm	$RTSCR_{N1}$	30μm		
π-RTSCR_100_31	$RTSCR_{P1}$	50μm	$RTSCR_{P1}$	50μm	L	0.31nH
	$RTSCR_{N1}$	50μm	$RTSCR_{N1}$	50μm		
π-RTSCR_100_41	$RTSCR_{P1}$	50μm	$RTSCR_{P1}$	50μm	L	0.41nH
	$RTSCR_{N1}$	50μm	$RTSCR_{N1}$	50μm		



(a) (b)

Fig. 3.27. Layout top view of (a) π-RTSCR_60_31 (b) π-RTSCR_60_41.



(a) (b)

Fig. 3.28. Layout top view of (a) π-RTSCR_100_31 (b) π-RTSCR_100_41.

3.5 Simulation Results

The high-frequency performance of traditional π-diode, π-MOS, proposed π-SDSCR and π-RTSCR are evaluated by S-parameter. By examining S_{21} and S_{11}, the impact of proposed ESD protection device on high-frequency applications is found out.

Larger S_{21} means that the signal is passed to another terminal with less loss. Smaller S_{11} means that the signal is delivered with less reflection. The proposed ESD protection device is designed to keep the S_{21} approach to 0 and make the S_{11} as smaller as possible.

Advanced design system (ADS) is used to simulate the S-parameter of all the protection device. The matching inductor is simulated with SONNET electromagnetic (EM) software. The simulation results of proposed design are compared with that of traditional design in similar parasitic capacitance.

Simulated S-parameter of π-diode_30_31 is compared with that of π-MOS_44_31, π-SDSCR_60_31 and π-RTSCR_60_31 in Fig. 3.29. Simulated S-parameter of π-diode_30_41 is compared with π-MOS_44_41, π-SDSCR_60_41 and π-RTSCR_60_41

in Fig. 3.30. Simulated S-parameter of π-diode_50_31 is compared with that of π-MOS_72_31, π-MOS_200_31, π-SDSCR_100_31 and π-RTSCR_100_31 in Fig. 3.31. Simulated S-parameter of π-diode_50_41 is compared with that of π-MOS_72_41, π-SDSCR_100_41 and π-RTSCR_100_41 in Fig. 3.32. Simulated S-parameter at 10GHz is listed in Table 3.5.

There are two different sizes in each test devices. The parasitic capacitance of π-diode with 30μm width, π-MOS with 44μm width, π-SDSCR with 60μm width and π-RTSCR with 60μm width are similar. The parasitic capacitance of π-diode with 50μm width, π-MOS with 72μm width, π-SDSCR with 100μm width and π-RTSCR with 100μm width are similar. Therefore, test devices with similar parasitic capacitance use the same matching inductor to connect between two stages. From the simulation results, there is little difference between traditional device and proposed design. In addition, the S_{21} of all the smaller test cells at 20GHz is higher than -3dB.

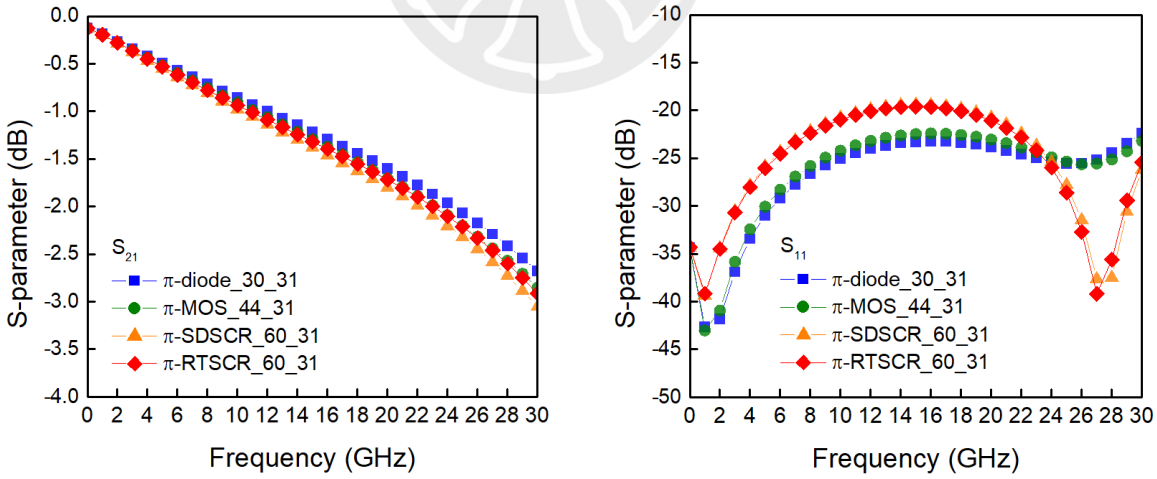


Fig. 3.29. The simulated S-parameter of π-diode_30_31, π-MOS_44_31, π-SDSCR_60_31 and π-RTSCR_60_31.

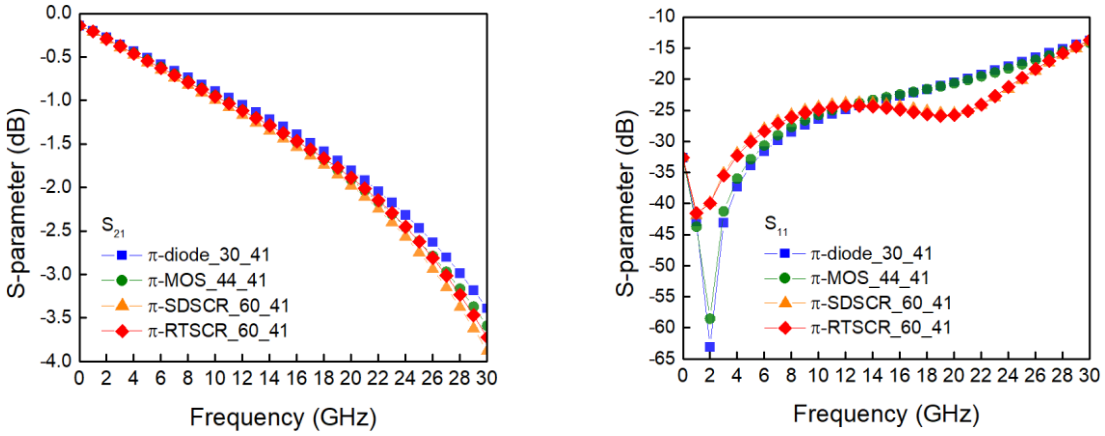


Fig. 3.30. The simulated S-parameter of π-diode_30_41, π-MOS_44_41, π-SDSCR_60_41 and π-RTSCR_60_41.

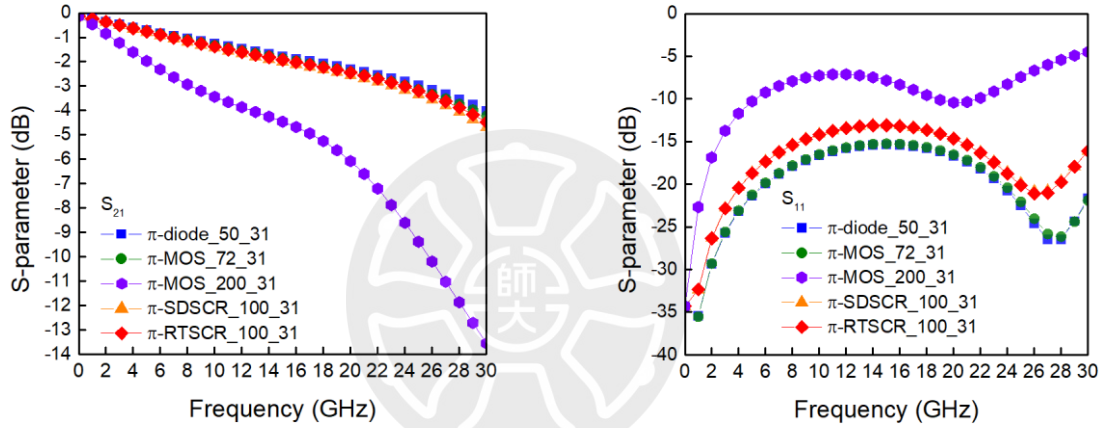


Fig. 3.31. The simulated S-parameter of π-diode_50_31, π-MOS_72_31, π-MOS_200_31, π-SDSCR_100_31 and π-RTSCR_100_31.

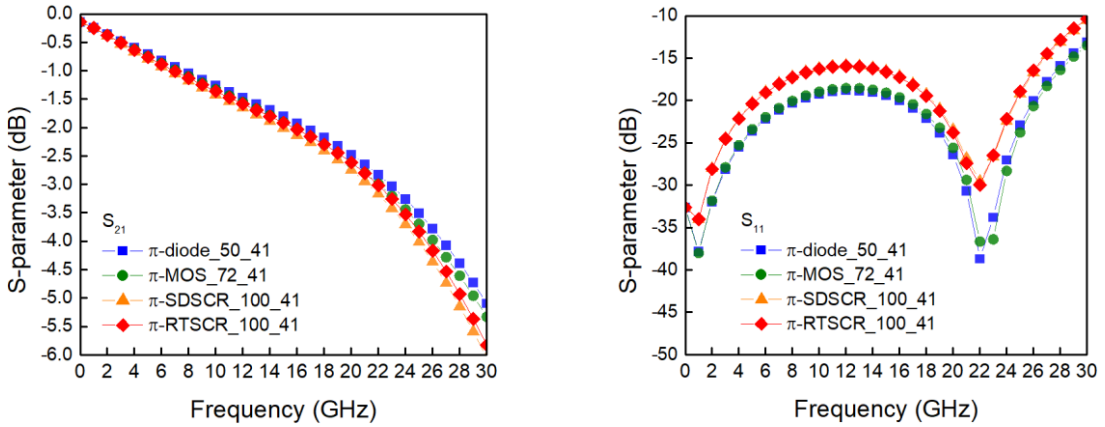


Fig. 3.32. The simulated S-parameter of π-diode_50_41, π-MOS_72_41, π-SDSCR_100_41 and π-RTSCR_100_41.

Table 3.5. Simulated S-parameter at 20GHz

Cell Name	S_{21} (dB) at 20GHz	S_{11} (dB) at 20GHz
π-diode_30_31	-1.60	-23.85
π-diode_30_41	-1.80	-26.41
π-diode_50_41	-2.29	-16.68
π-diode_50_41	-2.47	-19.22
π-MOS_44_31	-1.70	-23.05
π-MOS_44_41	-1.91	-25.75
π-MOS_72_41	-2.41	-16.52
π-MOS_72_41	-2.61	-18.98
π-MOS_200_31	-6.08	-10.43
π-SDSCR_60_31	-1.80	-20.73
π-SDSCR_60_41	-1.98	-24.40
π-SDSCR_100_41	-2.45	-14.66
π-SDSCR_100_41	-2.75	-16.17
π-RTSCR_60_31	-1.72	-21.06
π-RTSCR_60_41	-1.89	-24.90
π-RTSCR_100_41	-2.45	-10.43
π-RTSCR_100_41	-2.61	-16.29

3.6 Measurement Results

All the test devices are fabricated in 0.18μm CMOS process. The chip photograph is shown in Fig. 3.33. The width is 1296.8μm, and the length is 2265.2μm. There are four kinds of ESD protection devices, π-diode, π-MOS, π-SDSCR, and π-RTSCR in different size. The measurement results are introduced in following section.

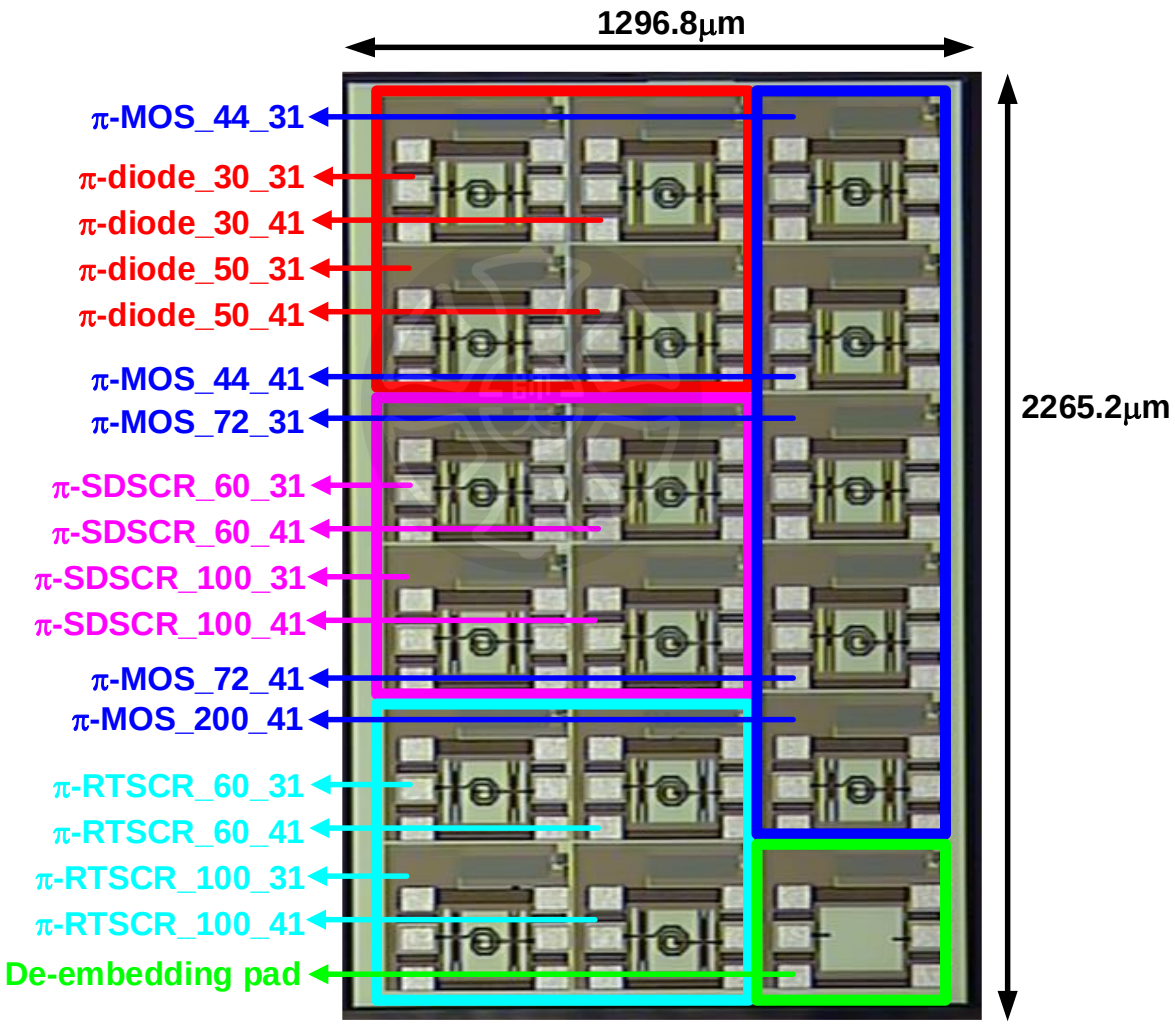


Fig. 3.33. The chip photograph of test device.

3.6.1 High-Frequency Performance

As shown in Fig. 3.34, the S-parameter is measured by 67GHz RFIC parameter measurement system with 2-port GSG probes [27]. However, the effect of pad is included in measured S-parameter. The S-parameter of de-embedding pad is measured at first as a reference in Fig. 3.35 (a). Then the S-parameter of the test device is measured in Fig. 3.35 (b). The de-embedding technique is used to remove the effects of pad to extract the real characteristics of devices [28]. After the de-embedding technique is applied, the measured results are shown as follows.

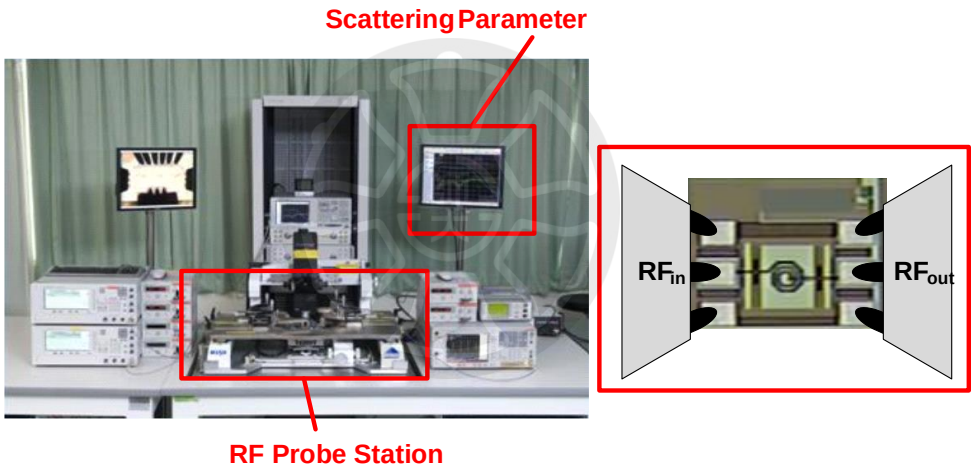


Fig. 3.34. The setup of high-frequency measurement system. [27]

(a) (b)

Fig. 3.35. The photograph of (a) de-embedding pad and (b) test device.

Measured S-parameter of π-diode_30_31 is compared with that of π-MOS_44_31, π-SDSCR_60_31 and π-RTSCR_60_31 in Fig. 3.36. Measured S-parameter of π-diode_30_41 is compared with that of π-MOS_44_41, π-SDSCR_60_41 and π-RTSCR_60_41 in Fig. 3.37. Measured S-parameter of π-diode_50_31 is compared with that of π-MOS_72_31, π-MOS_200_31, π-SDSCR_100_31 and π-RTSCR_100_31 in Fig. 3.38. Measured S-parameter of π-diode_50_41 is compared with that of π-MOS_72_41, π-SDSCR_100_41 and π-RTSCR_100_41 in Fig. 3.39. Measured S-parameters at 20GHz are listed in Table 3.6.

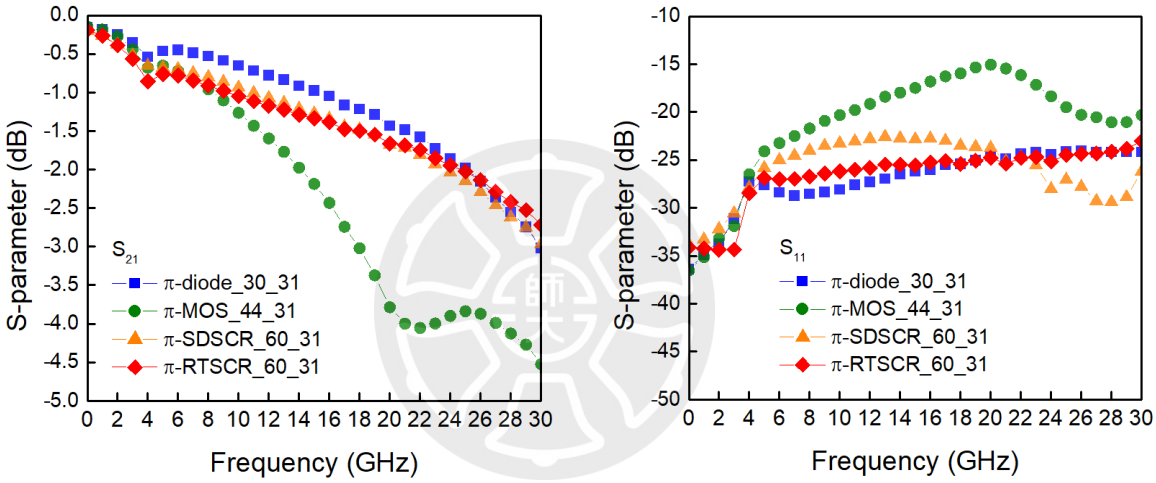


Fig. 3.36. The measured S-parameter of π-diode_30_31, π-MOS_44_31, π-SDSCR_60_31 and π-RTSCR_60_31.

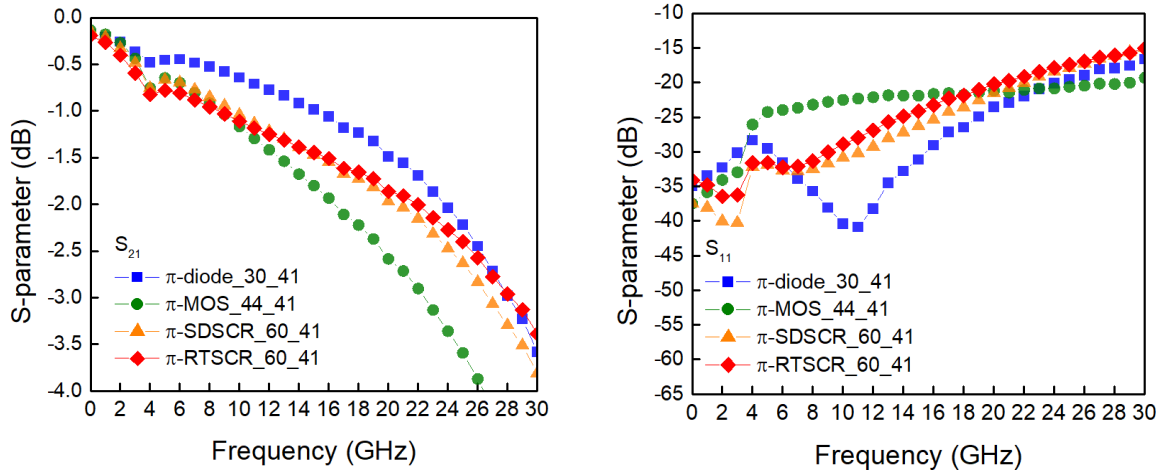


Fig. 3.37. The measured S-parameter of π-diode_30_41, π-MOS_44_41, π-SDSCR_60_41 and π-RTSCR_60_41.

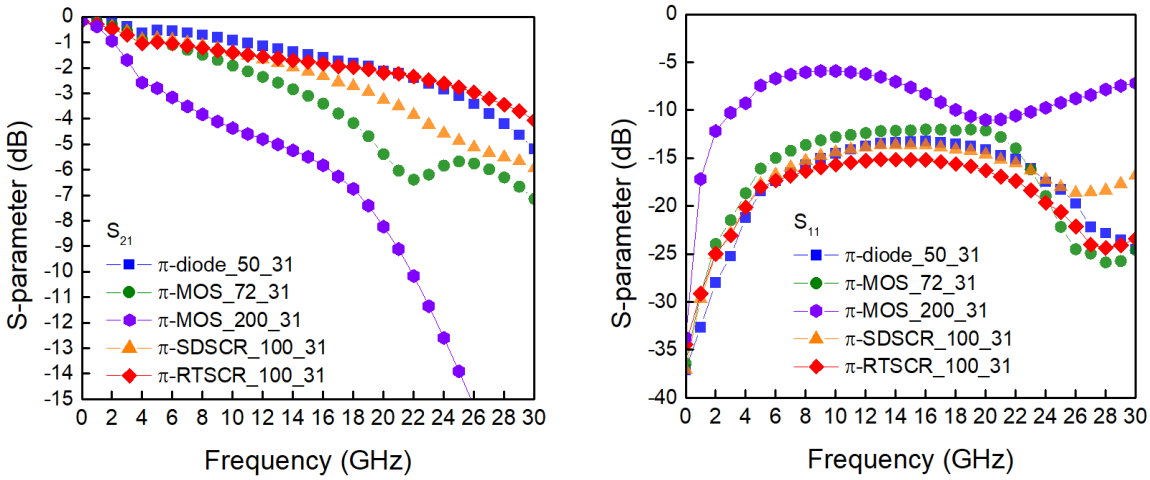


Fig. 3.38. The measured S-parameter of π-diode_50_31, π-MOS_72_31, π-MOS_200_31, π-SDSCR_100_31 and π-RTSCR_100_31.

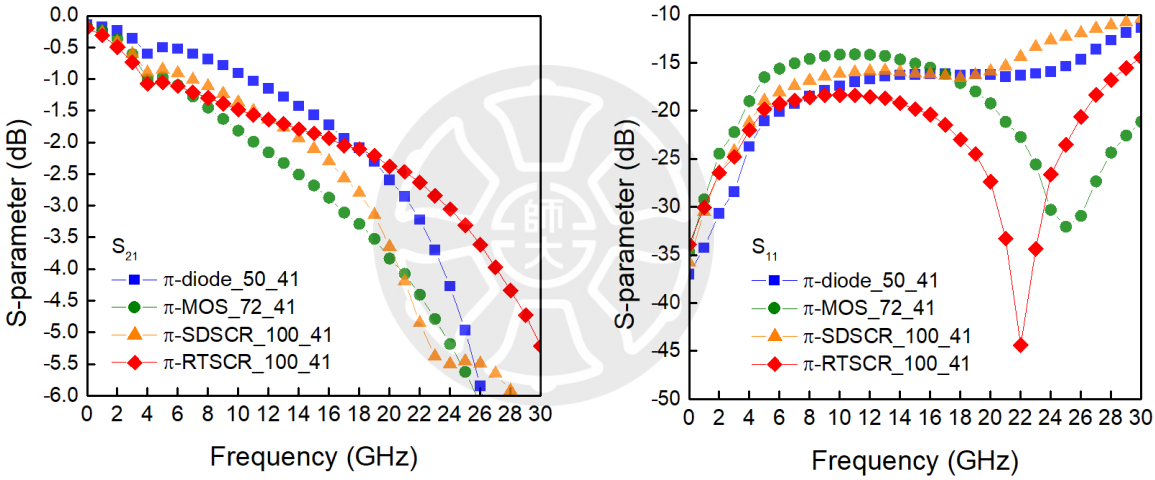


Fig. 3.39. The measured S-parameter of π-diode_50_41, π-MOS_72_41, π-SDSCR_100_41 and π-RTSCR_100_41.

Table 3.6. Measured S-parameter at 20GHz

Cell Name	S_{21} (dB) at 20GHz	S_{11} (dB) at 20GHz
π-diode_30_31	-1.43	-24.6
π-diode_30_41	-1.58	-21.4
π-diode_50_31	-2.13	-14.1
π-diode_50_41	-2.59	-16.2
π-MOS_44_31	-3.79	-15.0
π-MOS_44_41	-2.58	-21.1
π-MOS_72_31	-5.39	-12.1
π-MOS_72_41	-3.83	-19.2
π-MOS_200_31	-8.24	-11.0
π-SDSCR_60_31	-1.68	-23.7
π-SDSCR_60_41	-1.97	-21.5
π-SDSCR_100_31	-3.27	-14.6
π-SDSCR_100_41	-3.64	-15.8
π-RTSCR_60_31	-1.66	-24.7
π-RTSCR_60_41	-1.86	-20.1
π-RTSCR_100_31	-2.20	-16.3
π-RTSCR_100_41	-2.38	-27.4

3.6.2 TLP I-V Curves

The characteristics of ESD protection devices are obtained by the transmission-line-pulsing (TLP) system. TLP systems generates high-energy pulse to simulate the current of ESD events. A set of voltage and current value is recorded for one pulse. All

of the data form the TLP I-V curves [29]. TLP system used in this work is shown in Fig. 3.40. [30]

Trigger voltage (V_{t1}), holding voltage (V_h), turn-on resistance (R_{on}), and the secondary breakdown current (I_{t2}) can be observed from TLP I-V curves. The criterion to determine the failure of device in TLP measurement is that the leakage current changes by 30%. The devices are measured under PS mode, PD mode, NS mode, and ND mode respectively. The It_2 of all the test devices are recorded in Table 3.7. The TLP I-V curves are also normalized by insertion loss (S_{21}) at 20GHz to tell the difference. The $It_2/|S_{21}|$of all the test devices are recorded in Table 3.8.

Fig. 3.40. Transmission-line pulsing (TLP) system. [30]

(1) Power-Rail ESD Clamp Circuit

The power-rail ESD clamp circuit provides ESD current path between V_{DD} and V_{SS}. It is composed by an RC inverter as a trigger circuit and a NMOS as a discharging device. The length and width of the NMOS are 0.36 μm and 50μm respectively, and the multiple is 60.

During normal operation, the supply voltage rises in several microseconds. The capacitor of RC inverter has enough time to be charged to a high level. Through the inverter, the voltage level of the gate of the NMOS is low and the channel of NMOS will keep off. When ESD stress hitting, the channel of NMOS is turned on by the RC inverter circuit. The parasitic NPN is triggered and turns on to discharge the ESD current from V_{DD} to V_{SS}. The parasitic diode inside NMOS also provides the ESD current path from V_{SS} to V_{DD}.

As shown in Fig.3.41, the TLP I-V curves of power-rail ESD clamp circuit of test cells are measured. From V_{DD} to V_{SS}, the power-rail ESD clamp circuit is triggered at 1.9V, and the I_{t2} is 8.9A. From V_{SS} to V_{DD}, the power-rail ESD clamp circuit is triggered at 0.6V, and the I_{t2} is 9.7A.

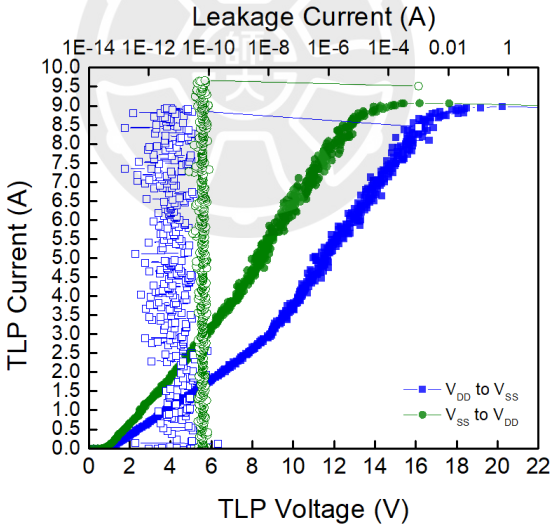


Fig. 3.41. TLP I-V curves of power-rail ESD clamp circuit

(2) PD Mode

The test circuit discharges ESD current of PD mode through the devices placed from I/O pad to V_{DD}. The TLP I-V curve of π-diode_30_31 is compared with that of π-MOS_44_31, π-SDSCR_60_31 and π-RTSCR_60_31 in Fig. 3.42 (a). The TLP I-V

curve of π-diode_30_41 is compared with that of π-MOS_44_41, π-SDSCR_60_41 and π-RTSCR_60_41 in Fig. 3.42 (b). The TLP I-V curve of π-diode_50_31 is compared with that of π-MOS_72_31, π-MOS_200_31, π-SDSCR_100_31 and π-RTSCR_100_31 in Fig. 3.42 (c). The TLP I-V curve of π-diode_50_41 is compared with that of π-MOS_72_41, π-SDSCR_100_41 and π-RTSCR_100_41 in Fig. 3.42 (d). The TLP I-V curves after normalized by insertion loss (S_{21}) at 20GHz are shown in Fig. 3.43.

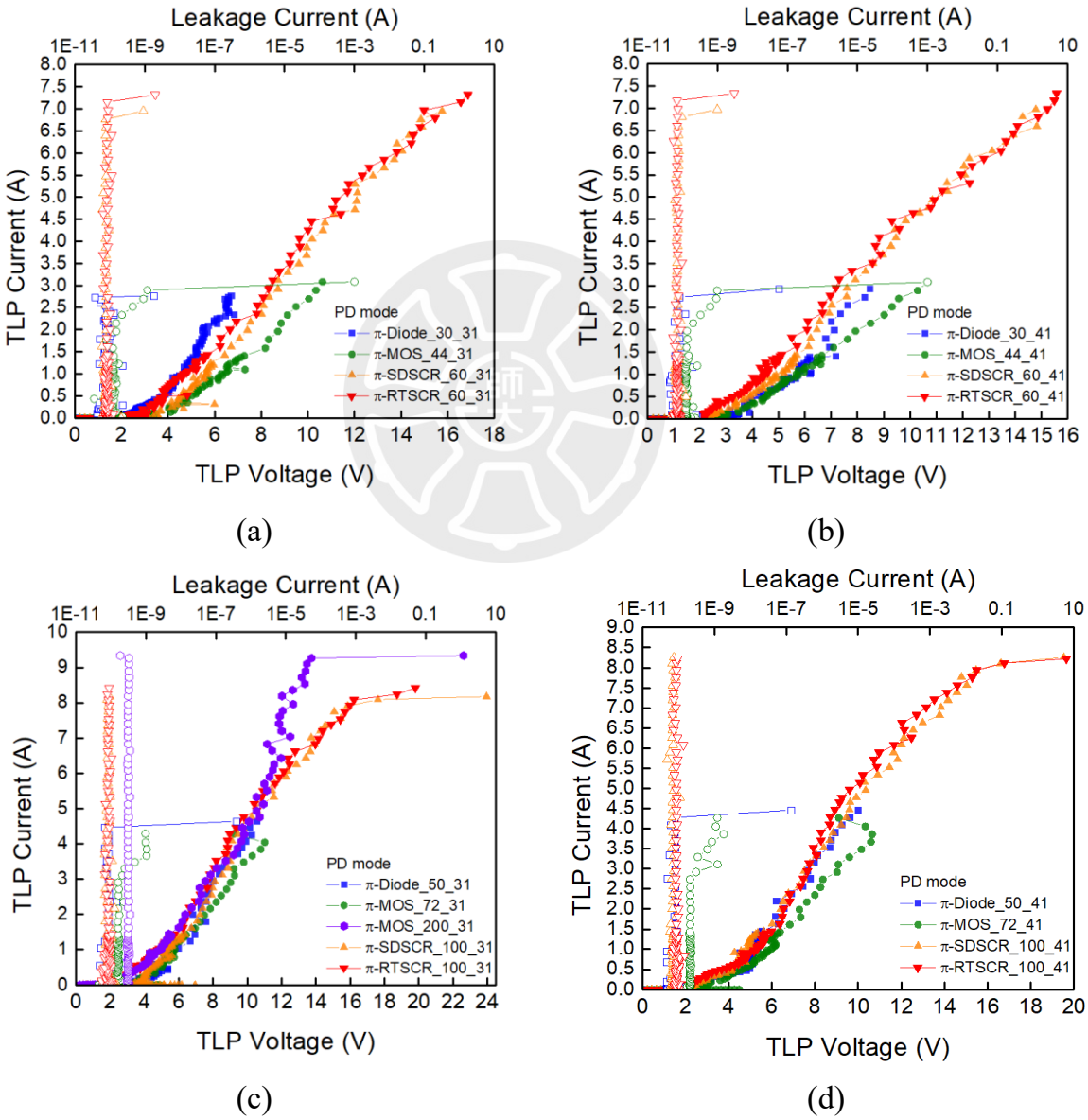


Fig. 3.42. TLP I-V curves of test devices under PD mode

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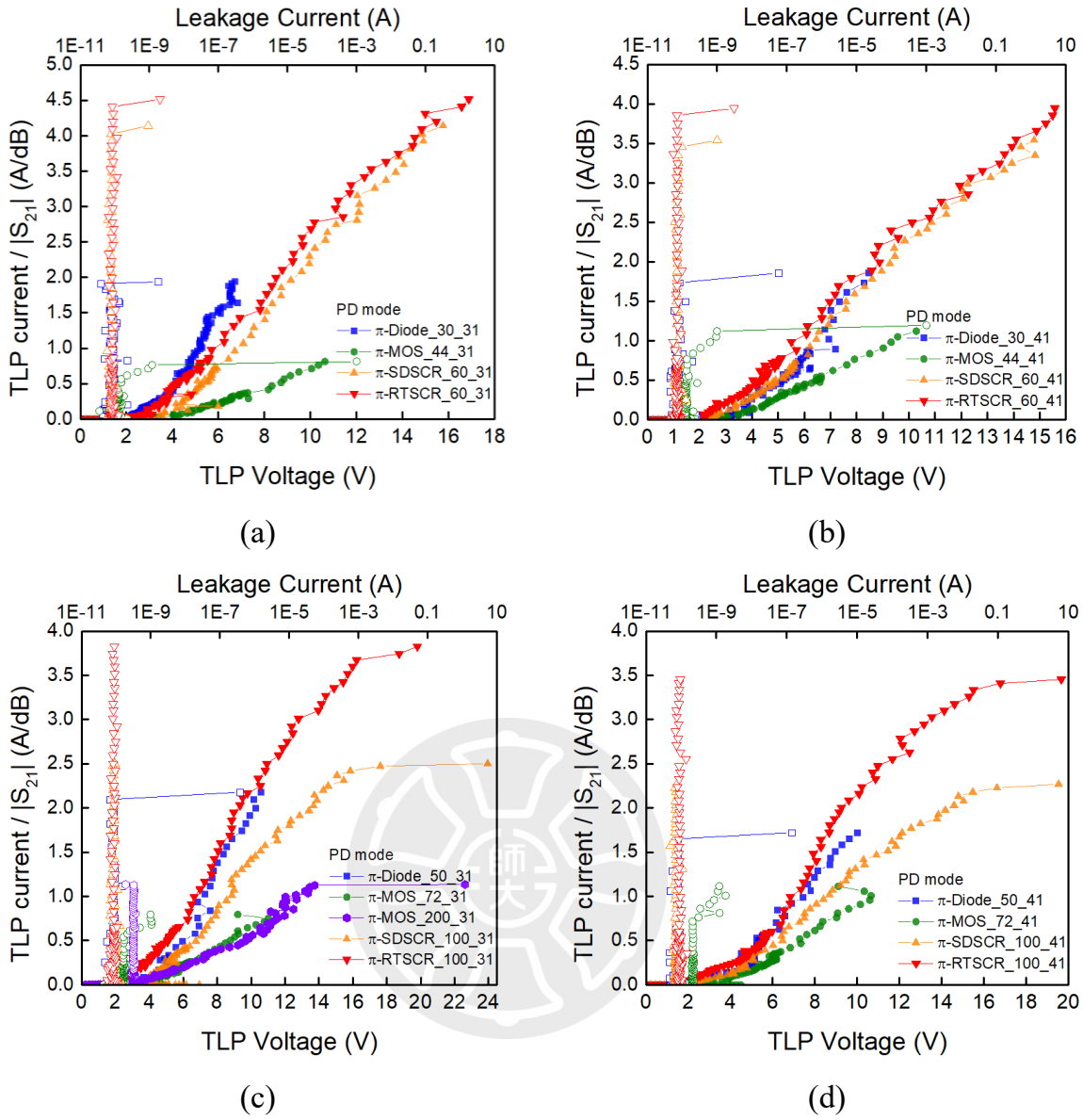


Fig. 3.43. TLP I-V curves of test devices under PD mode after normalized by insertion loss at 20GHz.

(3) PS Mode

The test circuit discharges ESD current of PS mode through the devices placed from I/O pad to V_{DD} in series with the power-rail ESD clamp circuit. The TLP I-V curve of π-diode_30_31 is compared with that of π-MOS_44_31, π-SDSCR_60_31 and π-RTSCR_60_31 in Fig. 3.44 (a). The TLP I-V curve of π-diode_30_41 is compared with that of π-MOS_44_41, π-SDSCR_60_41 and π-RTSCR_60_41 in Fig. 3.44 (b). The

TLP I-V curve of π-diode_50_31 is compared with that of π-MOS_72_31, π-MOS_200_31, π-SDSCR_100_31 and π-RTSCR_100_31 in Fig. 3.44 (c). The TLP I-V curve of π-diode_50_41 is compared with that of π-MOS_72_41, π-SDSCR_100_41 and π-RTSCR_100_41 in Fig. 3.44 (d). The TLP I-V curves after normalized by insertion loss (S_{21}) at 20GHz are shown in Fig. 3.45.

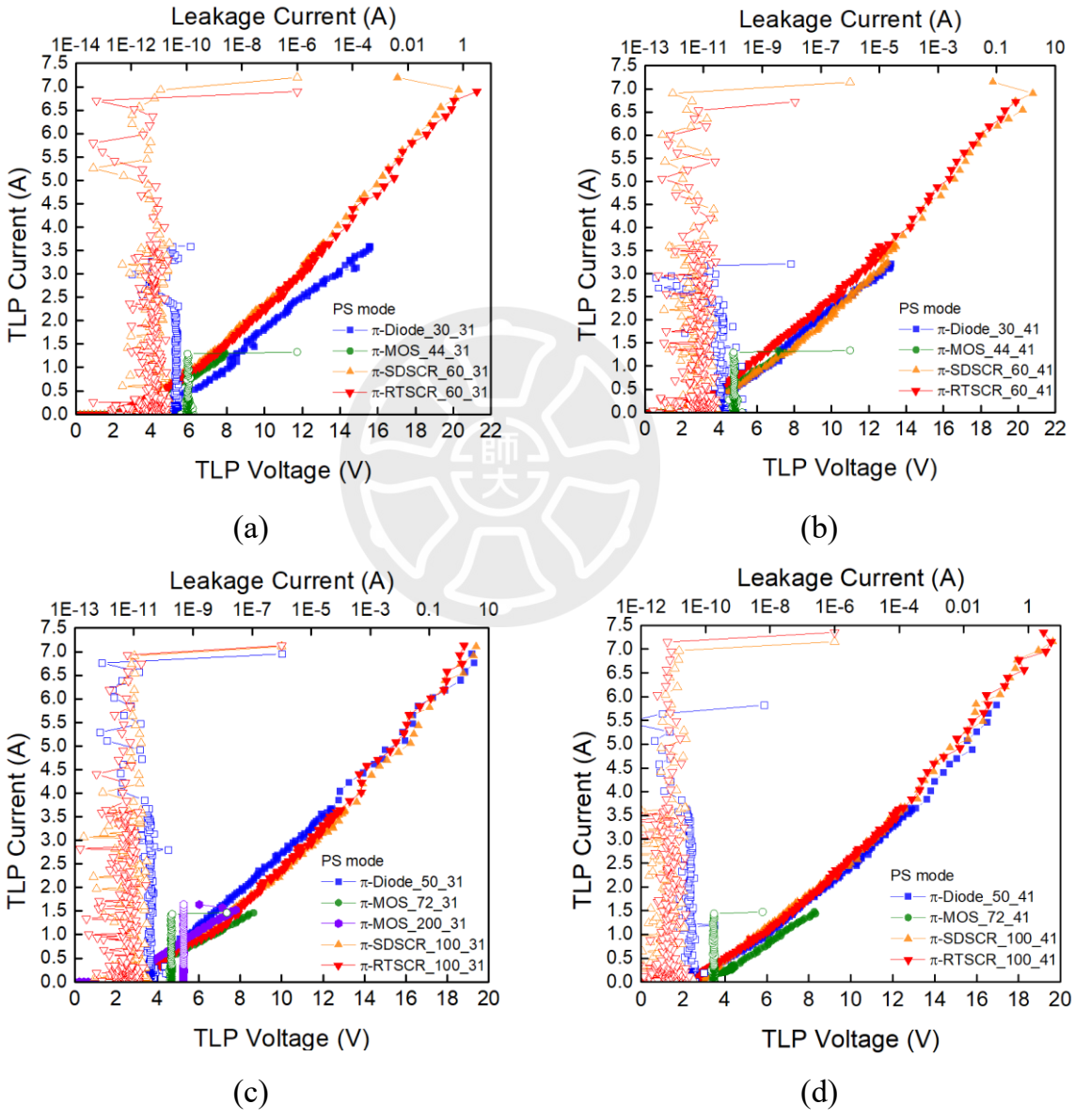


Fig. 3.44. TLP I-V curves of test devices under PS mode.

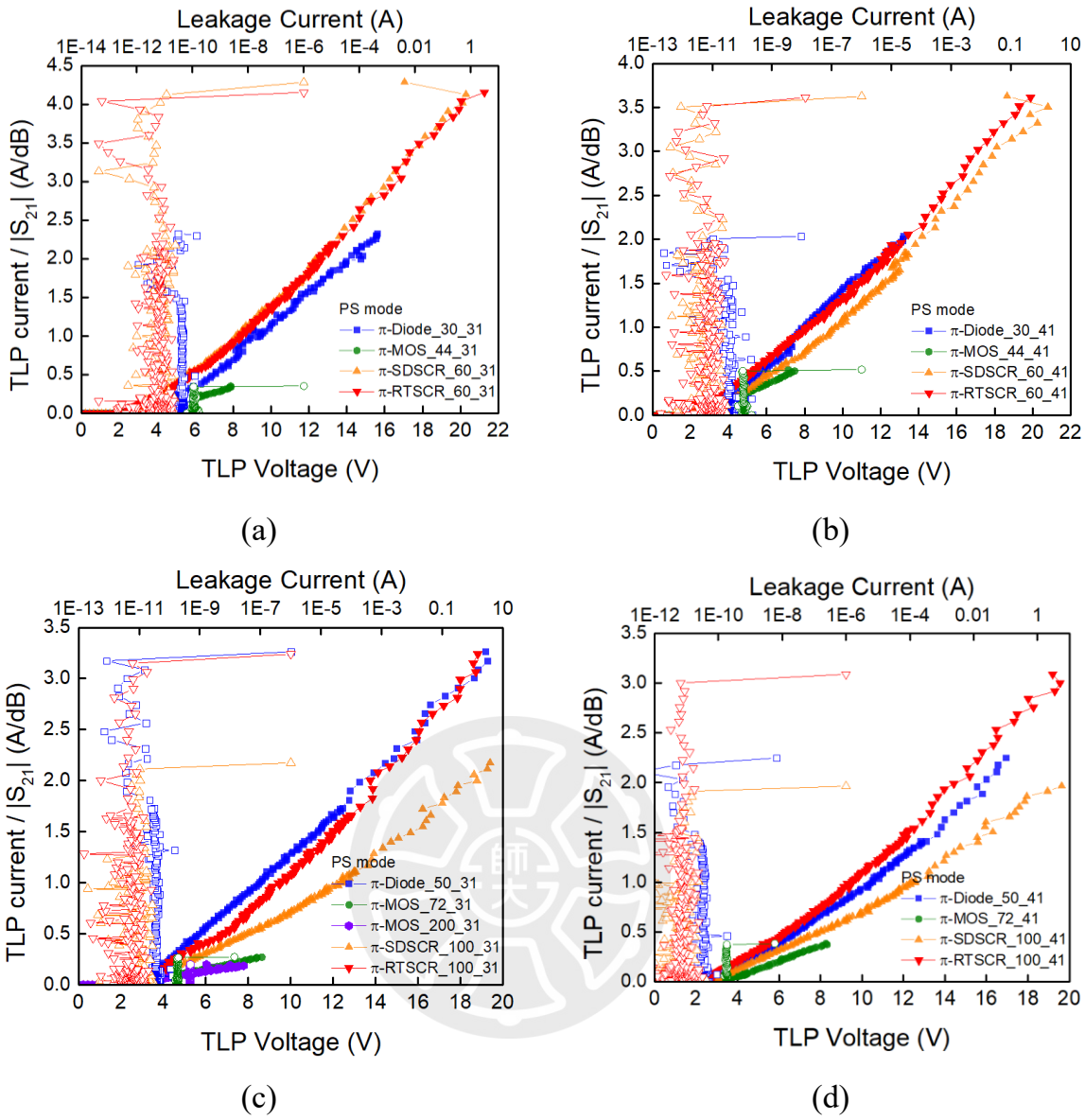


Fig. 3.45. TLP I-V curves of test devices under PS mode after normalized by insertion loss at 20GHz.

(4) ND Mode

The test circuit discharges ESD current under ND mode through the power-rail ESD clamp circuit and devices placed from V_{SS} to I/O pad. The TLP I-V curve of π-diode_30_31 is compared with that of π-MOS_44_31, π-SDSCR_60_31 and π-RTSCR_60_31 in Fig. 3.46 (a). The TLP I-V curve of π-diode_30_41 is compared with that of π-MOS_44_41, π-SDSCR_60_41 and π-RTSCR_60_41 in Fig. 3.46 (b). The

TLP I-V curve of π-diode_50_31 is compared with that of π-MOS_72_31, π-MOS_200_31, π-SDSCR_100_31 and π-RTSCR_100_31 in Fig. 3.46 (c). The TLP I-V curve of π-diode_50_41 is compared with that of π-MOS_72_41, π-SDSCR_100_41 and π-RTSCR_100_41 in Fig. 3.46 (d). The TLP I-V curves after normalized by insertion loss (S_{21}) at 20GHz are shown in Fig. 3.47.

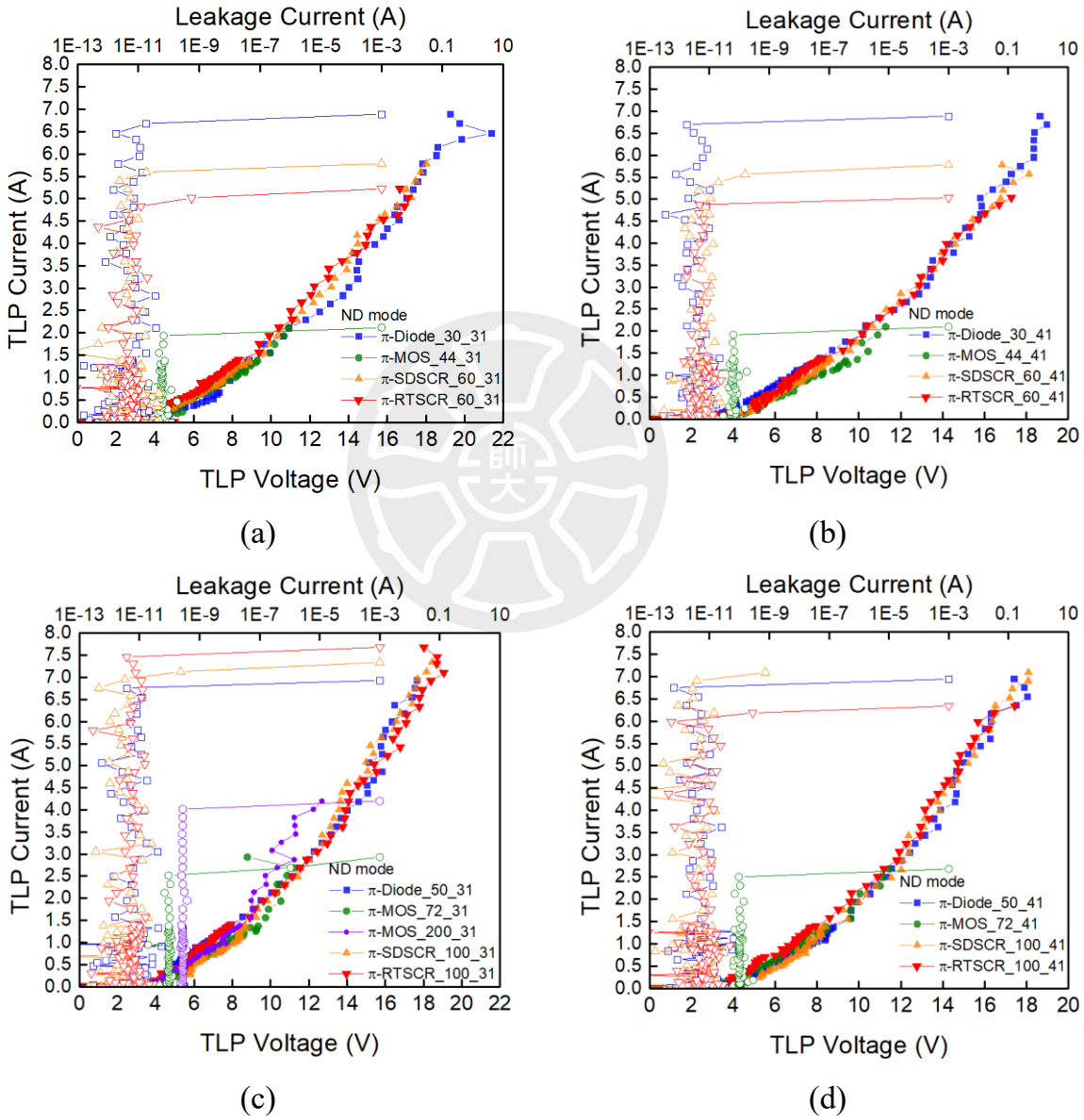


Fig. 3.46. TLP I-V curves of test devices under ND mode.

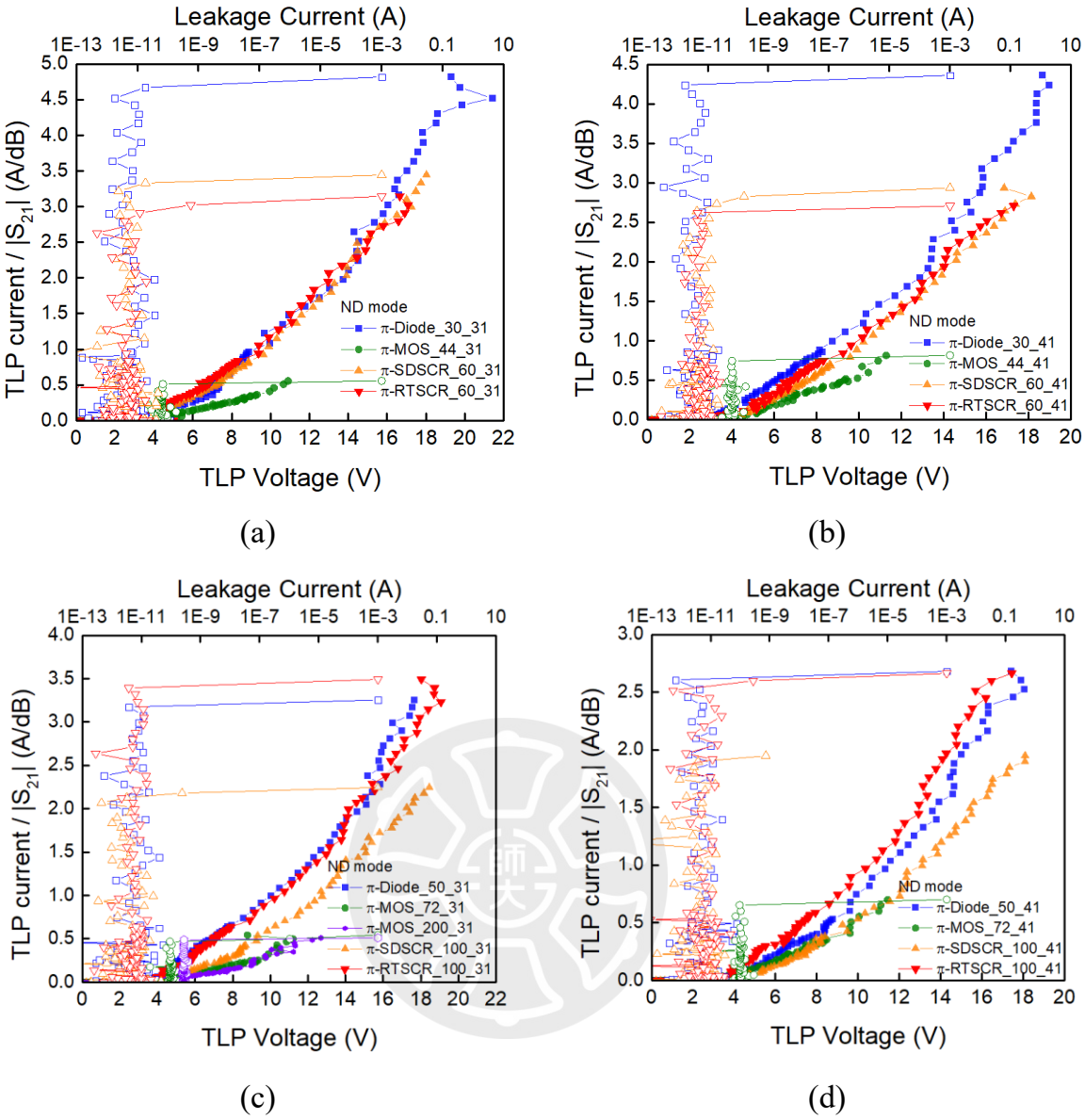


Fig. 3.47. TLP I-V curves of test devices under ND mode after normalized by insertion loss at 20GHz.

(5) NS Mode

The test circuit discharges ESD current of NS mode through the device placed from V_{SS} to I/O pad. The TLP I-V curve of π-diode_30_31 is compared with that of π-MOS_44_31, π-SDSCR_60_31 and π-RTSCR_60_31 in Fig. 3.48 (a). The TLP I-V curve of π-diode_30_41 is compared with that of π-MOS_44_41, π-SDSCR_60_41 and π-RTSCR_60_41 in Fig. 3.48 (b). The TLP I-V curve of π-diode_50_31 is compared

with that of π-MOS_72_31, π-MOS_200_31, π-SDSCR_100_31 and π-RTSCR_100_31 in Fig. 3.48 (c). The TLP I-V curve of π-diode_50_41 is compared with that of π-MOS_72_41, π-SDSCR_100_41 and π-RTSCR_100_41 in Fig. 3.48 (d). The TLP I-V curves after normalized by insertion loss (S_{21}) at 20GHz are shown in Fig. 3.49.

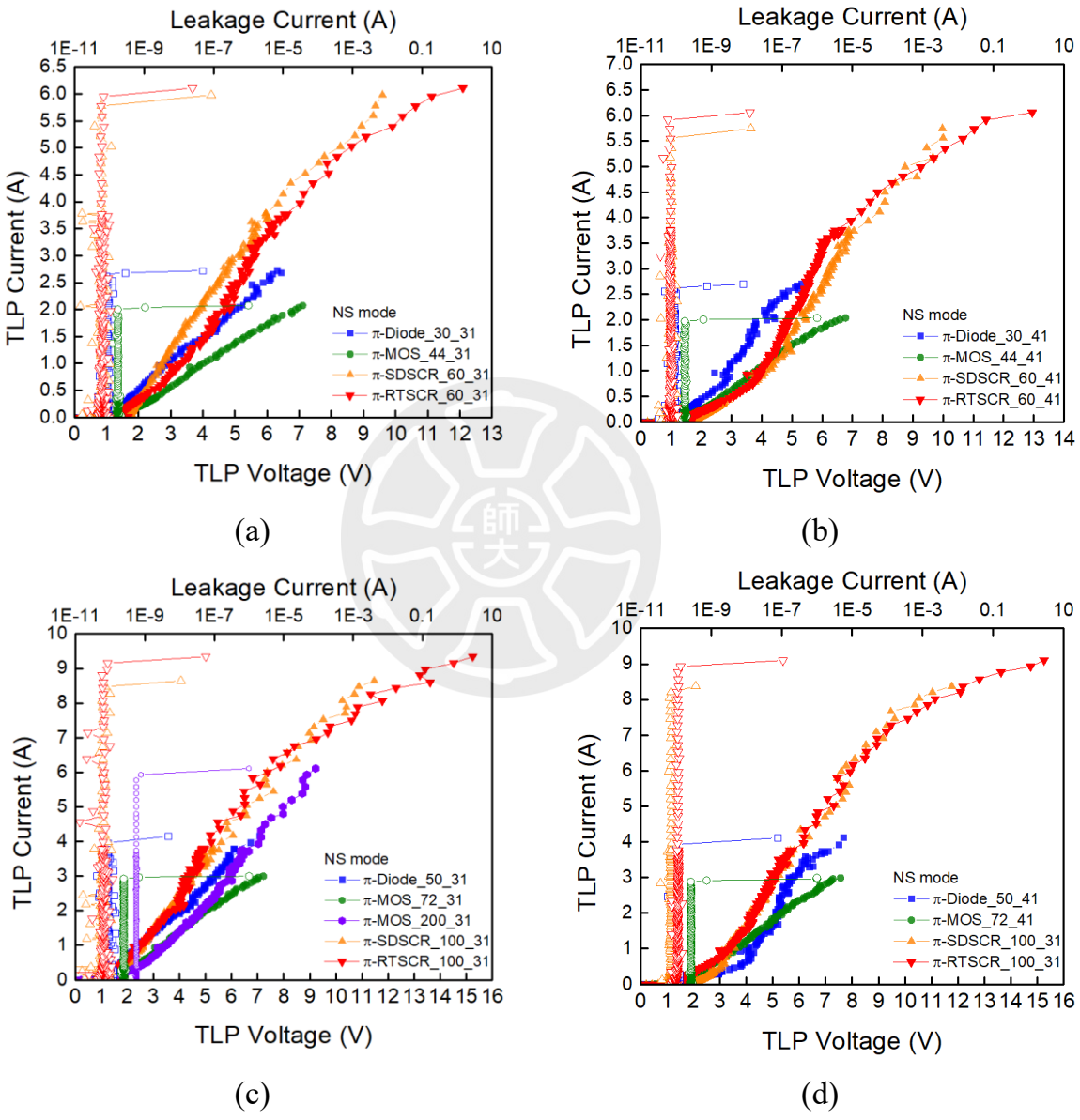


Fig. 3.48. TLP I-V curves of test devices under NS mode.

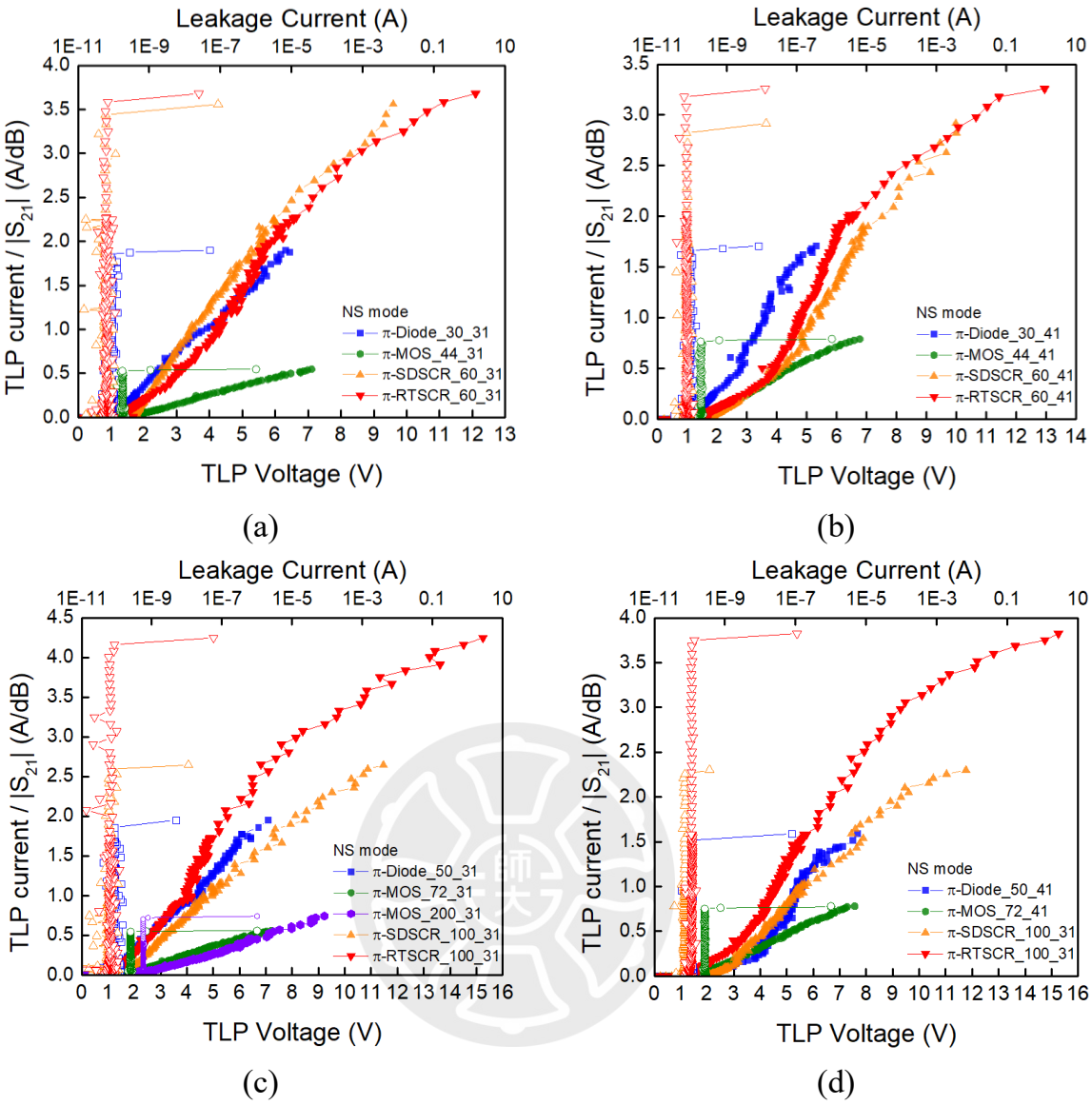


Fig. 3.49. TLP I-V curves of test devices under NS mode after normalized by insertion loss at 20GHz.

Table 3.7. Measured I_{t2} results

Cell Name	I_{t2} (A)			
	PS mode	PD mode	NS mode	ND mode
π-diode_30_31	3.59	2.73	2.68	6.89
π-diode_30_41	3.17	2.74	2.70	6.89
π-diode_50_31	6.76	4.64	4.15	6.93
π-diode_50_41	5.64	4.46	3.92	6.94
π-MOS_44_31	1.29	2.89	2.00	1.93
π-MOS_44_41	1.30	2.89	2.00	1.91
π-MOS_72_31	1.43	4.04	3.00	2.51
π-MOS_72_41	1.43	4.05	2.91	2.50
π-MOS_200_31	6.53	7.17	5.91	4.87
π-SDSCR_60_31	6.93	6.76	5.78	5.78
π-SDSCR_60_41	6.90	6.81	5.56	5.78
π-SDSCR_100_31	6.91	8.09	8.47	7.34
π-SDSCR_100_41	6.97	8.10	8.38	6.91
π-RTSCR_60_31	6.70	7.16	5.95	5.02
π-RTSCR_60_41	6.53	7.17	5.91	4.87
π-RTSCR_100_31	6.93	8.08	9.16	7.68
π-RTSCR_100_41	7.15	8.11	8.93	6.19

Table 3.8. Measured $I_{t2}/|S_{21}|$ results

Cell Name	$I_{t2}/\|S_{21}\|$(A/dB)			
	PS mode	PD mode	NS mode	ND mode
π-diode_30_31	2.51	1.91	1.87	4.82
π-diode_30_41	2.01	1.73	1.71	4.36
π-diode_50_31	3.17	2.18	1.95	3.25
π-diode_50_41	2.18	1.72	1.51	2.68
π-MOS_44_31	0.34	0.76	0.53	0.51
π-MOS_44_41	0.50	1.12	0.78	0.74
π-MOS_72_31	0.27	0.75	0.56	0.47
π-MOS_72_41	0.37	1.06	0.76	0.65
π-MOS_200_31	0.79	0.87	0.72	0.59
π-SDSCR_60_31	4.13	4.02	3.44	3.44
π-SDSCR_60_41	3.50	3.46	2.82	2.93
π-SDSCR_100_31	2.11	2.47	2.59	2.24
π-SDSCR_100_41	1.91	2.23	2.30	1.90
π-RTSCR_60_31	4.04	4.31	3.58	3.02
π-RTSCR_60_41	3.51	3.85	3.18	2.62
π-RTSCR_100_31	3.15	3.67	4.16	3.49
π-RTSCR_100_41	3.00	3.41	3.75	2.60

3.6.3 HBM Test

The secondary breakdown current (I_{t2}) is obtained after measuring the TLP I-V curves. HBM tests are implemented to find out the ESD level of protection device. To determine the failure of device, the criteria is defined as the leakage current changes by 30%. As shown in Fig. 3.50, HBM test is implemented with HBM tester. [30] The measurement results are listed in Table 3.9.

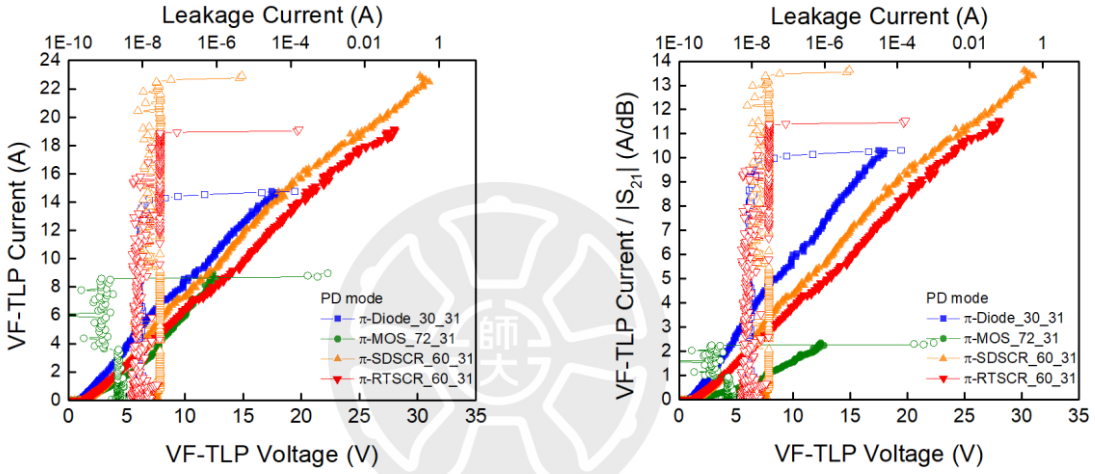
Fig. 3.50. HBM tester. [30]

Table 3.9. HBM test results

Cell Name	HBM (kV)			
	PS mode	PD mode	NS mode	ND mode
π-diode_30_31	5	5	4	>8
π-diode_30_41	5	5	4	>8
π-diode_50_31	>8	>8	5	>8
π-diode_50_41	>8	>8	5	>8
π-MOS_44_31	<1	6	3	2
π-MOS_44_41	<1	6	3	2
π-MOS_72_31	<1	>8	4	3
π-MOS_72_41	<1	>8	4	3
π-MOS_200_31	3	>8	>8	7
π-SDSCR_60_31	>8	>8	>8	>8
π-SDSCR_60_41	>8	>8	>8	>8
π-SDSCR_100_31	>8	>8	>8	>8
π-SDSCR_100_41	>8	>8	>8	>8
π-RTSCR_60_31	>8	>8	>8	>8
π-RTSCR_60_41	>8	>8	>8	>8
π-RTSCR_100_31	>8	>8	>8	>8
π-RTSCR_100_41	>8	>8	>8	>8

3.6.4 Very Fast TLP Test

Very fast TLP system is used to simulate the charged-device model (CDM) ESD stresses [31]. The VF-TLP I-V curves of π-diode_30_31, π-MOS_72_31, π-SDSCR_60_31 and π-RTSCR_60_31 under PD mode are shown in Fig. 3.51 (a). The VF-TLP I-V curves normalized by insertion loss (S_{21}) at 20GHz are shown in Fig. 3.51 (b). The measurement results of VF-TLP test are recorded in Table 3.10.



(a) (b)

Fig. 3.51. (a) VF-TLP I-V curves of test devices under PD mode. (b) VF-TLP I-V curves of test devices under PD mode after normalized by insertion loss.

Table 3.10. VF-TLP test results

Cell name	V_{Clamp_VFTLP} (V)				I_{t2} (A)
	3A	5A	7A	9A	
π-diode_30_31	4.39	6.17	8.00	10.87	14.42
π-MOS_72_31	6.87	8.83	10.59	-	8.59
π-SDSCR_60_31	5.44	7.25	9.34	12.01	22.62
π-RTSCR_60_31	5.71	8.32	10.72	14.01	18.93

3.7 Comparison

Form the layout top view, the layout area of device relates to the size of the protection element and the matching inductor. However, the size of protection element determines the ESD robustness as well. Therefore, it becomes a tradeoff between the small layout area and high ESD robustness. To compare the test devices, there is a figure of merit (FOM) is defined as

$$FOM_{1\_device\_area} = \frac{I_{t2}}{area}$$

where I_{t2} is measured secondary breakdown current in TLP test and area is layout area of each test device. The comparison results are list in Table 3.11 and shown in Fig. 3.52.

From the comparison result, the traditional π-MOS devices are the worst because of the weak ESD robustness. Proposed π-SDSCR devices have larger size than traditional π-diode because the size of each SDSCR element is designed larger. However, it provides further higher ESD robustness. As compare with another proposed device, π-RTSCR, π-SDSCR has similar ESD robustness in smaller layout area so that the $FOM_{1\_device\_area}$ of π-SDSCR is better than others. Another phenomenon worthy of attention is that the $FOM_{1\_device\_area}$ of π-diode in larger size is better than the small one and π-SDSCR is the opposite. The reason is that π-SDSCR in smaller size here is already had a high ESD robustness. When the size increases, the ESD robustness doesn't proportionally increase because the metal wire will burn first. On the other hand, π-diode devices haven't reached this ESD level yet.

Table 3.11. Comparison table of $FOM_{1\_device\_area}$

Cell Name	Area (μm^2)	ESD Robustness		$FOM_{1\_device\_area}$ (kA/mm^2)
		I_{t2} (A)	HBM(kV)	
π-diode_30_31	10902	2.68	4	0.25
π-diode_30_41	12540	2.70	4	0.22
π-diode_50_31	12482	4.15	5	0.33
π-diode_50_41	13035	3.92	5	0.30
π-MOS_44_31	11109	1.29	<1	0.12
π-MOS_44_41	12768	1.30	<1	0.10
π-MOS_72_31	11592	1.43	<1	0.12
π-MOS_72_41	12768	1.43	<1	0.11
π-MOS_200_31	13193	2.27	3	0.17
π-SDSCR_60_31	14018	5.78	>8	0.41
π-SDSCR_60_41	16562	5.56	>8	0.34
π-SDSCR_100_31	21546	6.91	>8	0.32
π-SDSCR_100_41	23491	6.91	>8	0.29
π-RTSCR_60_31	16686	5.02	>8	0.30
π-RTSCR_60_41	18421	4.87	>8	0.26
π-RTSCR_100_31	23166	6.93	>8	0.30
π-RTSCR_100_41	25181	6.19	>8	0.25

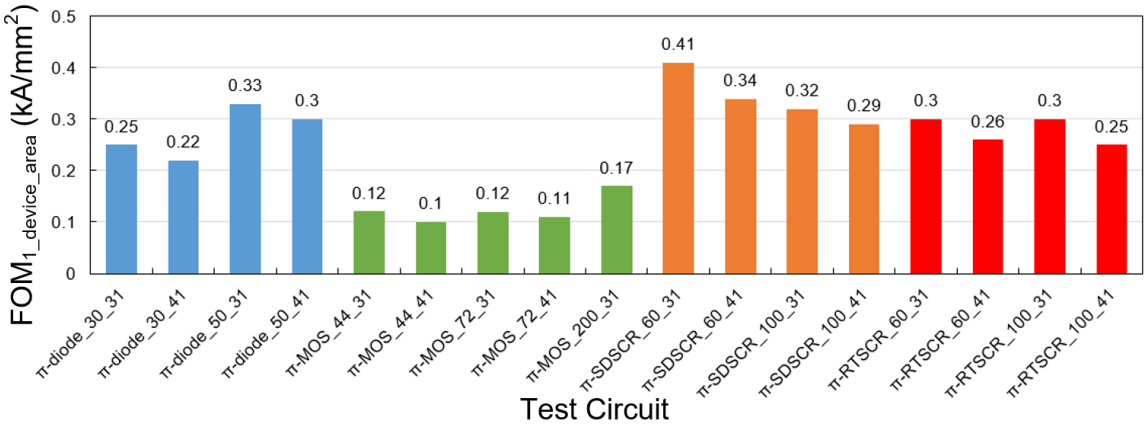


Fig. 3.52. Comparison of $FOM_{1\_device\_area}$

For the high-frequency applications, the ESD protection devices are wished to have low insertion loss under normal circuit operating conditions and high robustness during ESD events. The high-frequency performance is determined by the parasitic capacitance of the protection element. The parasitic capacitance can be estimated by the width of P-N junction in each protection element and it relates to the size of the protection element. As the result, the lower parasitic capacitance of device or the smaller size of protection element provide the better high-frequency performance. However, ESD protection devices in small size may cause the worse ESD robustness. As the result, it becomes a tradeoff between low high-frequency signal loss and high ESD robustness. To compare the test devices, the FOM here is defined as

$$FOM_{2\_device\_S21} = \frac{I_{t2}}{|S_{21}|}$$

where I_{t2} is measured secondary breakdown current in TLP test and S_{21} is measured insertion loss at 20GHz. The comparison results are list in Table 3.12 and shown in Fig. 3.53.

Table 3.12. Comparison table of $FOM_{2\_device\_S21}$

Cell Name	ESD Robustness		High-Frequency Performance at 20GHz		$FOM_{2\_device\_S21}$ (A/dB)
	I_{t2} (A)	HBM(kV)	S_{21}(dB)	S_{11}(dB)	
π-diode_30_31	2.68	4	-1.43	-24.6	1.87
π-diode_30_41	2.70	4	-1.58	-21.4	1.71
π-diode_50_31	4.15	5	-2.13	-14.1	1.95
π-diode_50_41	3.92	5	-2.59	-16.2	1.51
π-MOS_44_31	1.29	<1	-3.79	-15.0	0.34
π-MOS_44_41	1.30	<1	-2.58	-21.1	0.50
π-MOS_72_31	1.43	<1	-5.39	-12.1	0.27
π-MOS_72_41	1.43	<1	-3.83	-19.2	0.37
π-MOS_200_31	2.27	3	-8.24	-11.0	0.28
π-SDSCR_60_31	5.78	>8	-1.68	-23.7	3.44
π-SDSCR_60_41	5.56	>8	-1.97	-21.5	2.82
π-SDSCR_100_31	6.91	>8	-3.27	-14.6	2.11
π-SDSCR_100_41	6.91	>8	-3.64	-15.8	1.90
π-RTSCR_60_31	5.02	>8	-1.66	-24.7	3.02
π-RTSCR_60_41	4.87	>8	-1.86	-20.1	2.62
π-RTSCR_100_31	6.93	>8	-2.20	-16.3	3.15
π-RTSCR_100_41	6.19	>8	-2.38	-27.4	2.60

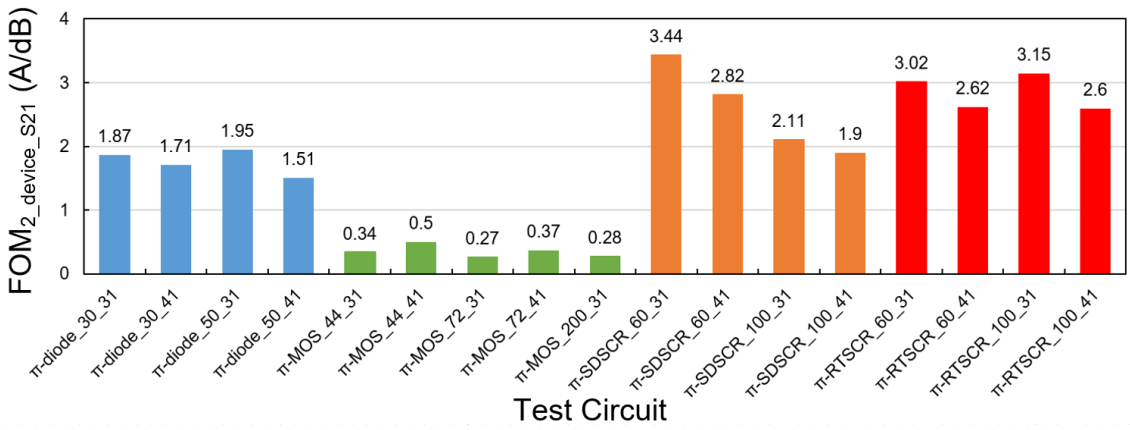


Fig. 3.53. Comparison of $FOM_{2\_device\_S21}$

From the measurement results, the high-frequency performance and ESD robustness of traditional π-MOS are both the worst case of all test cells. The $FOM_{2\_device\_S21}$ of proposed π-SDSCR and π-RTSCR is better than traditional π-diode because the proposed designs can perform higher ESD robustness in similar high-frequency performance than traditional designs. It means SDSCR and RTSCR device have lower parasitic capacitance per unit device width. As the result, π-SDSCR and π-RTSCR can be design larger to provide higher ESD robustness in same condition of high-frequency performance. As compare between π-SDSCR and π-RTSCR, they have similar ESD robustness and high-frequency performance in smaller size. However, π-RTSCR has better high-frequency performance in larger size but still similar ESD robustness. The advantage of low parasitic capacitance of π-RTSCR is obvious when the devices are designed larger.

3.8 Summary

Proposed π-SDSCR, π-RTSCR, traditional π-diode and π-MOS are realized in silicon. From the S-parameter measurement results, the S_{21} of test device is higher than -2dB with appropriate size. In addition, the S_{11} is lower than -20dB. It can be used in high-frequency applications with less distorting. During TLP test, the I_{t2} of both π-SDSCR and π-RTSCR are higher than traditional designs. It means that the ESD robustness of proposed designs are better. The same conclusion is shown in HBM test results. The traditional π-diode and π-MOS reach at most 5kV ESD level. As compare with traditional designs, all of proposed π-SDSCR and π-RTSCR can sustain more than 8kV HBM robustness. From very fast TLP test, the measurement result shows that proposed devices can also turn on during fast ESD events and the robustness is better than traditional designs.

In next chapter, the proposed design is added into high-speed TIA to verify the capability of ESD protection.

Chapter 4

Realization of Proposed Design with TIA

4.1 Introduction

In recent years, the demand for high-speed transmission products is gradually increasing. As the result, the data rate of optical communication system is also pushed. To sustain such a high operating speed, circuit must be designed with a large bandwidth.

Trans-impedance amplifier (TIA) plays an important role in the optical communications. To accomplish an optical receiver, TIA is necessary to transfer photo current to voltage signal. Fig. 4.1 shows the architecture of optical receiver system.

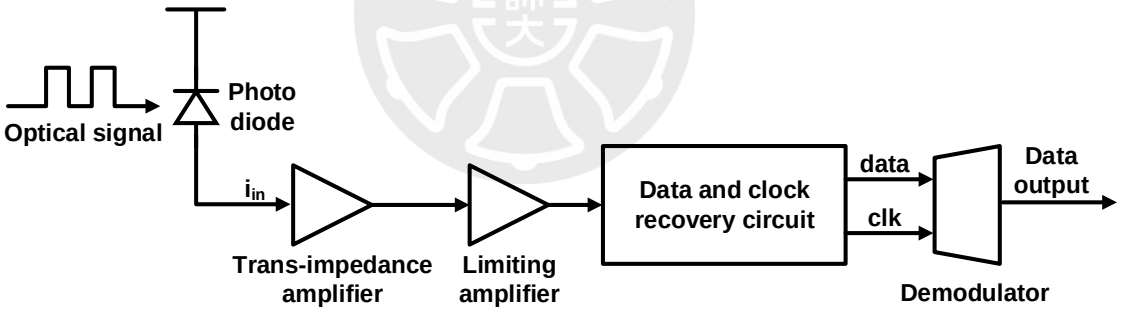


Fig. 4.1. The architecture of optical receiver system.

4.2 Structure of TIA

Fig. 4.2 shows the architecture of TIA circuit. The TIA circuit is composed of three cascaded common-source stages. Drain-bias resistors (R_D) are employed in each stage. To increase the bandwidth, the inductors are connected as π-shape in input stage, output stage and between stages for matching [32], [33]. For high-frequency measurement,

input and output impedance are design as 50Ω through the resistor R_1-R_4. To achieve whole chip ESD protection, ESD protection device and power rail ESD clamp circuit are equipped in the TIA circuit. L_2 and the protection devices form a π-shape to reduce the effect of the parasitic capacitance.

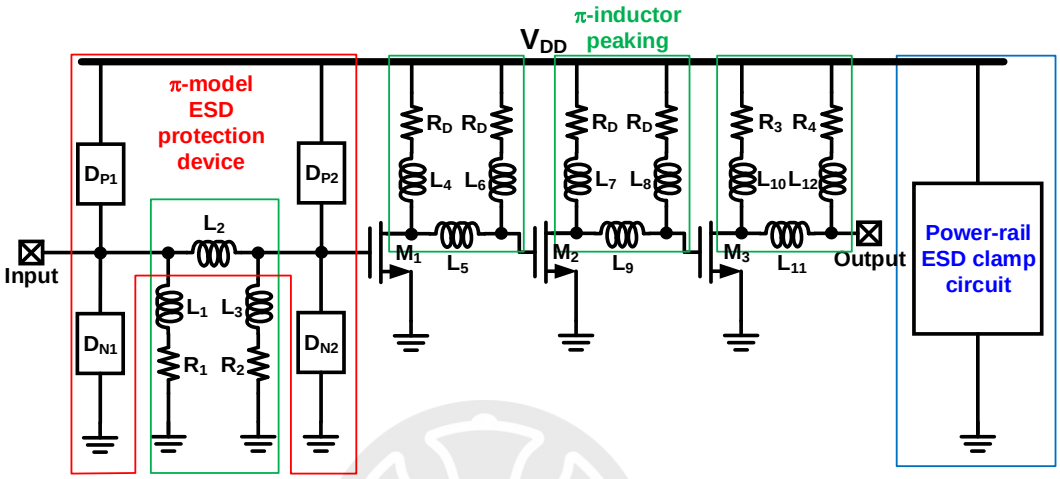


Fig. 4.2. The architecture of TIA circuit.

4.3 Simulation Results of TIA

TIA circuits are equipped with traditional π-diode, proposed π-SDSCR and π-RTSCR to verify the capability of ESD protection. Advanced Design System (ADS) is used to simulate the S-parameter and noise figure of all the test circuits. SONNET electromagnetic (EM) is also used to do the electromagnetic simulation of inductor and metal routing.

4.3.1 TIA w/o Protection

The architecture of TIA w/o protection is presented in Fig. 4.3 It is a three-stage CS amplifier. The maximum voltage (V_{DD}) is 1.8V, and the input bias voltage is 1V.

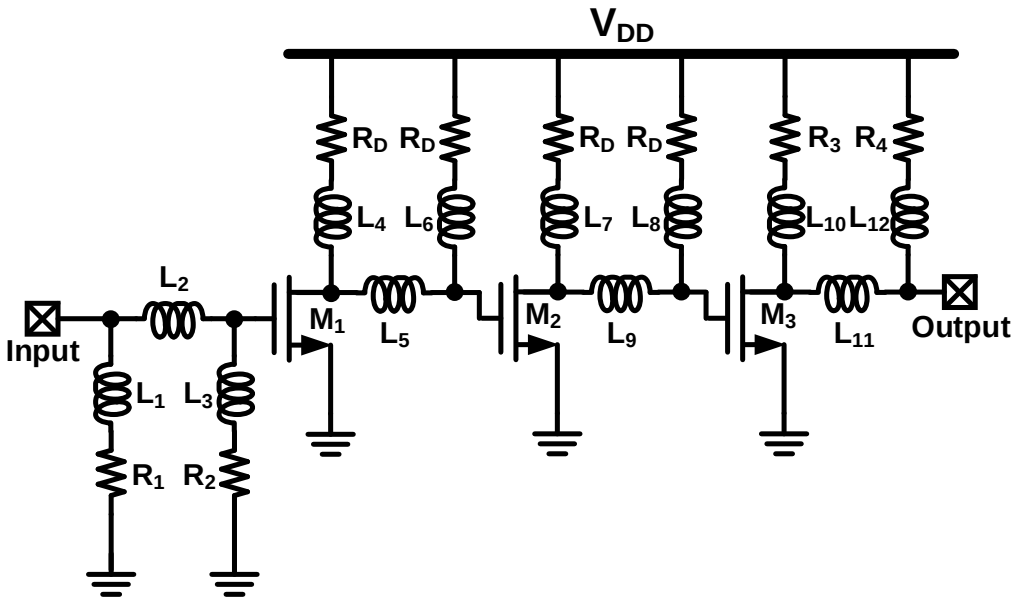
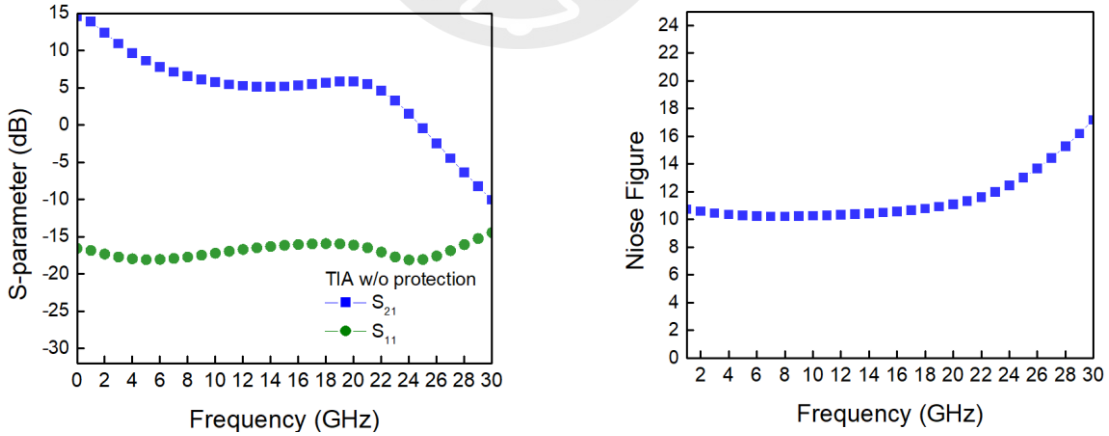


Fig. 4.3. The architecture of TIA w/o protection.

As shown in Fig. 4.4 (a), simulated S_{21} is 5.5dB, and S_{11} is -16.0dB at 17GHz. As shown in Fig. 4.4 (b), simulated noise figure of TIA w/o protection is 10.7 at 17GHz. Layout top view of TIA w/o protection is shown in Fig. 4.5.



(a) (b)

Fig. 4.4. Simulated (a) S-parameter and (b) noise figure of TIA w/o protection.

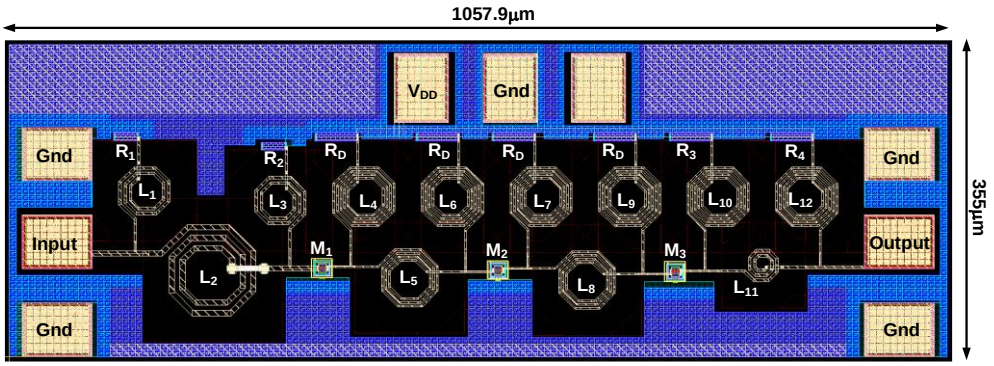


Fig. 4.5. Layout top view of TIA w/o protection.

4.3.2 TIA with Traditional π-Diode

The architecture of TIA with π-diode is presented in Fig. 4.6. As compare to TIA w/o protection, π-diode and power-rail ESD clamp circuit are added into TIA circuit. The size of each diode is chosen as 20μm.

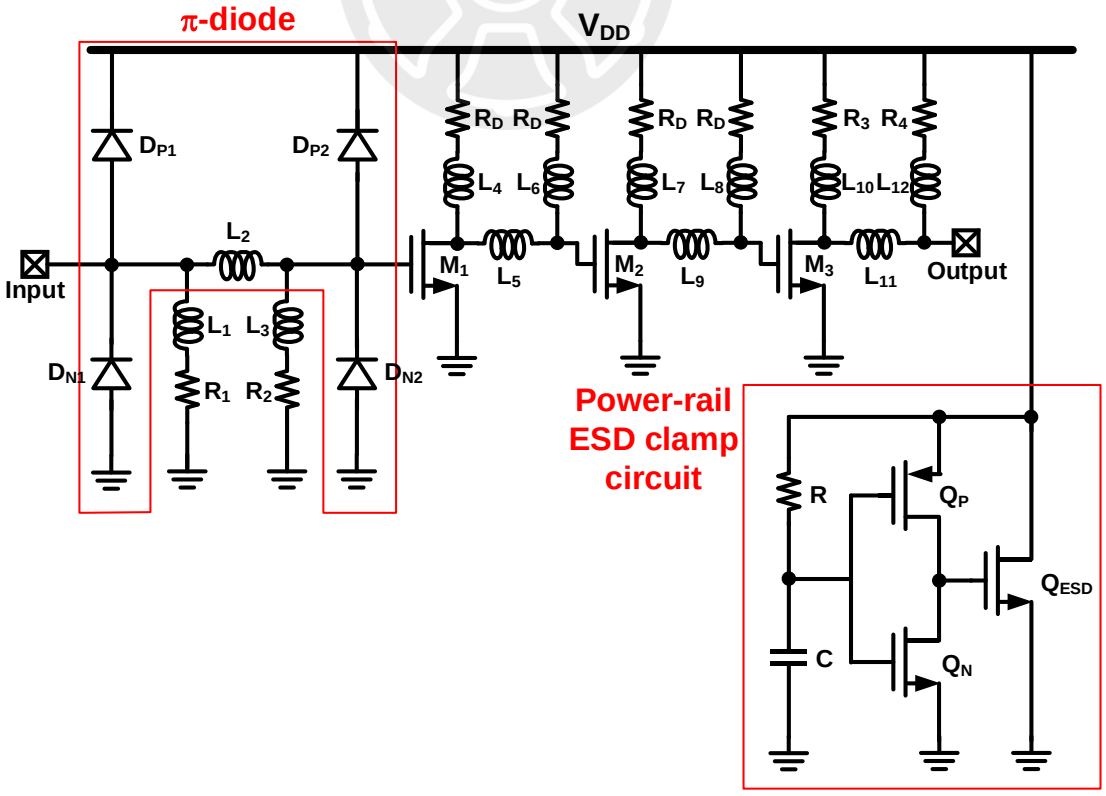
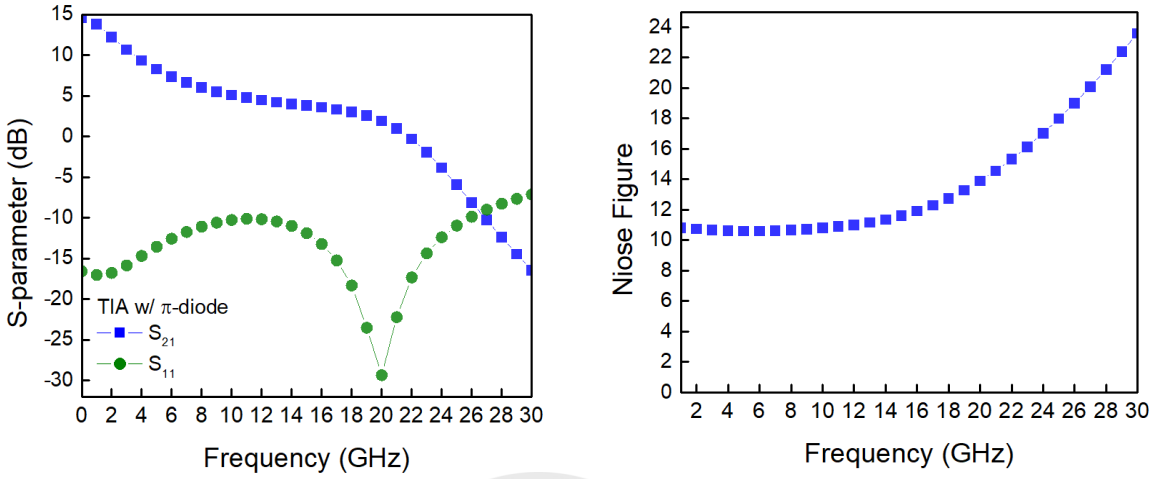


Fig. 4.6. The architecture of TIA with π-diode.

As shown in Fig. 4.7 (a), simulated S_{21} is 3.3dB, and S_{11} is -15.2dB at 17GHz. As shown in Fig. 4.7(b), simulated noise figure of TIA with π-diode is 12.3 at 17GHz. Layout top view of TIA with π-diode is shown in Fig. 4.8.



(a) (b)

Fig. 4.7. Simulated (a) S-parameter and (b) noise figure of TIA with π-diode.

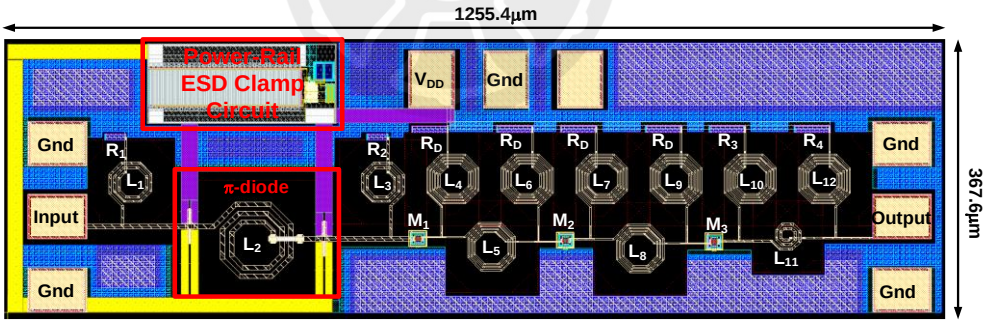


Fig. 4.8. Layout top view of TIA with π-diode.

4.3.3 TIA with Proposed π-SDSCR

The architecture of TIA with π-SDSCR is presented in Fig. 4.9. As compare to TIA w/o protection, π-SDSCR and power-rail ESD clamp circuit are added into TIA circuit. The size of each SDSCR is chosen as 20μm.

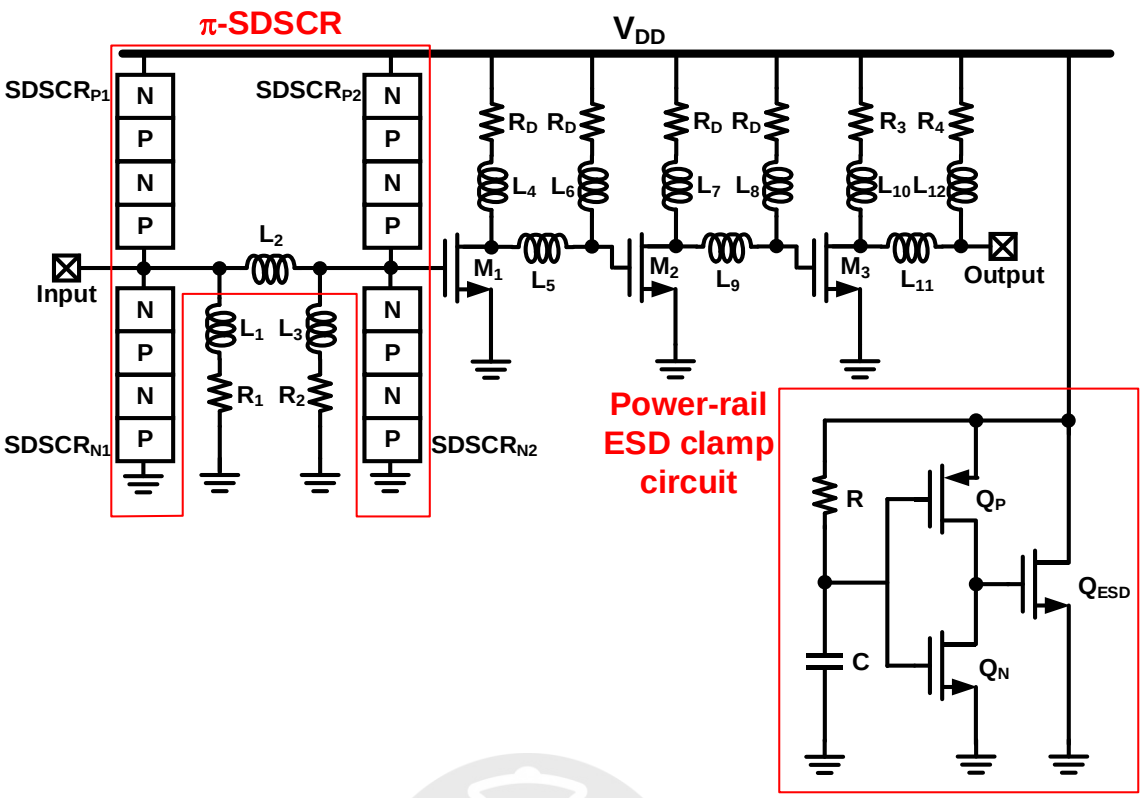
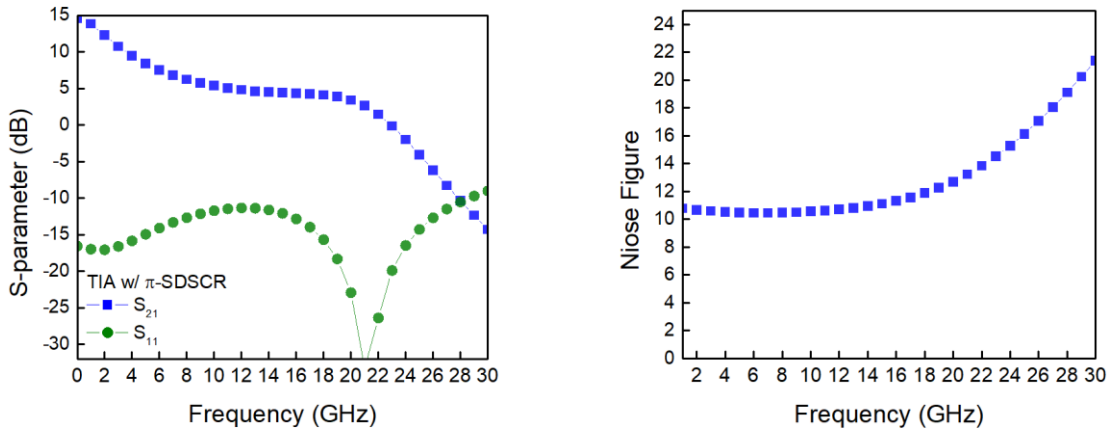


Fig. 4.9. The architecture of TIA with π-SDSCR.

As shown in Fig. 4.10 (a), simulated S_{21} is 4.2dB, and S_{11} is -14.0dB at 17GHz. As shown in Fig. 4.10 (b), simulated noise figure of TIA with π-SDSCR is 11.6 at 17GHz. Layout top view of TIA with π-SDSCR is shown in Fig. 4.11.



(a) (b)

Fig. 4.10. Simulated (a) S-parameter and (b) noise figure of TIA with π-SDSCR.

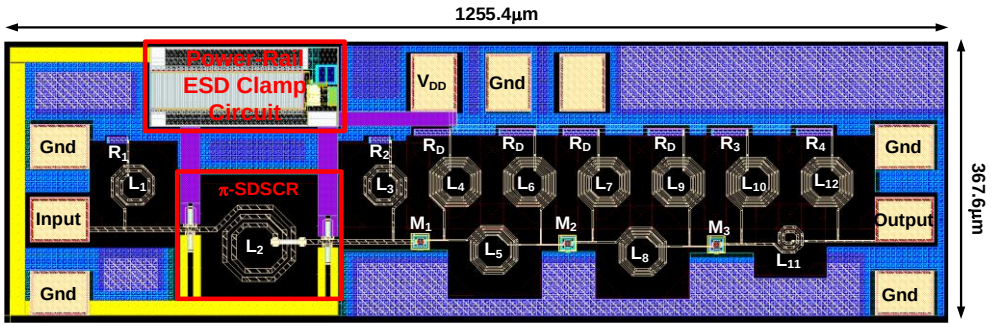


Fig. 4.11. Layout top view of TIA with π-SDSCR.

4.3.4 TIA with Proposed π-RTSCR

The architecture of TIA with π-RTSCR is presented in Fig. 4.12. As compare to TIA w/o protection, π-RTSCR and power-rail ESD clamp circuit are added into TIA circuit. The size of each RTSCR is chosen as 20μm.

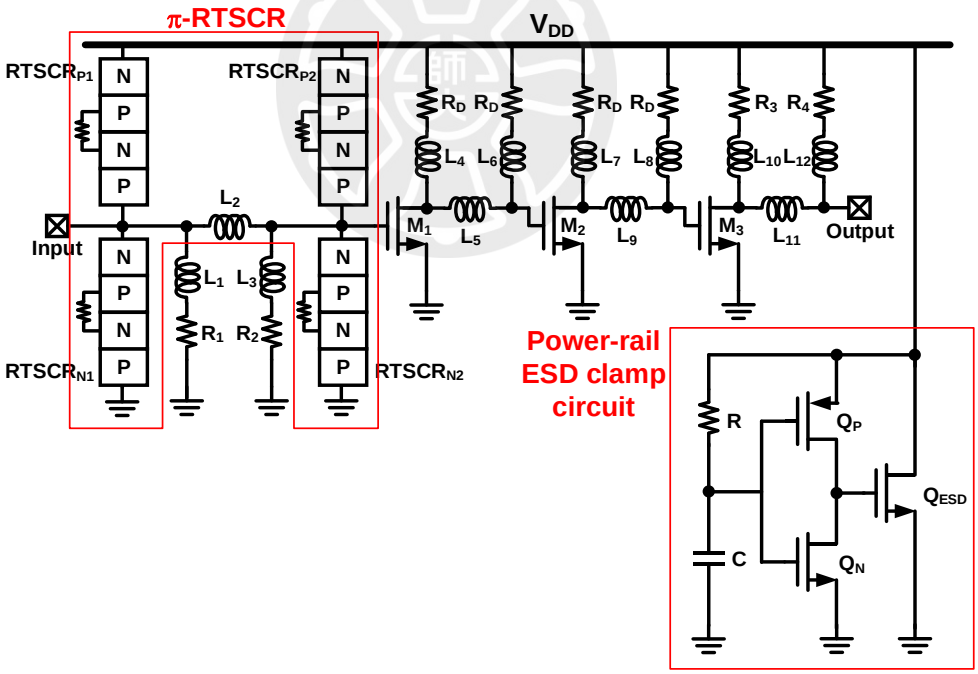
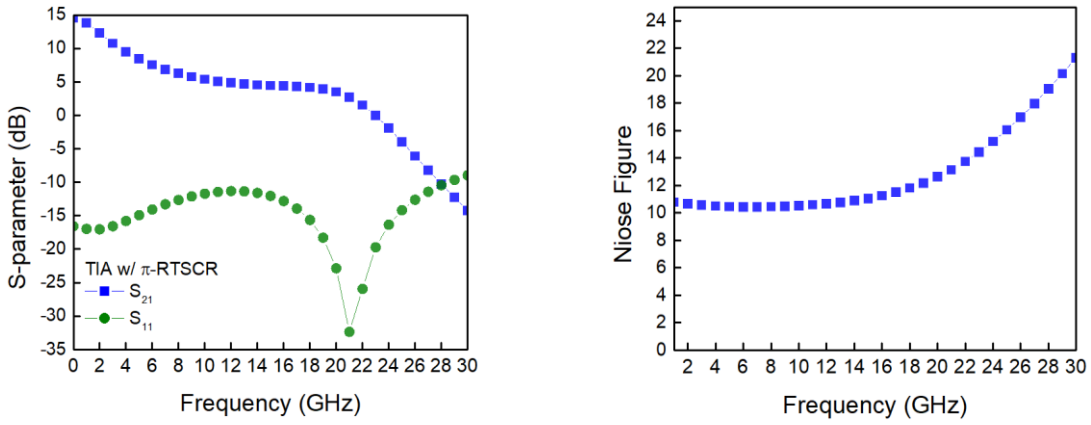


Fig. 4.12. The architecture of TIA with π-RTSCR.

As shown in Fig. 4.13 (a), simulated S_{21} is 4.3dB, and S_{11} is -13.9dB at 17GHz. As shown in Fig. 4.13 (b), simulated noise figure of TIA with π-RTSCR is 11.5 at 17GHz. Layout top view of TIA with π-RTSCR is shown in Fig. 4.14.



(a) (b)

Fig. 4.13. Simulated (a) S-parameter and (b) noise figure of TIA with π-RTSCR.

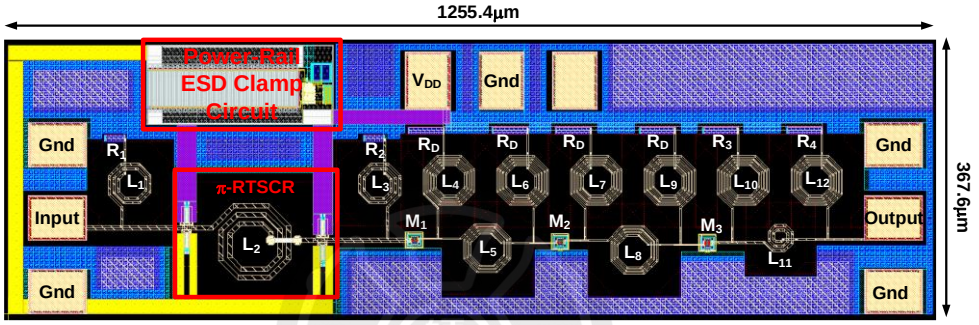


Fig. 4.14. Layout top view of TIA with π-RTSCR.

4.4 Measurement Results of TIA

Three TIA circuits are fabricated in 0.18μm CMOS process. There are four test circuits. The first one is TIA without protection, and the second one is TIA equipped with π-diode, another is TIA with π-SDSCR and the other is TIA with π-RTSCR. The photograph is shown in Fig. 4.15. The width is 1560.7μm, and the length is 1487.7μm. S-parameter and noise figure are measured with RFIC parameter measurement system on 2-port GSG probe station. The voltage of power supply (V_{DD}) is 1.8V, and the input bias is 1V. HBM tests are also implemented to find out the ESD robustness. The measurement results are introduced in following section.

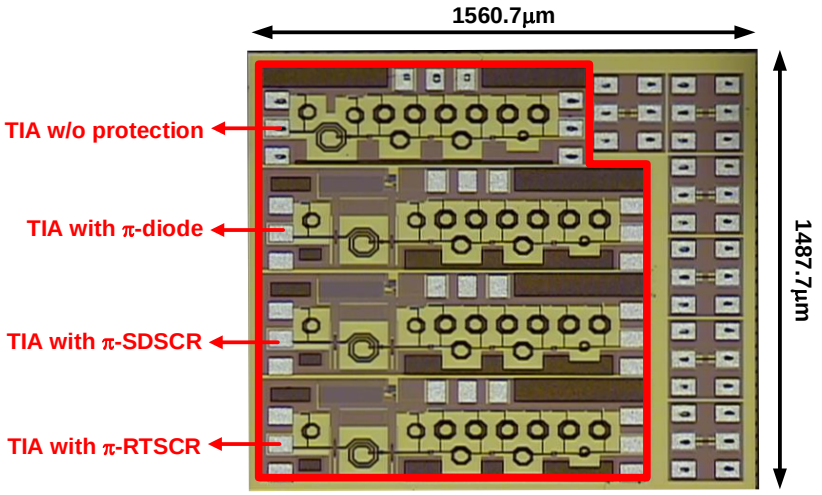
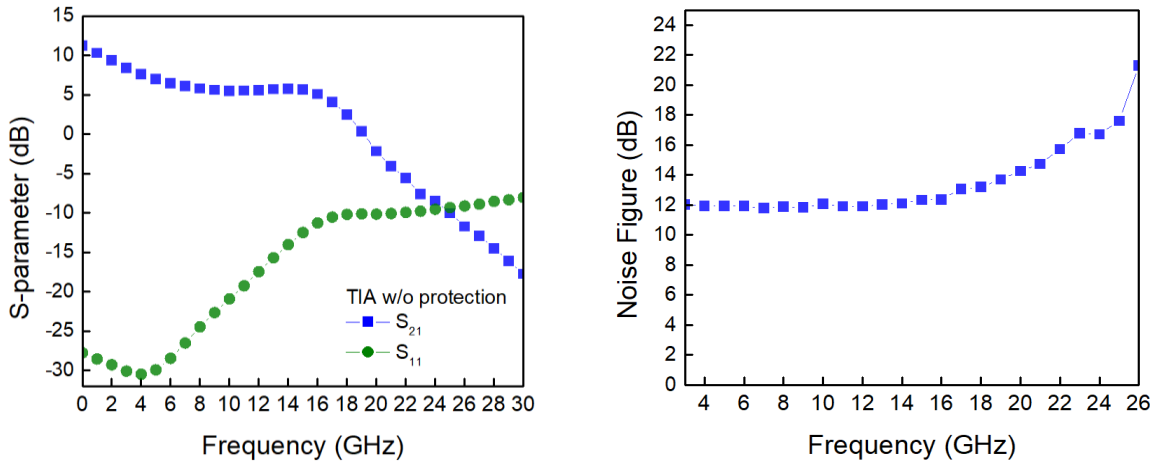


Fig. 4.15. The chip photograph of test TIA circuits.

4.4.1 High-Frequency Performance

The S-parameters of each test circuits are measured by 67GHz RFIC parameter measurement system. Measured S-parameter at 17GHz is listed in Table 4.1.

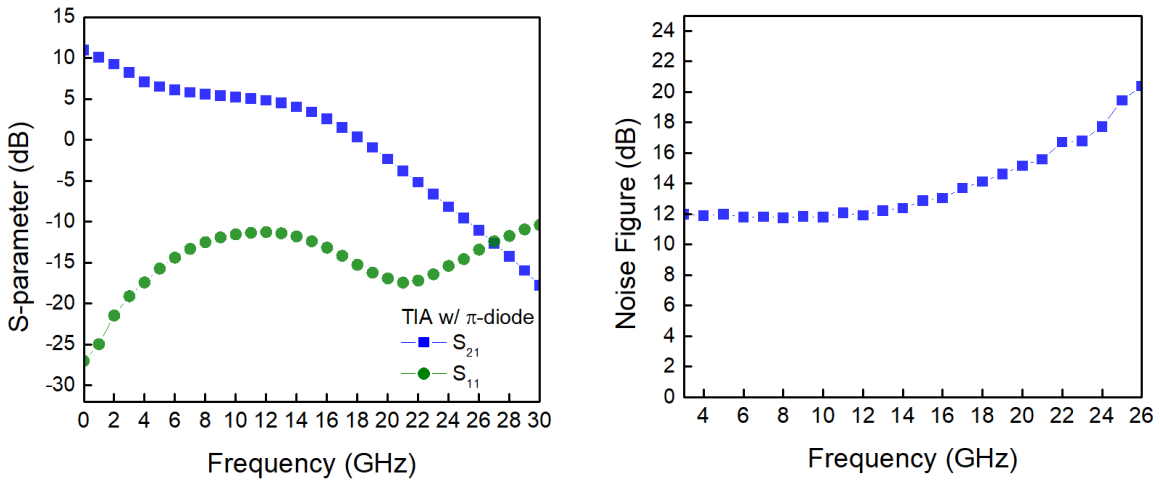
The measurement result of TIA w/o protection is shown in Fig. 4.16. Measured S_{21} is 4.10dB, and S_{11} is -10.5dB at 17GHz, and measured noise figure is 13.1 at 17GHz.



(a) (b)

Fig. 4.16. Measured (a) S-parameter and (b) noise figure of TIA w/o protection.

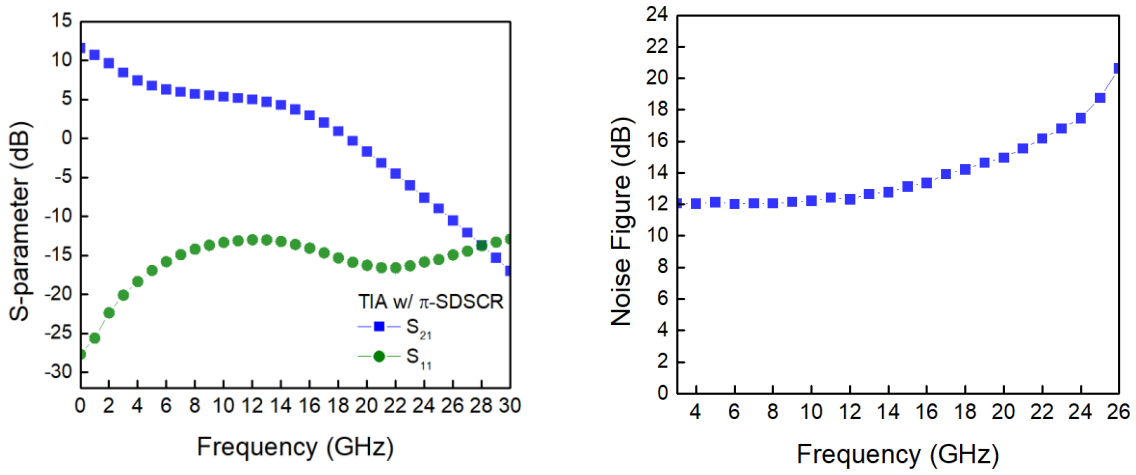
The measurement result of TIA with π-diode is shown in Fig. 4.17. Measured S_{21} is 1.53dB, and S_{11} is -14.2dB at17GHz, and measured noise figure is 13.7 at 17GHz.



(a) (b)

Fig. 4.17. Measured (a) S-parameter and (b) noise figure of TIA with π-diode.

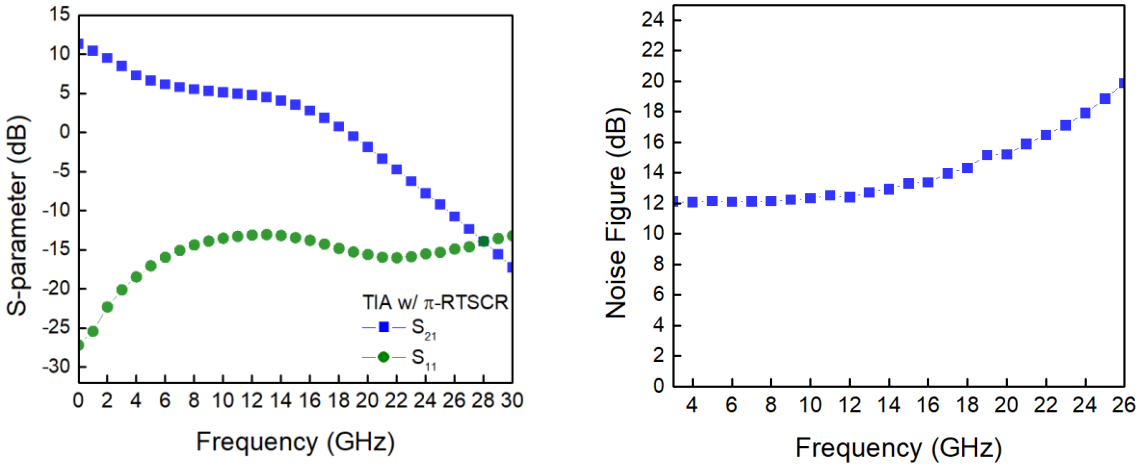
The measurement result of TIA with π-SDSCR is shown in Fig. 4.18. Measured S_{21} is 2.02dB, and S_{11} is -14.7dB at17GHz, and measured noise figure is 13.9 at 17GHz.



(a) (b)

Fig. 4.18. Measured (a) S-parameter and (b) noise figure of TIA with π-SDSCR.

The measurement result of TIA with π-RTSCR is shown in Fig. 4.19. Measured S_{21} is 1.85dB, and S_{11} is -14.3dB at17GHz, and measured noise figure is 12.7 at 17GHz.



(a) (b)

Fig. 4.19. Measured (a) S-parameter and (b) noise figure of TIA with π-RTSCR.

Table 4.1. Measured S-parameter at 17GHz

Cell Name	**S_{21} (dB) at 17GHz**	**S_{11} (dB) at 17GHz**	**Noise figure at 17GHz**
TIA w/o protection	4.10	-10.5	13.1
TIA with π-diode	1.53	-14.2	13.7
TIA with π-SDSCR	2.02	-14.7	13.9
TIA with π-RTSCR	1.85	-14.3	12.7

4.4.2 TLP I-V Curves

After verifying the high-frequency performance, TIA with ESD protection devices are tested by TLP system to learn the characteristic. The TLP I-V curves of each test circuit under PS mode, PD mode, NS mode, and ND mode are compared in Fig. 4.20

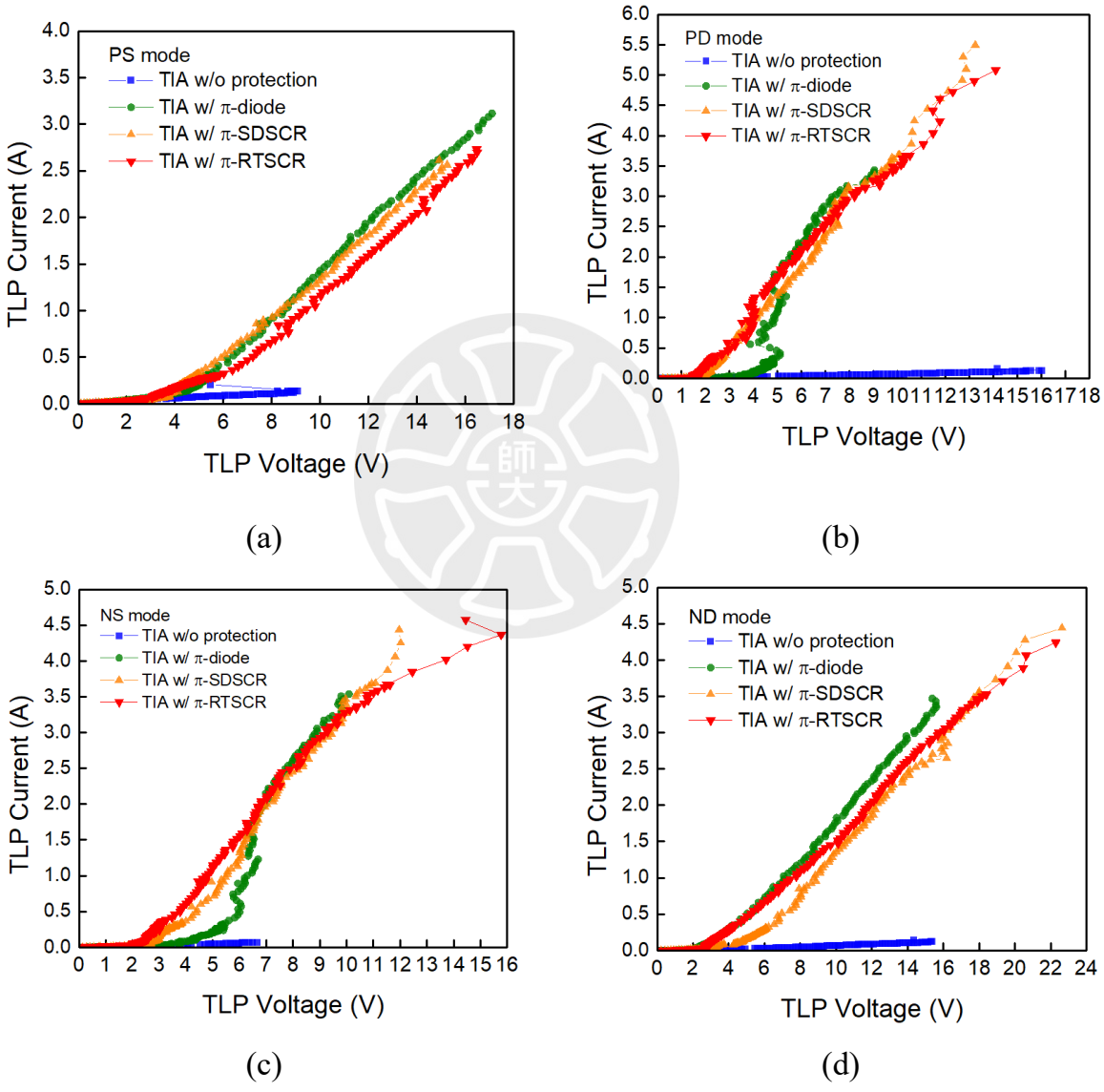


Fig. 4.20. Measured TLP I-V curves of test circuits under (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

From this measurement result, the TLP I-V curves show different turn-on resistance (R_{on}) among the TIA with traditional π-diode and those with proposed π-SDSCR and π-RTSCR. To tell the difference, when the TLP current is 1A, the voltage across the device is defined as clamping voltage (V_{Clamp_TLP}). The measured V_{Clamp_TLP} of each test circuit under four modes is listed in Table 4.2.

Table 4.2. Measured V_{Clamp_TLP} of each test circuit under four modes.

Cell Name	**V_{Clamp_TLP} (V)**			
	PS mode	**PD mode**	**NS mode**	**ND mode**
TIA w/o protection	-	-	-	-
TIA with π-diode	8.46	4.85	6.29	7.11
TIA with π-SDSCR	8.34	4.13	5.47	8.39
TIA with π-RTSCR	9.24	4.03	4.74	7.43

4.4.3 HBM Test

The ESD robustness of TIA can be learned by the HBM tests. After 0.5kV HBM test, S_{21} and S_{11} are both distorted as shown in Fig. 4.21 (a) and Fig. 4.21 (b). In addition, the noise figure rise sharply as shown in Fig. 4.21 (c). It means that TIA circuit without any protection is destroyed by ESD stress after 0.5kV HBM test.

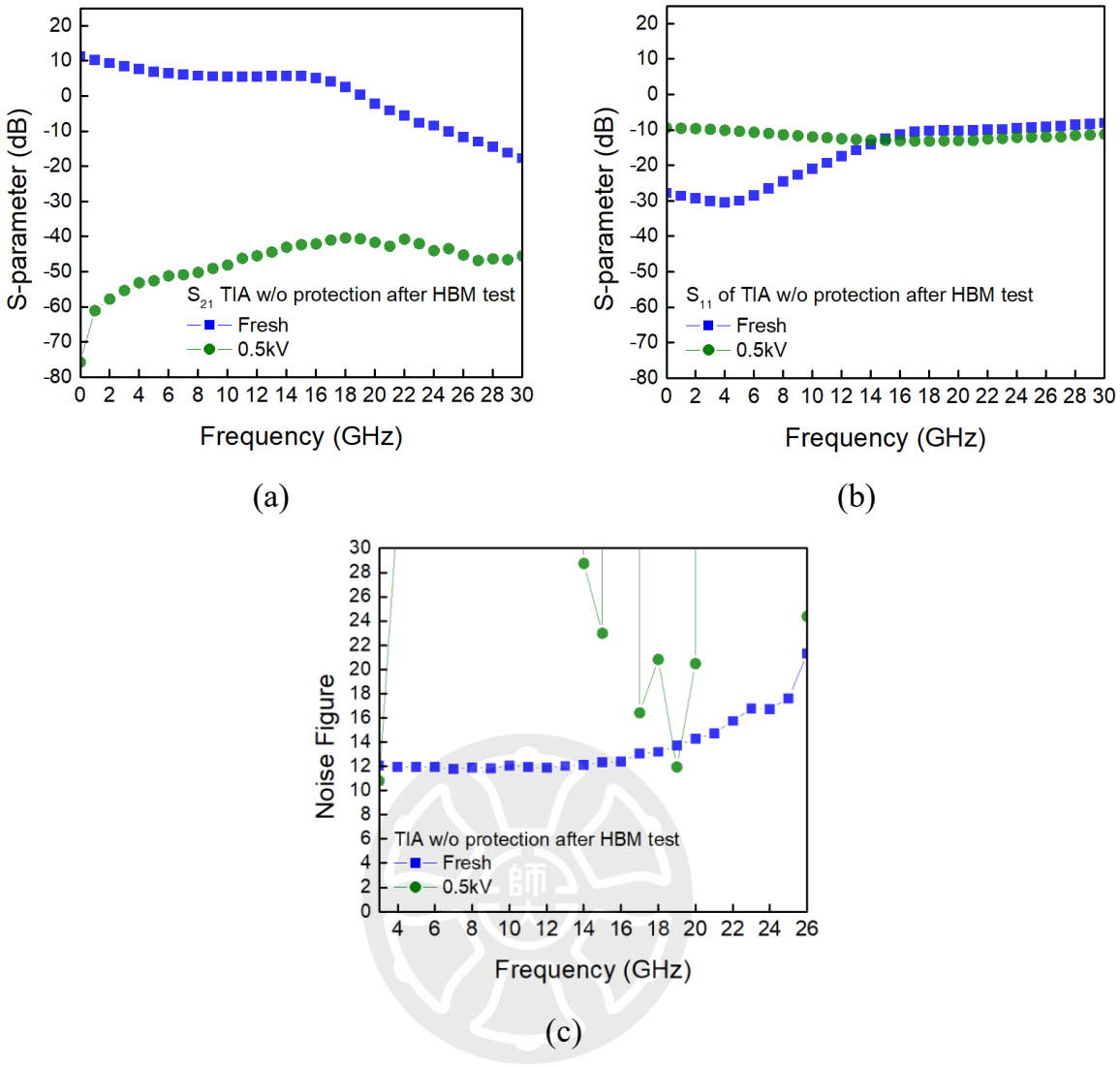


Fig. 4.21. Measured (a) S_{21} and (b) S_{11} (c) noise figure of TIA w/o protection after HBM test.

S_{21} and S_{11} of TIA with π-diode after HBM test are shown in Fig. 4.22 (a) and Fig. 4.22 (b). Measured noise figure of TIA with π-diode after HBM test is shown in Fig. 4.22 (c).

The S_{21} and S_{11} of TIA with π-diode are sustained after 4kV HBM test. However, both the S_{21} and S_{11} are distorted after 5kV HBM test, and the noise figure rises as well. The HBM level of TIA with π-diode is 4kV.

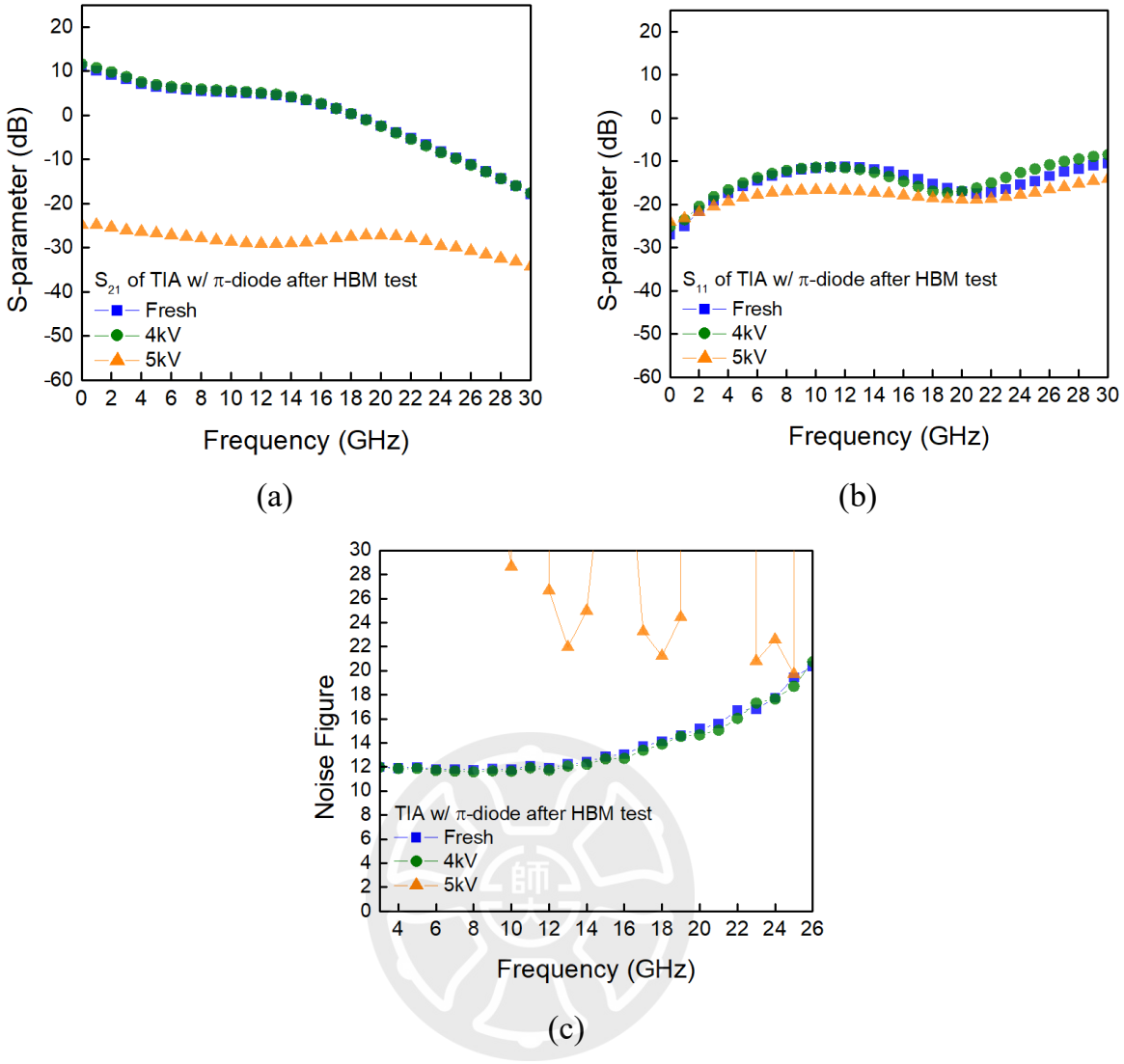


Fig. 4.22. Measured (a) S_{21} (b) S_{11} (c) noise figure of TIA with π-diode after HBM test.

S_{21} and S_{11} of TIA with π-SDSCR after HBM test are shown in Fig. 4.23 (a) and Fig. 4.23 (b). Measured noise figure of TIA with π-SDSCR after HBM test is shown in Fig. 4.23 (c).

The S_{21} and S_{11} of TIA with π-SDSCR are sustained after 4kV HBM test. However, both the S_{21} and S_{11} are distorted after 5kV HBM test, and the noise figure rises as well. The HBM level of TIA with π-SDSCR is 4kV.

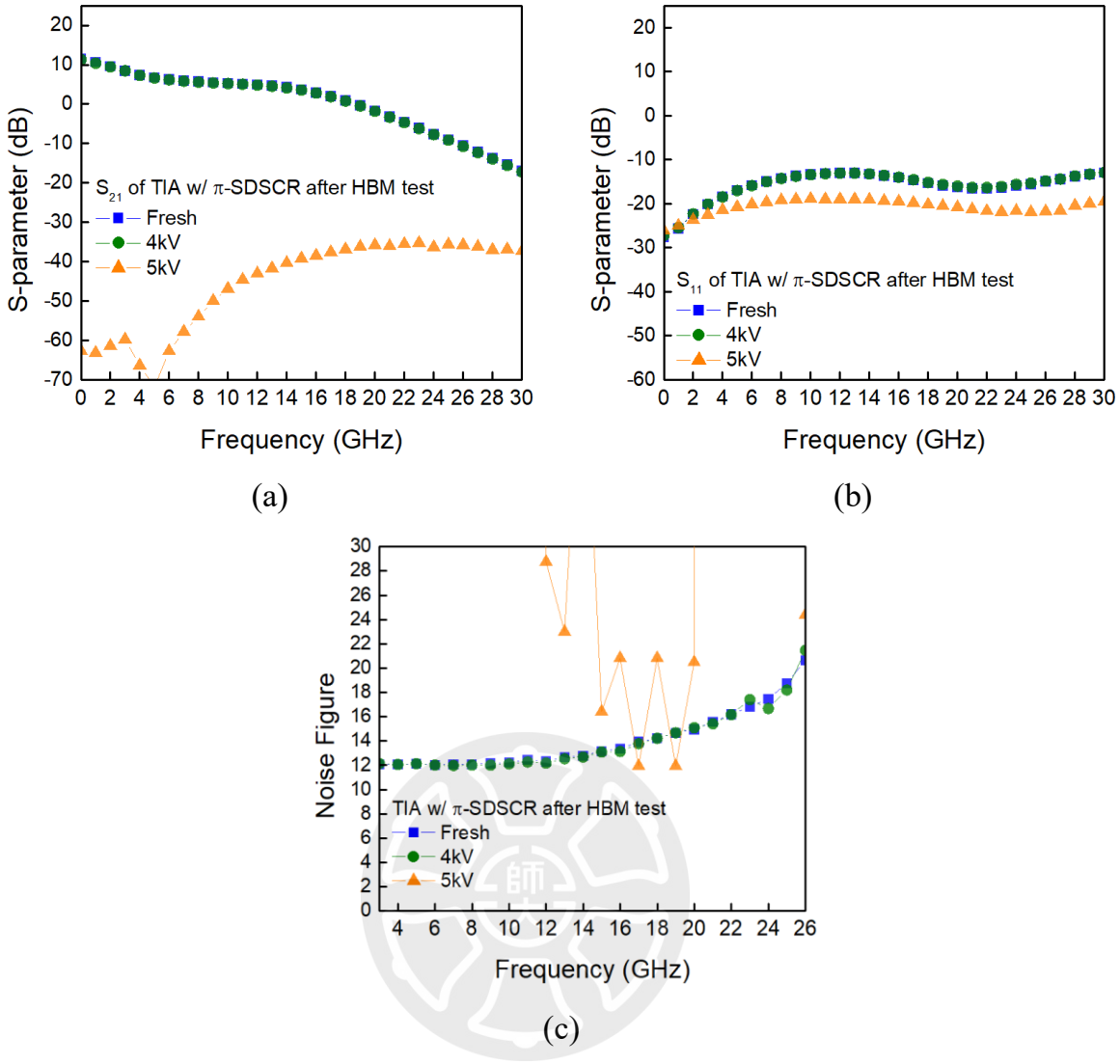


Fig. 4.23. Measured (a) S_{21} (b) S_{11} (c) noise figure of TIA with π-SDSCR after HBM test.

S_{21} and S_{11} of TIA with π-RTSCR after HBM test are shown in Fig. 4.24 (a) and Fig. 4.24 (b). Measured noise figure of TIA with π-RTSCR after HBM test is shown in Fig. 4.24 (c).

The S_{21} and S_{11} of TIA with π-RTSCR is sustained after 4kV HBM test. However, both the S_{21} and S_{11} are distorted after 5kV HBM test, and the noise figure rises as well. The HBM level of TIA with π-RTSCR is 4kV.

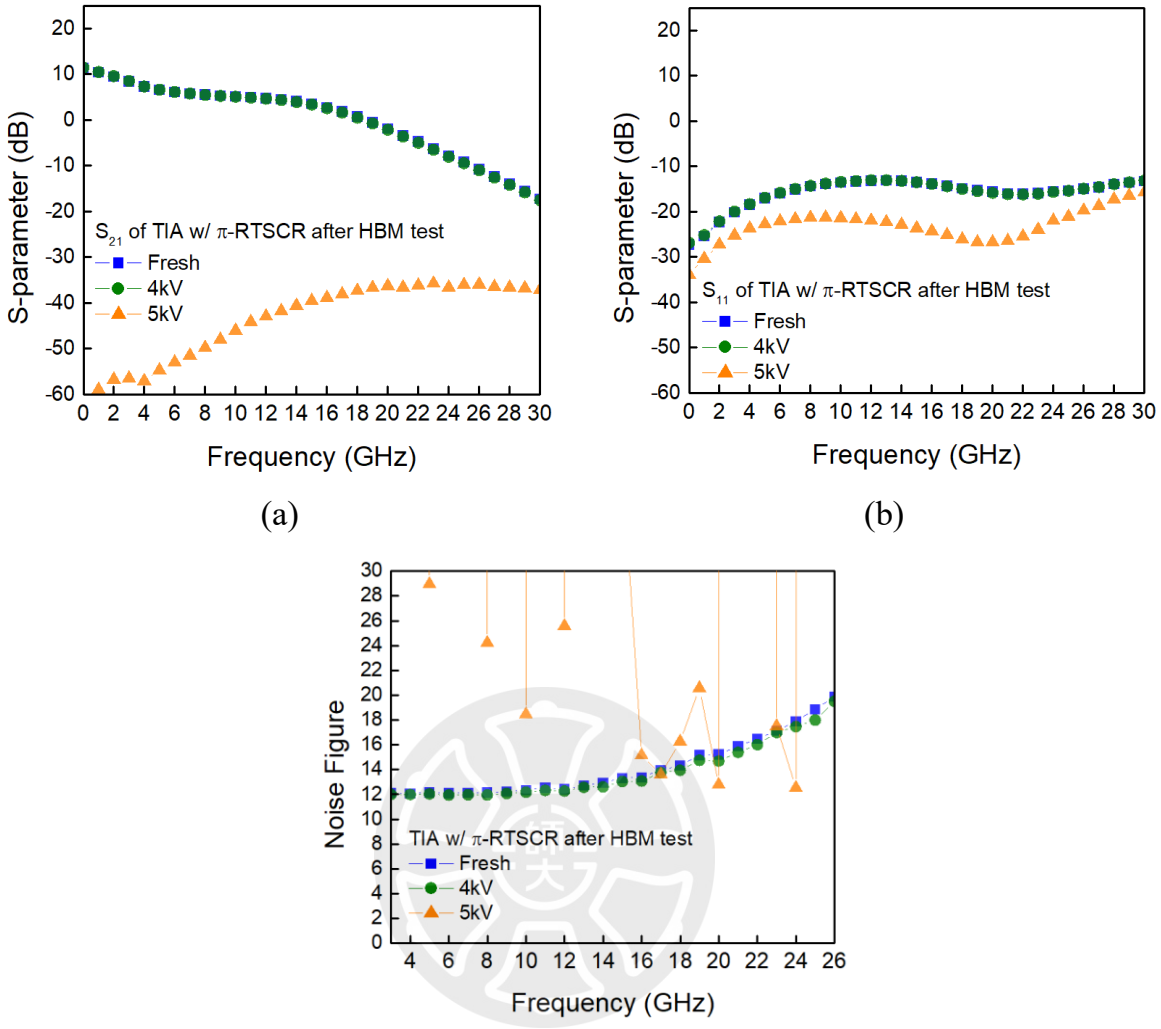


Fig. 4.24. Measured (a) S_{21} (b) S_{11} (c) noise figure of TIA with π-RTSCR after HBM test.

4.4.4 Very Fast TLP Test

Very fast TLP system is used to simulate the charged-device model (CDM) ESD stresses. The VF-TLP I-V curves of TIA w/o protection, TIA with π-diode, TIA with π-SDSCR and TIA with π-RTSCR under PS mode are shown in Fig. 4.25. When the VF-TLP current is 3A, the voltage across the device is defined as clamping voltage (V_{Clamp_VFTLP}). The measured V_{Clamp_VFTLP} of each test circuit is listed in Table 4.3.

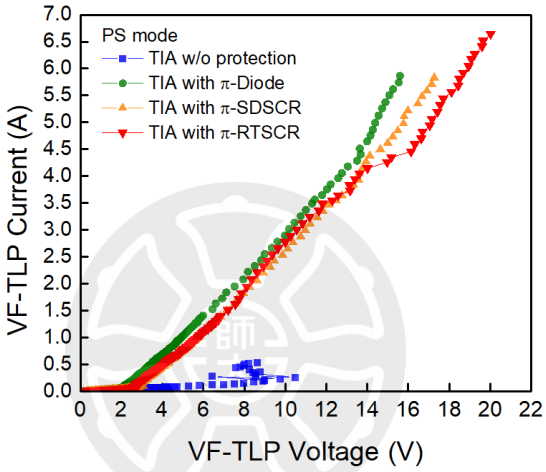


Fig. 4.25. VF-TLP I-V curves of test circuits under PS mode.

Table 4.3. VF-TLP test results

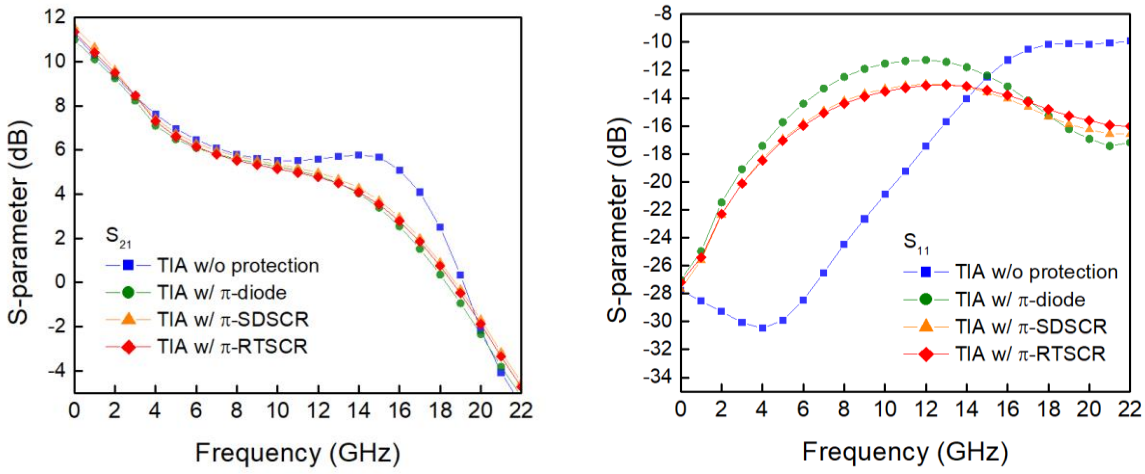
Cell name	**V_{Clamp_VFTLP} (V)**
TIA w/o protection	-
TIA with π-diode	10.19
TIA with π-SDSCR	10.97
TIA with π-RTSCR	10.56

4.5 Comparison and Discussion

As shown in Table 4.4, the layout area and the measurement results of TIA without protection, TIA equipped with traditional design and TIA equipped proposed devices are compared. Fig.4.26 shows the measured S-parameters of test circuits. With the use of ESD protection circuit, the area of whole TIA circuit increases by about 1.2 times. The S_{21} of TIA without protection is 4.10dB at 17GHz. With the use of traditional π-diode, the S_{21} at 17GHz is distorted to 1.53dB. The S_{21} at 17GHz of TIA with π-SDSCR decreased to 2.02dB and that of TIA with π-RTSCR decreased to 1.85dB. However, the TIA with proposed and traditional design still work after 4kV HBM test. The HBM level of TIA is improved from less than 0.5kV to 4kV with the use of ESD protection circuit. The proposed design is proved to have ESD protection capability on high-speed TIA with less signal distortion than the traditional design.

Table 4.4. Comparison of high-frequency applications.

Cell name	Area		HBM (kV)	S_{21} at 17GHz (dB)	S_{11} at 17GHz (dB)	ΔS_{21} at 17GHz (dB)
	ESD Device (μm^2)	Total (mm^2)				
TIA w/o protection	-	0.376	<0.5	4.10	-10.5	-
TIA with π-diode	21216	0.461	4	1.53	-14.2	-2.51
TIA with π-SDSCR	22048	0.461	4	2.02	-14.7	-2.08
TIA with π-RTSCR	22684	0.461	4	1.85	-14.3	-2.25



(a) (b)

Fig. 4.26. Measured (a) S_{21} and (b) S_{11} of test circuits

In TLP test, V_{Clamp_TLP} under each mode is measured. Lower V_{Clamp_TLP} means that there is less heat during current discharging. To compare TIA with three kinds of ESD protection circuit, there is a FOM defined as

$$FOM_{3\_TIA\_TLP} = \frac{1}{V_{Clamp\_TLP} \times |\Delta S_{21}|}$$

Where V_{Clamp_TLP} is measured clamping voltage when TLP current is equal to 1A under each mode in TLP test and ΔS_{21} is the S_{21} distortion of TIA after added ESD protection circuit. The comparison result is shown in Table 4.5 and Fig. 4.27. In PD and NS mode, V_{Clamp_TLP} of TIA with proposed π-SDSCR and π-RTSCR are lower than traditional design. That S_{21} distortion of proposed design is better than tradition one had also been proved in high-frequency measurement. As the result, the $FOM_{3\_TIA\_TLP\_PD}$ and $FOM_{3\_TIA\_TLP\_NS}$ of TIA with proposed ESD protection designs are obviously better than that of TIA with traditional π-diode. In PS and ND mode, in series with the power-rail ESD clamp circuit, the V_{Clamp_TLP} of three designs are similar but proposed designs still have advantage in high-frequency performance.

Table 4.5. Comparison table of $FOM_{3\_TIA\_TLP}$

Cell name	TIA with π-diode	TIA with π-SDSCR	TIA with π-RTSCR
V_{Clamp_TLP} of PS mode (V)	8.46	8.34	9.24
V_{Clamp_TLP} of PD mode (V)	4.85	4.13	4.03
V_{Clamp_TLP} of NS mode (V)	6.29	5.47	4.74
V_{Clamp_TLP} of ND mode (V)	7.11	8.39	7.43
ΔS_{21} (dB)	-2.51	-2.08	-2.25
$FOM_{3\_TIA\_TLP\_PS}$ ($mV^{-1}\times dB^{-1}$)	47.1	57.6	48.1
$FOM_{3\_TIA\_TLP\_PD}$ ($mV^{-1}\times dB^{-1}$)	82.1	116.4	110.3
$FOM_{3\_TIA\_TLP\_NS}$ ($mV^{-1}\times dB^{-1}$)	63.3	87.9	93.8
$FOM_{3\_TIA\_TLP\_ND}$ ($mV^{-1}\times dB^{-1}$)	56.0	57.3	59.8

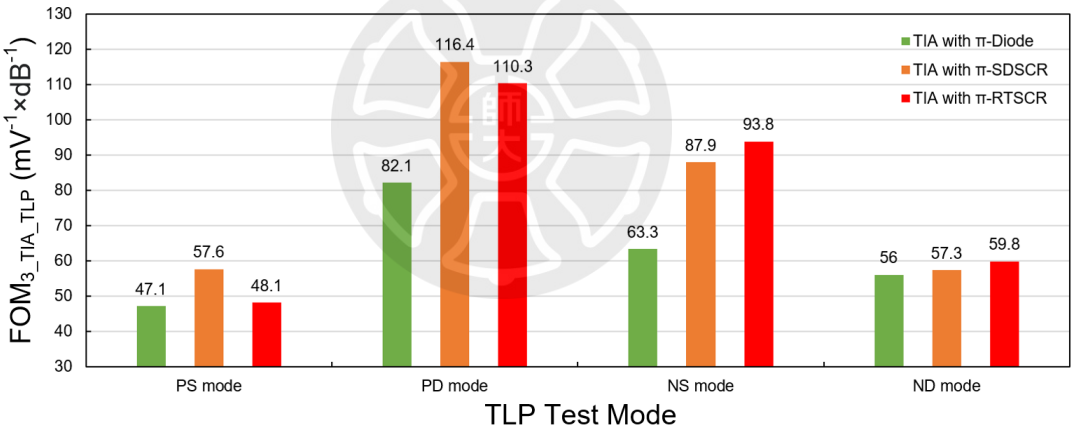


Fig. 4.27. Comparison of $FOM_{3\_TIA\_TLP}$

The discharging path under PS mode is the critical path in the whole-chip ESD protection network [34]. To learn the ESD protection capability of test circuits, VF-TLP test is measured under PS mode and the FOM is defined as

$$FOM_{4\_TIA\_VFTLP} = \frac{1}{V_{Clamp\_VFTLP} \times |\Delta S_{21}|}$$

Where V_{Clamp_VFTLP} is measured clamping voltage when VF-TLP current is equal to 3A under PS mode and ΔS_{21} is the S_{21} distortion of TIA after added ESD protection circuit. The comparison result is shown in Table 4.6 and Fig. 4.28. From the comparison table, although the V_{Clamp_VFTLP} of proposed designs are slightly higher than that of traditional design, the lower distortion of high-frequency performance still makes the proposed designs more suitable for high-speed application than traditional design.

Table 4.6. Comparison table of $FOM_{4\_TIA\_VFTLP}$

Cell name	TIA with π-diode	TIA with π-SDSCR	TIA with π-RTSCR
V_{Clamp_VFTLP} (V)	10.19	10.97	10.56
ΔS_{21} (dB)	-2.51	-2.08	-2.25
$FOM_{4\_TIA\_VFTLP}$ ($mV^{-1}\times dB^{-1}$)	39.1	43.8	42.1

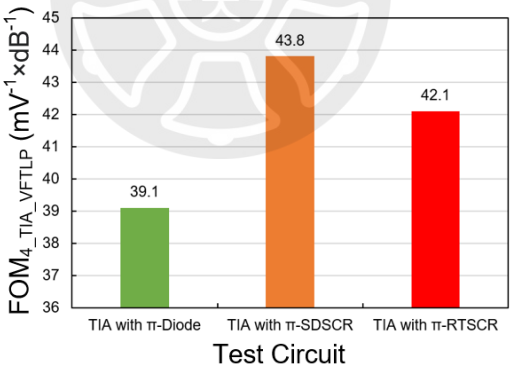


Fig. 4.28. Comparison of $FOM_{4\_TIA\_VFTLP}$

Several ESD tests are implement on the test circuits in this thesis. Fig.4.29 shows the TIA circuit in this work after ESD test. However, not all damage can be seen with the naked eyes. As the result, to figure out the real cause of the circuit failure, failure analysis (FA) can be did on the test circuits. Especially on PS and ND mode because the current discharge path is composed of more than two devices connected in series.

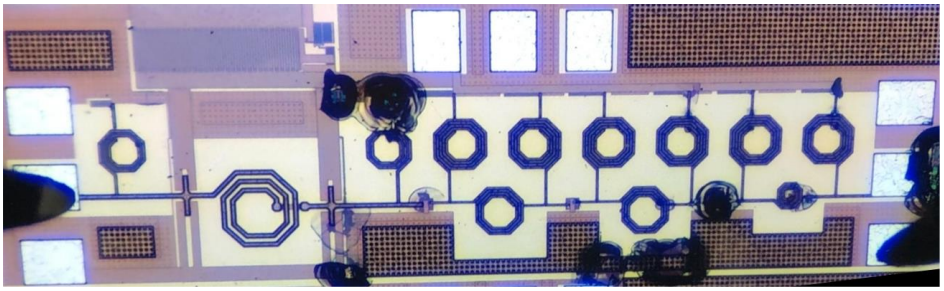


Fig. 4.29. TIA circuit after ESD test

As shown in Table 4.7, the measurement result of TIA w/o protection, TIA quipped with traditional π-diode, TIA quipped with proposed π-SDSCR and TIA quipped with π-RTSCR are compared with other TIA circuits. From the compared results, ESD robustness of TIA circuits is tested in this thesis. It is proved that TIA with proposed ESD protection design stands 4kV HBM test with a little high-frequency gain distortion.

Table 4.7. Comparison with circuits in literature

Cell name	**Process**	**Area (mm^2)**	**Bandwidth (GHz)**	**S_{21} at f_{-3dB} (dB)**	**S_{11} at f_{-3dB} (dB)**	**HBM (kV)**
TIA w/o protection	0.18μm CMOS	0.38	17	4.1	-10.5	<0.5
TIA with π-diode	0.18μm CMOS	0.46	17	1.5	-14.2	4
TIA with π-SDSCR	0.18μm CMOS	0.46	17	2	-14.7	4
TIA with π-RTSCR	0.18μm CMOS	0.46	17	1.9	-14.3	4
2008 JSSC [32]	0.18μm CMOS	0.54	31	12	-10	No provided
2016 BCTM [35]	0.25μm BiCMOS	0.32	32	2	-5	No provided
2008 PTL [36]	0.18μm CMOS	0.51	7.6	37	No provided	No provided
2018 MWCL [37]	0.13μm BiCMOS	0.36	72	19	-30	No provided
2019 JSSC [38]	65nm CMOS	0.6	40	7	-20	No provided

4.6 Summary

In this chapter, a three-stage cascaded TIA applied in high speed is designed. And a traditional and two proposed ESD circuits are equipped in TIA circuit respectively. The simulation and measurement results are shown. The high-frequency performance of TIA without protection is distorted after the 0.5kV HBM test. With the use of ESD protection, the high-frequency performance of TIA has little distortion. However, the whole-chip ESD protection can be realized. TIA with π-diode, π-SDSCR and π-RTSCR stands 4kV HBM test.

In this work, traditional π-diode, proposed π-SDSCR and π-RTSCR with TIA are fabricated in 0.18μm CMOS. Based on the measurement results, proposed devices are able to protect the high-speed circuits from ESD damage with less distortion. It is proved that the proposed designs have lower clamping voltage under PD and NS mode. Under the critical PS mode, propose designs also have low enough clamping voltage to protect TIA circuit.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In the beginning of this thesis, the background of ESD protection design and related test standards and specifications are introduced. Several studies about ESD protection design of high-speed application are present in the following chapter. The parasitic effect of ESD protection device at high frequency must be considered. Distributed circuit is a common way for broadband circuit.

In chapter 3, two different SCR devices with distributed circuit structure are proposed as π-SDSCR and π-RTSCR. The proposed designs are compared with the traditional π-diode and π-MOS. Both proposed designs and traditional designs are fabricated in 0.18μm CMOS process. From the measurement results, proposed designs have higher ESD robustness per unit layout area than traditional designs. In addition, in the similar high-frequency performance, proposed designs also have better ESD robustness. It means proposed designs can provide same ESD level with a lower parasitic capacitance.

In chapter 4, traditional π-diode and proposed π-SDSCR and π-RTSCR are verified in a high-speed TIA. The measurement results proved that the high-frequency performance of TIA can be maintained with the use of proposed ESD protection designs. Moreover, TIA with π-SDSCR and π-RTSCR still work after 4kV HBM test. With the lower high frequency performance distortion, proposed designs are more suitable for high-speed application than traditional design.

5.2 Future Work

There is a high-speed TIA designed in this work to verify the protection ability of the propose ESD protection designs. However, the gain of TIA can be further improved. To consider the parasitic resistance of inductors, the resistance of drain resistors and matching resistors (R_D, R_1-R_4) are changed slightly. With further adjustment, the S-parameter of re-designed TIA is shown in Fig. 5.1.

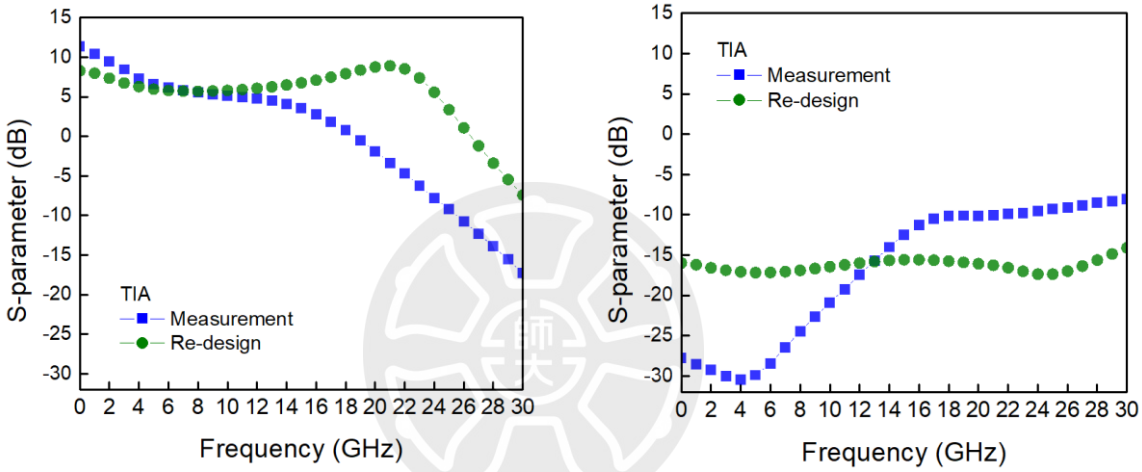


Fig. 5.1. The measured and re-designed (a) S_{21} and (b) S_{11} of TIA.

This work combined several ESD protection devices with the concepts of distributed circuit to realize the ESD protection for broadband circuit and made a comparison. From the results, the ESD robustness of proposed designs is limit by PS mode which is the critical path of whole-chip ESD protection network. To achieve a faster turn-on speed during PS mode, an innovation device called LCSCR is proposed [39]. The scheme of LCSCR is shown in Fig. 5.2 and the cross-section view of LCSCR is shown in Fig. 5.3.

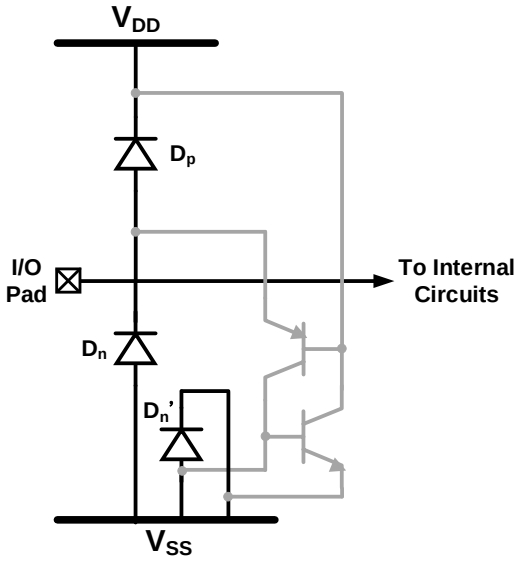


Fig. 5.2. The scheme of LCSCR [34]

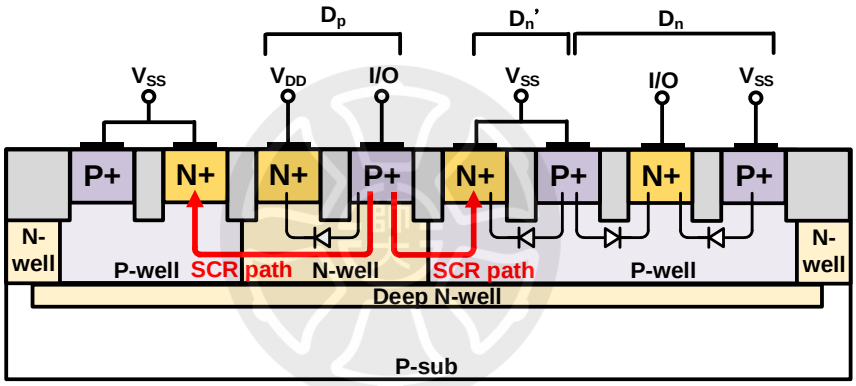


Fig. 5.3. The cross-section view of LCSCR [34]

Through a dummy diode D_n' inserted between D_p and D_n formed an SCR path. During PS mode ESD events, the conduction of D_p triggers the LCSCR and creates a shunting discharging path directly from I/O pad to ground to provide faster turn-on. The π-structure can be adopted to further reduce the parasitic capacitance. The whole-chip ESD protection circuit with π-LCSCR is shown in Fig. 5.4.

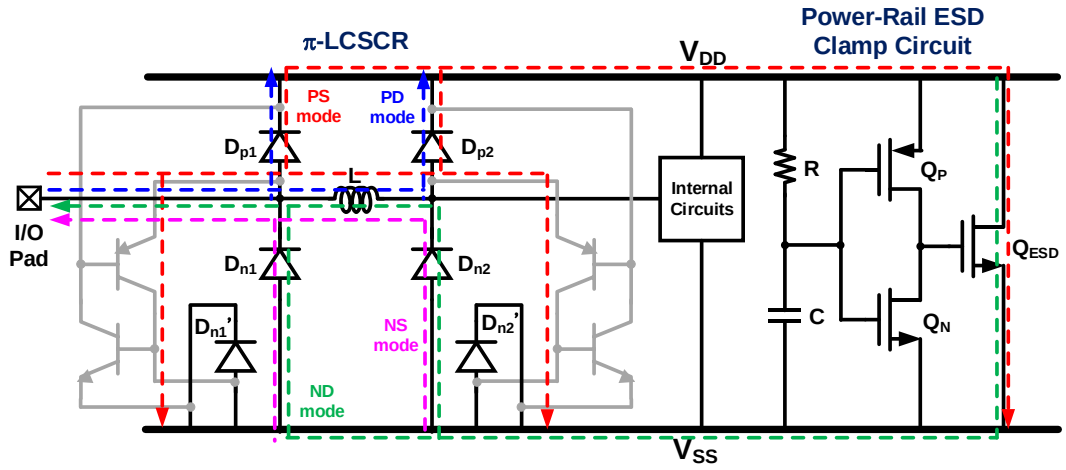


Fig. 5.4. The whole-chip ESD protection circuit with π-LCSCR

For further higher frequency application, lower parasitic capacitance is necessary. As compare with diode, SDSCR devices provide higher ESD robustness per unit parasitic capacitance. As the result, the second stage of π-LCSCR (D_{p2}、D_{n2} and D_{n2}') can be replace by dual-SDSCR to lower the parasitic capacitance. The LCSCR at first stage is retained to provide a fast turn-on discharging path of PS mode. An inductor is also used as a matching element between two stages to reduce the parasitic effect. The whole-chip ESD protection circuit with LCSCR and dual-SDSCR is shown in Fig. 5.5.

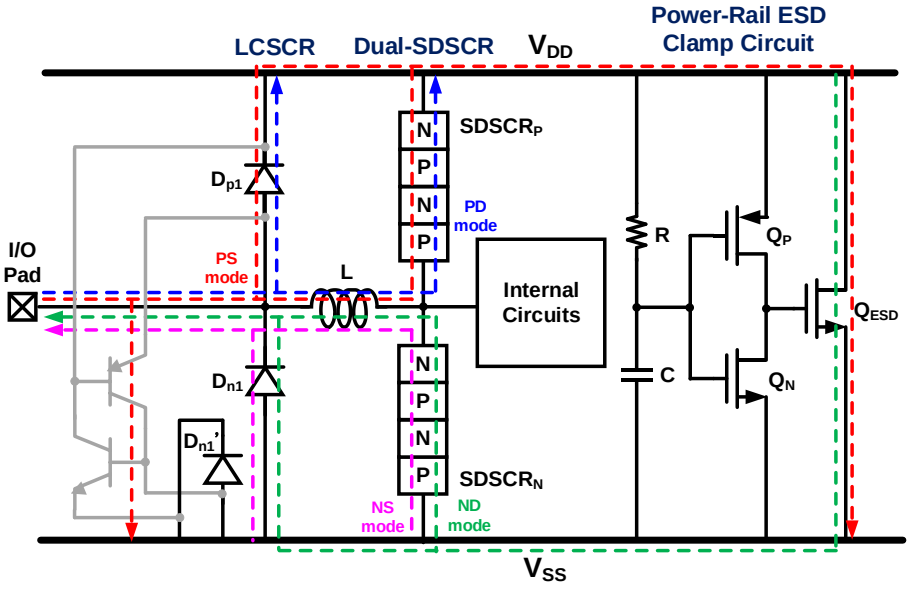


Fig. 5.5. The whole-chip ESD protection circuit with LCSCR and dual-SDSCR

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