國立臺灣師範大學科技與工程學院電機工程學系

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應用於高頻輸入/出端與電源端之靜電放電防護設計

ESD Protection Design for High-Frequency Input/Output Terminal and Power Terminal Application

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摘　　要

隨著 CMOS 製程越來越先進，電晶體尺寸微縮，使可操作於更高的工作頻率，但會使電晶體對於靜電越來越敏感，靜電放電是影響積體電路可靠度的主要因素，須設計出高耐受度的靜電放電防護電路，避免積體電路遭受靜電轟擊而損壞。

靜電放電防護通常設計於輸入/出端，當應用於高頻積體電路中，須具備較低的寄生電容，否則會影響高頻電路的特性，而傳統防護元件選擇簡單的二極體，但操作頻率越來越高時，造成高頻電路特性大幅衰減，因此本論文提出藉由電阻串並聯方式使二極體產生的負載減少，並採用 CMOS 製程實踐，透過各項量測證實在單位面積下有低的高頻訊號流失和擁有足夠高的靜電放電防護能力。

因靜電也會由電源端進內部電路，所以必須有電源箝制防護電路，而電源箝制防護電路中的觸發機制被用來判斷靜電是否發生，但當內部電路上電的時間常數與靜電相近時，電阻-電容充放電機制會使排放靜電的元件意外導通，造成電源端的訊號極大流失。因此，本論文使用 CMOS 製程實踐現有電源箝制電路，分析不同的靜電放電耐受度測試、正常上電與快速上電時的可行性。

關鍵字：靜電放電、高頻、寄生電容、靜電放電箝位電路、正常上電源、快速上電源

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ABSTRACT

The manufacturing process becomes more advanced for high-frequency applications than before. However, the transistor is sensitive to static electricity. Therefore, it is necessary to design an electrostatic discharge (ESD) protection circuit with high ESD robustness to prevent the integrated circuit from being damaged by ESD current bombardment.

The ESD protection device is usually designed at the input/output pad. When the internal circuits are operated at high frequency, the ESD protection device should have low parasitic capacitance. Otherwise, the ESD protection device will affect the character of the high-frequency circuit. Though the simple diodes are chosen as traditional protection component, they will cause severe signal loss at higher frequency. Therefore, the thesis proposed the RC-diode ESD protection device that is adopted CMOS process to reduce signal loss through the resistor series and parallel method. As a result, the RC-diode protection device has outstanding ESD robustness and low signal loss per unit

area by various testing.

Because the static electricity will also enter the internal circuit from the power supply terminal, the power-rail ESD clamp circuit is essential. The trigger mechanism in power-rail ESD clamp circuit is used to determine whether the static electricity occurs. However, the time constant of the internal circuit power-on and static electricity is close, the resistor-capacitor inverter mechanism will accidentally trigger the components of discharge current to cause significant power loss at the power supply terminal. Therefore, this thesis has adopted the CMOS process to fabricate present power-rail ESD clamp circuits for internal circuit. These power-rail ESD clamp circuits are analyzed under different testing methods of ESD robustness and discussed for internal circuit of normal and fast power-on feasibility.

Keyword：electrostatic discharge (ESD), high-frequency, parasitic capacitance, power-rail ESD clamp circuit, normal power-on, fast power-on.

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傅義全 謹誌於師大

中華民國一一零年十月

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Chapter 1

Introduction

1.1 Motivation

As semiconductor technology advances to the nanometer regime, the short channel length and shallow junction make the transistor achieve high frequency and low power consumption [1]. Unfortunately, the electrostatic discharge (ESD) protection ability has become one of the critical concerns on the reliability of integrated circuit products [2], [3]. With the development of electronic communication products, CMOS technologies have been used to implement radio-frequency integrated circuits (RFICs). However, static electricity usually occurs in input/output terminals. ESD protection circuits are essential to prevent overvoltage problem [4], [5]. When operating frequency increases gradually, the ESD protection device can cause significant signal loss [6]. In order to avoid attenuating the high-frequency characteristics, the parasitic capacitance effects must be considered for different applications such as low-noise amplifier (LNA) circuit and RF power amplifier (PA) circuit [7].

Besides, to keep an excellent whole-chip ESD protection for internal circuits, it is also required to design the power-rail ESD clamp circuits for power location. This ESD clamp circuit should not be accidentally turned on when the internal circuit is work, and it should be operated when static electricity occurs [8].

Therefore, the ESD protection design is a severe challenge for nanoscale complementary metal-oxide-semiconductor (CMOS) technology. The thesis proposes ESD protection devices for high-frequency circuits and studies power-rail ESD clamp circuits for various situations.

1.2 Background of ESD

When the electric potential of the objects is unbalanced and contacted on the surface, a phenomenon happens that the electric charge transfers between two different objects. ESD current generates high current about several amperes (A) in nanoseconds immediately. With the advantage of nanoscale CMOS technology, such as scaling-down feature size, improving circuit performance and reliability of IC products have been the ultimate task in the IC industry. However, the electronic equipment and semiconductor devices can cause permanent damage because the ESD owns powerful electricity. When the IC is affected by the ESD event, the temperature of the IC rises to lead to metal and silicon burned out. So, the integrated circuits are susceptible to ESD stress, and ESD protection circuits play an important role in solving high ESD current issues [9].

1.3 Component-Level Test Standards of ESD

Nowadays, before commercial electronic products are exhibited, they must be tested for ESD tolerance. Therefore, manufacturers are necessary to comply with the standard [10], [12]. Some related organizations, such as Joint Electron Device Engineering Council (JEDEC), Automotive Electronics Council (AEC), and US Military Standard (MIL-STD), have constructed standards for the ESD tests. According to the different discharge methods of ESD, component-level tests include Human-Body Model (HBM), Machine Model (MM), and Charged-Device Model (CDM). Since the HBM test and the MM test have a positive correlation, the MM has not attended in recent years. The following is equivalent circuit diagram and detailed description of HBM and CDM.

1.3.1 Human-Body Model (HBM)

The model of HBM is shown in Fig. 1.1. The equivalent circuit consists of 100pF capacitor and 1.5kΩ resistor. During the HBM test, the 100pF capacitor will be charged and then discharge through a 1.5kΩ resistor into the device under test. The standard simulates the human body rubs against the ground, and it causes static electricity storage on the human body. Then, the body comes into contact with the device, and there will be a discharge path and risk of damage to it. The ANSI/ESD STM5.1 of the ESD Association classifies three types according to the protection level in Table 1.1 [10].

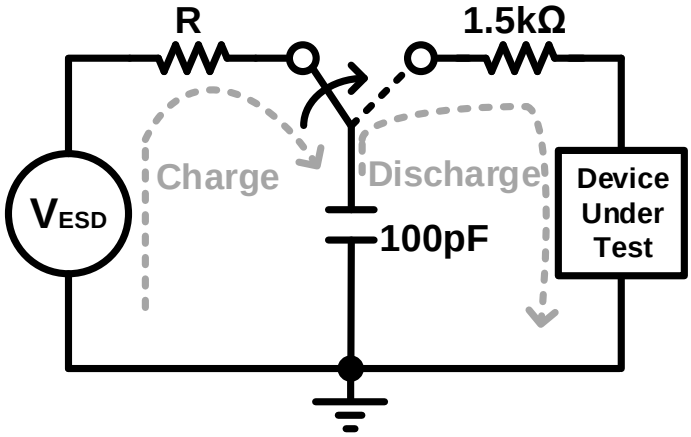


Fig. 1.1. The equivalent circuit of HBM.

Table 1.1. The protection level classification of HBM.

Class	Voltage Range
0	250V
1A	250V to 500V
1B	500V to 1000V
1C	1000V to 2000V
2	2000V to 4000V
3A	4000V to 8000V
3B	8000V

1.3.2 Charged-Device Model (CDM)

The integrated circuits are rubbed to generate static electricity during the manufacturing process and transportation. Once an external ground touches the pin of the IC, the stored charge of the IC will be discharged from the inside of the IC to the outside ground [11]. The model of CDM is shown in Fig. 1.2. The CDM event is more difficult to reproduce through a tester than the HBM and MM events. The ANSI/ESD STM5.3.1 of ESD Association is classified based on the ESD protection level in Table 1.2 [12].

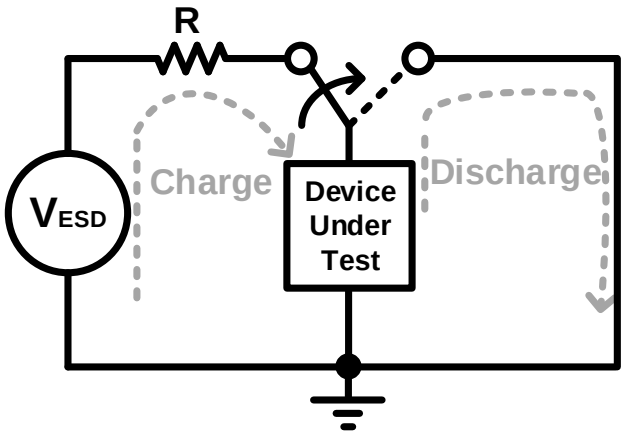


Fig. 1.2. The equivalent circuit of CDM.

Table 1.2. The protection level classification of CDM.

Class	Voltage Range
C1	150V
C2	150V to 250V
C3	250V to 500V
C4	500V to 1000V
C5	1000V to 1500V
C6	1500V to 2000V
C7	2000V

1.4 Consideration of Designing Whole-Chip ESD Protection Circuits

Electrostatic discharge (ESD) protection circuit is mainly used to prevent external ESD stress for IC products. Because the pins of integrate circuits are quickly struck by external static electricity, the ESD protection circuit is placed around the input and output (I/O) pads to discharge the ESD current. There are four discharge path such as positive I/O-to-V_{SS} (PS-mode), positive I/O-to-V_{DD} (PD-mode), negative I/O-to-V_{SS} (NS-mode), and negative I/O-to-V_{DD} (ND-mode). The power bus lines are also pretty crucial for overall ESD immunity. Therefore, the power-rail ESD clamp circuit between V_{DD} and V_{SS} effectively is used to provide an ESD discharge path before ESD current flows internal circuit. As noted above, the traditional ESD protection architecture will be detailed to introduce in the next section. The typical whole-chip ESD protection proposal is demonstrated with the power-rail ESD clamp circuit in Fig. 1.3 [13].

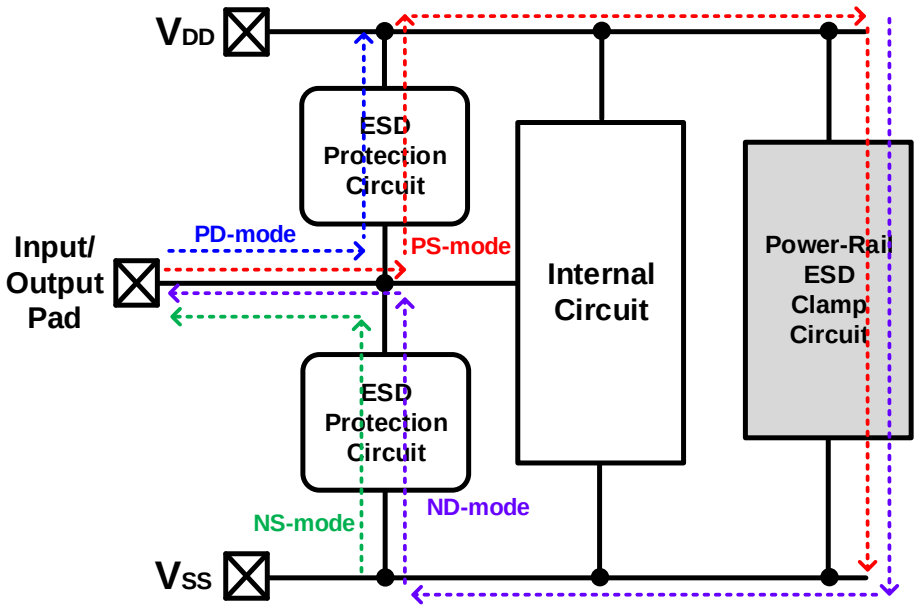


Fig. 1.3. Typical whole-chip ESD protection design.

1.4.1 ESD Protection Design Window

When the ESD protection circuit is designed, it is essential to realize the working specification. Therefore, the design window of the ESD protection circuit is established in Fig. 1.4. The internal circuit operates typically between the power supply voltage (V_{DD}) and ground (V_{SS}), and the boundaries of the ESD protection circuit must turn on between V_{DD} and gate-oxide breakdown voltage (V_{BD}). Besides, the trigger voltage (V_{t1}) of protection circuit must be lower than the breakdown voltage. Otherwise, the internal circuit causes failure by ESD current before the protection circuit is operated. Some previous protection circuits have a snapback phenomenon. The holding voltage (V_h) must be higher than V_{DD} to avoid occurring latch-up. The turn-on resistance (R_{on}) of the protection circuit will expect to minimize power accumulation. Finally, secondary breakdown current (I_{t2}) means that maximum ESD current the protection circuit can withstand [14].

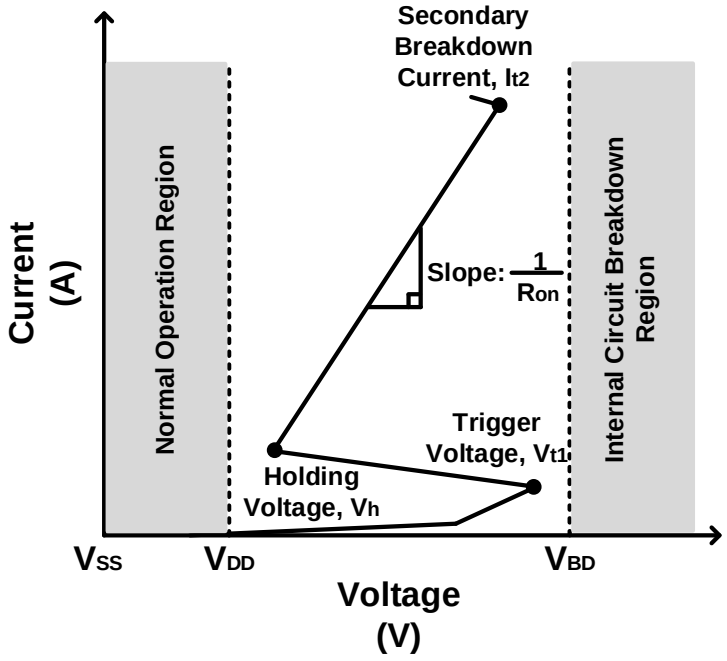


Fig. 1.4. ESD protection design window.

1.5 ESD Protection Components for High-Frequency Application

In recent years, commercial mobile and wireless applications develop fast, which leads to operating frequencies increase. The RF circuits are susceptible to ESD in CMOS technologies that causes circuits failure. As shown in Fig. 1.5, the ESD protection circuits are connected to the RF_{IN} pad and RF_{OUT} pad against ESD damages. However, the additional ESD protection circuit makes the performance of RF internal circuits attenuate. Because the ESD protection circuit has parasitic capacitance, parts of the RF signal are transferred to the ground (Vss) at high frequency. Moreover, the parasitic capacitance also changes the input matching network condition. Consequently, designing an ESD protection device needs special design consideration [15]. The following is introduction that common ESD protection circuits apply to high frequency.

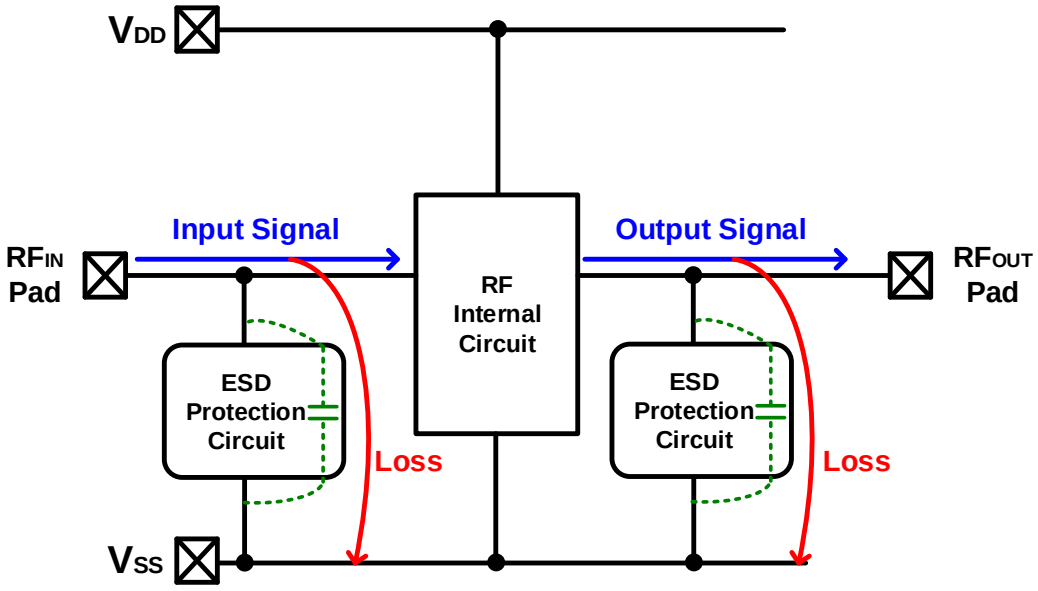


Fig. 1.5. RF signal loss at RF_{IN}/RF_{OUT} pads with ESD protection devices.

1.5.1 Dual Diodes [16]

The forward-biased diodes play good capabilities of ESD protection. As shown in Fig. 1.6, it is double-diode topology that consists of P-type diode (D_P) and N-type diode (D_N). In addition, the power-rail ESD clamp circuit assists in preventing ESD current to RF internal circuit. Therefore, under positive static electricity occurs at input or output pad with grounded V_{DD}, ESD current is discharged through the P-type diode (PD-mode). On the other hand, when negative static electricity emerges at input or output pad with grounded V_{SS}, the N-type diode provides a discharge path (NS-mode). Furthermore, ESD current is discharged from the input or output pad through a P-type diode and power-rail ESD clamp circuit to V_{SS} (PS-mode). Similarly, ESD current flows path from the V_{DD} through power-rail ESD clamp circuit and N-type diode to input or output pad (ND-mode). However, this structure is suitable for small ESD robustness level because the dimension of diode affects the performance of RF internal circuit.

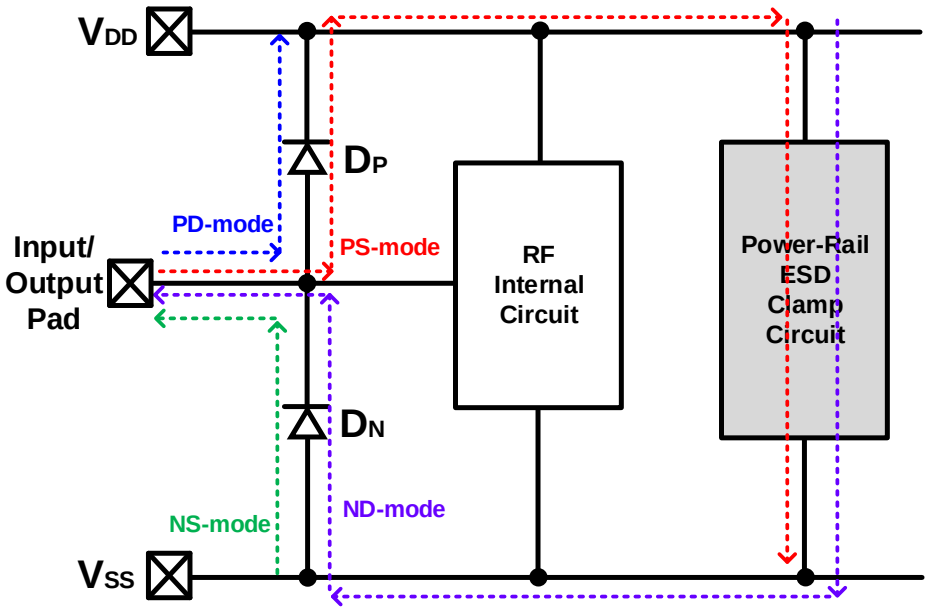


Fig. 1.6. ESD Protection design with dual diodes.

1.5.2 Dual Stacked Diodes [17]

In order to reduce the parasitic capacitance of ESD protection devices without sacrificing ESD tolerance level, the ESD protection circuit is presented by stacked configuration. As a result, the equivalent parasitic capacitance theoretically becomes only half of each ESD protection device. As shown in Fig. 1.7, the two P-type diodes (D_{P1} and D_{P2}) are placed between the input or output pad and V_{DD} in series. The two N-type diodes (D_{N1} and D_{N2}) are similarly placed between V_{SS} and input or output pad in series. With a power-rail ESD clamp circuit, the whole discharge paths are the same as those of the above dual-diodes structure. The architecture leads to more significant parasitic capacitance reduction. However, the diodes cannot be stacked unlimited because this technique can increase the turn-on resistance (R_{on}) and trigger voltage (V_{t1}) of the ESD protection circuit. If the ESD protection circuit cannot turn on in time, the RF internal circuit may be burned out by static electricity.

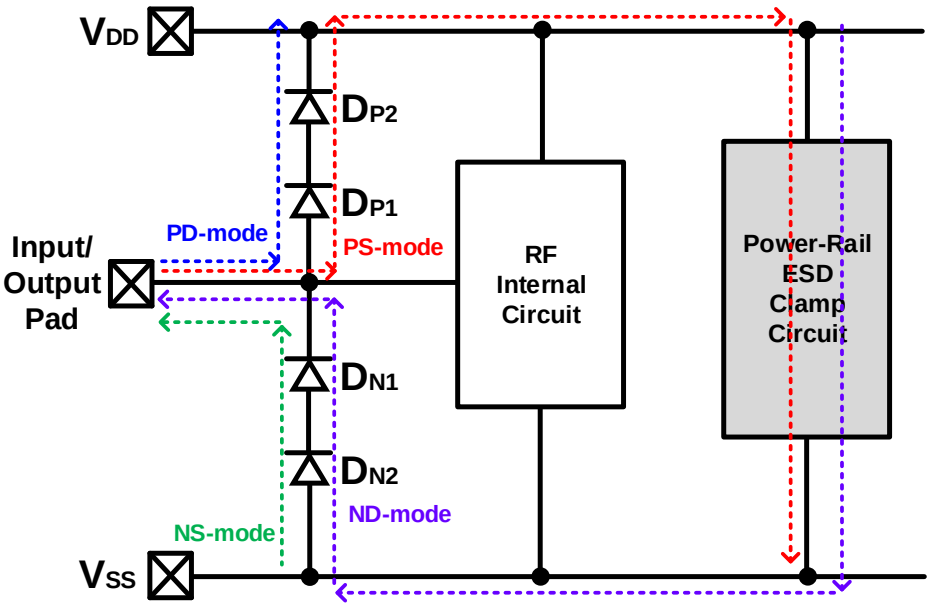


Fig. 1.7. ESD Protection design with dual stacked diodes.

1.5.3 LC Tanks [18]

As shown in Fig. 1.8, the ESD protection circuit is placed in the input or output pad. The LC-tanks ESD protection circuit is consisted of the inductor (L_P and L_N), the parasitic capacitance of the diode (D_{P1} and D_{N1}), and the ESD diode (D_{P2} and D_{N2}). Adding a power-rail ESD clamp circuit forms a whole-chip ESD protection circuit. The technique reduces the parasitic capacitance by using LC parallel resonator theorem. At the resonant frequency, the ESD protection circuit makes signal loss is ideally zero, which means the equivalent parasitic capacitance is zero. Furthermore, the inductor can mitigate the impact on the RF internal circuit and provide an ESD protection device. Nevertheless, the LC-tanks ESD protection circuit applies to commercial products that will cause higher costs because the inductor occupies a more extensive layout area than dual-diode architecture and dual-stacked diodes architecture.

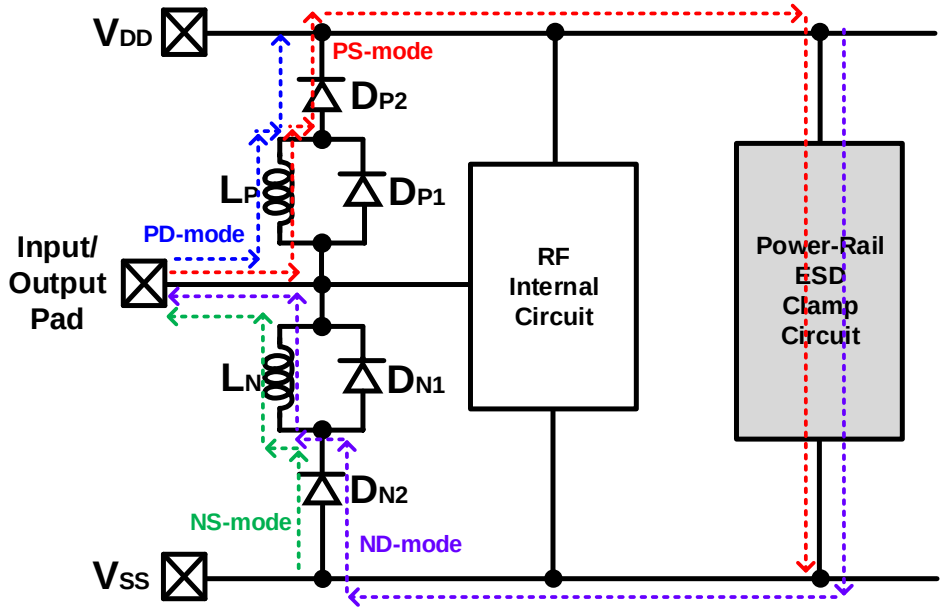


Fig. 1.8. ESD Protection design with LC tanks.

1.6 Power-Rail ESD Clamp Circuits

Because electrostatic discharge consists of a spiked current of several amperes in a short time about nanoseconds, ESD has become a significant reliability issue in the modern integrated circuits industry. The ESD protection component is placed around the input or output pad that is incomplete. As shown in Fig. 1.9, to provide the practical whole-chip ESD protection circuit for the internal circuit, the power-rail ESD clamp circuit plays a vital role between the power lines pad (V_{DD}) and ground pad (V_{SS}). The principal discharge component of the power-rail ESD clamp circuit usually chooses NMOS of a large size (M_{ESD}). Before the internal circuit is damaged, the M_{ESD} should be turned on by the ESD transient mechanism circuit. The ESD transient mechanism circuit can detect the ESD event and convey high-level voltage to the gate of M_{ESD}. When the normal operating voltage provides to the V_{DD} pad, this gate of M_{ESD} should obtain low-level voltage from ESD transient mechanism.

The rise time of normal power-supply voltage is about milliseconds during regular operation. The ESD transient mechanism of the present power-rail ESD clamp circuit architectures judges the rise time of normal operating voltage and static discharge voltage differently to control the gate of $M_{ESD.}$ However, in some conditions, such as a hot plug-in, the rise time is as quick as static electricity about nanoseconds called the fast power-on event. Some design methods will cause the problem of M_{ESD} false triggering and great power dissipation. This research will analyze four power-rail ESD clamp circuit architectures in detail in Chapter 3.

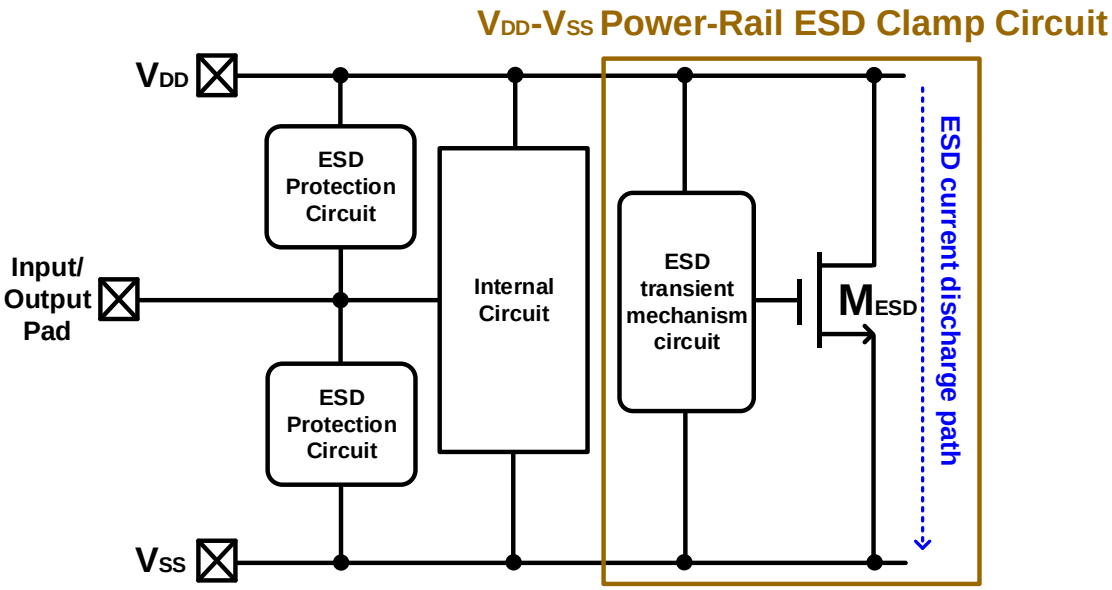


Fig. 1.9. Power-rail ESD clamp circuit with transient mechanism circuit.

1.6.1 Power-Rail ESD Circuit with Resistor-Capacitor Inverter Mechanism [19]

A typical power-rail ESD clamp circuit with resistor-capacitor inverter mechanism is shown in Fig. 1.10. The power-rail ESD clamp circuit is formed with a control circuit of resistor-capacitor mechanism, an inverter gate, and a large-size NMOS transistor (M_{ESD}). During the positive ESD voltage applied to the V_{DD} node, the ESD clamp NMOS transistor is commanded to turn on. The turn-on time of the ESD clamp NMOS can be adjusted by the RC-time constant of the resistor-capacitor mechanism. As a result, to reach the desired operation, the RC-time constant's rise time is designed approximately microseconds (μs). However, the rising time of the operating voltage on the V_{DD} node may like the rising time of the ESD to cause some mis-triggered on the ESD clamp NMOS transistor. The mis-triggered event will affect the function and reliability of internal circuits. In order to overcome the problem, another solution method is presented in the next part.

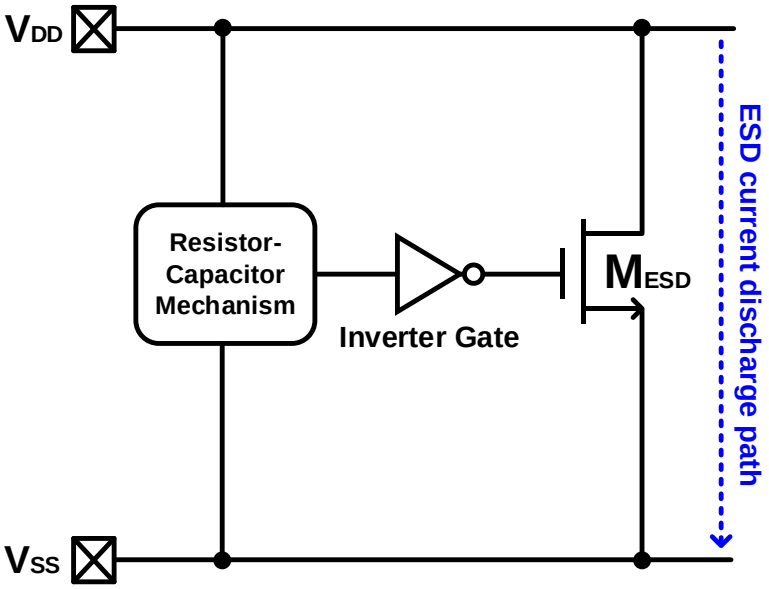


Fig. 1.10. Power-rail ESD clamp circuit with resistor-capacitor inverter.

1.6.2 Power-Rail ESD Circuit with Diode-Trigger Mechanism [20]

As shown in Fig. 1.11, the power-rail ESD clamp circuit consists of the diode-trigger control circuit, inverter gate, and a large-size NMOS transistor (M_{ESD}). The diode-trigger mechanism of the power-rail ESD clamp circuit was used to detect the voltage level of the V_{DD} node. When the voltage on the V_{DD} node is larger than the turn-on voltage level of the diode-trigger control mechanism, the diode-trigger mechanism can output a low voltage. At the same time, the gate of the NMOS transistor (M_{ESD}) can be converted to high level by the inverter gate, and then the M_{ESD} is trigged to discharge ESD current. During normal operating conditions, the operating voltage level on the V_{DD} node must be lower than the turn-on voltage of the diodes-trigger control mechanism to let the M_{ESD} in the OFF state. Though the power-rail ESD clamp circuit cannot happen mis-triggering at the fast power-on event, the diode string often suffered a leakage issue in the high-temperature environment.

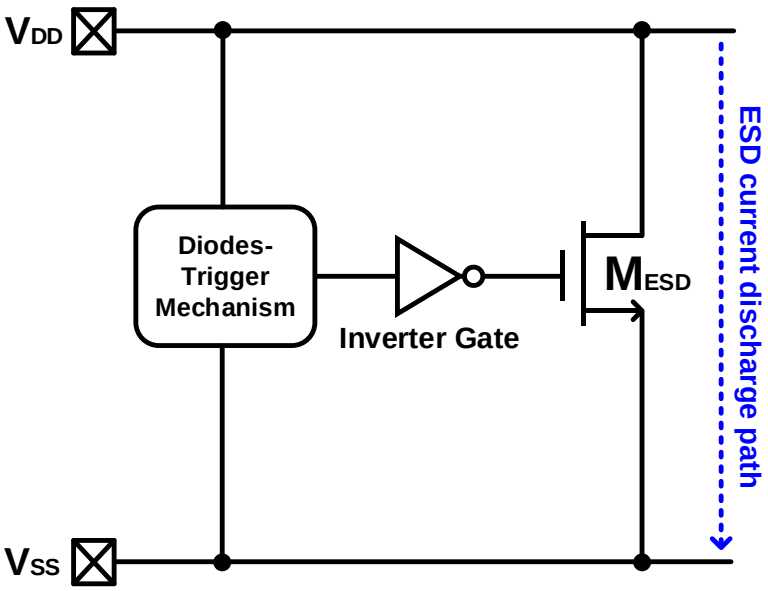


Fig. 1.11. Power-rail ESD clamp circuit with diode trigger.

1.6.3 Power-Rail ESD Circuit with Positive-Feedback Mechanism [21]

As shown in Fig. 1.12, the power-rail ESD clamp circuit consists of a positive-feedback control circuit and a large-size NMOS transistor (M_{ESD}). The positive-feedback control circuit with feedback technique is assembled by the diode, resistance, PMOS transistor, and NMOS transistor. The ESD clamp NMOS transistor is necessary to be turned on when the positive ESD voltage occurs at V_{DD} node. The ESD current flows through the drain-gate parasitic capacitance (C_{gd}) of the large-size NMOS transistor to cause voltage upward of the NMOS transistor (M_{ESD}) gate. By the positive-feedback control circuit, the voltage level of NMOS transistor (M_{ESD}) gate can be continuously elevated during ESD event. Therefore, the NMOS transistor (M_{ESD}) is turned on to discharge the ESD current. Under the normal operating condition, the positive-feedback control circuit that is designed to apply different operating voltages can make the ESD clamp NMOS transistor (M_{ESD}) turn off. In the essay, this architecture is selected to design the parameter of device and compares with the others. This detailed production process is presented in Chapter 3.

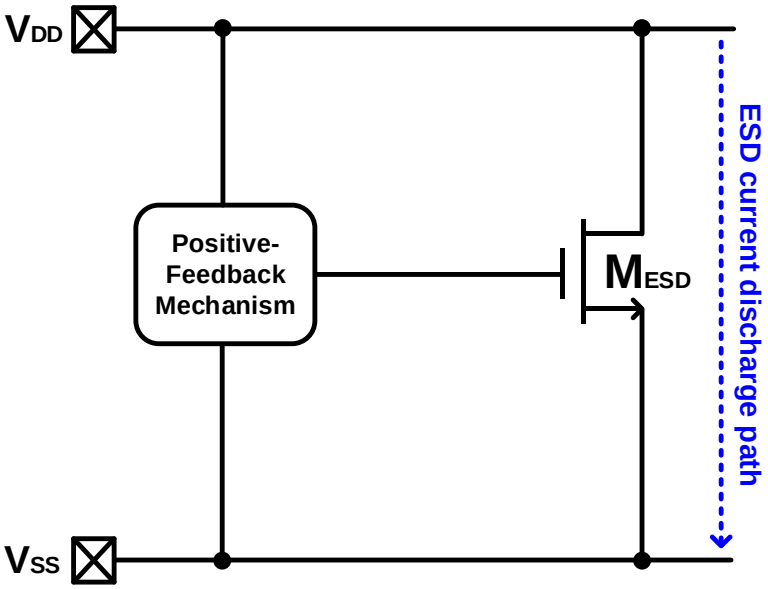


Fig. 1.12. Power-rail ESD clamp circuit with positive feedback.

1.6.4 Power-Rail ESD Circuit with Double-Detector Mechanism [22]

In order to make the M_{ESD} accurate triggering against false trigger under normal operating voltage event, the power-rail ESD clamp circuit of the double-detector mechanism was created in Fig. 1.13. The power-rail ESD clamp circuit is divided into four parts: diodes-triggered mechanism, resistor-capacitor mechanism, AND gate, and M_{ESD} of the large width. The diode numbers of the diodes-trigger mechanism are decided to refer to the normal power-on voltage level. The RC-time constant of the resistor-capacitor mechanism is usually designed to approximate microseconds. Even though the power-rail ESD clamp circuit with double-detector mechanism can enhance immunity against the false trigger during normal and fast power-on event, the power-rail ESD clamp circuit is complex to occupy much area.

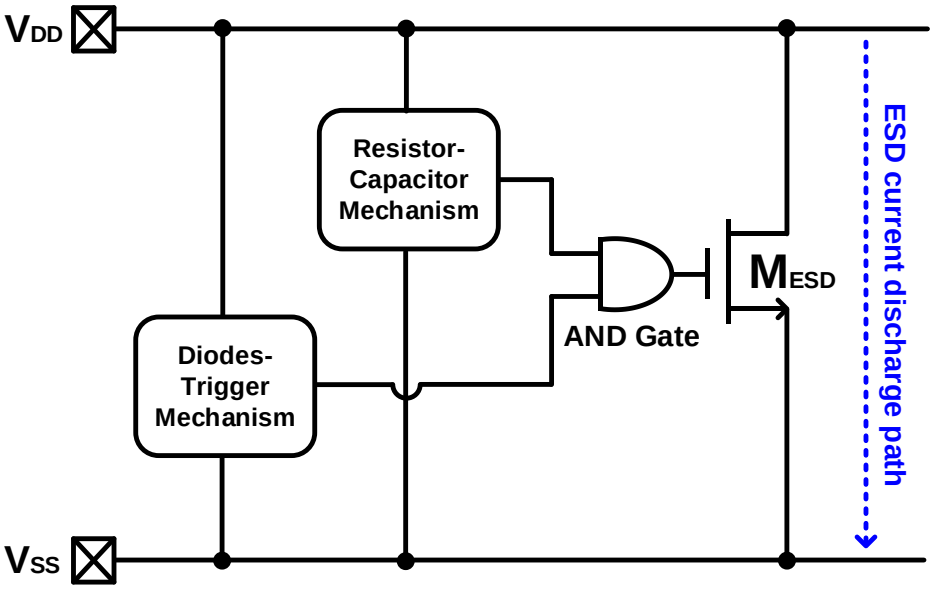


Fig. 1.13. Power-rail ESD clamp circuit with double detector.

1.7 Organization of This Dissertation

The thesis consists of four chapters. In Chapter 1, there is the motivation for designing the ESD protection circuit, testing method, background, and applications containing some traditional ESD protection circuits that will be structured to apply for the high-frequency and the power-rail ESD clamp circuit with different triggering mechanisms. In Chapter 2, the ESD protection circuit will be proposed with resistance and diode, including interpreting design steps and measurement results. In Chapter 3, these present power-rail ESD clamp circuits are analyzed to apply the internal circuit of normal power-on and fast power-on events, including parameter selection flow and measurement results. Finally, Chapter 4 summarizes all research and future work.

Chapter 2

Resistance-Capacitance Diode for High-Frequency Application

The ESD protection circuit of resistance-capacitance diode (RC-diode) is proposed to apply to high frequency in the chapter. The resistor can be used to reduce the parasitic capacitance of ESD protection circuit. Therefore, the RC diode can diminish the severe high-frequency signal loss and have small layout area. All ESD protection circuits with traditional dual diode, traditional LC tank, and proposed resistance-capacitance diode are fabricated in CMOS process.

2.1 Traditional Dual-Diode Design

It is universal that the diode is used to compose ESD protection circuit in CMOS technology. As shown in Fig. 2.1, the whole-chip ESD protection circuit is composed of a P-type diode (D_P) placed from RF_{IN}/RF_{OUT} pad to V_{DD}, N-type diode (D_N) placed from RF_{IN}/RF_{OUT} pad to V_{SS}, and the power-rail ESD clamp circuit placed from V_{DD} to V_{SS}. Additionally, the ESD current can be discharged by different diodes under four modes. First of all, the ESD current can be discharged by a P-type diode under PD mode. Then, a P-type diode and power-rail ESD clamp circuit can discharge the ESD current under the PS mode. Next, an N-type diode can discharge the ESD current under NS mode. Finally, the ND mode can discharge the ESD current by an N-type diode and power-rail ESD clamp circuit.

Furthermore, the traditional dual-diode ESD protection circuit comprises a D_P, a D_N and power-rail ESD clamp circuit. As shown in Fig. 2.2 (a), P+ diffusion is connected to the RF_{IN}/RF_{OUT} pad as the anode, while N+ diffusion can be a cathode when connects to the V_{DD}. As shown in Fig. 2.2 (b), the RF_{IN}/RF_{OUT} pad is connected to N+ diffusion as cathode, and the V_{SS} is connected to P+ diffusion as the anode.

These test parameters of the traditional dual-diode ESD protection circuit with D_P and D_N are listed in Table 2.1. The thesis makes dual-diode ESD protection circuit with fixed 1.9μm length and different widths including 20μm, 40μm, and 60μm in order to compare the value of signal loss and ESD robustness. Fig. 2.3 shows the layout top view contains a D_P of 20μm width and a D_N of 20μm width. The layout top view contains a D_P of 40μm width and a D_N of 40μm width is shown in Fig. 2.4. Fig. 2.5 shows the layout top view contains a D_P of 60μm width and a D_N of 60μm width.

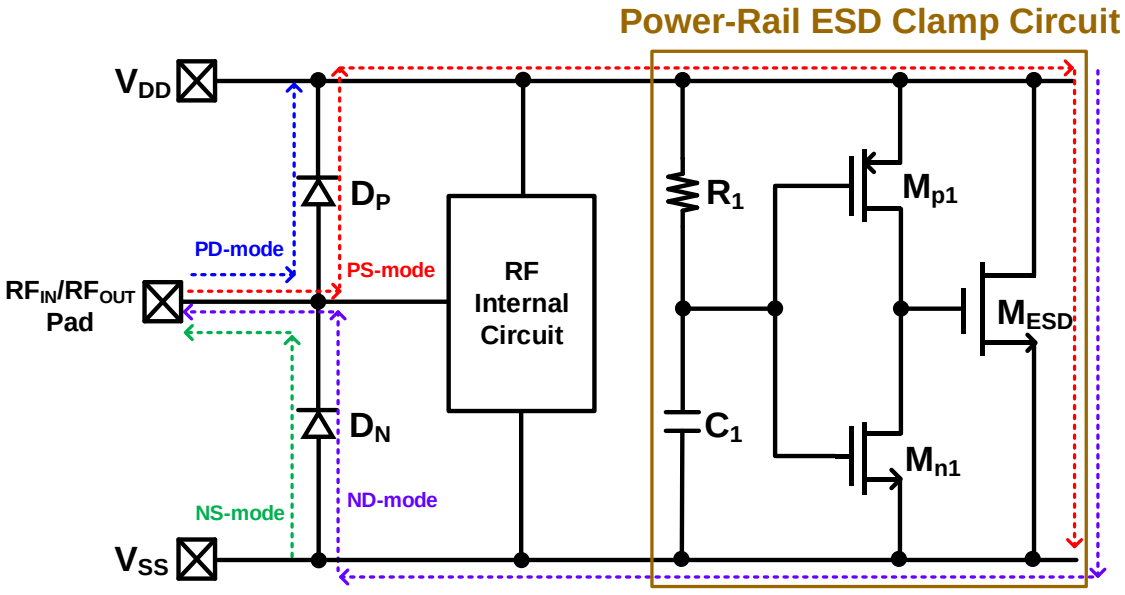
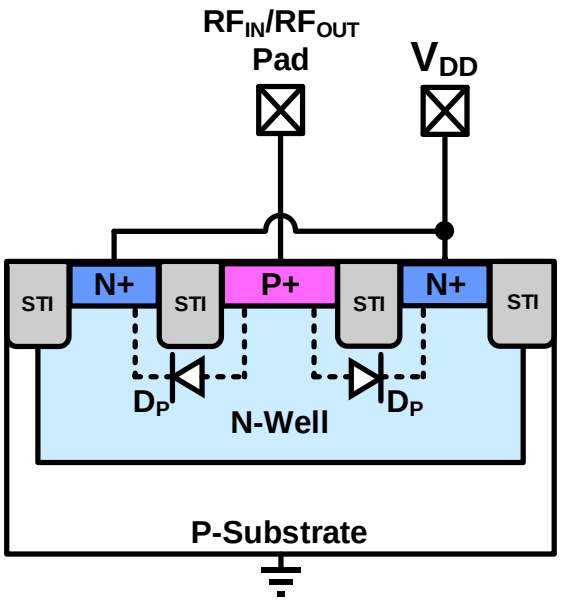
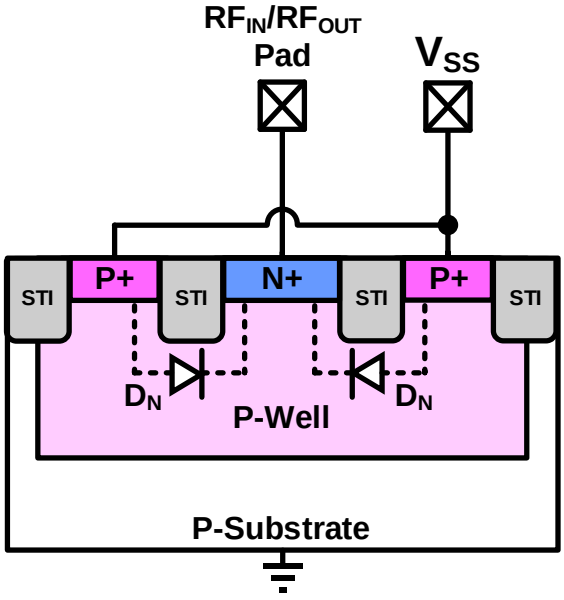


Fig. 2.1. The whole-chip ESD protection circuit with traditional dual diode.



(a)



(b)

Fig. 2.2. The cross-sectional view of the (a) P-type and (b) N-type diode.

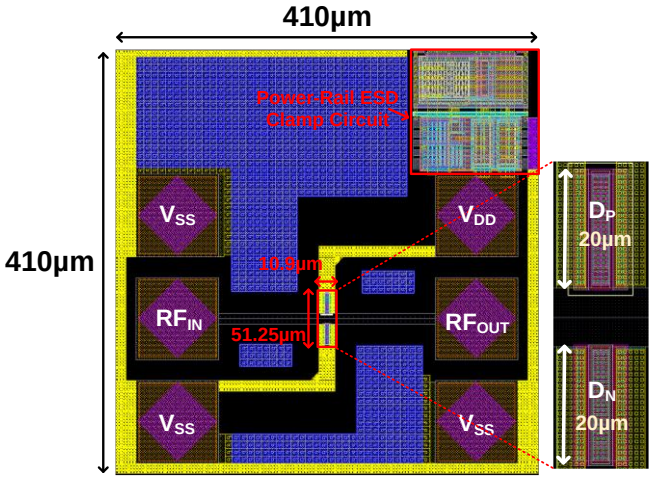


Fig. 2.3. The layout top views of Dual-Diode_20μm

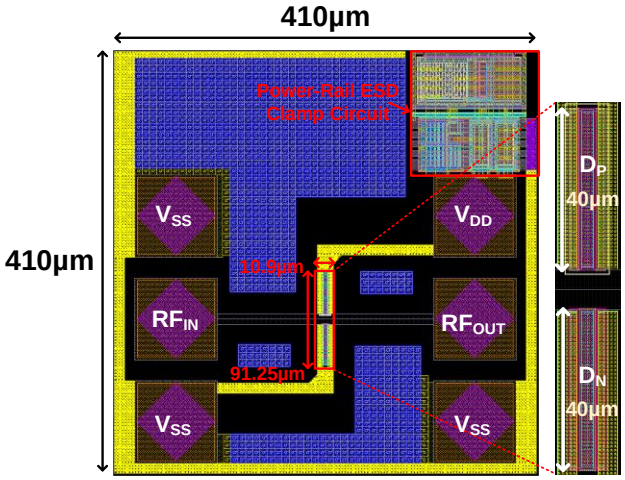


Fig. 2.4. The layout top views of Dual-Diode_40μm

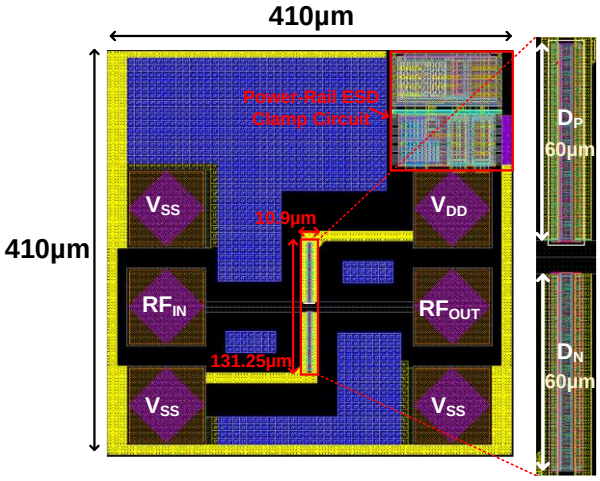


Fig. 2.5. The layout top views of Dual-Diode_60μm

Table 2.1. The parameter of ESD protection circuit with dual diode.

Cell Name	Device	Width (μm)	Length (μm)
Dual-Diode_20μm	D_P	20	1.9
	D_N		
Dual-Diode_40μm	D_P	40	1.9
	D_N		
Dual-Diode_60μm	D_P	60	1.9
	D_N		

2.2 Traditional LC-Tank Design

Though the dual-diode design parameter chooses big dimension to provide high ESD robustness, the equivalent parasitic capacitance will increase to cause signal loss appropriately at high frequency. In order to eliminate the equivalent parasitic capacitance, the designed method can use extra inductor to resonate. Aforementioned technique can design traditional LC-tank ESD protection circuit. It is called the impedance cancellation that using parallel LC reduces the parasitic capacitance. As shown in equation 2.1, the inductor value (L_{EXTRA}) and parasitic capacitance value of ESD protection device (C_{ESD}) can decide resonant frequency (ω_0). The resonant frequency is designed operating frequency of the RF internal circuit by the inductor.

$$\omega_0 = \frac{1}{\sqrt{L_{Extra} * C_{ESD}}} \tag{2.1}$$

As shown in Fig. 2.6, the whole-chip ESD protection circuit consists of two pairs of LC tank, P-type diode (D_{P2}), N-type diode (D_{N2}) and power-rail ESD clamp circuit. The LC tank is composed of the inductor (L_P) and the parasitic capacitance of ESD protection diode (D_{P1}) placed from RF_{IN}/RF_{OUT} pad to ESD protection diode (D_{P2}). Another LC tank is composed of the inductor (L_N) and the parasitic capacitance of ESD protection diode (D_{N1}) placed from RF_{IN}/RF_{OUT} pad to ESD protection diode (D_{N2}). The power-rail ESD clamp circuit placed between V_{DD} and V_{SS}.

The ESD current can be discharged by the inductor (L_P) and ESD protection diode (D_{P1} and D_{P2}) under PD mode. The ESD current can be discharged by the inductor (L_P), ESD protection diode (D_{P1} and D_{P2}), and power-rail ESD clamp circuit under PS mode. The ESD current can be discharged by the inductor (L_N) and ESD protection diode (D_{N1} and D_{N2}) under NS mode. The ESD current can be discharged by the inductor (L_N), ESD protection diode (D_{N1} and D_{N2}), and power-rail ESD clamp circuit under ND mode. Under the normal circuit operating condition, the ESD protection diode of D_{P2} and D_{N2} can be used to isolate the steady current from V_{DD} to V_{SS}. As shown in Fig. 2.7 (a), the RF_{IN}/RF_{OUT} pad is connected to P+ diffusion and inductor (L_P). The ESD protection diode (D_{P2}) is connected to LC tank of inductor (L_P) and ESD protection diode (D_{P1}). The V_{DD} is connected to N+ diffusion. As shown in Fig. 2.7 (b), the RF_{IN}/RF_{OUT} pad is connected to N+ diffusion and inductor (L_N). The ESD protection diode (D_{N2}) is connected to LC tank of inductor (L_N) and ESD protection diode (D_{N1}). The V_{SS} is connected to P+ diffusion.

The test parameters of the LC-tank ESD protection circuit with P-type diode (D_{P1}

and D_{P2}) and N-type diode (D_{N1} and D_{N2}) are listed in Table 2.2. The thesis makes LC-tank ESD protection circuit with fixed 1.9μm length and inductor value (L_P and L_N). The widths include 20μm, 40μm and 60μm to compare value of signal loss and ESD robustness. The layout top view contains D_{P1} and D_{P2} of 20μm width and D_{N1} and D_{N2} of 20μm width are shown in Fig. 2.8. The layout top view contains D_{P1} and D_{P2} of 40μm width and D_{N1} and D_{N2} of 40μm width are shown in Fig. 2.9. The layout top view contains D_{P1} and D_{P2} of 60μm width and D_{N1} and D_{N2} of 60μm width are shown in Fig. 2.10.

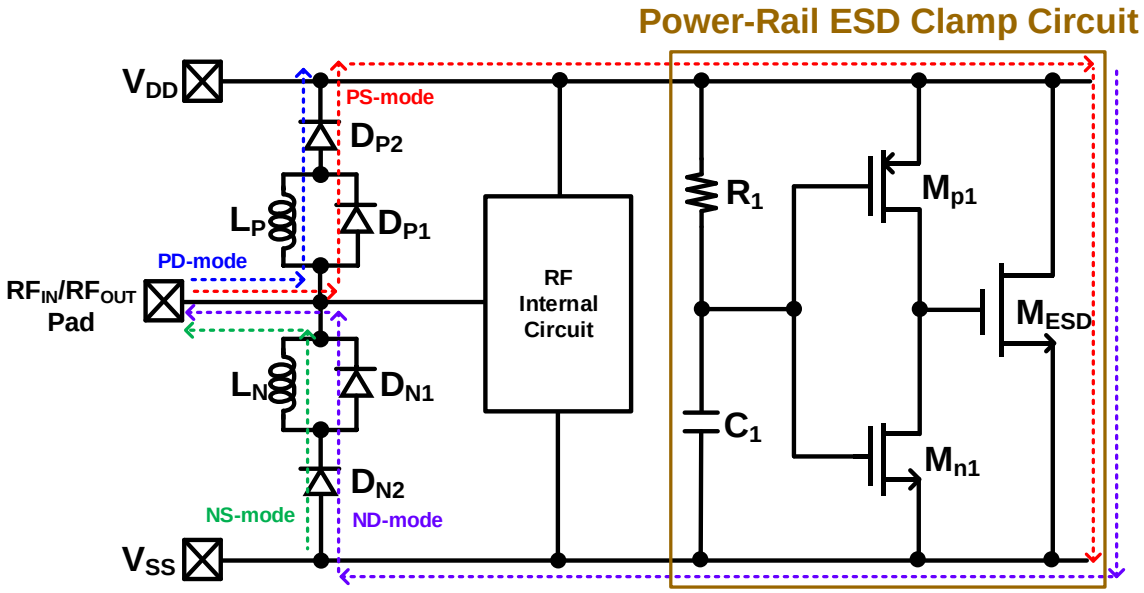
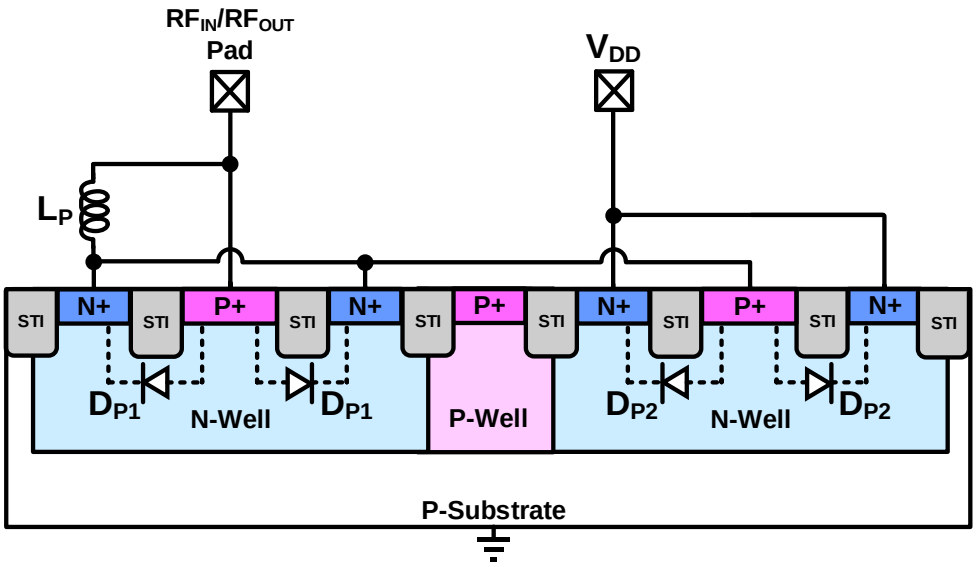
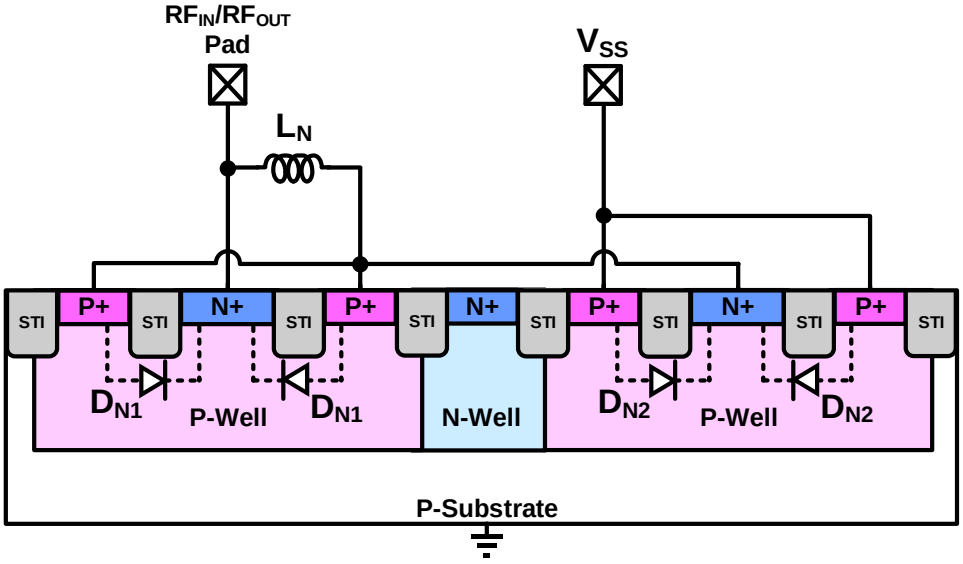


Fig. 2.6. The whole-chip ESD protection circuit with traditional LC tank.



(a)



(b)

Fig. 2.7. The cross-sectional view of the (a) P-type diode with L_P and (b) N-type diode with L_N.

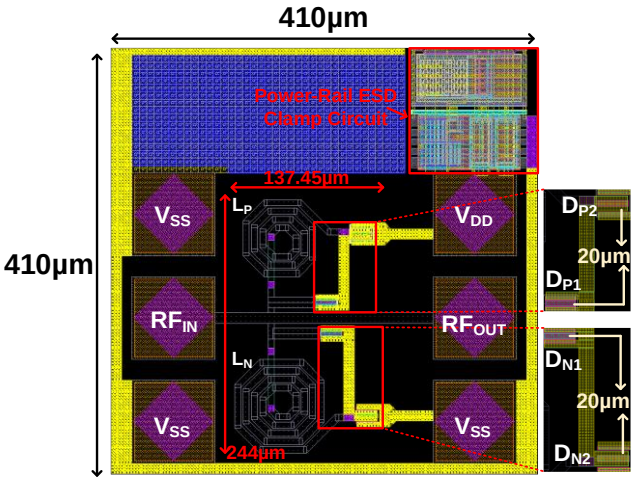


Fig. 2.8. The layout top views of LC-tank_20μm

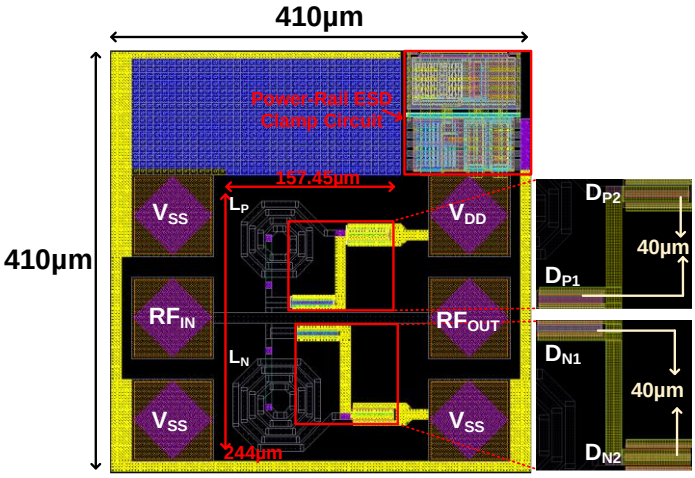


Fig. 2.9. The layout top views of LC-tank_40μm

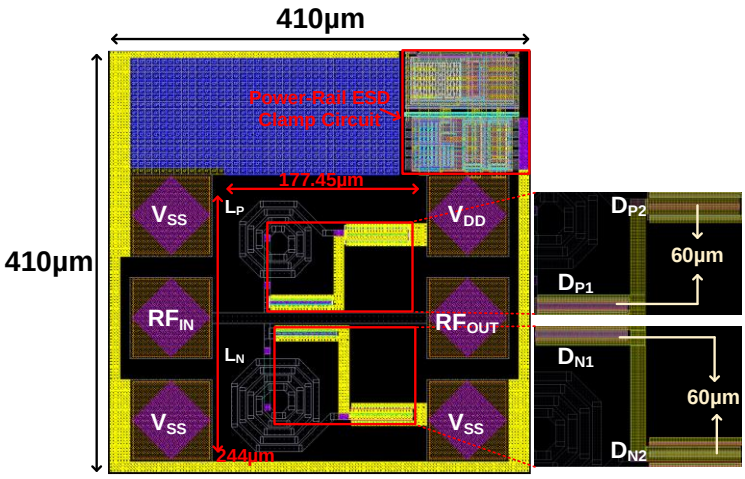


Fig. 2.10. The layout top views of LC-tank_60μm

Table 2.2. The parameter of ESD protection circuit with LC tank.

Cell Name	Device	Width (μm)	Length (μm)
LC-tank_20μm	D_{P1} and D_{P2}	20	1.9
	D_{N1} and D_{N2}		
LC-tank_40μm	D_{P1} and D_{P2}	40	1.9
	D_{N1} and D_{N2}		
LC-tank_60μm	D_{P1} and D_{P2}	60	1.9
	D_{N1} and D_{N2}		

2.3 Proposed RC-Diode Design

As shown in Fig. 2.11, the novel RC-diode ESD protection circuit is proposed in the thesis. The RC-diode ESD protection circuit combines with P-type diode (D_{P1}), N-type diode (D_{N2}), and two pairs of RD-tanks. In order to achieve a whole-chip ESD protection circuit, the power-rail ESD clamp circuit is incorporated into the RC-diode ESD protection circuit. The RD tank is consisted of the resistor (R_P) and the ESD protection diode (D_{N1}) placed from the ESD protection diode (D_{P1}) to V_{DD}. Another RD tank is consisted of the resistor (R_N) and the ESD protection diode (D_{P2}) placed from ESD protection diode (D_{N2}) to V_{SS}. In addition, the power-rail ESD clamp circuit is placed between V_{DD} and V_{SS}. If these diodes (D_{P1}, D_{N1}, D_{N2}, and D_{P2}) are regarded as capacitors (C_{DP1}, C_{DN1}, C_{DN2}, and C_{DP2}), the equations (2.2) and (2.3) can be used to calculate the equivalent parasitic capacitance from RF_{IN}/RF_{OUT} pad to V_{DD} and V_{SS}, respectively. The $Y_{RFIN/RFOUT\text{-}to\text{-}VDD}$ and $Y_{RFIN/RFOUT\text{-}to\text{-}VSS}$, which denoted the admittance,

are seen from RF_{IN}/RF_{OUT} pad to V_{DD} and V_{SS}. As shown in Fig. 2.12, if the parasitic capacitance of each diode is 100fF and the operating frequency are 10GHz, 14GHz, and 20GHz, the parasitic capacitance can be reduced through increasing the R_P and R_N, and then the signal loss can also be reduced.

The ESD current can be discharged by ESD protection diode (D_{P1} and D_{N1}) and the resistor (R_P) under PD mode. The ESD current can be discharged by ESD protection diode (D_{P1} and D_{N1}), the resistor (R_P), and power-rail ESD clamp circuit under PS mode. The ESD current can be discharged by ESD protection diode (D_{N2} and D_{P2}) and the resistor (R_N) under NS mode. The ESD current can be discharged by ESD protection diode (D_{N2} and D_{P2}), the resistor (R_N), and power-rail ESD clamp circuit under ND mode. The ESD protection diode of D_{P1} and D_{N2} can be used to isolate the steady current from V_{DD} to V_{SS} under the normal circuit operating condition. As shown in Fig. 2.13 (a), the RF_{IN}/RF_{OUT} pad is connected to P+ diffusion. The ESD protection diode (D_{P1}) is connected to resistor (R_P) and ESD diode (D_{N1}). As shown in Fig. 2.13 (b), the RF_{IN}/RF_{OUT} pad is connected to N+ diffusion. The ESD protection diode (D_{N2}) is connected to resistor (R_N) and ESD diode (D_{P2}).

The test sizes of RC-diode ESD protection circuit with P-type diode (D_{P1} and D_{P2}) and N-type diode (D_{N1} and D_{N2}) are listed in Table 2.3. The proposed RC-diode ESD diode length is fixed to 1.9μm. The proposed RC-diode ESD diode widths include 20μm, 40μm, and 60μm, respectively. The proposed RC-diode resistance value is 100ohms and 200ohms, respectively. The different ESD diode widths and resistance values are used to compare the values of signal loss and ESD robustness. The layout top view contains a 100ohms resistor value, P-type diode (D_{P1} and D_{P2}), and N-type diode (D_{N1} and D_{N2}) of 20μm width are shown in Fig. 2.14. The layout top view contains a 100ohms resistor value, P-type diode (D_{P1} and D_{P2}), and N-type diode (D_{N1} and D_{N2}) of 40μm width are shown in Fig. 2.15. The layout top view contains a 100ohms resistor value, P-type diode

(D_{P1} and D_{P2}), and N-type diode (D_{N1} and D_{N2}) of 60µm width are shown in Fig. 2.16. The layout top view contains a 200ohms resistor value, P-type diode (D_{P1} and D_{P2}), and N-type diode (D_{N1} and D_{N2}) of 20µm width are shown in Fig. 2.17. The layout top view contains a 200ohms resistor value, P-type diode (D_{P1} and D_{P2}), and N-type diode (D_{N1} and D_{N2}) of 40µm width are shown in Fig. 2.18. The layout top view contains a 200ohms resistor value, P-type diode (D_{P1} and D_{P2}), and N-type diode (D_{N1} and D_{N2}) of 60µm width are shown in Fig. 2.19.

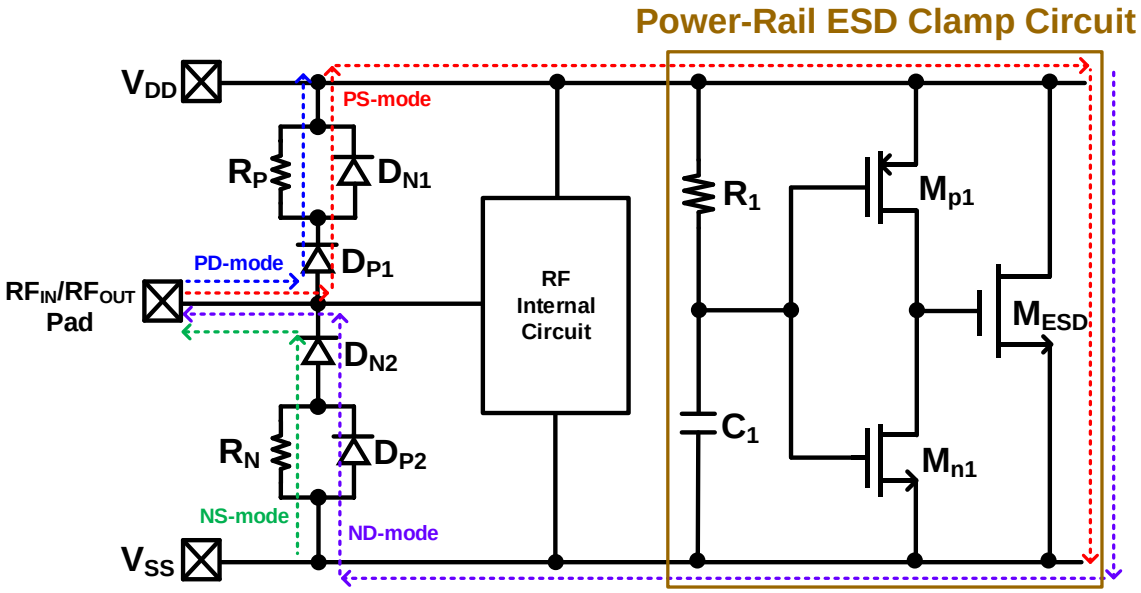


Fig. 2.11. The whole-chip ESD protection circuit with proposed RC diode.

$$C_{\mathrm{RF_{IN}/RF_{OUT}-to-}V_{DD}} = \frac{Im\left(Y_{\mathrm{RF_{IN}/RF_{OUT}-to-}V_{DD}}\right)}{\omega} = \frac{Im\left(\dfrac{1}{\dfrac{1}{j\omega C_{D_{N1}} + \dfrac{1}{R_P}} + \dfrac{1}{j\omega C_{D_{P1}}}}\right)}{\omega}$$

$$= \frac{\omega^2 {R_P}^2 C_{D_{N1}} C_{D_{P1}} \left(C_{D_{N1}} + C_{D_{P1}}\right) + C_{D_{P1}}}{\omega^2 {R_P}^2 \left(C_{D_{N1}} + C_{D_{P1}}\right)^2 + 1} \tag{2.2}$$

$$C_{\mathrm{RF_{IN}/RF_{OUT}-to-}V_{SS}} = \frac{Im\left(Y_{\mathrm{RF_{IN}/RF_{OUT}-to-}V_{SS}}\right)}{\omega} = \frac{Im\left(\dfrac{1}{\dfrac{1}{j\omega C_{D_{P2}} + \dfrac{1}{R_N}} + \dfrac{1}{j\omega C_{D_{N2}}}}\right)}{\omega}$$

$$= \frac{\omega^2 {R_N}^2 C_{D_{N2}} C_{D_{P2}} \left(C_{D_{N2}} + C_{D_{P2}}\right) + C_{D_{N2}}}{\omega^2 {R_N}^2 \left(C_{D_{N2}} + C_{D_{P2}}\right)^2 + 1} \tag{2.3}$$

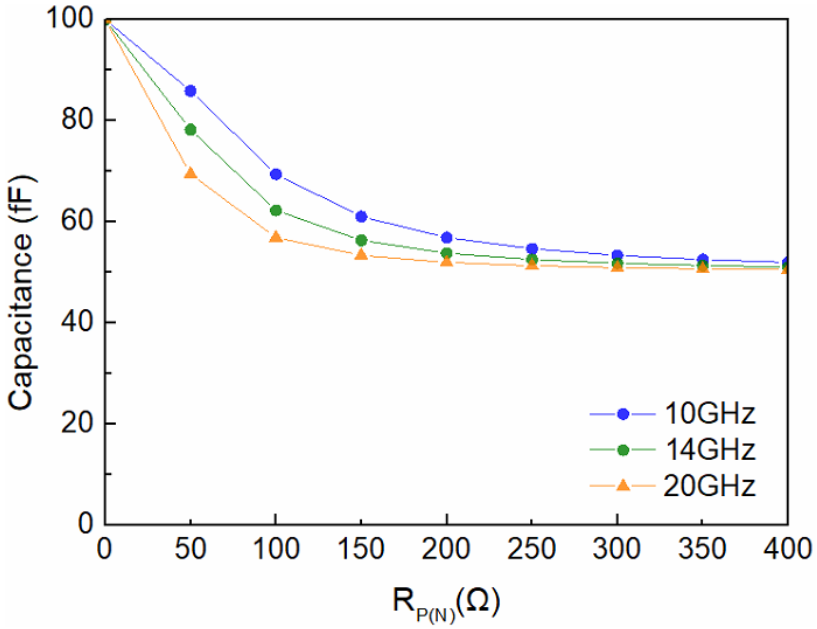
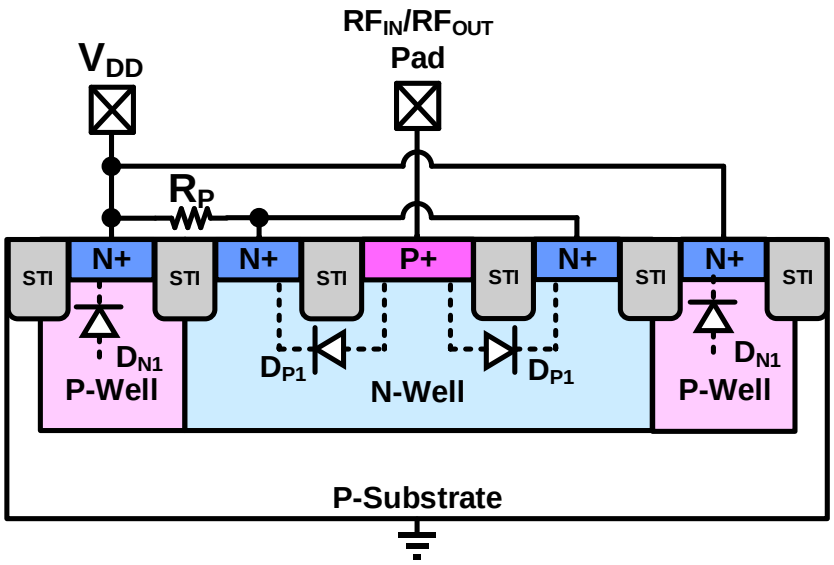
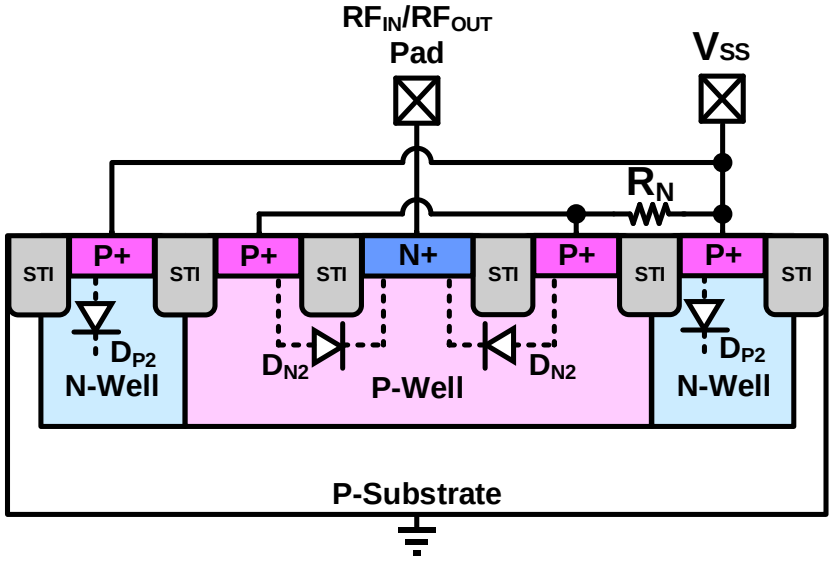


Fig. 2.12. The calculation results of the $R_{P(N)}$ and the parasitic capacitance at 10GHz, 14GHz and 20GHz.



(a)



(b)

Fig. 2.13. The cross-sectional view of the (a) P-type diode with R_P and (b) N-type diode with R_N.

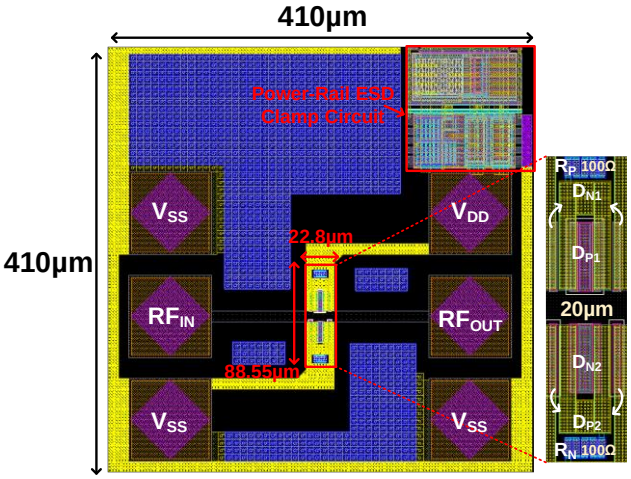


Fig. 2.14. The layout top views of RC-Diode_100Ω_20µm.

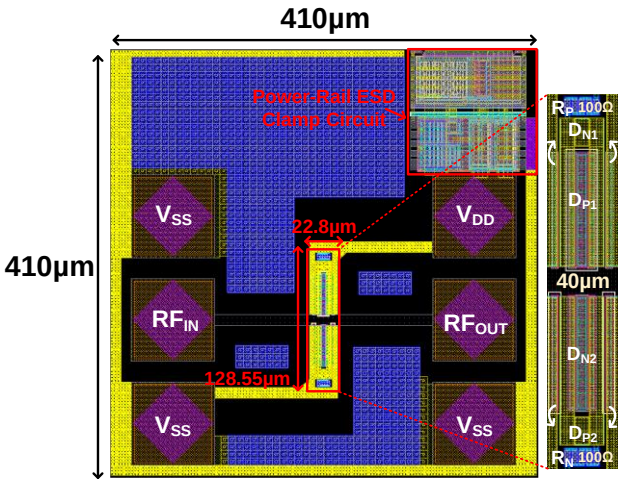


Fig. 2.15. The layout top views of RC-Diode_100Ω_40µm.

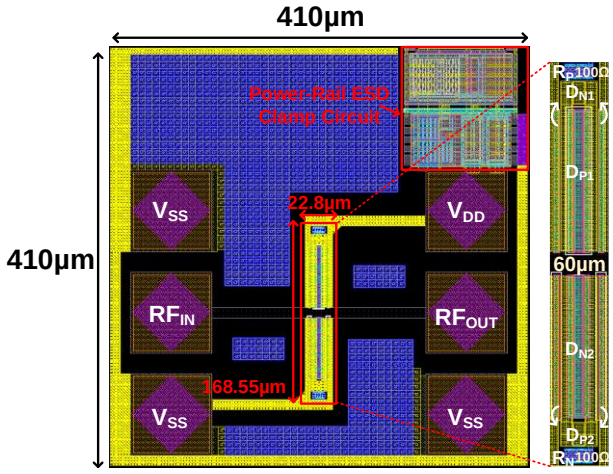


Fig. 2.16. The layout top views of RC-Diode_100Ω_60µm.

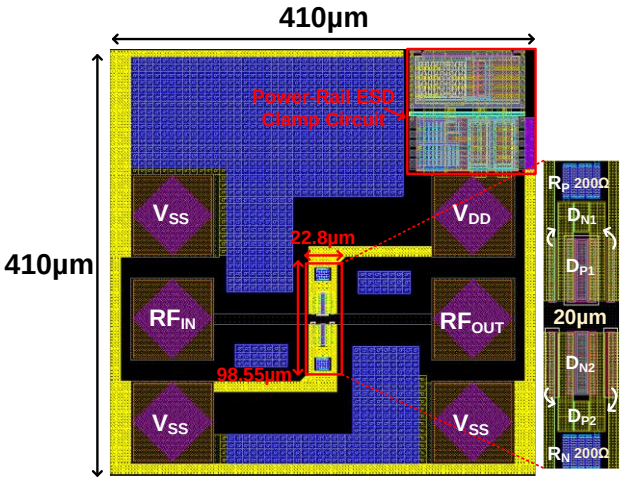


Fig. 2.17. The layout top views of RC-Diode_200Ω_20µm.

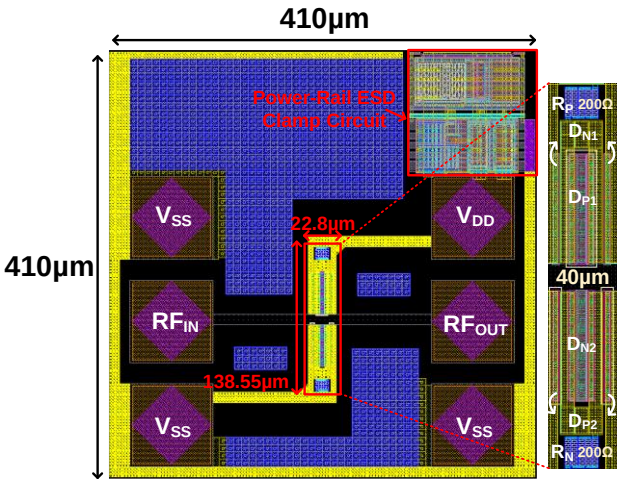


Fig. 2.18. The layout top views of RC-Diode_200Ω_40µm.

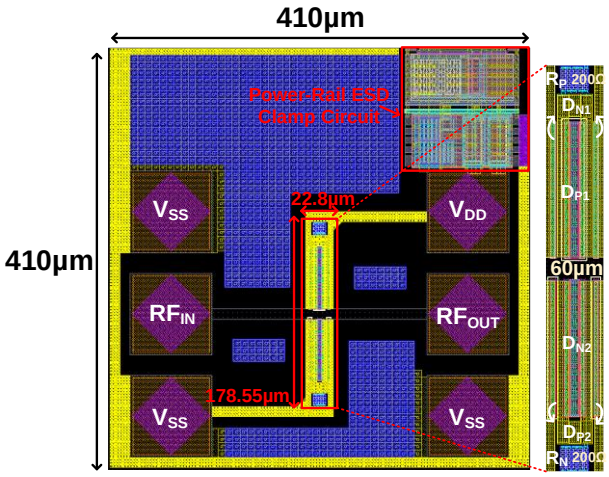


Fig. 2.19. The layout top views of RC-Diode_200Ω_60µm.

Table 2.3. The parameter of ESD protection circuit with RC diode.

Cell Name	Device	Width (μm)	Length (μm)	Resistor (Ω)
RC-Diode_100Ω_20μm	D_{P1} and D_{P2}	20	1.9	N/A
	D_{N1} and D_{N2}			
	R_P and R_N	6.2	11.8	100
RC-Diode_100Ω_40μm	D_{P1} and D_{P2}	40	1.9	N/A
	D_{N1} and D_{N2}			
	R_P and R_N	6.2	11.8	100
RC-Diode_100Ω_60μm	D_{P1} and D_{P2}	60	1.9	N/A
	D_{N1} and D_{N2}			
	R_P and R_N	6.2	11.8	100
RC-Diode_200Ω_40μm	D_{P1} and D_{P2}	20	1.9	N/A
	D_{N1} and D_{N2}			
	R_P and R_N	11.2	11.8	200
RC-Diode_200Ω_40μm	D_{P1} and D_{P2}	40	1.9	N/A
	D_{N1} and D_{N2}			
	R_P and R_N	11.2	11.8	200
RC-Diode_200Ω_60μm	D_{P1} and D_{P2}	60	1.9	N/A
	D_{N1} and D_{N2}			
	R_P and R_N	11.2	11.8	200

2.4 Measurement Results

These traditional and proposed ESD test circuits are fabricated in a 350nm CMOS process, and the length and width of the chip are 1250μm and 2090μm. As shown in Fig. 2.20, the chip micrograph of ESD protection circuits is containing three types of circuits: traditional dual diode, traditional LC tank, and proposed RC diode. These ESD test circuits are intended to measure the two-port S-parameter of high frequency, TLP measurement, VF-TLP measurement, and Human-Body Model (HBM) robustness measurement. The measurement method and results are introduced in the following section.

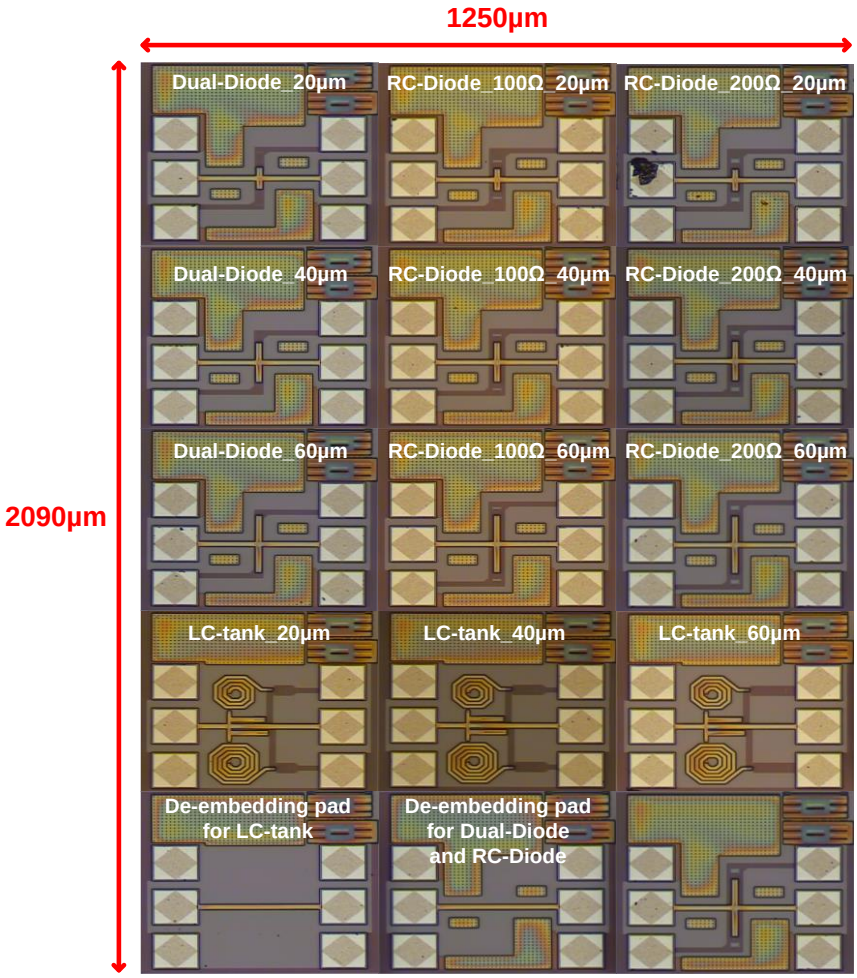


Fig. 2.20. The chip micrograph of all ESD protection circuits.

2.4.1 High-Frequency Performance

As shown in Fig. 2.21, these test circuits of ESD protection are measured by the high-frequency measurement system [23]. The vector network analyzer uses a two-port ground-signal-ground (G-S-G) probe to get the high-frequency two-port S-parameter characteristic of each test circuit. When the voltage difference of the PN junction in the diode is 0V, the diode can be extracted the maximum parasitic capacitance. So, the V_{DD}, RF_{IN} / RF_{OUT} and V_{SS} terminals are provided bias voltage of 0V. Moreover, the high-frequency measurement results of these test circuits include the parasitic effect of the G-S-G test pad, these test circuits should be adopted the de-embedding technique to extract the precision of the test circuits' measured results. The de-embedding technique is used to extract intrinsic characteristics of these test circuits at high-frequency [24], [25]. It is necessary to measure the effect of de-embedding G-S-G pads as a reference in Fig. 2.22 (a) and Fig. 2.22 (b). Finally, these test circuits are carried out de-embedding technique into practice as following measured results.

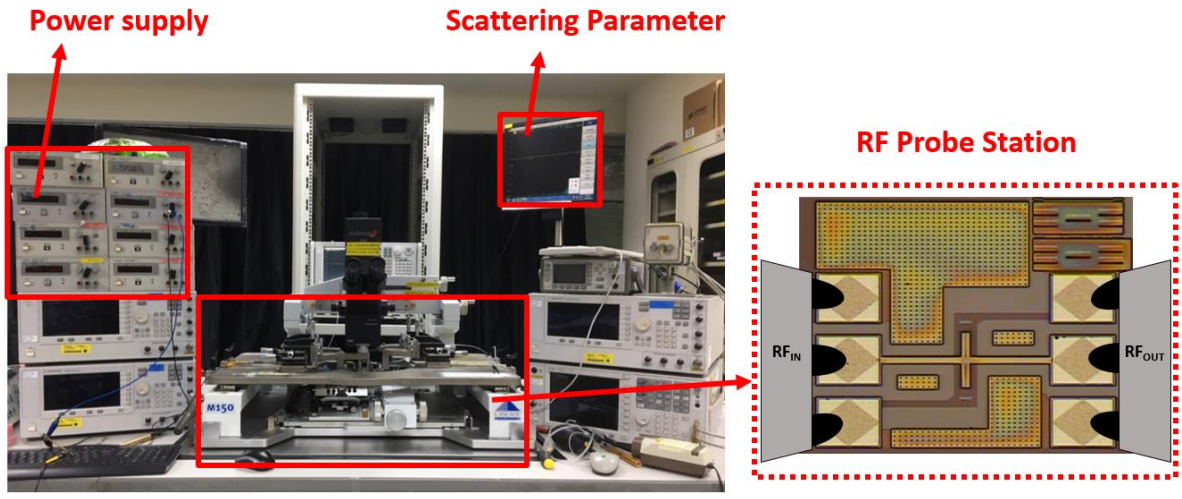
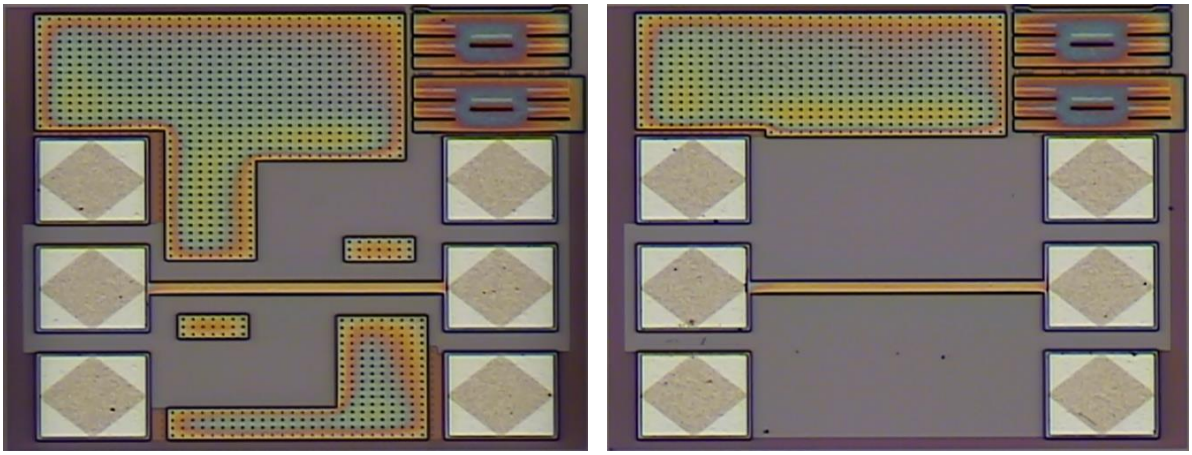
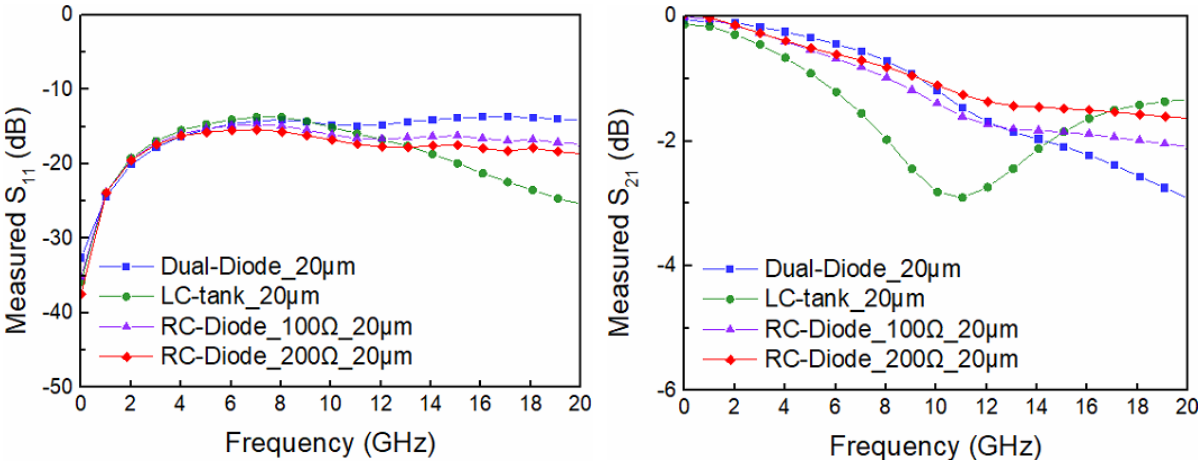


Fig. 2.21. The picture of high-frequency measurement system [23].



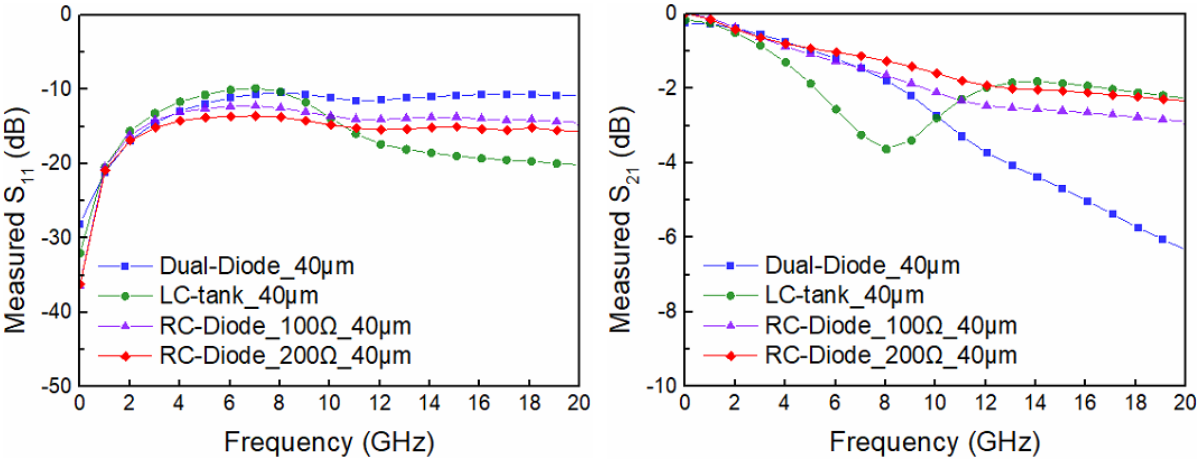
(a) (b)

Fig. 2.22. The de-embedding pad for test circuit of (a) dual diode, RC diode and (b) LC tank.



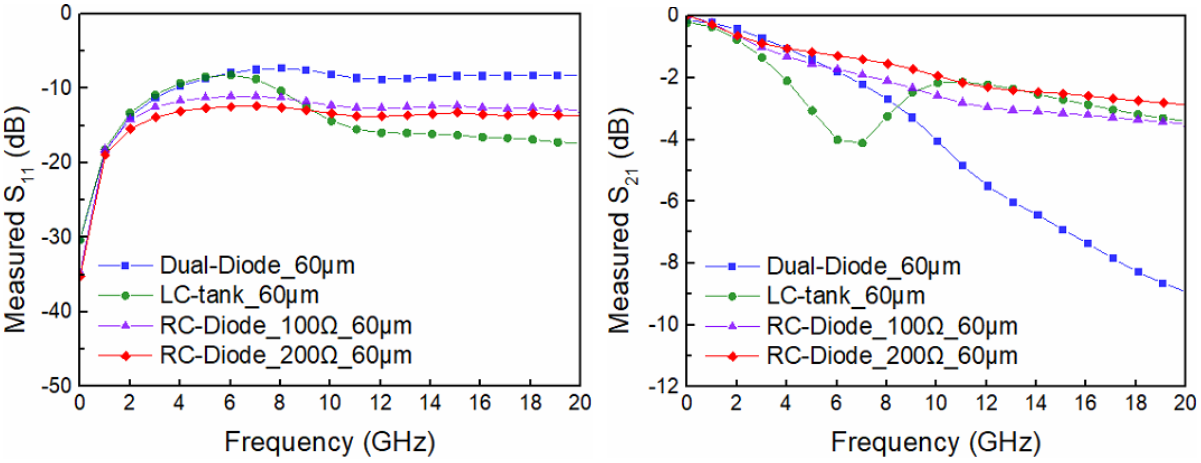
(a) (b)

Fig. 2.23. Measured S-parameters of Dual-Diode_20µm, LC-tank_20µm, RC-Diode_100Ω_20µm and RC-Diode_200Ω_20µm.



(a) (b)

Fig. 2.24. Measured S-parameters of Dual-Diode_40µm, LC-tank_40µm, RC-Diode_100Ω_40µm and RC-Diode_200Ω_40µm.



(a) (b)

Fig. 2.25. Measured S-parameters of Dual-Diode_60µm, LC-tank_60µm, RC-Diode_100Ω_60µm and RC-Diode_200Ω_60µm.

As shown in Fig. 2.23, the measured S-parameters of RC-Diode_100Ω_20μm and RC-Diode_200Ω_20μm are compared with those of Dual-Diode_20μm and LC-tank_20μm. As shown in Fig. 2.24, the measured S-parameters of RC-Diode_100Ω_40μm and RC-Diode_200Ω_40μm are compared with those of Dual-Diode_40μm and LC-tank_40μm. As shown in Fig. 2.25, the measured S-parameters of RC-Diode_100Ω_60μm and RC-Diode_200Ω_60μm are compared with those of Dual-Diode_60μm and LC-tank_60μm. The smaller width such as RC-Diode_100Ω_20μm, RC-Diode_200Ω_20μm, LC-tank_20μm and Dual-Diode_20μm are displayed the better high-frequency performance at same ESD protection architecture.

The measured S-parameters of these traditional and proposed designs are listed in Table 2.4. The S_{21} of proposed RC diode is obviously degraded than the S_{21} of the traditional dual diode at the same diode width. Though the S_{21} of the traditional LC tank and proposed RC diode are about -2dB, traditional LC tank need a large layout area to place matching inductor. Except for Dual-Diode_60μm, the S_{11} of the other test circuits are lower than -10dB.

Table 2.4. The measured results of S-parameter.

Cell Name	Frequency (GHz)	S_{11} (dB)	S_{21} (dB)
Dual-Diode_20μm	20	-14.1	-2.9
LC-tank_20μm	20	-25.5	-1.3
RC-Diode_100Ω_20μm	20	-17.4	-2.0
RC-Diode_200Ω_20μm	20	-18.6	-1.6
Dual-Diode_40μm	14	-11.0	-4.3
LC-tank_40μm	14	-18.5	-1.8
RC-Diode_100Ω_40μm	14	-13.8	-2.5
RC-Diode_200Ω_40μm	14	-15.2	-1.9
Dual-Diode_60μm	10	-8.1	-4.0
LC-tank_60μm	10	-14.3	-2.2
RC-Diode_100Ω_60μm	10	-12.2	-2.5
RC-Diode_200Ω_60μm	10	-13.3	-1.9

2.4.2 Transmission-line pulsing (TLP) Measurement

The transmission-line pulsing (TLP) generator measured system can investigate and characterize the performance of each ESD protection circuit under the testing. The TLP measured system can provide high energy pulse such as an electrostatic discharge (ESD) event. When a voltage pulse is inputted, a current value is recorded. The TLP I-V curve is formed with all voltage values and current values [26]. As shown in Fig. 2.26, the TLP system is used to acquire the data of this study. There are several significant parameters, including trigger voltage (V_{t1}), secondary breakdown current (I_{t2}), and turn-on resistance (R_{on}) from observing the I-V curve. Deciding failure criterion of these ESD protection devices is defined the leakage current shifting 30% from its initial curve after each TLP level testing. Four ESD current paths are shown, including PS mode, PD mode, NS mode, and ND mode. The I_{t2} results of these ESD discharges are summarized in Table 2.5.

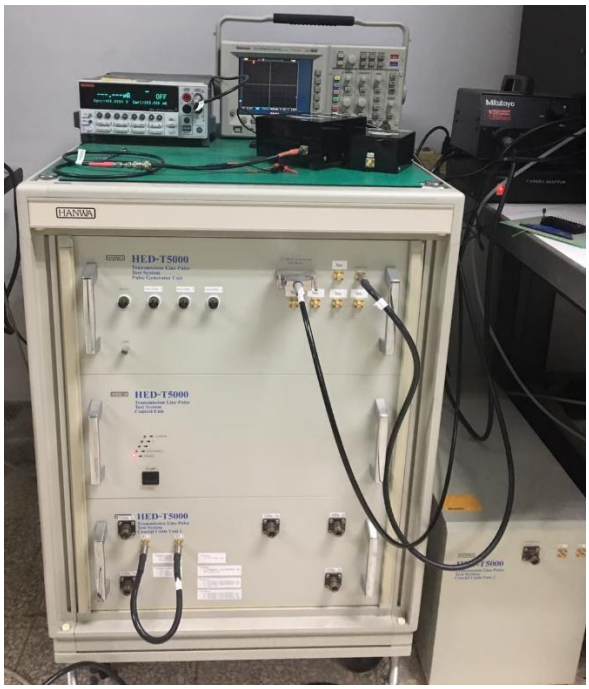


Fig. 2.26. The picture of transmission-line pulse (TLP) measurement system.

(1) Positive to V_{SS} (PS-mode)

The PS-mode discharge path of these traditional and proposed ESD protection circuits is through the diode from the I/O pad to the V_{DD} and power-rail ESD clamp circuit in series. Fig. 2.27 (a) shows that the TLP I-V curves of RC-Diode_100Ω_20μm and RC-Diode_200Ω_20μm are compared with the TLP I-V curves of Dual-Diode_20μm and LC-tank_20μm. Fig. 2.27 (b) shows that the TLP I-V curves of RC-Diode_100Ω_40μm and RC-Diode_200Ω_40μm are compared with the TLP I-V curves of Dual-Diode_40μm and LC-tank_40μm. Fig. 2.27 (c) show that the TLP I-V curves of RC-Diode_100Ω_60μm and RC-Diode_200Ω_60μm are compared with the TLP I-V curves of Dual-Diode_60μm and LC-tank_60μm.

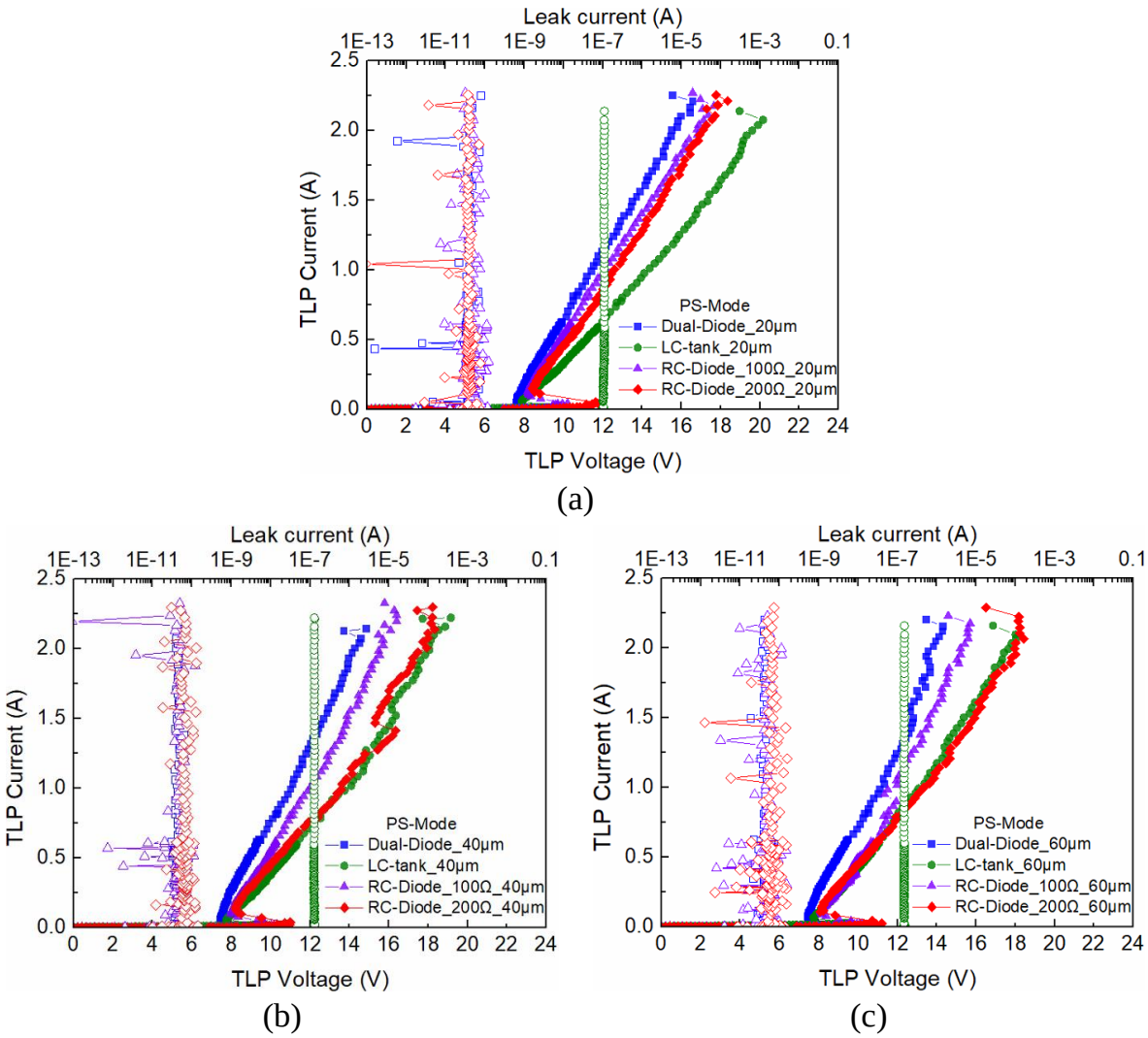


Fig. 2.27. The TLP I-V curves of traditional and proposed designs under PS mode.

(2) Positive to V_{DD} (PD-mode)

The PD-mode discharge path of these traditional and proposed ESD protection circuits is through the diode from the I/O pad to V_{DD}. Fig. 2.28 (a) shows that the TLP I-V curves of RC-Diode_100Ω_20μm and RC-Diode_200Ω_20μm are compared with the TLP I-V curves of Dual-Diode_20μm and LC-tank_20μm. Fig. 2.28 (b) shows that the TLP I-V curves of RC-Diode_100Ω_40μm and RC-Diode_200Ω_40μm are compared with the TLP I-V curves of Dual-Diode_40μm and LC-tank_40μm. Fig. 2.28 (c) shows that the TLP I-V curves of RC-Diode_100Ω_60μm and RC-Diode_200Ω_60μm are compared with the TLP I-V curves of Dual-Diode_60μm and LC-tank_60μm.

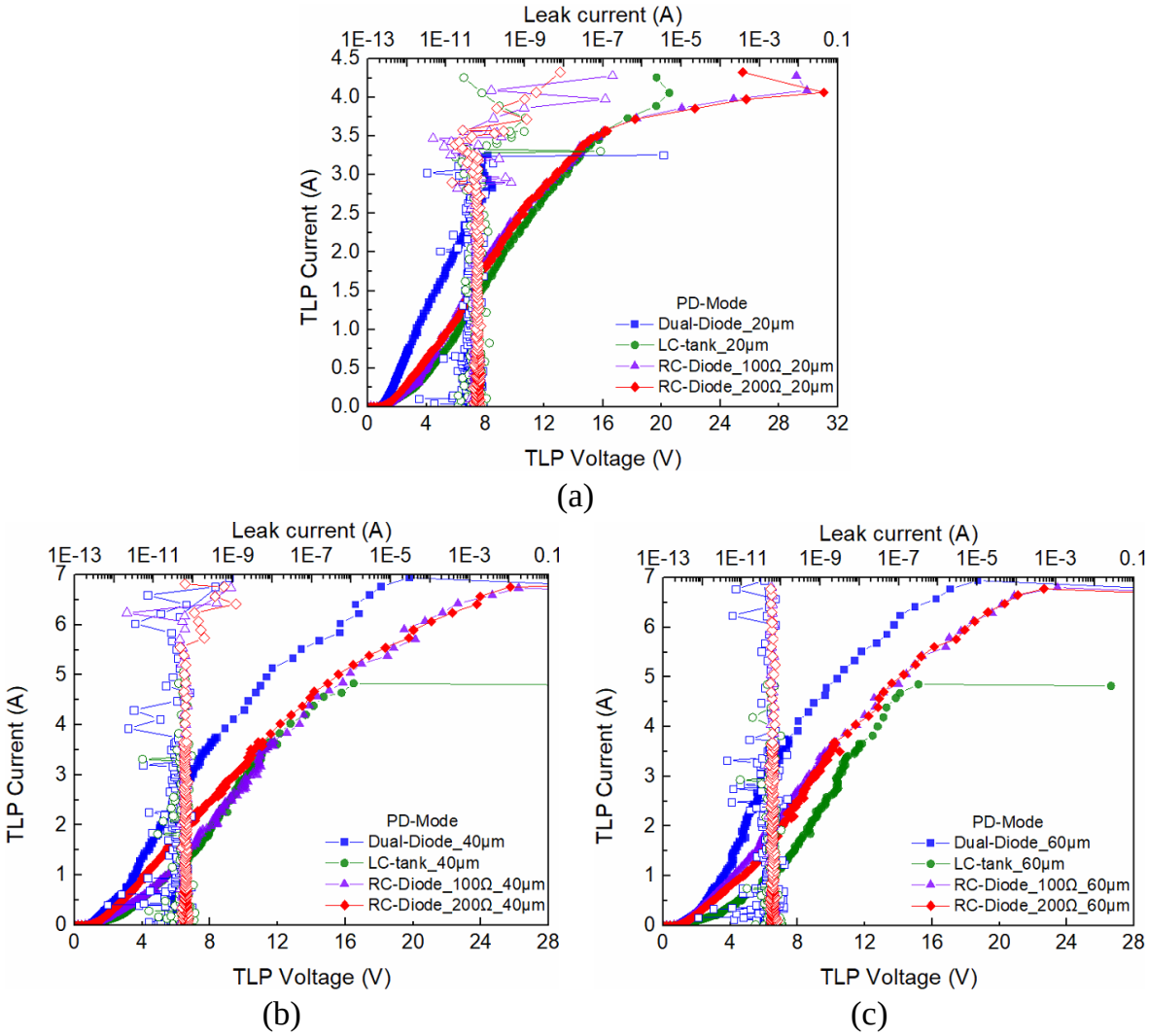


Fig. 2.28. The TLP I-V curves of traditional and proposed designs under PD mode.

(3) Negative to V_{SS} (NS-mode)

The NS-mode discharge path of these traditional and proposed ESD protection circuits is through the diode located from the I/O pad to V_{SS}. Fig. 2.29 (a) shows that the TLP I-V curves of RC-Diode_100Ω_20μm and RC-Diode_200Ω_20μm are compared with the TLP I-V curves of Dual-Diode_20μm and LC-tank_20μm. Fig. 2.29 (b) shows that the TLP I-V curves of RC-Diode_100Ω_40μm and RC-Diode_200Ω_40μm are compared with the TLP I-V curves of Dual-Diode_40μm and LC-tank_40μm. Fig. 2.29 (c) shows that the TLP I-V curves of RC-Diode_100Ω_60μm and RC-Diode_200Ω_60μm are compared with the TLP I-V curves of Dual-Diode_60μm and LC-tank_60μm.

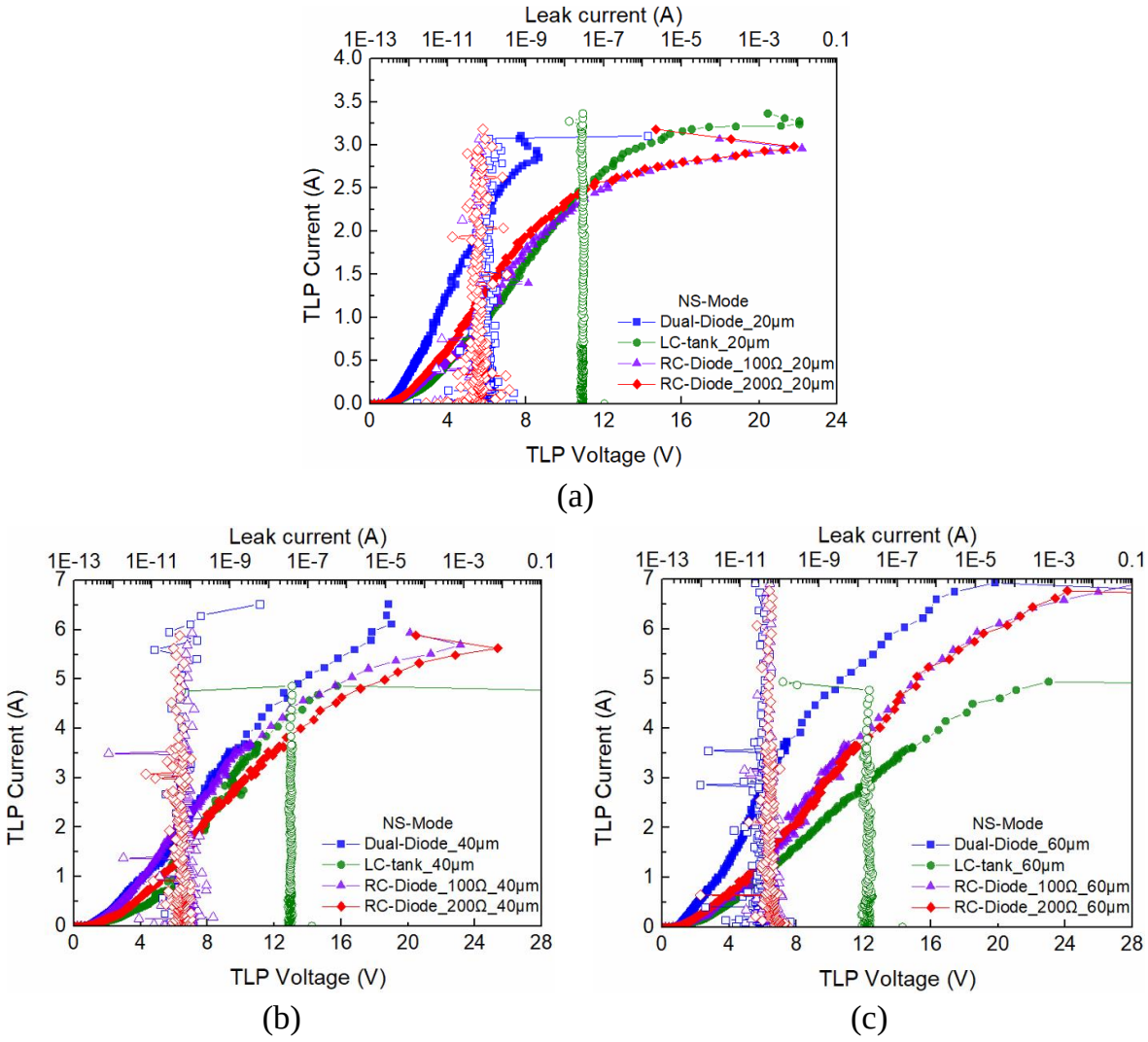


Fig. 2.29. The TLP I-V curves of traditional and proposed designs under NS mode.

(4) Negative to V_{DD} (ND-mode)

The ND-mode discharge path of these traditional and proposed ESD protection circuits is through the diode located from the I/O pad to V_{SS} and power-rail ESD clamp circuit in series. Fig. 2.30 (a) shows that the TLP I-V curves of RC-Diode_100Ω_20μm and RC-Diode_200Ω_20μm are compared with the TLP I-V curves of Dual-Diode_20μm and LC-tank_20μm. Fig. 2.30 (b) shows that the TLP I-V curves of RC-Diode_100Ω_40μm and RC-Diode_200Ω_40μm are compared with the TLP I-V curves of Dual-Diode_40μm and LC-tank_40μm. Fig. 2.30 (c) shows that the TLP I-V curves of RC-Diode_100Ω_60μm and RC-Diode_200Ω_60μm are compared with the TLP I-V curves of Dual-Diode_60μm and LC-tank_60μm.

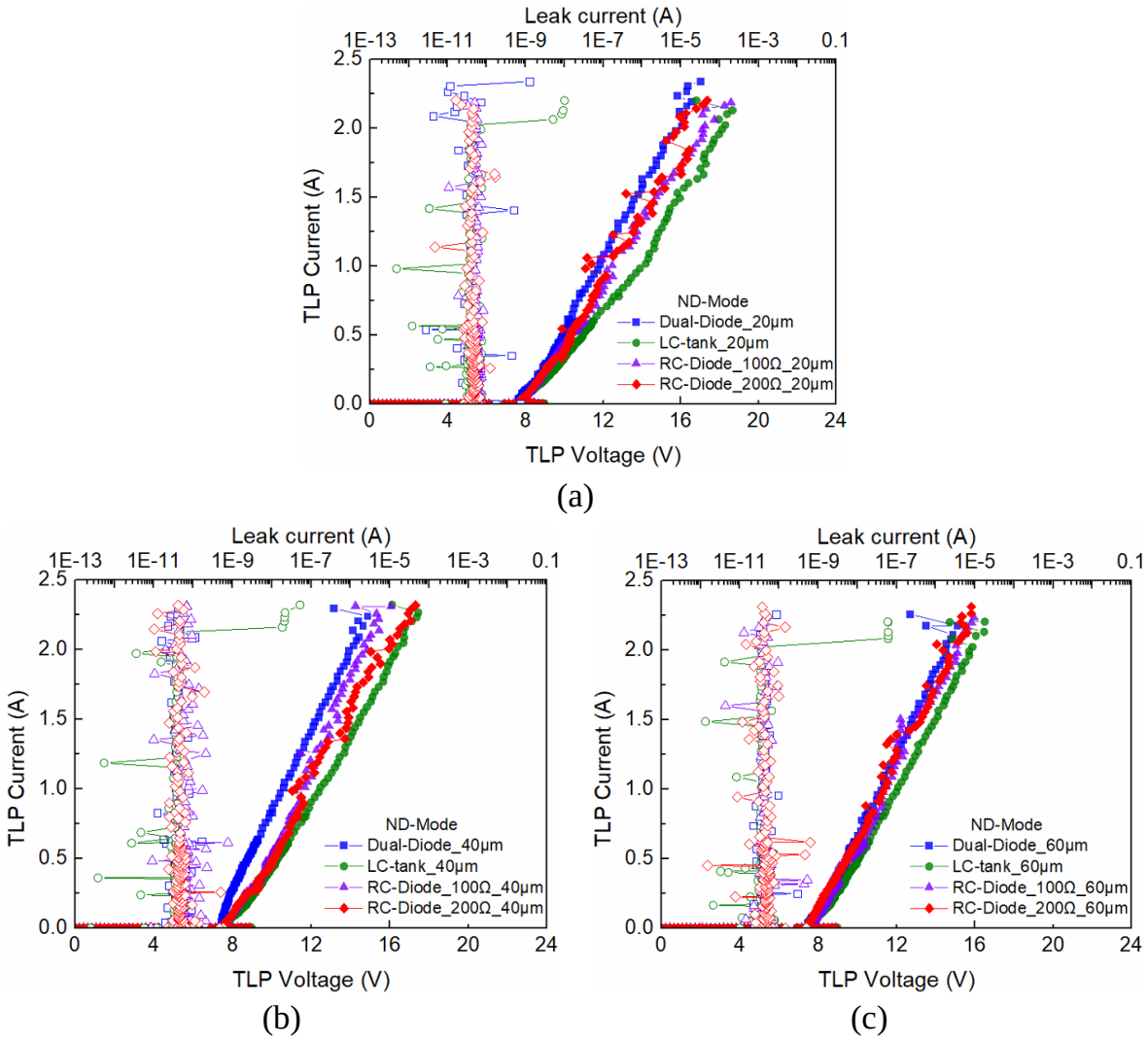
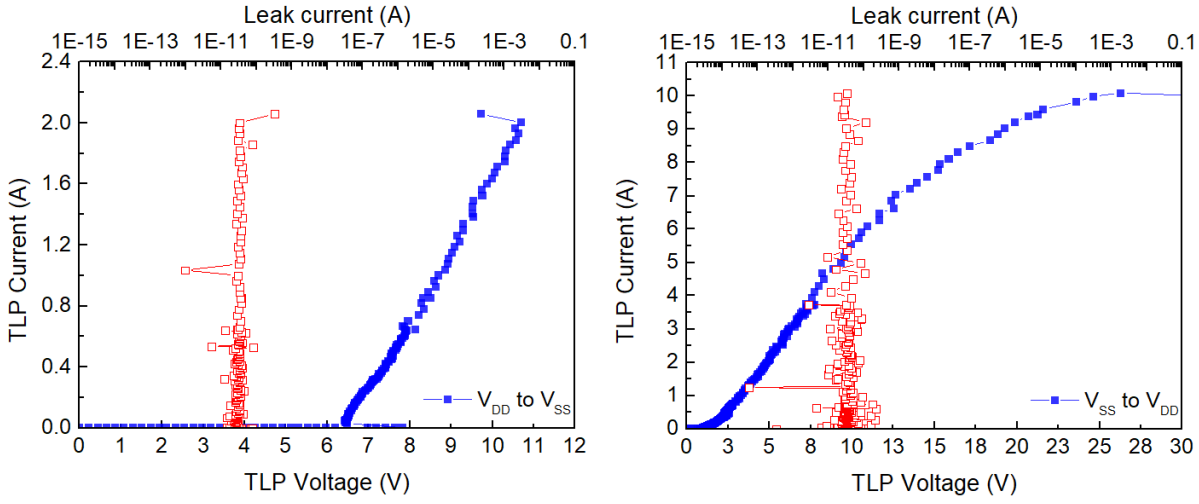


Fig. 2.30. The TLP I-V curves of traditional and proposed designs under ND mode.

(5) Power-Rail ESD Clamp Circuit

The power-rail ESD clamp circuit can discharge ESD current from V_{DD} to V_{SS} when an ESD event occurred on the V_{DD} pad. An NMOS device with an RC network control circuit forms the primary ESD discharge path. The inside parasitic diode of NMOS also provides an ESD discharge path from V_{SS} to V_{DD}.

As shown in Fig. 2.31, the TLP I-V curves of the power-rail ESD clamp circuit is measured. The trigger voltage of the power-rail ESD clamp circuit is 7.8V, and the power-rail ESD clamp circuit can withstand ESD current (I_{t2}) of 2A from V_{DD} to V_{SS}. The trigger voltage of the power-rail ESD clamp circuit is 0.7V, and the power-rail ESD clamp circuit can withstand ESD current (I_{t2}) of 10.2A from V_{SS} to V_{DD}.



(a) (b)

Fig. 2.31. The TLP I-V curves of power-rail ESD clamp circuit under (a) V_{DD} to V_{SS} and (b) V_{SS} to V_{DD}.

Table 2.5. The measured results of secondary breakdown current (I_{t2}).

It2 (A)				
Cell Name	PS-mode	PD-mode	NS-mode	ND-mode
Dual-Diode_20µm	2.2	2.8	2.9	2.1
LC-tank_20µm	2.0	3.3	3.2	2.0
RC-Diode_100Ω_20µm	2.0	3.9	3.0	2.0
RC-Diode_200Ω_20µm	2.1	3.6	3.0	2.0
Dual-Diode_40µm	2.0	6.9	6.1	2.1
LC-tank_40µm	2.1	4.8	4.8	2.0
RC-Diode_100Ω_40µm	2.0	6.7	5.7	2.0
RC-Diode_200Ω_40µm	2.0	6.2	5.6	2.0
Dual-Diode_60µm	2.1	6.9	6.9	2.1
LC-tank_60µm	2.1	4.9	4.8	2.0
RC-Diode_100Ω_60µm	2.0	6.8	6.9	2.0
RC-Diode_200Ω_60µm	1.9	6.8	6.8	2.0

2.4.3 HBM Robustness

As shown in Fig. 2.32, the human-body model (HBM) test is implemented to obtain HBM ESD robustness of traditional and proposed architecture by compact ESD simulator HCE-5000 in the thesis. The HBM tester is regulated the stress from 0.5kV to 8kV and one step 0.5kV during the measurement process. In order to ascertain these traditional and proposed ESD protection circuits are broken, the standard is defined as leakage current shifting more than 30%. The HBM level results of these traditional and proposed ESD protection circuits are consolidated in Table 2.6.

Fig. 2.32. The picture of HBM tester.

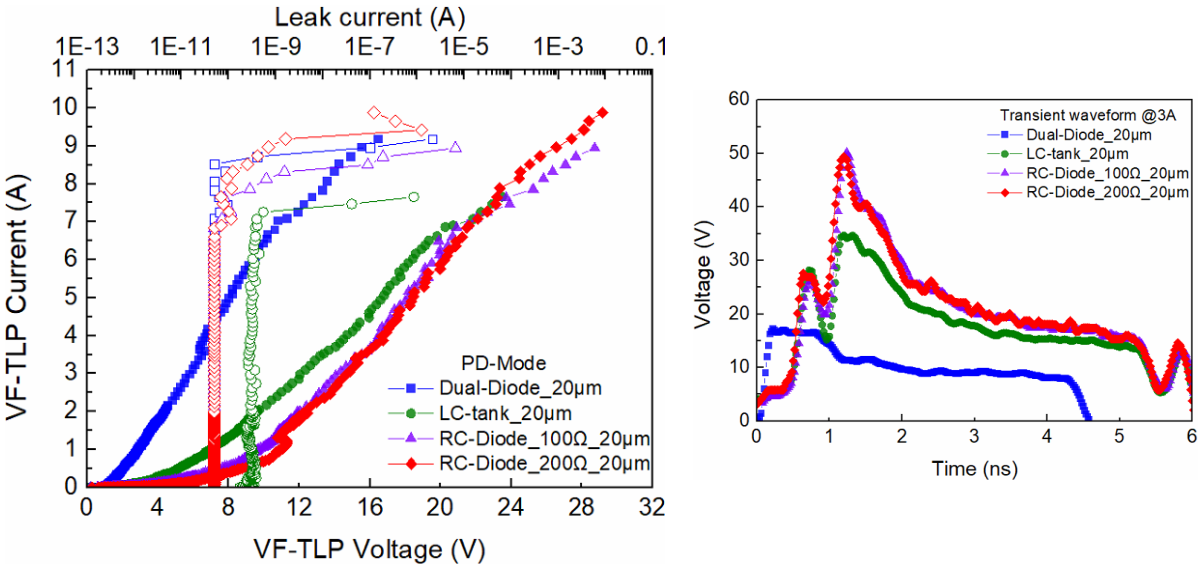
Table 2.6. The HBM test results.

HBM (kV)				
Cell Name	PS-mode	PD-mode	NS-mode	ND-mode
Dual-Diode_20µm	3.5	4.5	4.5	3.5
LC-tank_20µm	3.5	5.5	5.5	3.5
RC-Diode_100Ω_20µm	3.5	5.5	5.5	3.5
RC-Diode_200Ω_20µm	3.5	5.5	5.5	3.5
Dual-Diode_40µm	3.5	>8	>8	3.5
LC-tank_40µm	3.5	>8	>8	3.5
RC-Diode_100Ω_40µm	3.5	>8	>8	3.5
RC-Diode_200Ω_40µm	3.5	>8	>8	3.5
Dual-Diode_60µm	3.5	>8	>8	3.5
LC-tank_60µm	3.5	>8	>8	3.5
RC-Diode_100Ω_60µm	3.5	>8	>8	3.5
RC-Diode_200Ω_60µm	3.5	>8	>8	3.5

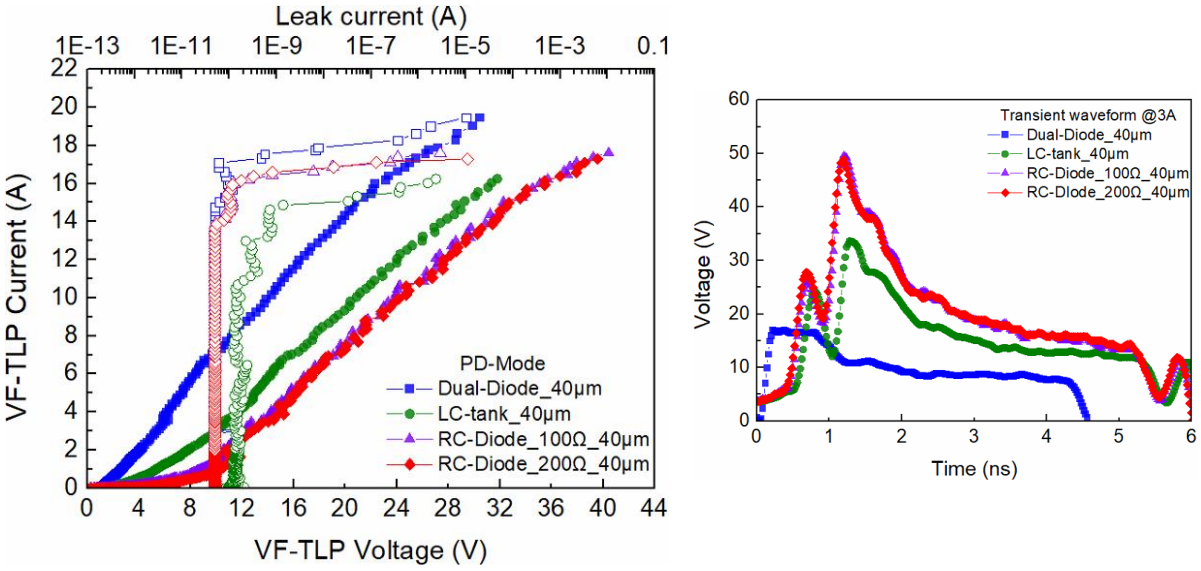
2.4.4 Very-Fast Transmission-line pulsing (VF-TLP) Measurement

As shown in Fig. 2.33, the very-fast TLP (VF-TLP) measured system is used to investigate the effectiveness of these ESD protection devices in the time domain of a Charged-device model (CDM) ESD event [27], [28]. The VF-TLP is set with a rise time of 200ps and a pulse width of 5ns to evaluated the turn-on behavior of the traditional and proposed designs under CDM-like fast-transient conditions. Fig. 2.34 (a) shows the measured VF-TLP I-V curves and transient waveforms at 3A of Dual-Diode_20μm, LC-tank_20μm, RC-Diode_100Ω_20μm, and RC-Diode_200Ω_20μm under PD mode. Fig. 2.34 (b) shows the measured VF-TLP I-V curves and transient waveforms at 3A of Dual-Diode_40μm, LC-tank_40μm, RC-Diode_100Ω_40μm, and RC-Diode_200Ω_40μm under PD mode.

Fig. 2.33. The very-fast transmission-line pulse (VF-TLP) measured system [26].



(a)



(b)

Fig. 2.34. The VF-TLP I-V curves and transient waveform at 3A of traditional and proposed designs under PD mode.

2.5 Comparison and Discussion of This Test Chip

As shown in Table 2.7, these ESD protection circuits are measured under PS mode. The trigger voltage (V_{t1}) that is about 10V is defined as the current value of TLP measured results is more than 1mA. The turn-on resistance (R_{on}) is about 4~6Ω when they are becoming a conductor. The secondary breakdown current (I_{t2}) of these ESD protection circuits is similar. When operating at 1.8V, the leakage current of the traditional LC tank is about 130nA, and others are less than 0.1nA.

Table 2.7. The comparison of traditional and proposed designs under PS mode.

PS-mode					
Cell Name	V_{t1} (V)	I_{t2} (A)	R_{on} (Ω)	HBM (kV)	Leakage current (nA) @1.8V
Dual-Diode_20μm	9.4	2.2	4.1	3.5	<0.1
LC-tank_20μm	9.6	2.0	6.3	3.5	101
RC-Diode_100Ω_20μm	10.2	2.0	4.5	3.5	<0.1
RC-Diode_200Ω_20μm	11.8	2.1	4.7	3.5	<0.1
Dual-Diode_40μm	9.3	2.0	4.3	3.5	<0.1
LC-tank_40μm	9.4	2.1	6.5	3.5	130
RC-Diode_100Ω_40μm	10.3	2.0	4.4	3.5	<0.1
RC-Diode_200Ω_40μm	11.0	2.0	6.3	3.5	<0.1
Dual-Diode_60μm	9.2	2.1	4.5	3.5	<0.1
LC-tank_60μm	9.4	2.1	5.4	3.5	150
RC-Diode_100Ω_60μm	10.2	2.0	3.7	3.5	<0.1
RC-Diode_200Ω_60μm	11.2	1.9	6.2	3.5	<0.1

As shown in Table 2.8, the traditional and proposed ESD protection circuits are compared under PD mode. The trigger voltage (V_{t1}) is seen as the current value of TLP measured results is more than 1mA. The discharge path of the proposed RC-diode ESD protection circuit is almost the same as the discharge path of traditional dual-diode and LC-tank ESD protection circuit. Consequently, these traditional and proposed ESD protection circuits are triggered at about 0.8V. The secondary breakdown current (I_{t2}) of traditional dual diode and proposed RC diode is similar. However, the traditional LC tank is relatively tiny. The turn-on resistance (R_{on}) is about 2~3Ω when they are becoming a conductor.

Table 2.8. The comparison of traditional and proposed designs under PD mode.

PD-mode					
Cell Name	V_{t1} (V)	I_{t2} (A)	R_{on} (Ω)	HBM (kV)	Leakage current (nA) @1.8V
Dual-Diode_20μm	0.8	2.8	2.9	4.5	<0.1
LC-tank_20μm	0.8	3.3	3.2	5.5	<0.1
RC-Diode_100Ω_20μm	0.8	3.9	2.8	5.5	<0.1
RC-Diode_200Ω_20μm	0.8	3.6	3.1	5.5	<0.1
Dual-Diode_40μm	0.8	6.9	1.6	>8	<0.1
LC-tank_40μm	0.8	4.8	3.3	>8	<0.1
RC-Diode_100Ω_40μm	0.8	6.7	2.2	>8	<0.1
RC-Diode_200Ω_40μm	0.8	6.2	2.4	>8	<0.1
Dual-Diode_60μm	0.8	6.9	1.4	>8	<0.1
LC-tank_60μm	0.8	4.9	2.8	>8	<0.1
RC-Diode_100Ω_60μm	0.8	6.8	2.7	>8	<0.1
RC-Diode_200Ω_60μm	0.8	6.8	2.3	>8	<0.1

As shown in Table 2.9, the traditional and proposed ESD protection circuits are compared under NS mode. The trigger voltage (V_{t1}) is defined as the current value of TLP measured results is more than 1mA. The discharge path of dual diode, LC tank, and proposed RC diode are through N-type diode under NS mode. The V_{t1} of traditional and proposed ESD protection circuits is triggered at about 0.8V. The I_{t2} of Dual-Diode_60μm and RC-Diode_200Ω_60μm are higher than Dual-Diode_40μm and RC-Diode_200Ω_40μm, respectively. The turn-on resistance (R_{on}) is about 2~3Ω when they are becoming conductors. When operating at 1.8V, the leakage current of the traditional LC tank is about 130nA, and others are less than 0.1nA.

Table 2.9. The comparison of traditional and proposed designs under NS mode.

NS-mode					
Cell Name	V_{t1} (V)	I_{t2} (A)	R_{on} (Ω)	HBM (kV)	Leakage current (nA) @1.8V
Dual-Diode_20μm	0.8	2.9	2.1	4.5	<0.1
LC-tank_20μm	0.6	3.2	3.0	5.5	104
RC-Diode_100Ω_20μm	0.8	3.0	3.2	5.5	<0.1
RC-Diode_200Ω_20μm	0.8	3.0	3.1	5.5	<0.1
Dual-Diode_40μm	0.8	6.1	2.6	>8	<0.1
LC-tank_40μm	0.6	4.8	2.2	>8	130
RC-Diode _100Ω_40μm	0.8	5.7	2.1	>8	<0.1
RC-Diode_200Ω_40μm	0.8	5.6	3.0	>8	<0.1
Dual-Diode_60μm	0.8	6.9	2.0	>8	<0.1
LC-tank_60μm	0.6	4.8	3.1	>8	137
RC-Diode_100Ω_60μm	0.8	6.9	2.6	>8	<0.1
RC-Diode_200Ω_60μm	0.8	6.8	2.5	>8	<0.1

As shown in Table 2.10, the traditional and proposed ESD protection circuits are compared under ND mode. The discharge path of traditional dual-diode, LC-tank, and proposed RC-diode ESD protection circuits is through power-rail ESD clamp circuit under ND mode. The trigger voltage (V_{t1}) is defined as the current value of TLP measured results is more than 1mA. The V_{t1} of traditional dual-diode, LC-tank, and proposed RC-diode ESD protection circuits is about 9V. The secondary breakdown current (I_{t2}) of traditional dual diode, LC tank, and proposed RC diode are similar. The turn-on resistance (R_{on}) is about 3~4Ω when they are becoming a conductor.

Table 2.10. The comparison of traditional and proposed designs under ND mode.

ND-mode					
Cell Name	V_{t1} (V)	I_{t2} (A)	R_{on} (Ω)	HBM (kV)	Leakage current (nA) @1.8V
Dual-Diode_20μm	8.9	2.1	3.5	3.5	<0.1
LC-tank_20μm	9.0	2.0	6.4	3.5	<0.1
RC-Diode_100Ω_20μm	8.7	2.0	4.3	3.5	<0.1
RC-Diode_200Ω_20μm	8.9	2.0	3.9	3.5	<0.1
Dual-Diode_40μm	8.8	2.1	3.6	3.5	<0.1
LC-tank_40μm	9.0	2.0	4.3	3.5	<0.1
RC-Diode_100Ω_40μm	8.9	2.0	3.4	3.5	<0.1
RC-Diode_200Ω_40μm	8.9	2.0	4.2	3.5	<0.1
Dual-Diode_60μm	8.7	2.1	3.6	3.5	<0.1
LC-tank_60μm	9.0	2.0	4.0	3.5	<0.1
RC-Diode_100Ω_60μm	8.9	2.0	3.7	3.5	<0.1
RC-Diode_200Ω_60μm	8.9	2.0	3.9	3.5	<0.1

These measured results of traditional and proposed ESD protection circuits are discussed including TLP measurement and high-frequency measurement.

From TLP measurement results, the I_{t2} of PS-mode and ND-mode discharge paths is only 2A. It is why the discharge paths of all ESD protection circuits will pass through the power-rail ESD clamp circuit between V_{DD} and V_{SS}. As shown in Fig. 2.30 (a), this power-rail ESD clamp circuit can discharge up to 2A from V_{DD} to V_{SS}. The variable quantity of I_{t2} with 40μm and 60μm is slight under PD-mode discharge path and NS-mode discharge path because the metal line is not thick enough to burn out. Because the power-rail ESD clamp circuit is used to discharge from V_{DD} to V_{SS} by parasitic bipolar transistors, the V_{t1} of PS-mode and ND-mode discharge paths is higher than PD-mode and NS-mode discharge paths. The R_{on} of PS-mode discharge path is more significant than PD-mode discharge path since PS-mode discharge path requires additional the power-rail ESD clamp circuit. The same is true for the ND-mode discharge path and NS-mode discharge path.

From high-frequency measurement results, the S_{21} of the proposed RC-diode ESD protection circuit with widths of 20μm, 40μm, and 60μm are smaller than the S_{21} of the traditional dual-diode ESD protection circuits with widths of 20μm, 40μm, and 60μm, respectively. The proposed RC-diode ESD protection circuits with 200Ω are also smaller than RC-diode ESD protection circuits with 100Ω. The traditional LC-tank ESD protection circuits can be designed to match the parasitic capacitance of the ESD protection device by the inductor at the operating frequency. However, the inductor of the LC-tank ESD protection circuits require large layout area to increase the cost. Because the thickness of the metal layer is limited by the manufacturing process, the quality factor (Q) of the inductor in the LC tank can only be achieved about 5 according to the simulation result. Therefore, the measured high-frequency performance of LC tank which is still lossy is listed in Table 2.4.

In the research, the traditional and proposed ESD protection circuits are made with three diode sizes, including 20μm, 40μm, and 60μm. The high-frequency performance and layout area of traditional and proposed ESD protection circuits which are compared are listed in Table 2.11. Under the size of the diode is the same, although traditional dual diode is higher signal loss than proposed RC diode, the traditional dual diode occupies smaller layout area. Although traditional LC tank have less signal loss than proposed RC diode, traditional LC tank occupies larger layout area. Therefore, a comprehensive comparison is found that proposed RC-diode ESD protection circuits can occupy a smaller layout area and have low signal loss to apply to high frequency at the same time.

Table 2.11. The comparison results of traditional and proposed designs.

Cell Name	Freq. (GHz)	$\|S_{21}\|$ (dB)	HBM (kV)	Area (μm^2)
Dual-Diode_20μm	20	2.9	4.5	559
LC-tank_20μm	20	1.3	5.5	33537
RC-Diode_100Ω_20μm	20	2.0	5.5	2018
RC-Diode_200Ω_20μm	20	1.6	5.5	2246
Dual-Diode_40μm	14	4.3	>8	995
LC-tank_40μm	14	1.8	>8	38417
RC-Diode_100Ω_40μm	14	2.5	>8	2930
RC-Diode_200Ω_40μm	14	1.9	>8	3157
Dual-Diode_60μm	10	4.0	>8	1431
LC-tank_60μm	10	2.2	>8	43297
RC-Diode_100Ω_60μm	10	2.5	>8	3842
RC-Diode_200Ω_60μm	10	1.9	>8	4069

2.6 Comparison of Proposed RC Diode and Literature

As shown in Table 2.12, this proposed RC-diode ESD protection circuits are compared with other traditional ESD protection circuits for high-frequency applications. The HBM level is high, which means the protection circuit has better ESD robustness. The ESD protection circuit is small that can save area and cost. The signal loss ($|S_{21}|$) is as small as possible to reduce the influence performance of the internal circuit. Therefore, the figure-of-merit (FOM) is defined (HBM/$|S_{21}|$/Area) by the above points. The value of larger FOM will be the best. The proposed RC-diode ESD protection circuits have better characteristics than other traditional.

Table 2.12. The comparison of ESD protection design for high-frequency application.

ESD protection design	Process	Freq. (GHz)	$\|S_{21}\|$ (dB)	HBM (kV)	Area (μm^2)	FOM ($V \cdot dB^{-1} \cdot \mu m^{-2}$)
Pi-type [29]	65nm CMOS	60	1.0	2.5	27040	0.09
LESD [30]	65nm CMOS	77	0.9	4.05	10000	0.45
LASCR _W30_3D [31]	180nm CMOS	30	1.3	4.5	9500	0.36
RC-Diode _100Ω_20μm	350nm CMOS	20	2.0	5.5	2018	1.36
RC-Diode _200Ω_20μm	350nm CMOS	20	1.6	5.5	2246	1.53

2.7 Summary

The traditional and proposed RC-diode ESD protection circuits have been implemented in CMOS process. These ESD protection circuits need outstanding ESD robustness and bring low signal loss because they are applied to RF_{IN}/RF_{OUT} pad. Based on the measurement results, the traditional dual-diode ESD protection circuits can provide the ESD tolerance, but the high-frequency signal will be lost. At the same size of the diode, the proposed RC-diode ESD protection circuits cause signal loss that is lower than the traditional dual-diode ESD protection circuits. Although the traditional LC-tank ESD protection circuits can diminish the signal loss, they occupy much larger area than the proposed RC-diode ESD protection circuits. These measurement results ascertain that the proposed RC-diode ESD protection circuits have higher ESD robustness and lower signal loss than the traditional ones.

In the next chapter, to construct a whole-chip ESD protection, the power-rail ESD clamp circuits will be introduced and analyzed for operating normal and fast power-on at the power terminal.

Chapter 3

ESD Clamp Circuits for Power Terminal Application

Although ESD protection circuits of application the input/output terminal are presented in Chapter 2, the internal circuits are not protected comprehensively. As a result, this chapter has studied and analyzed the power-rail ESD clamp circuits that apply to the power-supply terminal and are fabricated in CMOS process. Furthermore, it discusses whether the power-rail ESD clamp circuits with different trigging mechanisms discharge the ESD current through the transistor and the feasibility of the normal power-on and fast power-on.

3.1 Power-Rail ESD Clamp Circuits

These power-rail ESD clamp circuits are equipped with different detection mechanism circuits to trigger large-size NMOS transistors. In the essay, the large-size NMOS transistor is designed to discharge the ESD current is called M_{ESD}. These detection circuit architectures are made, including resistor-capacitor inverter mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism as follows.

3.1.1 Resistor-Capacitor Inverter Mechanism [19]

As shown in Fig. 3.1, the power-rail ESD clamp circuit with resistor-capacitor inverter mechanism consists of the resistor (R_1), capacitor (C_1), inverter (M_{p1} and M_{n1}) and a large-size NMOS transistor (M_{ESD}). Firstly, the M_{ESD} can be controlled by the resistor (R_1), capacitor (C_1), and inverter. Typically, the rising time of the normal power-on event is milliseconds, while the ESD event is nanoseconds. Therefore, the RC-time constant is designed to be 0.1 microseconds, R_1 is 100kΩ, and C_1 is 1pF in the research. Secondly, the inverter comprises M_{p1} and M_{n1}. The width and length of the former are set to be 80μm and 0.3μm, while the latter is 20μm and 0.35μm. Furthermore, the width of the M_{ESD} is 400μm because it can provide to discharge the ESD current. These test parameters are listed in Table 3.1. This thesis makes power-rail ESD clamp with resistor-capacitor inverter mechanism compare ESD robustness and power loss with the others turn-on mechanism. The layout top view of the power-rail ESD clamp with the resistor-capacitor inverter mechanism is shown in Fig. 3.2.

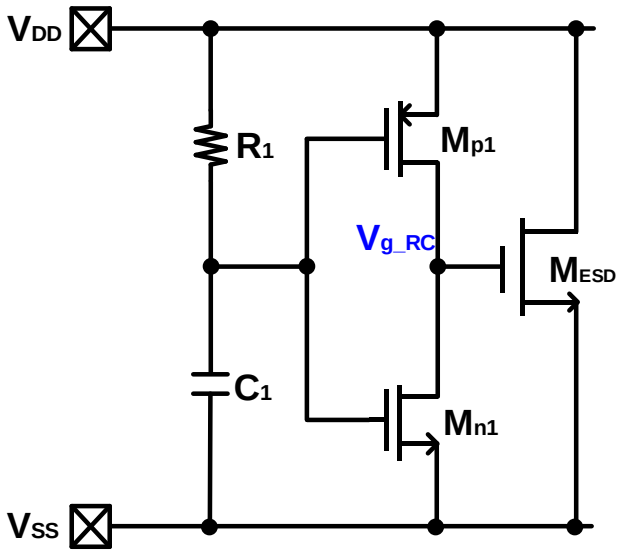


Fig. 3.1. The power-rail ESD clamp with resistor-capacitor inverter mechanism.

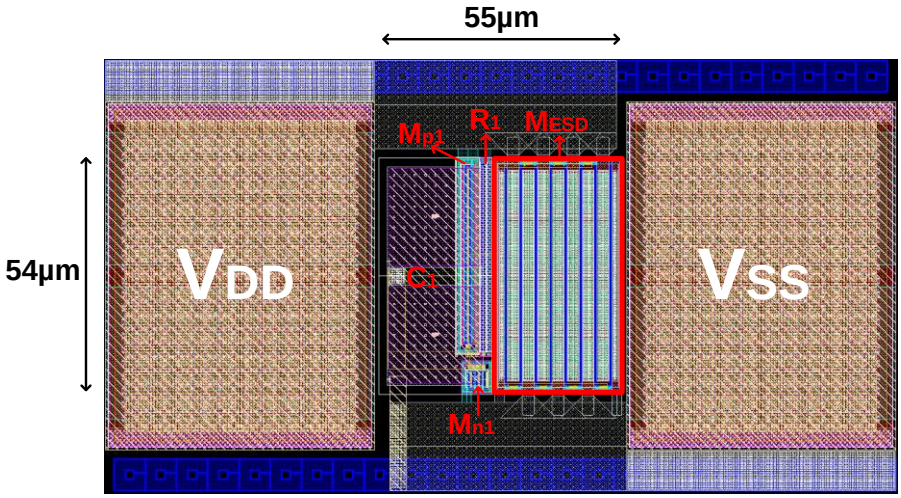


Fig. 3.2. The layout top view of resistor-capacitor inverter mechanism

Table 3.1. The parameter of power-rail ESD clamp circuit with resistor-capacitor inverter mechanism.

Cell Name	Device	Value
Resistor-Capacitor Mechanism	Resistor	R_1=100kΩ
	Capacitor	C_1=1pF
	PMOS W/L	M_{p1}=80μm/0.3μm
	NMOS W/L	M_{n1}=20μm/0.35μm M_{ESD}=400μm/0.35μm

3.1.2 Diode-Trigger Mechanism [20]

As shown in Fig. 3.3, the power-rail ESD clamp circuit with a diode-trigger mechanism is composed of resistor (R_1), diode string, inverter (M_{p1} and M_{n1}), and a large-size NMOS transistor (M_{ESD}). The M_{ESD} can be controlled by the resistor (R_1), diode string, and inverter. In order to make the power-rail ESD clamp circuit is turned off under the condition of the normal power-on at 1.8V, the diode string is selected with four diodes. First of all, the size of all diodes are set to 10μm × 10μm and R_1 is 100kΩ. Then, the width and length of the M_{p1} are 80μm and 0.3μm while the M_{n1} are 20μm and 0.35μm. Finally, to provide high robustness, the width of the M_{ESD} is selected as 400μm. These test parameters are presented in Table 3.2. The thesis makes a power-rail ESD clamp with diode-trigger mechanism to compare ESD robustness and power loss with the other turn-on mechanism. The layout top view is shown in Fig. 3.4.

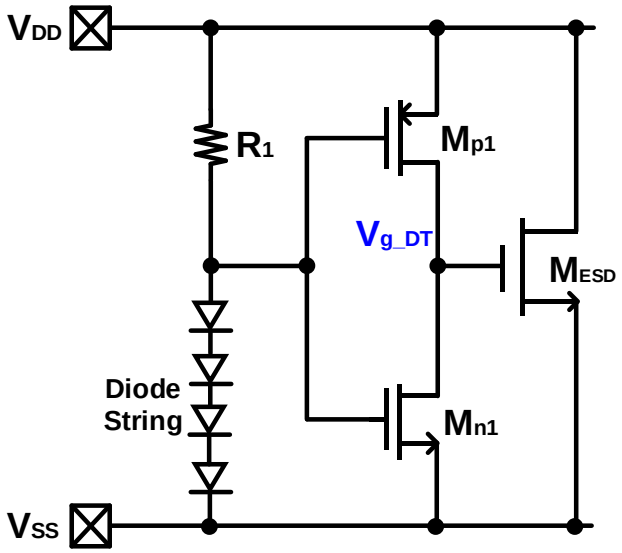


Fig. 3.3. The power-rail ESD clamp with diode-trigger mechanism.

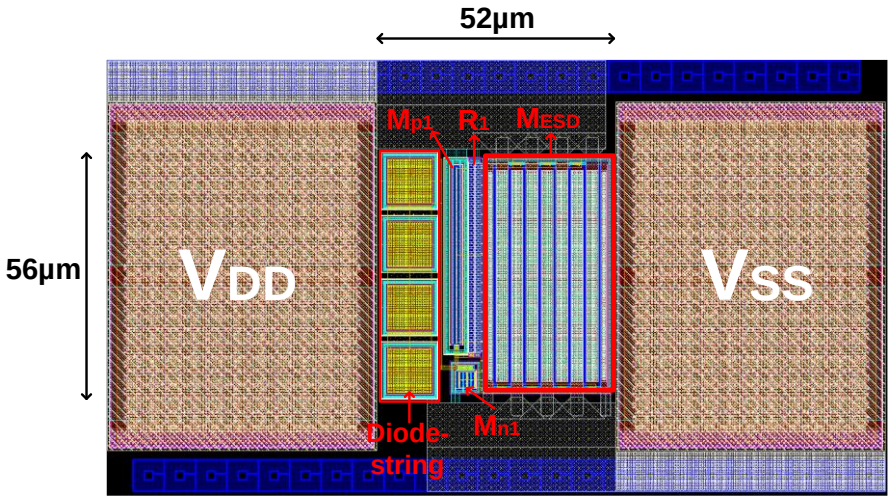


Fig. 3.4. The layout top view of diode-trigger mechanism.

Table 3.2. The parameter of power-rail ESD clamp circuit with diode-trigger mechanism.

Cell Name	Device	Value
Diode-Trigger Mechanism	Resistor	R_1=100kΩ
	Diode W*L	10μm*10μm
	PMOS W/L	M_{p1}=80μm/0.3μm
	NMOS W/L	M_{n1}=20μm/0.35μm M_{ESD}=400μm/0.35μm

3.1.3 Positive-Feedback Mechanism [21]

The desired specification of power-rail ESD clamp circuit with positive-feedback mechanism should operate on the normal power-on and fast power-on without being triggered and conserve silicon area. The architecture is shown in Fig. 3.5. In order to ensure the power-rail ESD clamp circuit is turned off under the condition of normal power-on at 1.8V, the diode string is composed of four diodes. In addition, each diode dimension of the diode string is designed as 10μm × 10μm. The NMOS (M_{n1}) is used to reduce the standby leakage current along the diode string with a width of 2μm. The resistor (R_1) which is used to trigger PMOS (M_{p1}) isolates the static electricity direct contact diode string. The purpose of the PMOS (M_{p1}) is to control the gate of M_{ESD} quickly under ESD conditions, and that is why the width is set to be 80μm. Furthermore, to provide a discharging path under the ESD event, the width of the M_{ESD} is designed to be 400 μm because the ESD robustness is primarily affected by it. When static electricity occurs at the V_{DD} terminal, the gate level of the M_{ESD} has a high potential that will be coupled through the parasitic capacitance (C_{gd}). The layout top view is shown in Fig. 3.6, and the test parameters are listed in Table 3.3. The power-rail ESD clamp with a positive-feedback mechanism compares ESD robustness and power loss with the others turn-on mechanism. The design parameter of the devices is discussed among the power-rail ESD clamp circuit in the next section.

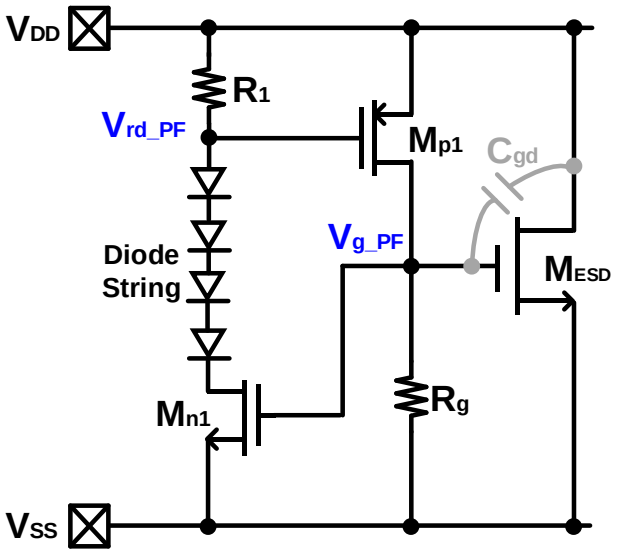


Fig. 3.5. The power-rail ESD clamp with positive-feedback mechanism.

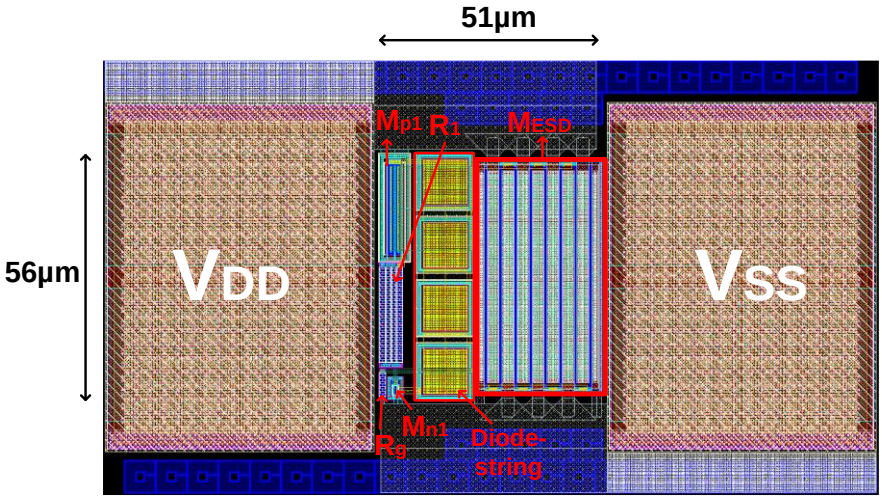


Fig. 3.6. The layout top views of positive-feedback mechanism.

Table 3.3. The parameter of power-rail ESD clamp circuit with positive-feedback mechanism.

Cell Name	Device	Value
Positive-Feedback Mechanism	Resistor	R_1=100kΩ and R_g=2kΩ
	Diode W*L	10μm*10μm
	PMOS W/L	M_{p1}=80μm/0.3μm
	NMOS W/L	M_{n1}=2μm/0.35μm M_{ESD}=400μm/0.35μm

3.1.4 Double-Detector Mechanism [22]

As shown in Fig. 3.7, the power-rail ESD clamp circuit with double-detector mechanism is divided into four parts that included resistance (R_1)-capacitance (C_1) transient mechanism, diode string, stacked PMOS transistors (M_{p1} and M_{p2}) and NMOS transistor (M_{ESD}) of a large width. The M_{ESD} can be controlled by stacked PMOS transistors (M_{p1} and M_{p2}). The diode string is selected with four diodes to turn off the M_{ESD} under the condition of the power-on at 1.8V. Firstly, the size of all diodes is selected as 10μm × 10μm, and the R_1 and R_2 are both selected as 100kΩ. Then, the width and length of the M_{p1} and M_{p2} are both 80μm and 0.3μm. Lastly, the width and length of the M_{n1} are 2μm and 0.35μm. In order to provide high robustness, the width of the M_{ESD} is selected as 400μm. The test parameters are listed in Table 3.4. Finally, the purpose of the thesis is to compare the ESD robustness and power loss of the power-rail ESD clamp with a double-detector mechanism to the others with turn-on mechanism. The layout top view is shown in Fig. 3.8.

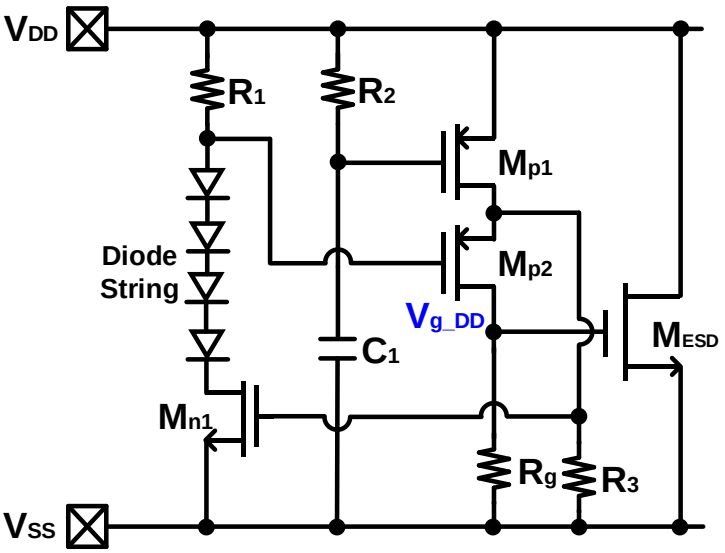


Fig. 3.7. The power-rail ESD clamp with double-detector mechanism

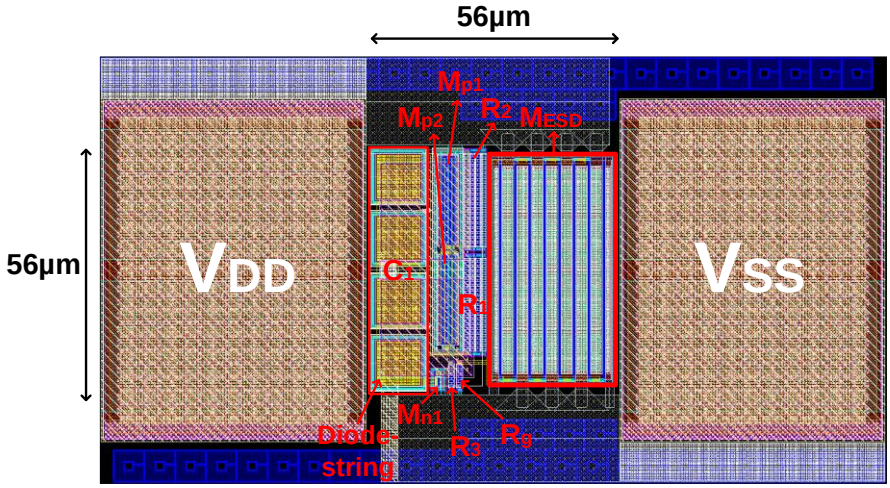


Fig. 3.8. The layout top views of double-detector mechanism.

Table 3.4. The parameter of power-rail ESD clamp circuit with double-detector mechanism.

Cell Name	Device	Value
Double-Detector Mechanism	Resistor	R_1 and R_2=100kΩ R_3 and R_g=2kΩ
	Capacitor	C_1=1pF
	Diode W*L	10µm*10µm
	PMOS W/L	M_{p1}=80µm/0.3µm M_{p2}=80µm/0.3µm
	NMOS W/L	M_{n1}=2µm/0.35µm M_{ESD}=400µm/0.35µm

3.2 Simulation Results

These power-rail ESD clamp circuits with different triggering mechanisms is simulated by Advanced Design System (ADS) simulation. These power-rail ESD clamp circuits are mainly divided into three-type situations for simulation, including the condition of ESD stress occurrence, normal power-on at 1.8V, and fast power-on at 1.8V. Furthermore, to compare the performance of the power-rail ESD clamp circuit, there are simulation architectures of resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism.

3.2.1 ESD-like waveform condition

The rising time and pulse width are chosen 10ns and 100ns respectively in the simulation of ESD occurrence. The voltage level of the simulated ESD waveform is selected 5V to prevent drain-substrate junction breakdown of M_{ESD} from affecting the simulation result. From the architecture of the power-rail ESD clamp with positive-feedback mechanism, the characteristics will be affected by resistor R_1, resistor R_g and diode string. The following description is to explain the parameter of these devices in detail and discussion.

The first affecting element is the resistor R_1 that is used to trigger the M_{p1}. At the same time, it will be affected to turn on the speed of the M_{ESD}. The value of the resistor R_1 is adjusted to 25kΩ, 50kΩ, and 100kΩ, and the other parameter are fixed for simulation. The positive-feedback mechanism with three different resistor values is simulated. The voltage on the gate node of the M_{ESD} is simulated and shown in Fig. 3.9. The small resistor value reduces the conduction speed of the power-rail ESD clamp

circuit. Therefore, the resistor value of the R_1 is selected as 100kΩ.

The second effecting element is the trigger resistor R_g that is used to trigger the M_{ESD}. The resistor value of R_g is related to the turn-on speed and coupling effect of the M_{ESD} during the ESD event. The resistor value of the R_g is adjusted to 2kΩ, 5kΩ, and 10kΩ, and the other parameter of the power-rail ESD clamp with positive-feedback mechanism is fixed for simulation. As shown in Fig. 3.10, the large resistor value can improve the turn-on speed of the power-rail ESD clamp circuit with positive-feedback mechanism under ESD stress event. However, the large R_g will be biased to the gate of the M_{ESD} through the parasitic capacitance of the M_{ESD} to cause the influence of the coupling effect. It is desired that the M_{ESD} of the power-rail ESD clamp circuit with positive-feedback mechanism can turn on quickly without a profound coupling effect. Thus, the resistor value of the R_g is chosen as 2kΩ.

The last effecting element is the diode string formed by the traditional P+/N-well junction series. The diode model in the Advanced Design System has provided the corresponding model from the foundry. By the Advanced Design System with these parameter, the junction sizes of each diode are adjusted to 2μm × 2μm, 5μm × 5μm and 10μm × 10μm, and the other parameter of the power-rail ESD clamp with positive-feedback mechanism are fixed for simulation. As shown in Fig. 3.11, the power-rail ESD clamp circuit of positive-feedback mechanism with different sizes of the diode string is simulated and shown gate voltage of M_{ESD} under ESD stress event. The large size can enhance the turn-on speed of the power-rail ESD clamp circuit with positive-feedback mechanism under ESD stress event. Therefore, the size of the diode string is selected as 10μm × 10μm.

In order to understand the positive-feedback mechanism power-rail ESD clamp circuit under simulated ESD stress event, the voltage level of each node is shown in Fig. 3.12. When the voltage level of the V_{DD} is higher than the normal operating voltage of

1.8V, this diode string is turned on to make the voltage level of V_{rd_PF} lower than V_{DD}. Therefore, the M_{p1} device is turned on to conduct a voltage to trigger the M_{ESD}. The Fig. 3.13 shows that the performance comparison results of the resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism with four diodes under ESD stress event. All of these power-rail ESD clamp circuits can be turned on during the simulated ESD waveform.

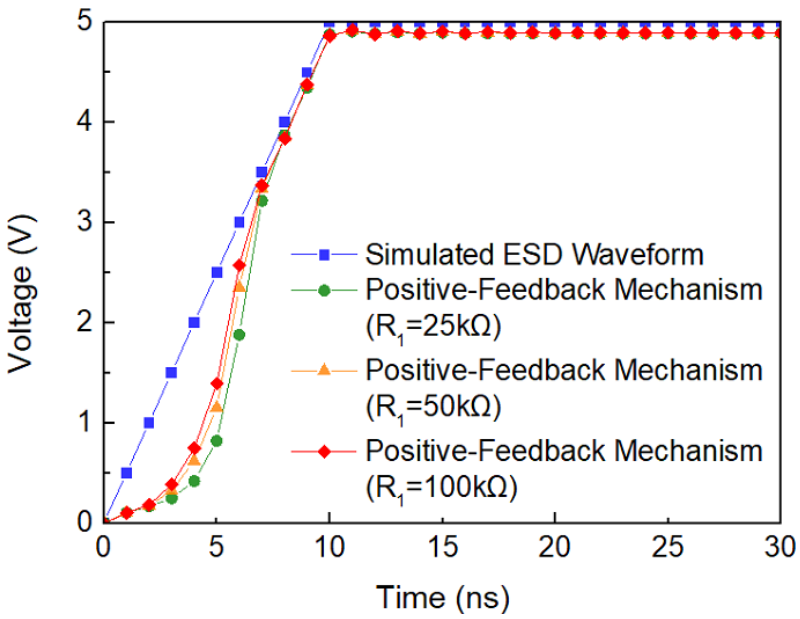


Fig. 3.9. The simulated result of the V_{g_PF} with three different resistor (R_1) value under ESD stress event.

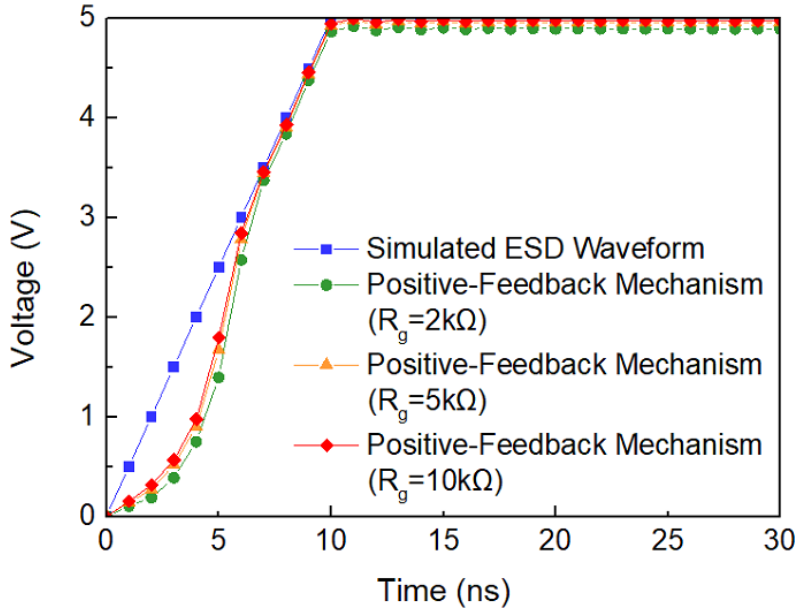


Fig. 3.10. The simulated result of the V_{g_PF} with three different resistor (R_g) value under ESD stress event.

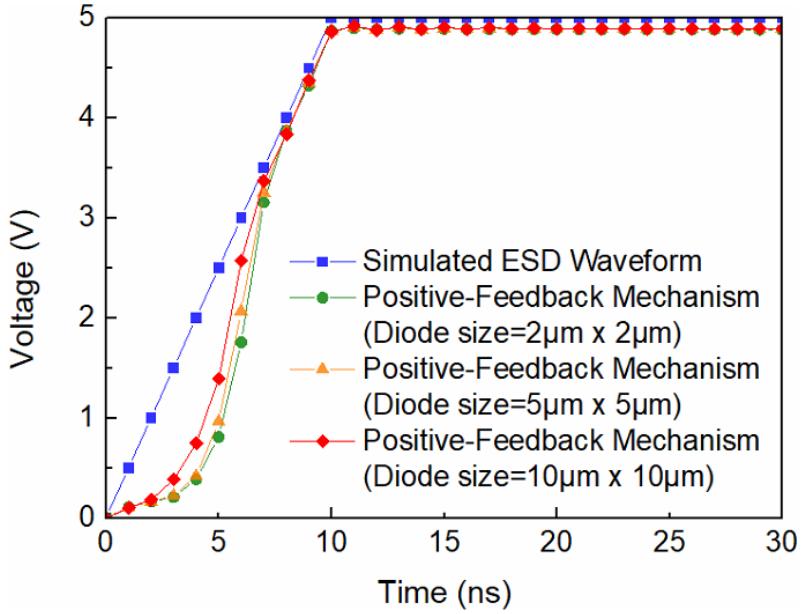


Fig. 3.11. The simulated result of the V_{g_PF} with three different diode sizes under ESD stress event.

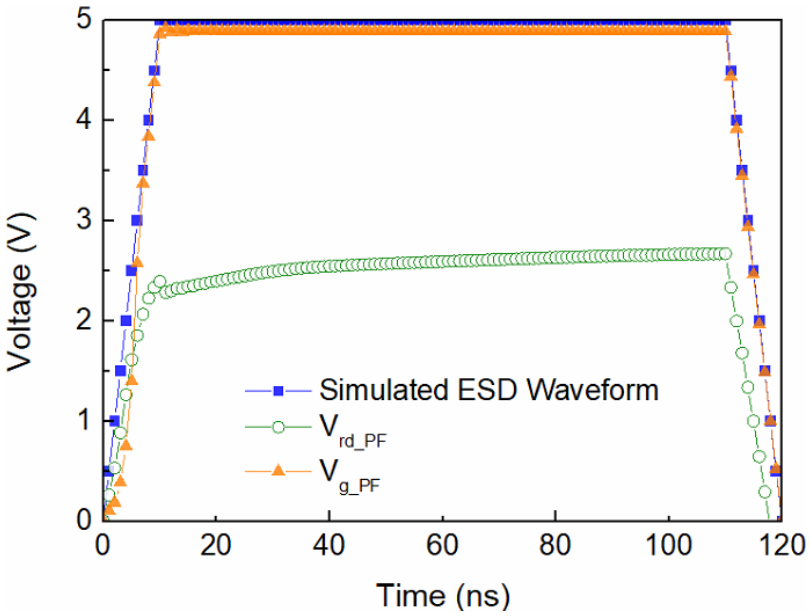


Fig. 3.12. Each node voltage level of the positive-feedback mechanism power-rail ESD clamp circuit under ESD stress event.

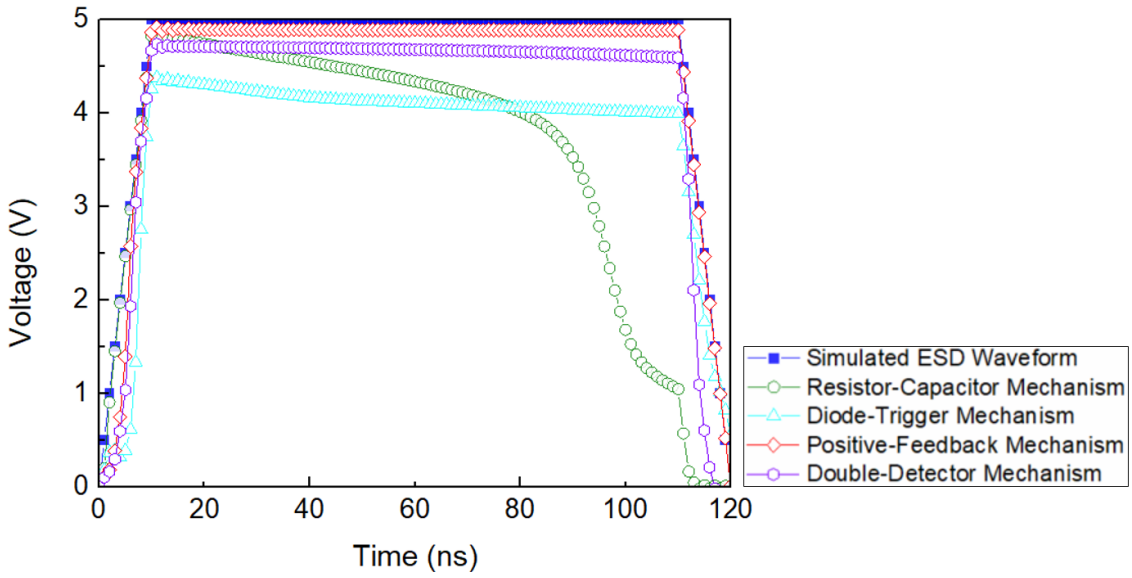


Fig. 3.13. The voltage level of these power-rail ESD clamp circuit on the gate of M_{ESD} under ESD stress event.

3.2.2 Normal Power-on Condition

The rising time of the normal operating voltage waveform is 10ms with a low voltage level of 1.8V. The voltage level of each node during the normal operating situation is shown in Fig. 3.14. Since the power supply provides a voltage of slow rising time, the node V_{rd_PF} can also follow the voltage of slow rising time simultaneously. The diode string is designed to detect the voltage. When the normal operating voltage is lower than the turn-on voltage of the diode string, the diode string is not triggered. As a result, the gate of the M_{p1} acquires a high potential to be turned off. Because the M_{p1} keeps closed, the node V_{g_PF} will be at 0V to keep off the M_{ESD}. As shown in Fig. 3.15, the voltage level of M_{ESD} includes the resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism with four diodes under normal operating voltage. These power-rail ESD clamp circuits can be turned off during the simulation of a normal operating waveform.

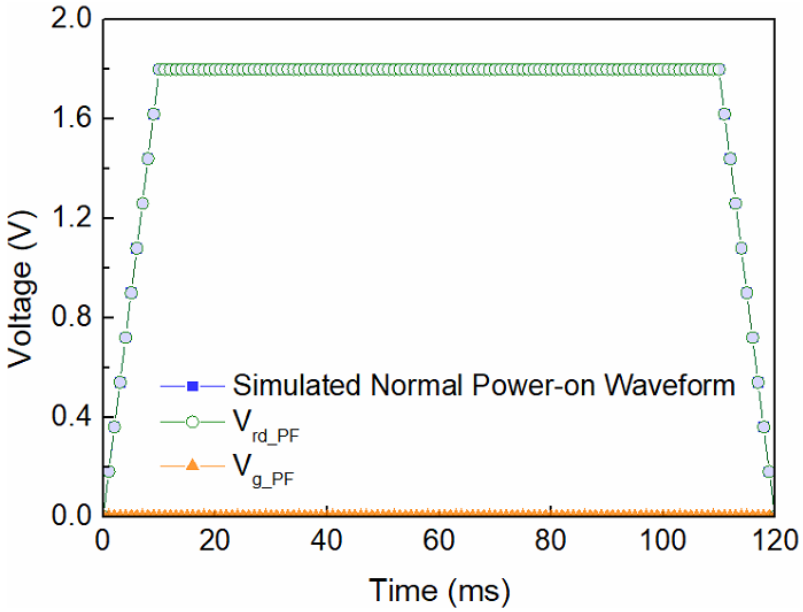


Fig. 3.14. Each node voltage level of the positive-feedback mechanism power-rail ESD clamp circuit under normal power-on event.

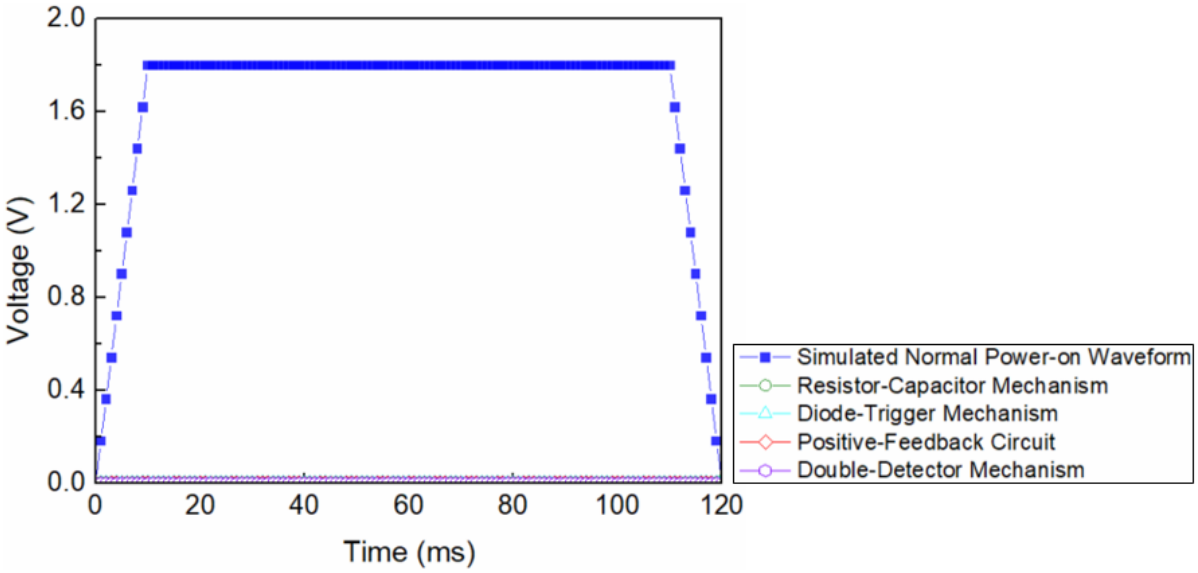


Fig. 3.15. The voltage level of these power-rail ESD clamp circuit on the gate of M_{ESD} under normal power-on event.

3.2.3 Fast Power-on Condition

The fast power-on provides a voltage waveform with a nanosecond rising time and a normal operating voltage level. This fast power-on condition is the combination of normal operating voltage at 1.8V and 10 nanosecond rising time. As shown in Fig. 3.16, the voltage level of each node is shown in the case of a fast power-on operating situation. The voltage level of this fast power-on cannot trigger the diode string. Since the V_{rd_PF} node voltage level is high, its channel will be closed. Therefore, the M_{ESD} of the power-rail ESD clamp circuit with positive-feedback mechanism is turned off. As shown in Fig. 3.17, the voltage level of M_{ESD} includes the resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism with four diodes during fast power-on operating voltage. The simulation results show that the resistor-capacitor mechanism is triggered quickly under a fast power-on event. The positive-feedback mechanism has a peak voltage higher than the diode-trigger mechanism and double-detector mechanism. This peak voltage will increase the risk of false triggering and cause significant power loss. Therefore, the power-rail ESD clamp circuit of the diode-trigger mechanism and double-detector mechanism can be better and effectively immune to the situation of the fast power-on.

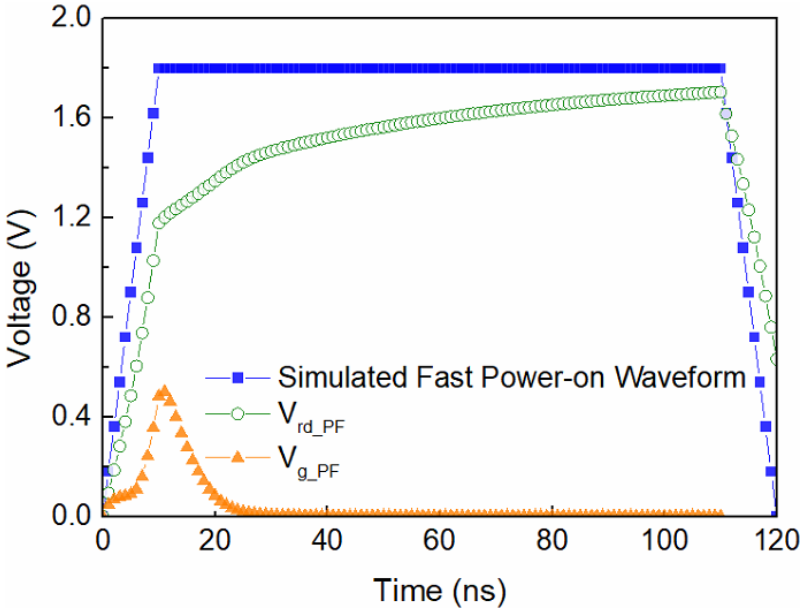


Fig. 3.16. Each node voltage level of the positive-feedback mechanism power-rail ESD clamp circuit under fast power-on event.

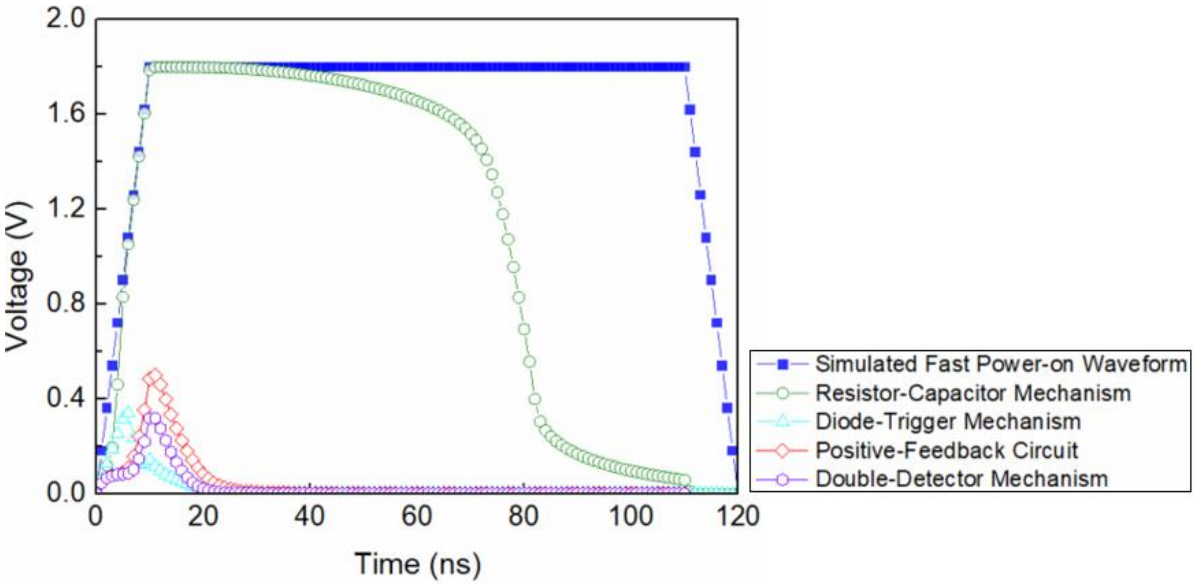


Fig. 3.17. The voltage level of these power-rail ESD clamp circuit on the gate of M_{ESD} under fast power-on event.

3.3 Measurement Methods and Results

All test circuits of the power-rail ESD clamp are fabricated through 180nm CMOS process, and the chip micrograph of all power-rail ESD clamp circuits is shown in Fig. 3.18. There are four types of detection mechanisms in this chip, including resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism. These power-rail ESD clamp test circuits are primary to measure TLP I-V curve measurement, VF-TLP I-V curve measurement, ESD robustness measurement, and power loss under normal power-on and fast power-on. The measurement method and results are introduced in the following section.

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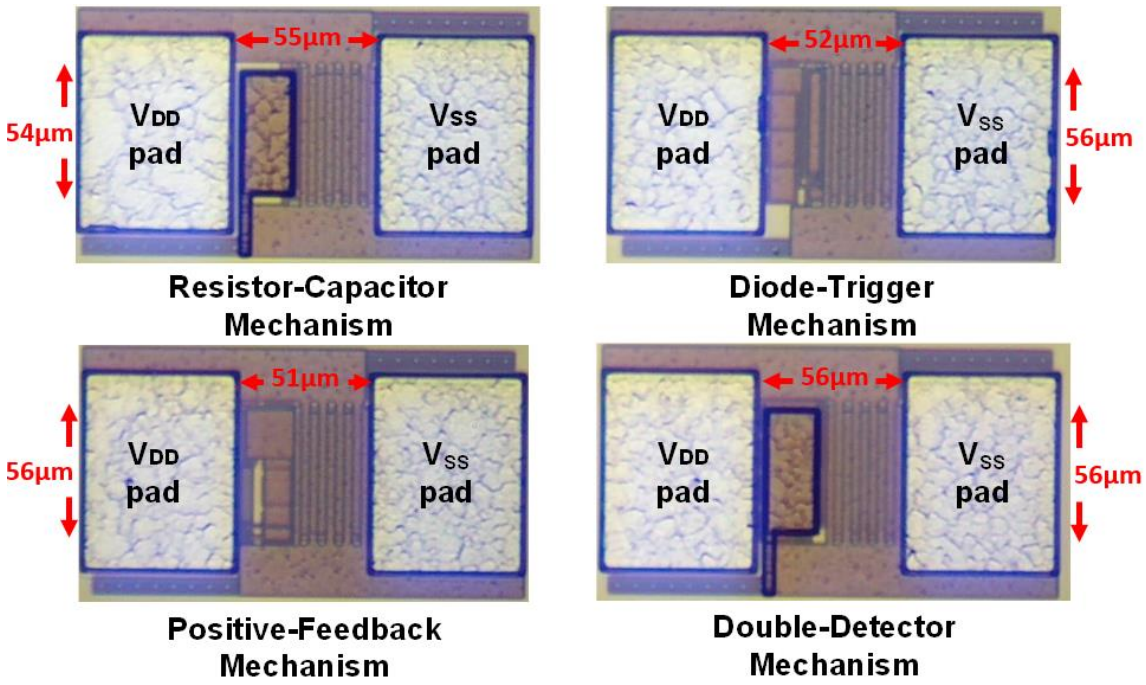

Fig. 3.18. The chip micrograph of all power-rail ESD clamp circuits.

3.3.1 Transmission-line pulsing (TLP) Measurement

The TLP measured system can provide high energy pulse such as electrostatic discharge (ESD). The power-rail ESD clamp circuit mainly discharges the ESD current from the power terminal (V_{DD}) to ground (V_{SS}). The starting voltage ($V_{starting}$) is the current value of TLP measured results more than 20mA. The failure criterion (I_{t2}) of the power-rail ESD clamp circuits is defined as the leakage current shifting 30% from its initial curve after each TLP level testing. As shown in Fig. 3.19, the TLP I-V curves of these power-rail ESD clamp circuits are compared, including resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism. The starting voltage ($V_{starting}$) of resistor-capacitor, diode-trigger, positive-feedback, and double-detector are 0.9V, 4.1V, 3.1V, and 3.3V under the 20mA, respectively. The I_{t2} of the resistor-capacitor, diode-trigger, positive-feedback, and double-detector are 2.2A, 2.2A, 1.2A, and 1.6A, respectively.

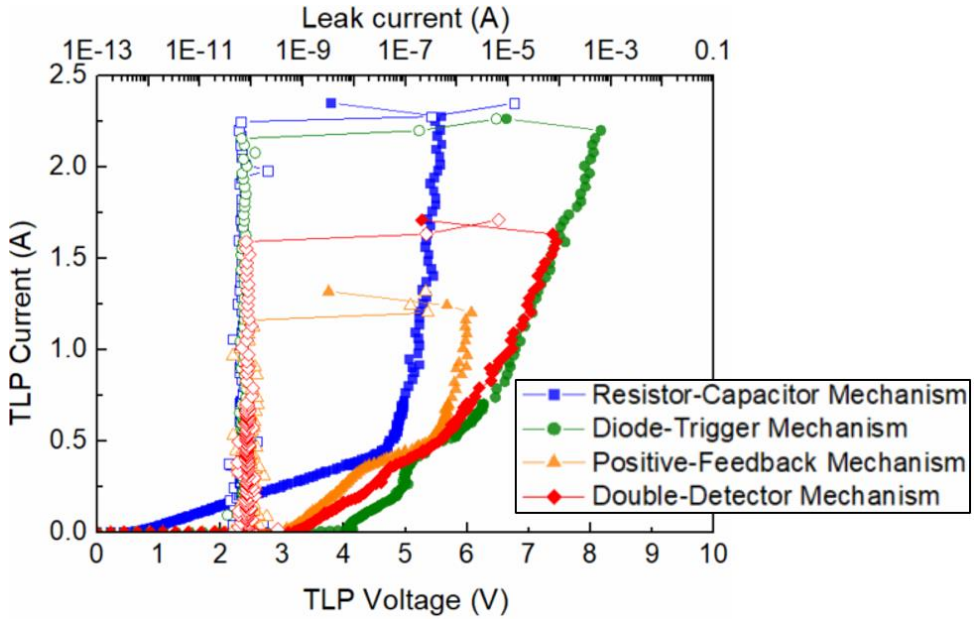

Fig. 3.19. The TLP I-V curves of these power-rail ESD clamp circuits.

3.3.2 Very-Fast Transmission-line pulsing (VF-TLP) Measurement

These power-rail ESD clamp circuits are measured by the very-fast TLP (VF-TLP) measured system. The apparatus of VF-TLP is used to investigate the effectiveness of these power-rail ESD clamp circuits in the time domain of a Charged-device model (CDM) ESD event. In order to evaluate the turn-on behavior of these power-rail ESD clamp circuits, the VF-TLP is set with a rise time of 200ps and a pulse width of 5ns under CDM-like fast-transient conditions. As shown in Fig. 3.20, the VF-TLP I-V curves of these power-rail ESD clamp circuits are compared, including resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism. The starting voltage ($V_{starting}$) of resistor-capacitor, diode-trigger, positive-feedback, and double-detector are 0.9V, 2.5V, 1.7V, and 1.8V under the 20mA, respectively. The I_{t2} of the resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism are 5.1A, 4.6A, 3.6A, and 3.9A, respectively.

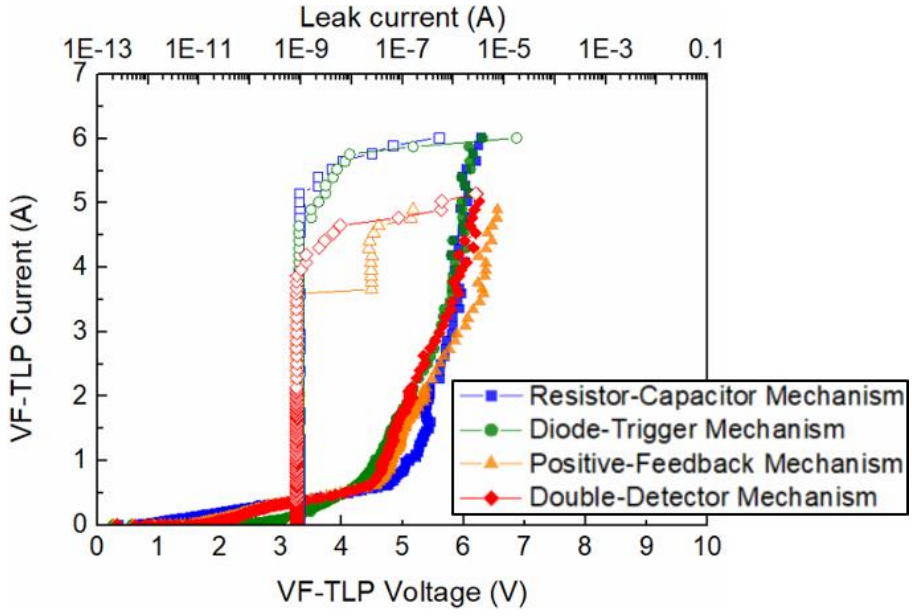

Fig. 3.20. The VF-TLP I-V curves of these power-rail ESD clamp circuits.

3.3.3 ESD Robustness

The research adopts the human-body model (HBM), commonly used to test the sensitive ESD to obtain the ESD robustness of these four mechanisms, including the resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism. The standard of the broken power-rail ESD protection circuits is defined as leakage current shifting more than 30%. In this research, the HBM robustness of resistor-capacitor mechanism, diode-trigger, positive-feedback mechanism, and double-detector mechanism are 3.3kV, 3.3kV, 1.6kV, and 2.3kV, respectively. These measured results are consolidated in Table 3.5 as follows.

In order to further gain a deeper understanding and compare the human-metal model (HMM) ESD robustness test of these power-rail ESD clamp circuits, these circuits are measured by the ESD gun instrument. As shown in Fig. 3.21, the study uses the ESD simulator ESS-B3011 to perform the ESD robustness of HMM. The HMM test is a more substantial ESD stress and much higher energy than the HBM test. In addition, the HMM test is shown on the component level to speculate about ESD performance at the system level. It is set from 0.2kV to fail and one stepper 0.1kV during the measurement process. Furthermore, the interval is applied to the circuit within 0.05 seconds in each step. The failure condition defined as leakage current shifting more than 30% is the same as the HBM test. The HMM robustness of resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism are 1.7kV, 1.7kV, 0.8kV, and 1.0kV, respectively. In this research, the measured results are also consolidated in Table 3.5 as follows.

Fig. 3.21. The ESD simulator ESS-B3011 measurement system.

Table 3.5. The test results of ESD robustness.

Cell Name	Resistor-Capacitor Mechanism	Diode-Trigger Mechanism	Positive-Feedback Mechanism	Double-Detector Mechanism
HBM (kV)	3.3	3.3	1.6	2.3
HMM (kV)	1.7	1.7	0.8	1.0

3.3.4 Power Loss under Fast Power-on Event

In order to understand the turn-on behavior of these different triggering mechanisms under the fast power-on condition, this research uses the function generator to create a waveform with a low voltage and nanoscale rising time. As a result, the pulse width is selected 175ns, the rising time is selected 25ns, and the voltage is set as 1.8V. During the fast power-on voltage, the measured result of these power-rail ESD clamp circuits is shown in Fig. 3.22. According to the results, the voltage waveform of the resistor-capacitor mechanism has dropped to approximately 1.1V and caused to be accidentally triggered for mere 125 nanoseconds. On the other hand, the diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism do not have false triggers under the fast power-on testing.

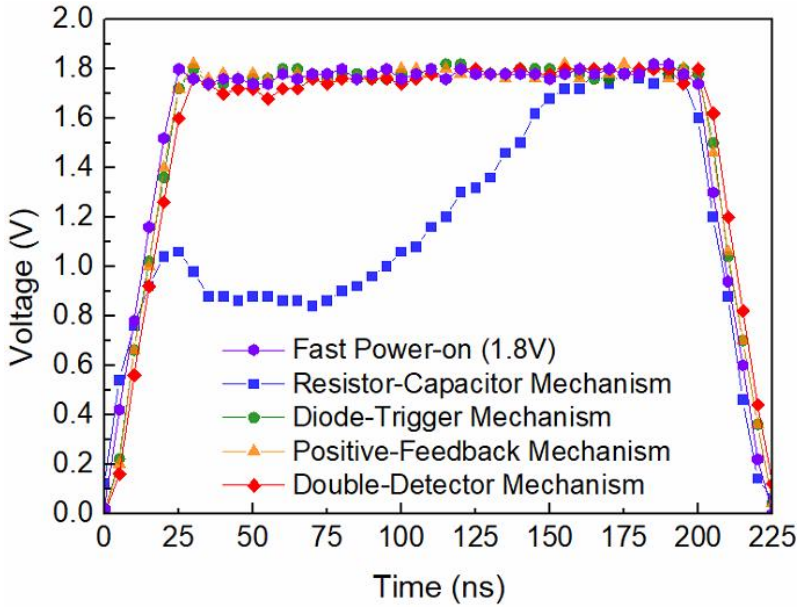

Fig. 3.22. The measured voltage of power-rail ESD clamp circuits under fast power-on event.

3.4 Comparison of This Test Chip

As shown in Table 3.6, the power-rail ESD clamp circuits with different mechanisms that include the resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism are compared. All test circuits are verified and implemented using CMOS technology. The “safe” is defined that the M_{ESD} NMOS of power-rail ESD clamp circuits are not triggered, and the “risk” is defined that the M_{ESD} NMOS of power-rail ESD clamp circuits is accidentally turned on. These power-rail ESD clamp circuit that are represented “safe” are not severe power loss during the normal power-on situation. In comparison, the power-rail ESD clamp circuit of the resistor-capacitor mechanism that is represented “risk” causes a power attenuation problem during the fast power-on event. The other mechanisms such as diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism can be safely used without any unexpected triggering issue.

Through the measurement results of TLP, VF-TLP, HBM, and HMM, it can be found that the tolerance of the resistor-capacitor and diode-trigger mechanism is better than that of the positive-feedback and double-detector mechanism. This exact reason will be analyzed in detail in Section 3.5. Furthermore, when operating normal power-on at 1.8V, the power-rail ESD clamp circuit of the diode-trigger mechanism has a large leakage current. Finally, these power-rail ESD clamp circuits are equipped with different trigger circuits and transistors of the same size to discharge the ESD current. As a result, the power-rail ESD clamp circuit of the double-detector mechanism occupies more silicon area to cause increased cost.

Table 3.6. The comparison of these power-rail ESD clamp circuits.

Power-rail ESD clamp circuit	Resistor-Capacitor Mechanism	Diode-Trigger Mechanism	Positive-Feedback Mechanism	Double-Detector Mechanism
CMOS Process	180nm	180nm	180nm	180nm
Normal power-on event	safe	safe	safe	safe
Fast power-on event	risk	safe	safe	safe
TLP I_{t2} (A)	2.2	2.2	1.2	1.6
VF-TLP I_{t2} (A)	5.1	4.6	3.6	3.9
HBM (kV)	3.3	3.3	1.6	2.3
HMM (kV)	1.7	1.7	0.8	1.0
Leakage current (nA) @1.8V	1.5	5.3	1.7	1.7
Area (μm^2)	2970	2912	2856	3136

3.5 Discussion of This Test Chip

The power-rail ESD clamp circuits are important protection circuits for power terminal. In the study, these power-rail ESD clamp circuits with different triggering mechanisms include resistor capacitor, diode trigger, positive feedback, and double detector. The M_{ESD} transistor of 400μm is used to discharge the ESD current. Under the operated voltage level, the M_{ESD} transistor should not be turned on. Otherwise, the power will be lost to bring about the power consumption from the drain of M_{ESD} to the source of M_{ESD}. When the ESD event occurs, this M_{ESD} should be triggered by the different detection mechanisms. This ESD current will be discharged favorably from the drain of M_{ESD} to the source of M_{ESD}.

The chip pictures of the power-rail ESD clamp circuits after TLP testing are shown in Fig. 3.23. They show the results that the primary burned location is on the drain of M_{ESD} rather than the source of M_{ESD}. Moreover, the drain of M_{ESD} is connected to V_{DD} by three-layer metal, while the source of M_{ESD} is connected to V_{SS} by four-layer metal. Therefore, the designs of the power-rail ESD clamp circuits should be further improved. The following description will display the solution.

The power-rail ESD clamp circuits with different triggering mechanisms have no power loss during normal power-on. The measurement result confirms that the M_{ESD} of the resistor-capacitor mechanism will be turned on unexpectedly to cause the risk of power loss during fast power-on. The path of discharging the ESD current should be from the drain of the M_{ESD} to the source of the M_{ESD}. According to the Fig. 3.23, there is a problem that the drain of the M_{ESD} burns alone. The improvement method is that V_{DD} needs to be connected to the drain of the M_{ESD} with thick metal. Through these ESD robustness tests include TLP, VF-TLP, HBM, and HMM measurement, it can be found

that resistor-capacitor mechanism and diode-trigger mechanism are larger than positive-feedback mechanism and double-detector mechanism. Since M_{ESD}'s gate of these power-rail ESD clamp circuits get high level voltage to turn on the channel of the M_{ESD}. The ESD current is discharged through the shallow channel region of the M_{ESD}. As the result of the shallower junction depths and the LDD structure at the drain and source regions of M_{ESD}, the M_{ESD} is weak to sustain the high-power ESD current [32] - [35]. In other words, when the triggering mechanism gives an excessively high potential bias to the gate of the M_{ESD}, it will cause the robustness decrease.

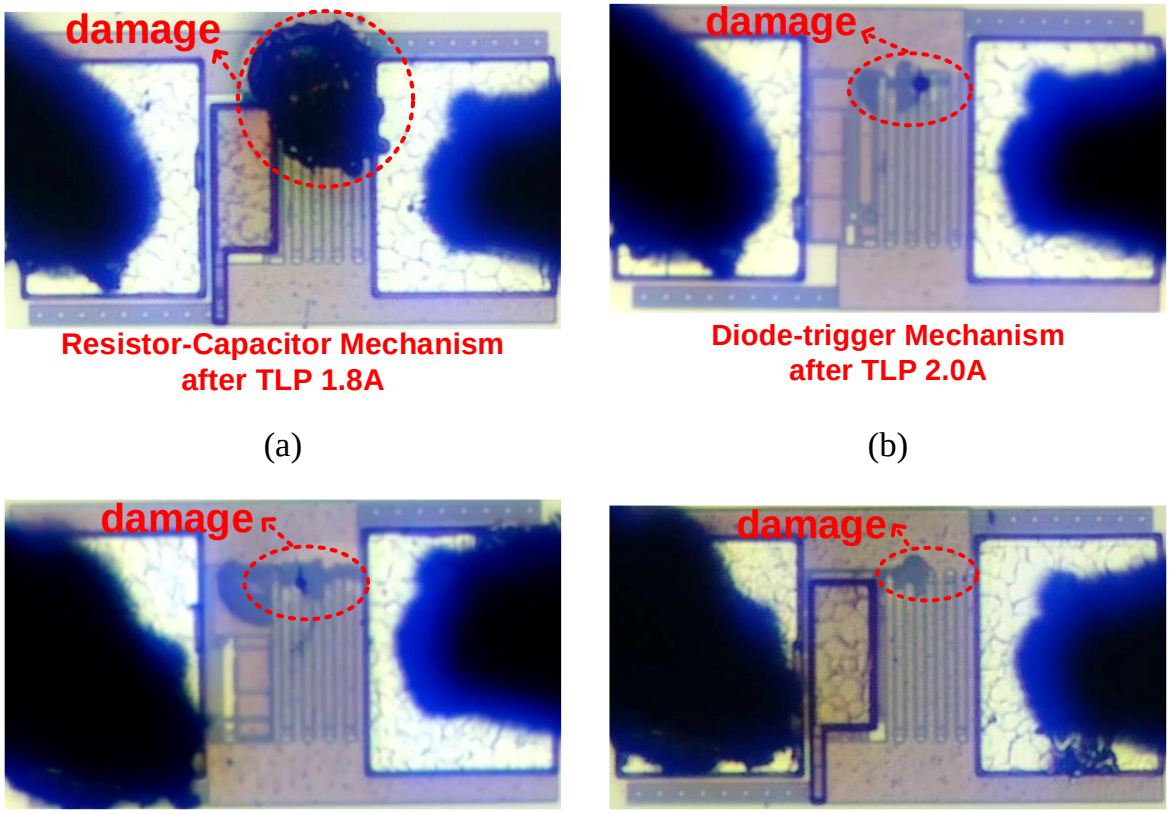

Fig. 3.23. The chip micrographs of these power-rail ESD clamp circuits (a) resistor-capacitor mechanism, (b) diode-trigger mechanism, (c) positive-feedback mechanism and (d) double-detector mechanism with M_{ESD} after the TLP test.

These power-rail ESD clamp circuits with different trigger mechanisms are used to the power supply node, and these different trigger mechanisms are used to trigger a large-size NMOS (M_{ESD}) to discharge the ESD current during the ESD event. Among them, the positive-feedback mechanism causes the gate of M_{ESD} to be overvoltage, which will reduce the ESD robustness. Therefore, the clamping-string method can prevent the gate of M_{ESD} from having an excessively high trigger voltage. As shown in Fig. 3.24, this diode element can be used to implement clamping string [36]. In addition to the overvoltage problem, there may be other reasons to cause different robustness. It is necessary that more in-depth and further discussion and research.

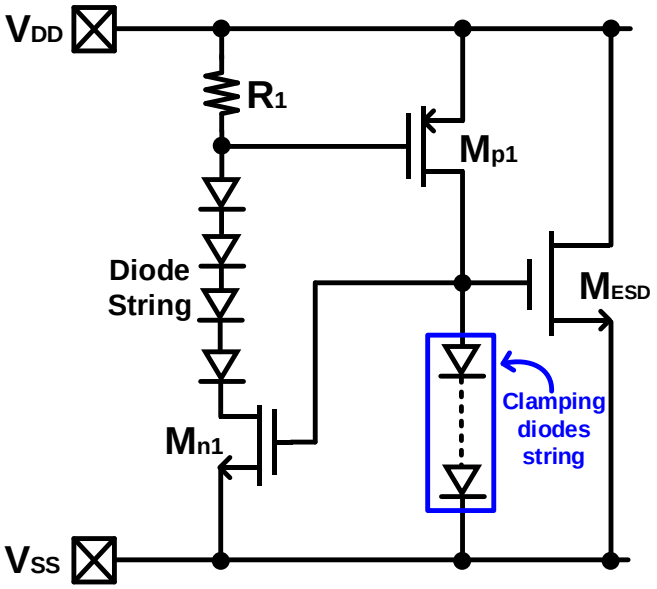

Fig. 3.24. The power-rail ESD clamp of positive-feedback mechanism with clamping diodes string.

3.6 Summary

These power-rail ESD clamp circuits are equipped four triggering mechanisms including resistor-capacitor mechanism, diode-trigger mechanism, positive-feedback mechanism and double-detector mechanism. They are successfully made with CMOS process. These power-rail ESD clamp circuits have important consideration on power supply terminal that are sufficiently high tolerance and the characteristics of no power loss during normal power-on and fast power-on. Except for the M_{ESD} of diode-trigger mechanism, positive-feedback mechanism, and double-detector mechanism, this resistor-capacitor mechanism briefly triggers the M_{ESD} to cause power loss during fast power-on. When these power-rail ESD clamp circuits operate at 1.8V, the diode-trigger mechanism has large leakage current than resistor-capacitor mechanism, positive-feedback mechanism and double-detector mechanism. The test results of different ESD robustness are shown that positive-feedback mechanism and double-detector mechanism are relatively small. This phenomenon needs to improve the bias voltage for gate of the M_{ESD}.

To sum up, when the problem is improved in the future, all performance including robustness, leakage current at 1.8V and layout area are compared. This positive-feedback mechanism is a more useful electrostatic discharge protection design to apply for the power supply terminal.

Chapter 4

Conclusion and Future Work

4.1 Conclusion

First of all, the background of this ESD and various related test standards are introduced. In order to protect the internal circuit effectively, the ESD protection circuits that are applied to the I/O terminal and the power supply node are indispensable. Although the diodes are widely used, the parasitic capacitance that needs improvement will affect high-frequency performance. These power-rail ESD clamp circuits are analyzed the performance to apply for different situation.

In chapter 2, these ESD protection designs are implemented in the CMOS process. From the high-frequency measured results, the $|S_{21}|$ of the proposed RC-diode ESD protection design is lower than the traditional dual diode at the same operating frequency and size. Furthermore, though the $|S_{21}|$ of traditional LC tank is lowest at the particular frequency, it occupies a large layout area. Finally, the FOM value of the proposed RC-diode ESD protection design is higher than previous designs, which means that the signal loss is low, the occupied layout area is small, and the ESD robustness is sufficient.

In Chapter 3, these power-rail ESD clamp circuits with different detection circuits are applied for the power terminal and fabricated in CMOS process. These power-rail ESD clamp circuits are measured under different power-on situations to test whether the M_{ESD} transistor of discharge ESD current is triggered and causes power loss accidentally. Although they did not have any power loss during normal power-on, it is found that the

resistor-capacitor mechanism has signal loss during fast power on. They are also measured a variety of ESD robustness tests, including TLP measurement, VF-TLP measurement, HBM measurement, and HMM measurement. The tolerance of positive-feedback mechanism and double-detector mechanism are lower than resistor-capacitor mechanism and diode-trigger mechanism. This issue has been proposed for discussion and it will be improved in future work. When the problem is solved, this positive-feedback mechanism occupies a smaller layout area and has a smaller leakage current at 1.8V, and there is no risk of false triggering under normal and fast power-on conditions. It is useful ESD protection circuit for power supply terminal.

To sum up, the research proposes RC-diode ESD protection circuits for applying to high-frequency. Furthermore, it verified low signal loss and high tolerance per unit area through measurement results. These power-rail ESD clamp circuits are also analyzed under the various ESD test methods and different power-on conditions successfully.

4.2 Future Work

In order to protect the internal circuit from being destroyed by static electricity, the ESD protection design is indispensable on the RF_{IN}/RF_{OUT} pad and the power terminal is shown in Fig. 4.1. In this research, the proposed RC diode can not only be used to discharge the static electricity at the RF_{IN}/RF_{OUT} pad, but also can be used to reduce the attenuation of high-frequency signals. These power-rail ESD clamp circuit with different trigger mechanisms are analyzed and applied to the power supply terminal.

In the future, this power-rail ESD clamp circuit with positive-feedback ESD transient mechanism circuit which can be used to provide resistance value to the proposed RC-diode design is shown in Fig. 4.2. As shown in Fig. 4.3, the high-frequency signal loss of the proposed RC diode is smaller than the high-frequency signal loss of the traditional dual diode. As shown in Fig. 4.4, this positive-feedback ESD transient mechanism circuit in the power-rail ESD clamp circuit not only helps the RC diode to reduce the attenuation of high-frequency signals, the gate potential of this M_{ESD} transistor is also low potential under normal power on. As shown in Fig. 4.5, when static electricity occurs, this power-rail ESD clamp circuit of positive-feedback ESD transient mechanism will have high potential to the M_{ESD} gate to discharge ESD current successfully. Other ESD transient mechanism circuits can use similar concepts to assist proposed RC-diode successfully.

Moreover, the resistance value in these ESD transient mechanism circuits is quite large, it can be adjusted according to the requirements of the RC-diode architecture. Even if this RC diode is required to use the kilo-ohms resistance value, it can also directly use the existing one. Therefore, the RC-diode ESD protection circuit can be adjusted according to the circuit requirements without additional layout area.

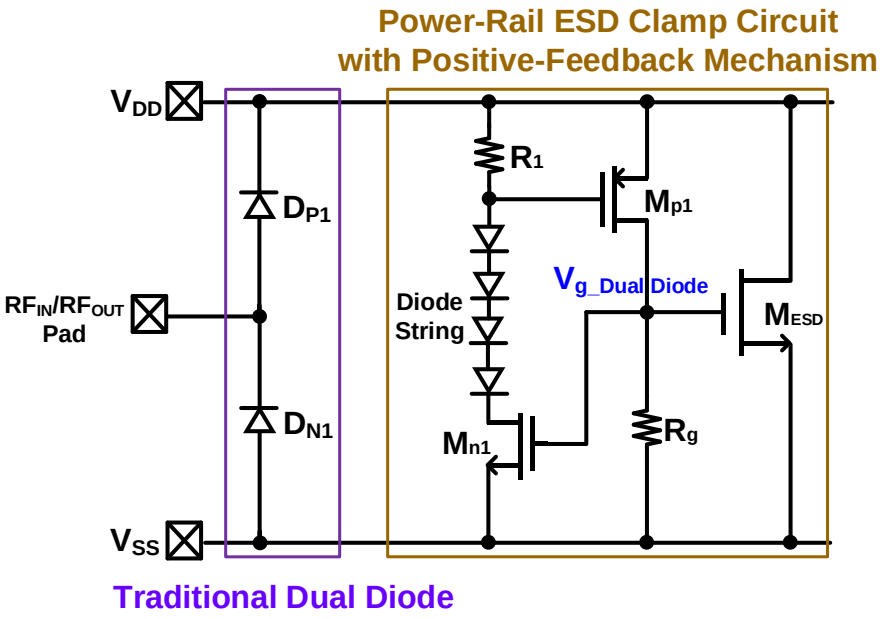

Fig. 4.1. The whole-chip ESD protection design with traditional dual diode and positive-feedback ESD transient mechanism.

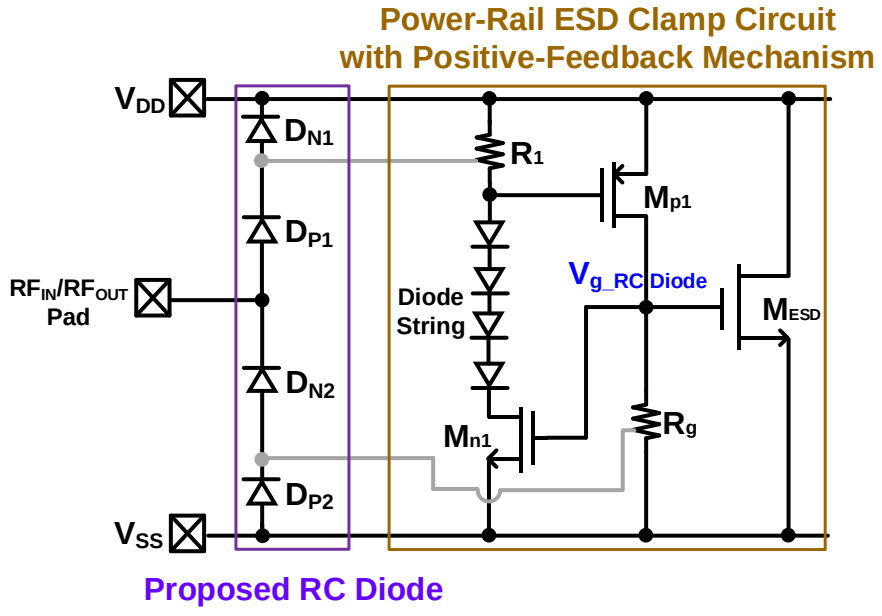

Fig. 4.2. The whole-chip ESD protection design with proposed RC diode and positive-feedback ESD transient mechanism.

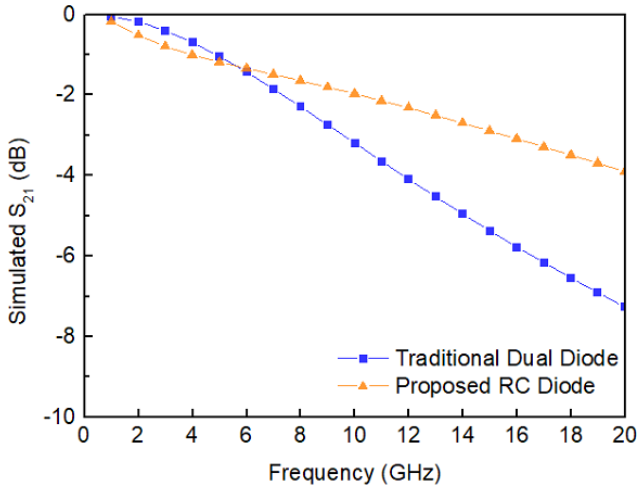

Fig. 4.3. Simulated S-parameter of traditional dual diode and proposed RC diode.

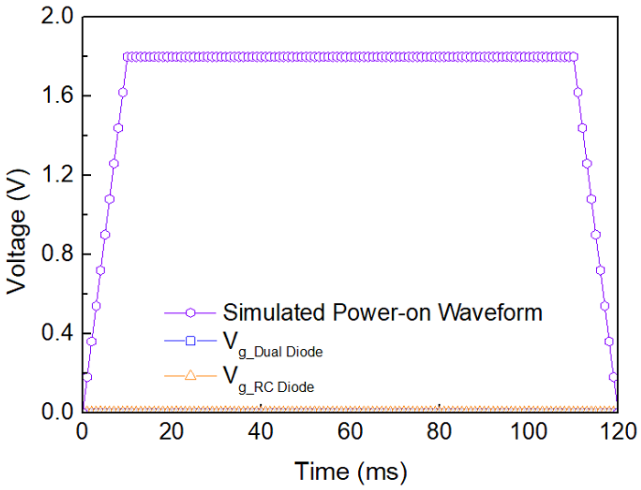

Fig. 4.4. The simulated voltage level of $V_{g\_Dual\ Diode}$ and $V_{g\_RC\ Diode}$ on the gate of M_{ESD} under power-on event.

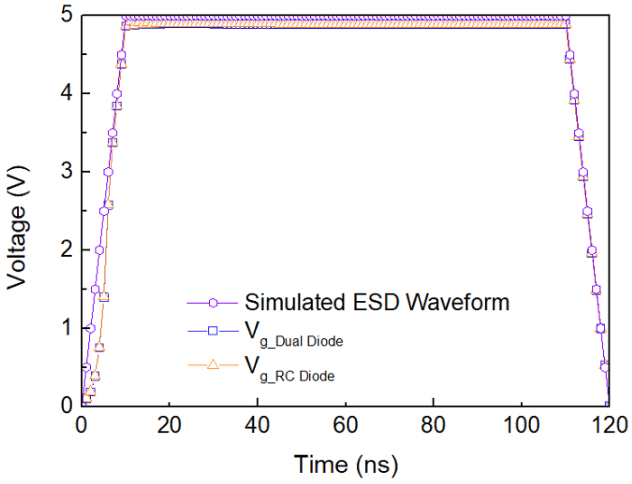

Fig. 4.5. The simulated voltage level of $V_{g\_Dual\ Diode}$ and $V_{g\_RC\ Diode}$ on the gate of M_{ESD} under ESD stress event.

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