國立臺灣師範大學電機工程學系

碩士論文

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收發轉換器之靜電放電防護設計

On-Chip ESD Protection Design for T/R Switch

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摘要

傳統雙二極體靜電放電防護架構已被廣泛運用在各個電路之中，但在現在晶片追求越來越小的情況，勢必得縮小其使用面積。本篇論文研究主旨是針對位在射頻電路最前端的收發轉換器電路設計全晶片靜電放電防護電路。在防護電路裡所選擇的元件大小是影響防護能力的重要關鍵，本論文防護電路所選用的電感及電源線間靜電放電箝制電路也會影響其保護能力。

為了驗證元件對於防護能力的差別，本論文在 0.18um CMOS 製程下，設計了 10 種不同佈局結構的測試電感及一組電源線間靜電放電箝制電路，並透過傳輸線脈衝及人體放電模型的測試來去驗證其耐受度的差別。另外在電源線間靜電放電箝制電路方面，也增加了在不同溫度下最大可承受靜電槍抨擊的次數測試，來驗證在不同溫度下電源線間靜電放電箝制電路的耐受度差別。

本論文利用二極體擺放位置的不同，設計了一種並聯二極體的靜電放電防護設計，將二極體與收發轉換器的內部電路結合。與先前參考論文所提出的傳統雙二極體靜電放電防護架構來去做比較之下，傳統雙二極體靜電放電防護架構面積為 0.25*0.225 mm^2，而本篇論文所提出的並聯二極體靜電放電防護架構面積為 0.25*0.17 mm^2，這可以有效降低使用面積 20%且有至少可以承受人體放電模型 3kV 的靜電防護能力。

關鍵字：收發轉換器、靜電放電、二極體、電感

On-Chip ESD Protection Design for T/R Switch

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Abstract

The traditional dual-diode electrostatic discharge (ESD) protection structure has been widely used in various circuits. In the situation that chips are pursuing smaller and smaller, it is necessary to reduce their used area. The purpose of this thesis is to design a full-chip ESD protection circuit for transceiver/receiver (T/R) switch at the front-end of the radio-frequency circuit. The components and their sizes selected in the protection circuit are important factors affecting the protection ability. The inductor and power-rail ESD clamp circuit selected for the protection circuit in this thesis will also affect the protection ability.

In order to verify the difference in the protection ability of the components, this thesis designed test inductors with 10 different layout structures and a power-rail ESD clamp circuit in 0.18um CMOS process, and through the transmission line pulse (TLP) and HBM tests to verify the difference in robustness. In addition, the power-rail ESD clamp circuit has also been tested for the maximum number of times it can withstand ESD gun punches at different temperatures to verify the difference in robustness at different temperatures.

In this thesis, an ESD protection circuit (parallel-diode design) is designed by using the different position of diode, and the diode is combined with the internal circuit of the T/R switch. As compared with the traditional dual-diode ESD protection architecture, the area of the traditional dual-diode ESD protection structure is 0.25*0.225 mm^2, and the area of the parallel-diode ESD protection structure proposed in this thesis is 0.25*0.17 mm^2. The proposed design can effectively reduce 20% used area and has an ESD protection ability that can withstand at least 3kV of the human body model (HBM) test.

Keywords: electrostatic discharge (ESD), transceiver/receiver (T/R) switch, diode, inductor