國立臺灣師範大學科技與工程學院電機工程學系

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應用於高速電路之π型靜電放電防護設計

π-Shape ESD Protection Design for High-Speed Circuit

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摘　　要

本論文主要研究應用在高速電路之靜電放電防護設計，所有測試電路皆在CMOS 製程中完成設計，透過分散式電路設計與低電容防護元件的組合，達到不影響高速性能並提供有效靜電放電防護的效果，並與傳統既有之二極體與矽控整流器做比較。

在本論文中，提出了一款新型的電源線觸發之矽控整流器 (PLTSCR)，π-PLTSCR 可以不用透過電源線間靜電放電箝制電路 (power-rail ESD clamp circuit) 便能夠達成四個模式 (PS, PD, NS, and ND) 的靜電排放。由於無需使用電源線間靜電放電箝制電路，電路的面積便可以節省 45%。本次提出的新型設計，除了可以應用在高速電路的防護，並且還可以省下更多的成本。

最後，為了驗證防護電路是否可以真正保護內部電路，本論文使用轉阻放大器 (Trans-impedance amplifier, TIA)，作為被保護的內部電路，分別搭配π-diode、π-SDSCR、π-RTSCR 以及π-PLTSCR 進行防護，並且進行高頻量測與靜電耐受度量測，確認防護電路的功能是否正常以及其對轉阻放大器的性能影響。透過實驗結果可知，創新設計可以提供給 TIA 電路 6kV 的靜電耐受度，且造成的增益下降大約為 1dB，並未對性能造成過大影響。

關鍵字：全晶片靜電放電防護、π型分散式電路、高速電路

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ABSTRACT

This paper mainly studies the design of electrostatic discharge protection applied in high-speed circuits. All test circuits are designed in CMOS process. Through the combination of distributed circuit design and low-capacitance protective elements, it achieves effective electrostatic discharge protection without affecting high-speed performance, and is compared with traditional diodes and silicon-controlled rectifiers.

In this paper, a new type of power line-triggered silicon-controlled rectifier (PLTSCR) is proposed. The π-PLTSCR can achieve electrostatic discharge in four modes (PS, PD, NS, and ND) . The circuit area can be saved by 45%. This new design can not only be applied to the protection of high-speed circuits but also can save more costs.

Finally, in order to verify whether the protective circuit can truly protect the internal circuit, this paper uses a trans-impedance amplifier (TIA) as the protected internal circuit and performs high-frequency measurement and electrostatic tolerance measurement to confirm whether the protective circuit is functioning normally and its impact on the performance. Through the experimental results, it is found that does not have a significant impact on the performance.

Keywords：whole-chip ESD protection, π-shape discrete circuits, high-speed circuit

Acknowledgment

求學階段來到了最後的時刻，首先最必須感謝的是我的家人，在天上的阿公阿嬤，還有供給我經濟需求的爸爸，若沒有你們的協助，我也無法順利完成學業。

感謝我的指導教授林群祐老師，老師在專業上的能力與學識都是我所不能企及的，老師不只知識的傳授上，對於處理任何事情都很嚴謹的態度也使我獲益良多。實驗室所提供的資源也是十分豐富，使用國家半導體研究中心的課程及量測儀器，也提供期刊投稿的機會，當討論研究內容時，老師給予的建議也是十分具有遠見，並且會放手讓學生去執行，即使實驗成果並不佳也能夠從中獲取經驗值，在這個領域中任何的經驗都是非常寶貴的。

感謝台灣半導體研究中心提供下線及量測的管道，也感謝國立陽明交通學電子工程學系的柯明道教授實驗室提供靜電量測相關的儀器，使實驗能夠順利進行。也謝謝蔡銘憲博士與彭盛裕教授能夠親自蒞臨指導我的碩士論文口試，透過兩位口試委員提供的意見，使得敝人的碩士論文能夠更加完善。

從大三加入奈米積體電路與系統實驗室的時候，便受到老師、學長、同屆與學弟妹的支持與陪伴,學習的路上有你們的陪伴實在是再好不過了。一起吃飯、熬夜、通宵趕下線等等，這些都是忘不了的。感謝義全與子鈞學長，從大三一路教導與協助，從我什麼都不會到自己可以處理事情，不會搞不清楚狀況，都多虧了學長們的叮嚀。謝謝庭炘、健群、裕程、柏諺學長，這些時間也是大家一起成長。謝謝洋守、宣賀，身為同屆的夥伴，我們所共同經歷的事情實在是太多了，畢竟也是紮實的認識六年，在同一個實驗室內除了研究上可以互相討論幫忙，若是遇到什麼緊急的事情也都能安全化解，若沒有你們兩個，研究的路上肯定是非常寂寞的，在實驗室聊聊好笑的事、令人生氣的事，打線有多搞，報告有多多，這些都是很棒的回憶。謝謝佳佑、欣慈、湘縈、青霖、柏孝學長、雖然在實驗室相處的時間短了點，但即便是這樣也是可以聊得開心，有你們在實驗室也增添了

許多色彩。謝謝從大學到現在一直都在的同學，人數眾多族繁不及備載，有你們在，在這短暫的學習生涯中，也能夠過得十分快樂。

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Chapter 1

Introduction

1.1 Motivation

The semiconductor industry is growing because the requirement for high-speed integrated circuits is increasing rapidly. When high-speed I/O circuits and radio-frequency (RF) circuits are widely fabricated in the CMOS process, the electrostatic-discharge (ESD) phenomenon is the major problem of quality and reliability [1]-[2]. In order to reduce the loss of IC products due to the irreversible failure caused by ESD events. In order to maintain the quality and ensure the reliability of IC products, the powerful way is learning the design method of ESD protection circuits.

To meet the demand for higher operating speeds in integrated circuits, the size of transistors must be minimized, resulting in thinner gate lengths and gate oxides that are more sensitive and susceptible to ESD stress. While ESD stress can significantly degrade electronic circuit performance, commercial IC products must still meet strict specifications. As a result, ESD protection design has become increasingly challenging in current IC fabrication.

As digital communication and high-speed transmission using radio-frequency circuits become more prevalent in CMOS process, traditional ESD protection design may not provide sufficient ability to reduce ESD current. The parasitic capacitance of ESD protection devices can affect signal integrity and lead to signal loss, which can compromise high-frequency performance at I/O pads. To mitigate this, reducing the parasitic capacitance of ESD protection devices is necessary for high-speed and high-frequency applications to prevent any negative impact on the core circuit's performance.

1.2 Concept of ESD

ESD occurs when two objects with different electric potentials form a discharging path, causing electric charge transfer between the objects. The resulting ESD current can reach several amperes and is generated in nanoseconds. The large ESD current can damage electronic components and cause malfunction, so all IC products require ESD protection circuits to ensure their capability to handle ESD events. As the process progresses rapidly, different types of ESD events have been identified, and the severity of the ESD problem is increasing.

1.3 ESD Test Standard

For IC products in mass production, the most important consideration is reliability. Each electronic product must pass several standards [5]-[6]. Several related organizations such as Electrostatic Discharge Association (ESDA), Joint Electron Device Engineering Council (JEDEC), US military standard (MIL-STD), and Automotive Electronic Council (AEC) have established some standards for ESD testing. Every electronic component should pass the ESD tests which is called component-level ESD test. The component level test consists of the human-body model (HBM), machine model (MM), and charged-device model (CDM). These models are different from their discharging mechanism. Because the MM robustness is positively correlated with HBM robustness, the MM test is reduced in recent years. The model and equivalent circuits of HBM will be introduced in the next part.

(1) Human-Body Model (HBM)

The human-body model means the human body will accumulate some electric charges by rubbing the floor when walking. If the people who accumulated charges touch the electronic products, the current loop between people and electronic products will be formed. A large amount of ESD current will flow into these products and cause the abnormal function of electronic products. The equivalent circuit model of HBM (MIL-STD-883C method 3015.7) is shown in Fig.1.1. The HBM model consists of a 1.5kΩ resistor and a 100pF capacitor. The capacitor represents the human body's capacitor and the 1.5kΩ resistor represents the IC's impedance. The ESD current will discharge through the resistor to the ground. The HBM target level in a manufacturing environment is shown in table1.1 [7]. All commercial IC products should pass at least 2kV HBM level.

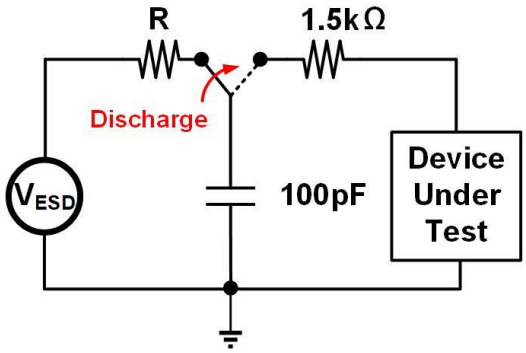


Fig. 1.1. The equivalent circuit of HBM.

Table 1.1. The target level of HBM

HBM Level	Impact on manufacturing environment
100V to <500V	Detailed ESD control method
500V	Basic ESD control methods for safe manufacturing
1kV	
2kV	

(2) Charged-Device Model (CDM)

During IC manufacturing, static charges can accumulate inside the devices, which can discharge if they touch a ground plane, resulting in ESD current that can damage internal circuits. This is known as CDM. Unlike HBM and MM, CDM has a shorter discharge time, making ICs more vulnerable to damage. Commercial ICs are required to pass the 250V CDM test, with target levels outlined in Table 1.2. The equivalent circuit of CDM is shown in Fig. 1.2 [8]. The ESD event of CDM ESD often happens in large socket ICs. In high-speed applications, the major type of ESD event is HBM. This thesis will mainly focus on HBM ESD protection.

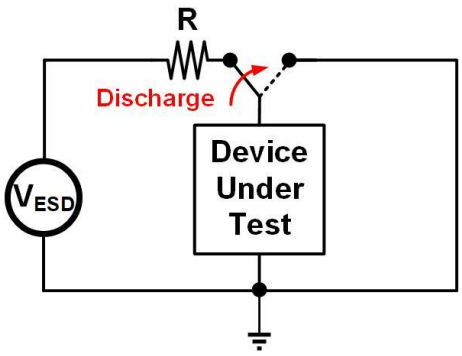


Fig. 1.2. The equivalent circuit of CDM.

Table 1.2. The target level of CDM

CDM Level	ESD Control Requirements
$V_{CDM} < 125V$	● Basic ESD control methods with grounding of metallic machine parts. ● Process specific measures to reduce the charging of the device. ● Charging/discharging measurements at each process step.
$125V < V_{CDM} < 250V$	● Basic ESD control methods with grounding of metallic machine parts. ● Process specific measures to reduce the charging of the device.
$V_{CDM} \geq 250V$	● Basic ESD control methods with grounding of metallic machine parts.

1.4 Design Criterion of ESD Protection Circuit

In the IC manufacturing environment, the ESD problem has become more significant due to process improvements. ESD can cause damage to IC products, making efficient ESD protection circuits essential. The I/O port is the most susceptible to damage from ESD currents that flow into the IC product through pins. The input pad is connected to the gate-oxide and controlled by DC bias [11]. Therefore, to prevent ESD current from flowing into the weak gate oxide, ESD protection circuits must be placed near the input pad. Additionally, power-rail ESD clamping circuits are required between the power pad (VDD) and the ground pad (VSS) [12]. Fig. 1.3 shows the block diagram of the whole-chip ESD protection schematic, which includes I/O ESD protection circuits

and power-rail ESD clamping circuits.

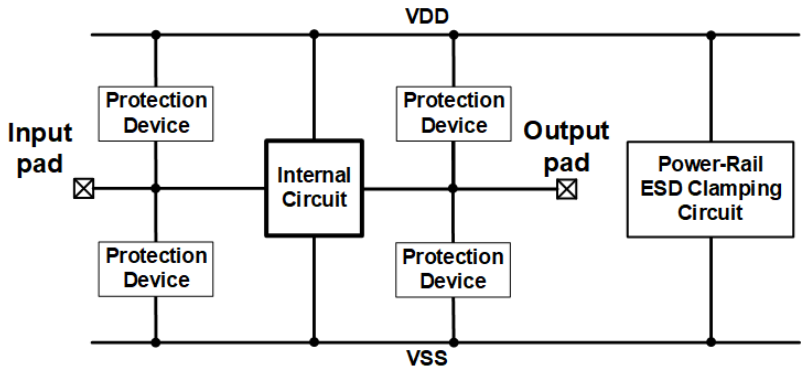


Fig. 1.3. The block diagram of whole-chip ESD protection schematic

To ensure the efficiency of ESD protection circuits, some design criteria should be considered. The criteria are called ESD protection window [13]-[14]. As shown in Fig. 1.4, the ESD protection window contains the measured voltage and current of the device under test. All the ESD protection devices should be designed in the range of supply voltage (V_{DD}) and gate-oxide breakdown voltage (V_{BD}). The upper bound of the supply voltage is $1.1*V_{DD}$, and the lower bound is $0.9*V_{BD}$. Some characteristics of ESD protection are introduced in the following part. To prevent extra power consumption, ESD protection circuits should be turned off in the normal operating condition of the core circuit. Furthermore, the ESD protection device shall not impact the performance of the internal circuit. When ESD current flows into the internal circuit, ESD protection circuits must turn on before the ESD stress damages the internal circuit. Thus, the trigger voltage (V_{t1}) should be lower than the breakdown voltage (V_{BD}). Some protection devices have a characteristic called snapback [15]. When device with snapback property turns on, the voltage drop between two terminals of protection device is large because of a large amount of current flowing into the protection device. The power consumption of ESD protection devices can be reduced because the voltage of devices after being turned on called holding voltage (V_h) is much lower. However, the lower V_h may cause latch-up issue if the V_h is lower than V_{DD}. The turn-on resistance (R_{on}) of ESD protection

device is defined by the slope of I-V curve. The turn-on resistance of protection device should be lower and discharge large ESD current with lower clamping voltage. Finally, when the ESD current is higher than the protection can tolerant called secondary-breakdown current (I_{t2}), the ESD protection device will be broken.

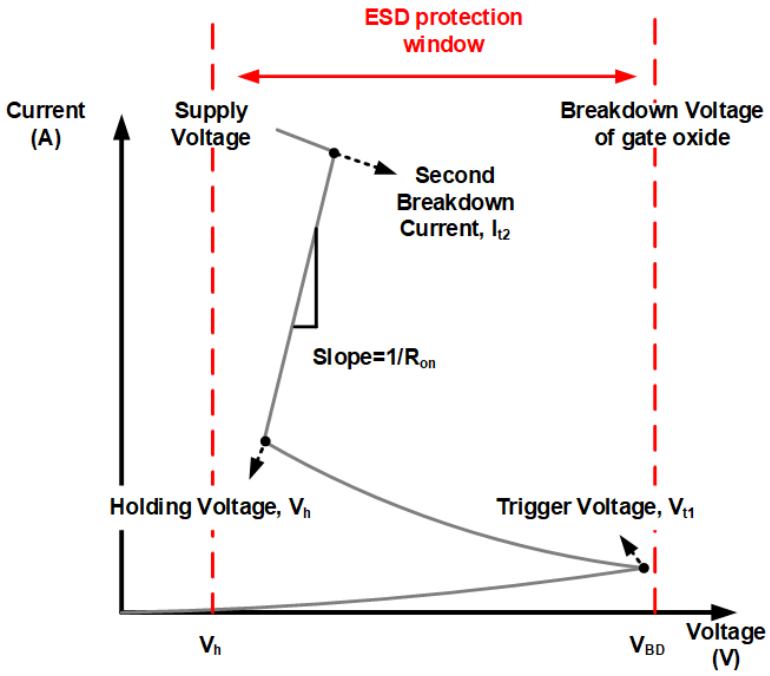


Fig. 1.4. ESD protection window

Because the ESD protection circuit is located in the I/O pad, V_{DD}, and V_{SS} pad, it can form four different discharging modes. As shown in Fig. 1.5, the ESD protection devices are connected from I/O to V_{DD} and I/O to V_{SS}. The power-rail ESD clamping circuit can provide a discharging path from V_{DD} to V_{SS}. For positive ESD stress flowing into grounded V_{SS} is called PS mode. For positive ESD stress flowing into grounded V_{DD} is called PD mode. For negative ESD stress flowing into grounded V_{SS} is called NS mode. For negative ESD stress flowing into grounded V_{DD} is called ND mode.

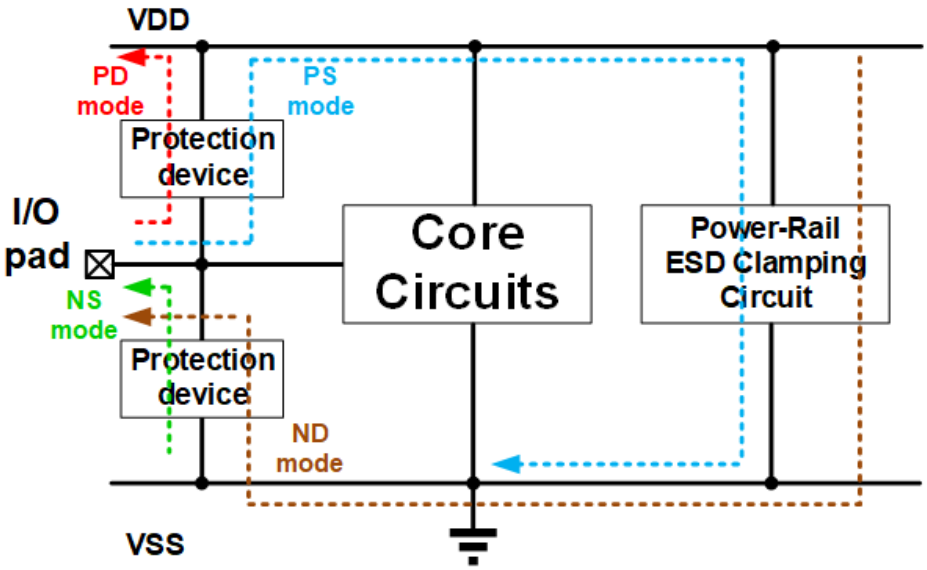


Fig. 1.5. Whole-chip ESD protection schematic

1.5 Organization of This Thesis

Chapter 1 of this thesis provides an introduction to the motivation behind this research, concepts of electrostatic discharge (ESD), standards for ESD testing, and the design criteria for ESD protection circuits. Chapter 2 offers a background on ESD protection circuits for high-speed applications and a review of prior high-speed ESD protection devices. In Chapter 3, traditional distributed ESD protection devices such as the π-diode, π-SDSCR, π-RTSCR, and proposed π-PLTSCR are discussed. Chapter 4 covers the trans-impedance amplifier (TIA) with π-model ESD protection circuits mentioned in the previous chapter, and Chapter 5 concludes the thesis and offers insights into future work.

Chapter 2

Studies of ESD Protection Circuits for High-Speed Applications

2.1 Effect of ESD Protection Circuits for High-Speed Circuits

In the past, the parasitic capacitance of ESD protection devices did not have a significant impact on the performance of internal circuits in traditional ESD protection designs. However, in recent years, as the operating speeds of ICs have increased, the parasitic capacitance of ESD protection devices can no longer be ignored. As shown in Fig. 2.1, the parasitic capacitance can result in signal loss from the input pad to the VSS pad during high-speed operation, leading to degraded performance of the internal circuit. Therefore, reducing and considering parasitic capacitance is crucial in modern ESD protection design.

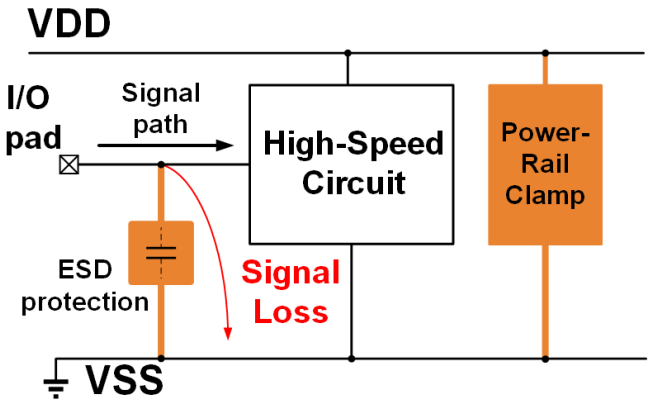
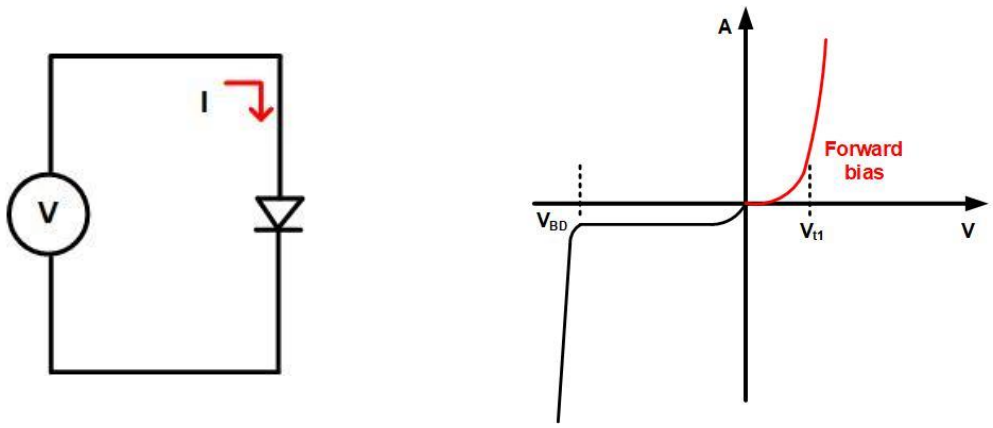


Fig. 2.1. The signal loss caused by ESD protection devices.

The robustness of an ESD protection device is typically proportional to its size. To provide sufficient robustness for internal circuits, the dimension of the protection device must be as large as possible. However, a larger protection device also leads to

more serious signal loss due to the higher parasitic capacitance, as described in references [16] - [17]. As a result, designing an ESD protection circuit that strikes a good balance between robustness and signal loss can be challenging due to the parasitic effects.

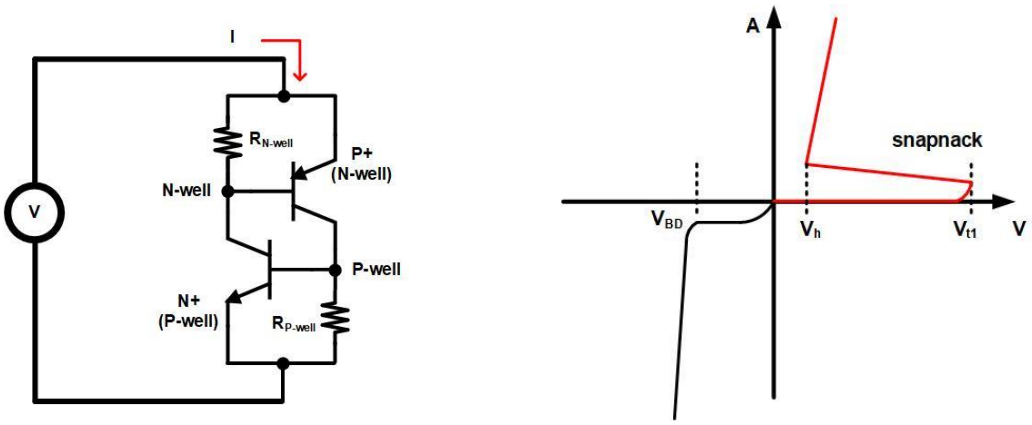
ESD protection design in CMOS technology commonly uses diodes and silicon-controlled rectifiers (SCRs) as protective components [18]. As illustrated in Fig. 2.2, diodes can be turned on with a lower forward bias and discharge a large amount of current, making them well-suited for ESD protection. Diodes can also be turned on in reverse bias, but the turn-on voltage is much higher, which can cause slower turn-on speed and higher temperature during discharging.



(a) (b)

Fig. 2.2. The (a) circuit diagram and (b) I-V curve of diode.

As shown in Fig. 2.3, the silicon-controlled rectifier (SCR) is a four-layer device consisting of p-n-p-n layers, which also features embedded PNP and NPN components, as described in references [19]-[20]. When a leakage current flows into the resistance of the base and emitter terminals, the SCR is activated by the voltage between the BJT's base and emitter. Due to its structure, the SCR has a positive feedback mechanism that enables it to turn on with a large current and exhibit a strong snapback phenomenon.



(a) (b)

Fig. 2.3. The (a) circuit diagram and (b) I-V curve of SCR.

2.2 Prior Art of High-Frequency and High-Speed applications

2.2.1 Single-stage ESD Protection Circuit

2.2.1.1. Dual diodes [21]

Dual diodes are a commonly used ESD protection circuit element, as depicted in Fig. 2.4. The reverse-biased diode (D_P) is placed from the I/O pad to VDD to protect against positive ESD current during PD mode. Similarly, the diode (D_N) is positioned from the VSS pad to the I/O pad to safeguard against negative ESD current during NS mode. To complete whole-chip ESD protection, the power-rail ESD clamping circuit must be located from VDD to VSS. The diode (D_P) and power-rail ESD clamping circuit work together to establish a discharge path for PS mode (positive input to VSS), while the diode and power-rail ESD clamping circuit create a discharge path for ND mode (negative input to VDD).

The size of the diodes in dual diodes must be reduced to reduce parasitic effects. However, reducing diode size can also decrease the ESD robustness of the dual diodes.

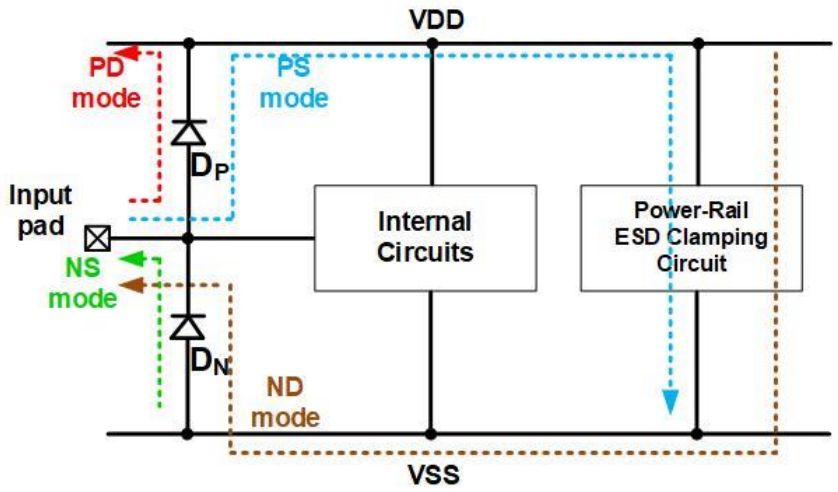


Fig. 2.4. The schematic of dual diode ESD protection [21].

2.2.1.2. Dual Stacked Diodes with Embedded SCR (SDSCR) [22]

To minimize parasitic effects and enhance ESD robustness in high-speed applications, an improved protection element known as the Stacked Diodes with embedded SCR (SDSCR) has been proposed. The use of SCR as an ESD protection component is common in high-speed applications due to its less parasitic capacitance and higher ESD robustness per area.

The whole-chip ESD protection schematic of SDSCR is presented in Fig. 2.5. The discharging path of the SDSCR is similar to that of dual diodes, with an SDSCR (SD_P) placed from input to VDD and another one (SD_N) positioned from VSS to input. The PS and ND modes operate in the same manner as dual diodes. A power-rail clamping circuit must be included to establish a complete discharging path. The stacking of diodes in the SDSCR results in lower parasitic capacitance and increases the turn-on speed of the SCR, allowing for the discharge of more ESD current. This design offers improved performance in terms of parasitic capacitance and ESD robustness in high-speed applications.

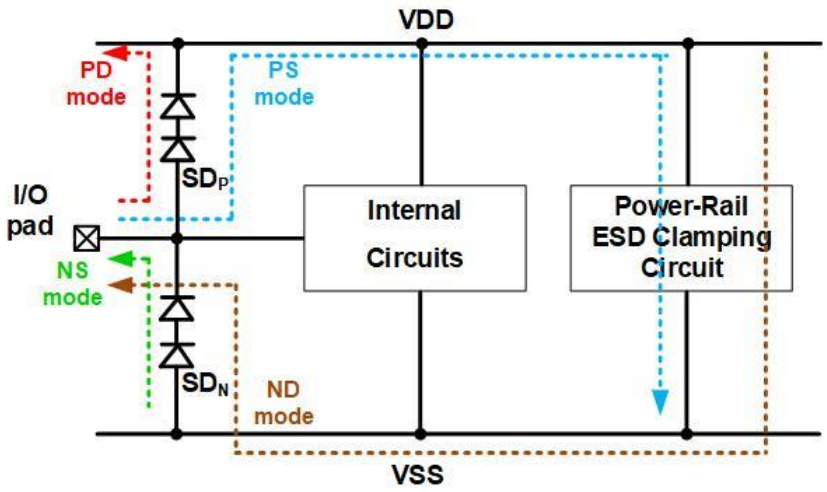


Fig. 2.5. The schematic of dual SDSCR ESD protection [22].

2.2.1.3. Dual Resistor-triggered SCR (RTSCR) [23]

Compared to the SDSCR, the RTSCR can be triggered by a small resistor of about 100Ω, as depicted in Fig. 2.6. This resistor is inserted between two stacked diodes, and the discharging path of the RTSCR is similar to that of dual diodes. To establish a complete discharging path, an RTSCR ($RTSCR_P$) is positioned from the input to VDD, while another one ($RTSCR_N$) is placed from VSS to the input. The PS and ND modes operate in the same way as dual diodes, and a power-rail clamping circuit must be incorporated to form a complete discharging path. In the design of the RTSCR, the small resistor helps to prevent large ESD currents from flowing into the stacked diode path, instead of the SCR path, resulting in higher ESD robustness. Additionally, the small resistor reduces parasitic capacitance in the small signal model observed at the input.

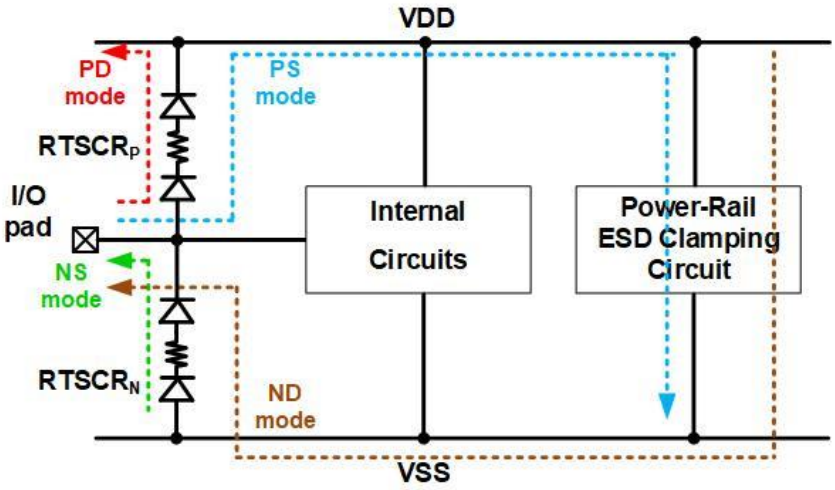


Fig. 2.6. The schematic of dual RTSCR ESD protection [23].

2.2.1.4. Inductor-Assisted SCR (LASCR) [24]

The proposed ESD protection device, known as the LASCR, offers a solution by combining an inductor with a diode string and an SCR. As depicted in Fig. 2.7, the LASCR is designed to have the SCR serve as the primary discharge path for ESD currents. The presence of a diode string in between the PNP base and NPN emitter provides a lower trigger voltage, resulting in a faster turn-on speed by allowing the trigger current to flow into the SCR. To minimize parasitic effects and minimize signal loss at the input, the inductor is utilized to match the ESD protection device, as it resonates with the parasitic capacitance. By optimizing the impedance matching, the LASCR provides improved ESD protection while preserving signal integrity.

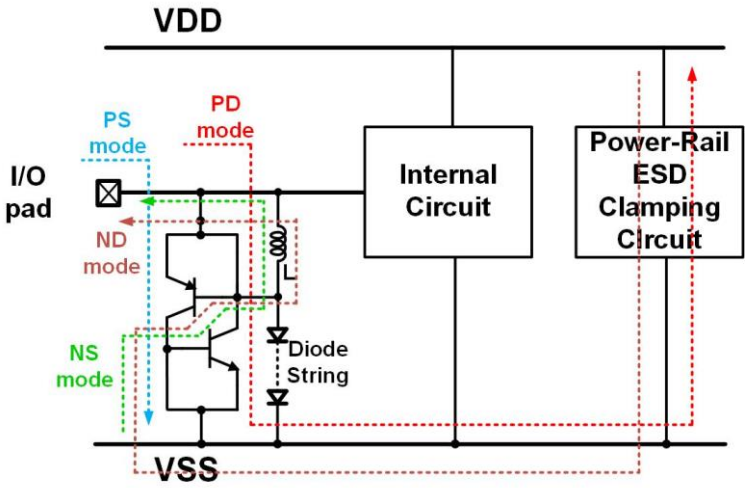


Fig. 2.7. The schematic of dual LASCR ESD protection [24].

2.2.2 Two-stage distributed ESD protection circuit

To minimize the capacitance of the ESD protection elements, it is necessary to limit the size of the ESD protection device. However, this reduction in size results in a decline in ESD robustness. Thus, there is a collision between reducing parasitic capacitance and maintaining ESD robustness.

To overcome the collision between parasitic capacitance and ESD robustness, a useful solution is to divide the ESD protection devices into multiple sections [25]. This approach can provide adequate ESD robustness while preserving high-frequency performance. For optimal high-frequency performance, all the ESD protection devices should be matched with elements such as inductors. Proper matching of the input stage can minimize signal loss.

The distributed ESD protection architecture is depicted in Fig. 2.8. A two-stage distributed ESD input protection solution with a matching inductor has been proposed [25]. This solution includes two stages of ESD protection elements, which can be diodes, SDSCR, or RTSCR. As shown in Fig. 2.9, a whole-chip ESD protection solution with a distributed ESD protection of diodes is presented [25]. This solution comprises of four diodes and a matching inductor (L). The inductor is utilized to match the parasitic

capacitance of the diodes, thereby reducing the signal loss at the input pad.

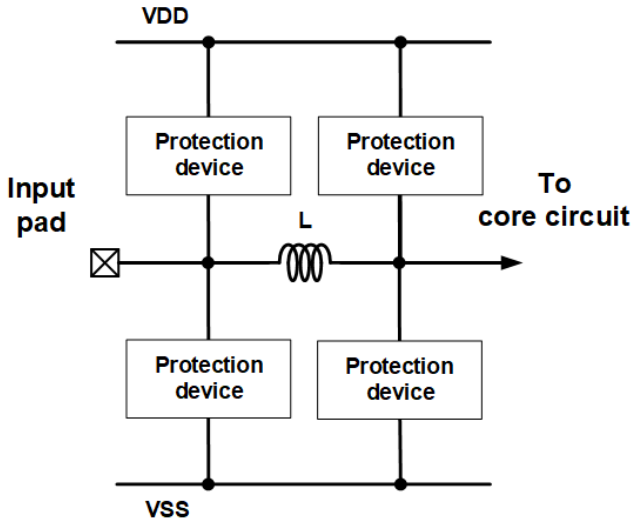


Fig. 2.8. The schematic of two-section distributed input ESD protection.

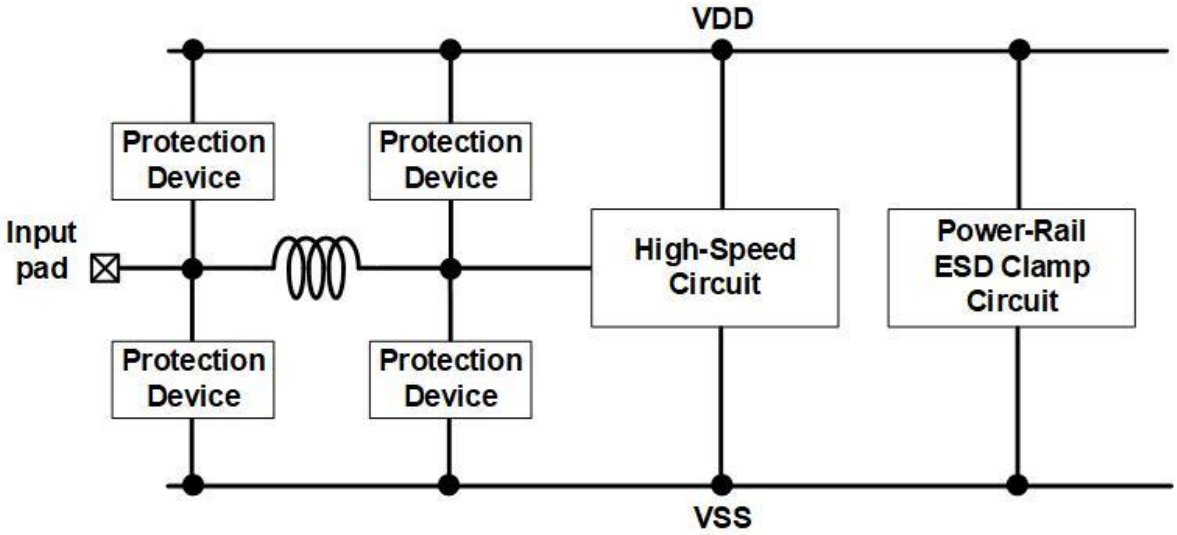


Fig. 2.9. The schematic of whole-chip ESD protection with π-diode input protection circuit [25].

Chapter 3

Proposed π-shape Power-Line Triggered Silicon-controlled rectifier (π-PLTSCR)

3.1 Design Concepts of π-shape ESD Protection Circuit

The rapid increase in the required operating speed of ICs has resulted in the widespread use of high-speed CMOS ICs in communication systems [2]. Despite their widespread use, MOSFET in CMOS technology are sensitive to electrostatic discharge (ESD) events [26]. To meet component-level ESD testing requirements, all integrated circuits must be designed with an on-chip ESD protection circuit. In high-speed applications, the ESD protection device must minimize the impact of parasitic capacitance while providing sufficient ESD protection. Traditional ESD protection devices such as diodes are not suitable for high-speed applications as they have a large parasitic capacitance that significantly impacts the input signal. At high frequencies, the parasitic capacitance of diodes has a low impedance characteristic, leading to significant input signal loss. To ensure robust ESD protection, the size of the ESD device must be increased, but this results in large parasitic capacitance that causes serious signal loss during normal operation. To mitigate this, a distributed circuit method can be employed [25].

The ESD protection devices in a distributed structure are split into two sections. These sections are connected by an inductor at both terminals. One end of the inductor is connected to the input pad while the other end is connected to the internal circuit, resulting in the formation of a π-shaped ESD protection circuit. The matching inductor is capable of resonating with the parasitic capacitance of the ESD protection devices. The equivalent circuit of the π-shaped ESD protection circuit is depicted in Fig. 3.1.

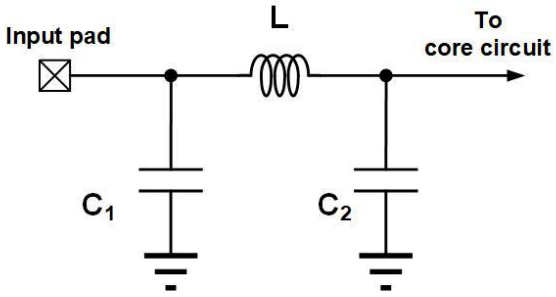


Fig. 3.1. The equivalent circuit of π-shape ESD protection circuit.

The π-shaped circuit has a matching inductor "L" and two parasitic capacitances, "C_1" and "C_2", belonging to the ESD protection device. The magnitude of the capacitance is determined by the dimension of the ESD protection device. Minimizing the impact of parasitic capacitance requires reducing the size of the ESD protection device. However, this solution creates a trade-off as smaller ESD protection devices result in a degradation of ESD robustness. The design flow of π-shape ESD protection circuit is shown in Fig. 3.2. First, determine the dimensions of the protective component. Then, estimate its parasitic capacitance value and match its impedance with an ideal inductor to achieve the desired performance. Once the inductance value is determined, use electromagnetic simulation software to simulate the real-world behavior of the inductor in the circuit, considering its parasitic effects. Replace the ideal inductor with the simulated inductor, taking into account its performance, and proceed with circuit layout and fabrication. Finally, execute measurements to confirm its performance.

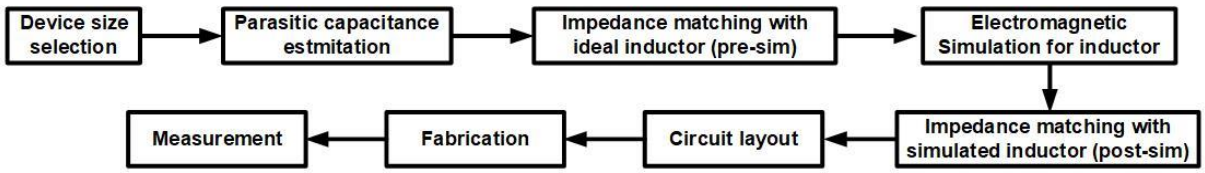
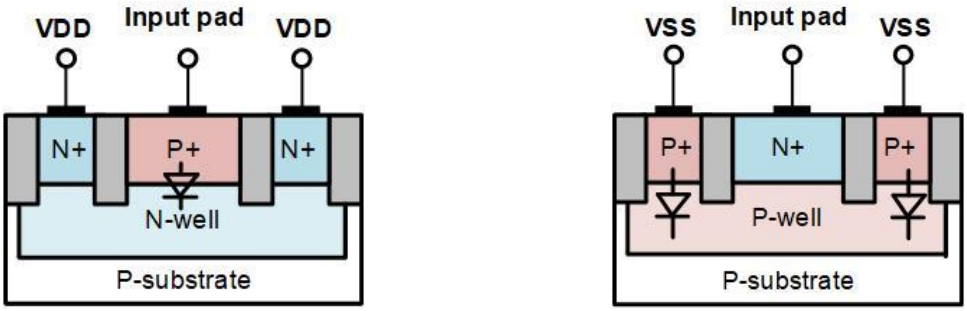


Fig. 3.2. The design flow chart of π-shape ESD protection circuit.

3.2 Traditional π-shape Diode (π-Diode)

In the CMOS process, the diode is a widely used solution for ESD protection. Two types of diodes are typically utilized: The P-type and the N-type diode. The anode of the

P-type diode is connected to the P+ region and the cathode is connected to the N-well, as shown in Fig. 3.3(a). On the other hand, the anode of the N-type diode is connected to the P-well and the cathode is connected to the N+ region, as illustrated in Fig. 3.3(b). In high-speed applications, the ESD diode must meet the parasitic capacitance requirement and provide sufficient ESD robustness [27]. When forward-biased, the diode will be turned on and discharge the ESD current at a low holding voltage. To optimized parasitic capacitance, the diode's layout is designed to be symmetrical. The layout top view of the P-diode and N-diode can be seen in Fig. 3.4.



(a) (b)

Fig. 3.3. Cross-sectional view of (a) P-diode (b) N-diode.

(a) (b)

Fig. 3.4. layout top view of (a) P-diode (b) N-diode.

The ESD protection circuit shown in Fig. 3.5 is a whole-chip ESD protection circuit with a π-diode structure that consists of two distributed circuit sections with diodes. The

first section, or stage 1, includes diodes placed from VSS to input pad (D_{N1}) and from input pad to VDD (D_{P1}), while the second section, or stage 2, includes diodes placed from VSS to input pad (D_{N2}) and from input pad to VDD (D_{P2}). A power-rail ESD clamp circuit is also included to discharge ESD currents between VDD and VSS.

The matching inductor between two section is made by metal 6 with 6μm width in 0.18μm CMOS process. It can resonate with capacitance of diode and reduce the signal loss at input pad.

In the π-diode structure of the whole-chip ESD protection circuit, the ESD current under PD mode is discharged by D_{P1} and D_{P2}, while the ESD current under NS mode is discharged by D_{N1} and D_{N2}. The power-rail ESD clamp circuit is responsible for discharging ESD currents between VDD and VSS. The ESD current under ND mode is discharged by the power clamp circuit in series with D_{N1} and D_{N2}, and the ESD current under PS mode is discharged by D_{P1} and D_{P2} in series with the power-rail ESD clamp circuit.

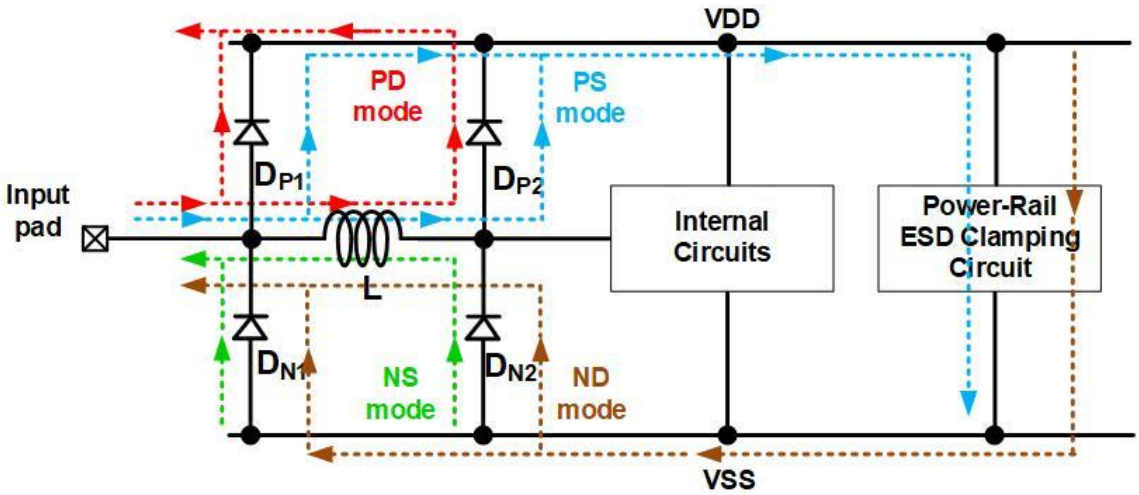
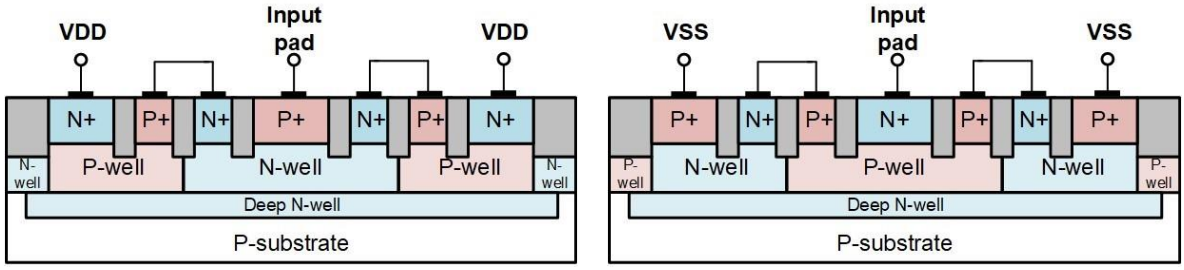


Fig. 3.5. The discharging path of whole-chip ESD protection with π-diode.

3.3 Traditional π- shape SDSCR (π-SDSCR)

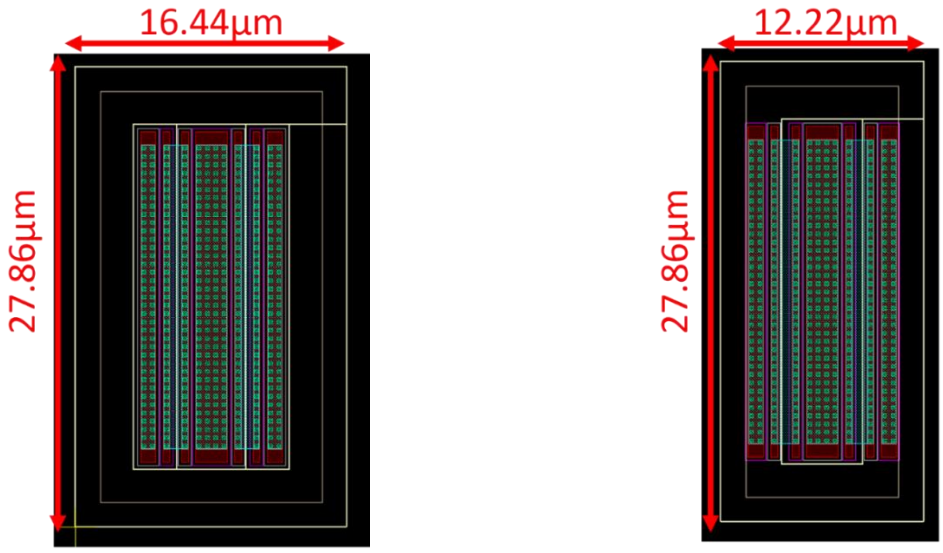
Figures 3.6(a) and 3.6(b) display the cross-sectional view of stacked diodes with an embedded SCR (SDSCR) in p-type and n-type, respectively. These SDSCRs consist of

two stacked diodes, and to minimize parasitic capacitance, it's essential to position the terminal connected to the input pad at the device structure's center. In the p-type SDSCR illustrated in Fig. 3.6(a), P+ is linked to the input pad, while N+ is connected to VDD. Conversely, in the n-type SDSCR in Fig. 3.6(b), the N+ is connected to the input pad, and the P+ is linked to VSS. In the event of an ESD occurrence, the ESD current flows into the input pad, and the diodes turn on to discharge current first. The remaining ESD current is then discharged by the embedded SCR. The top view of the P-SDSCR and N-SDSCR layout is visible in Fig. 3.7.



(a) (b)

Fig. 3.6. Cross-sectional view of (a) P-SDSCR (b) N-SDSCR.



(a) (b)

Fig. 3.7. layout top view of (a) P-SDSCR (b) N-SDSCR.

The matching inductor between two section is made by metal 6 with 6µm width in

0.18μm CMOS process. It can resonate with capacitance of SDSCR and reduce the signal loss at input pad.

As shown in Fig. 3.8, in the π-SDSCR structure of the whole-chip ESD protection circuit, the ESD current under PD mode is discharged by $SDSCR_{P1}$ and $SDSCR_{P2}$, while the ESD current under NS mode is discharged by $SDSCR_{N1}$ and $SDSCR_{N2}$. The power-rail ESD clamp circuit is responsible for discharging ESD currents between VDD and VSS. The ESD current under ND mode is discharged by the power clamp circuit in series with $SDSCR_{N1}$ and $SDSCR_{N2}$, and the ESD current under PS mode is discharged by $SDSCR_{P1}$ and $SDSCR_{P2}$ in series with the power clamp circuit.

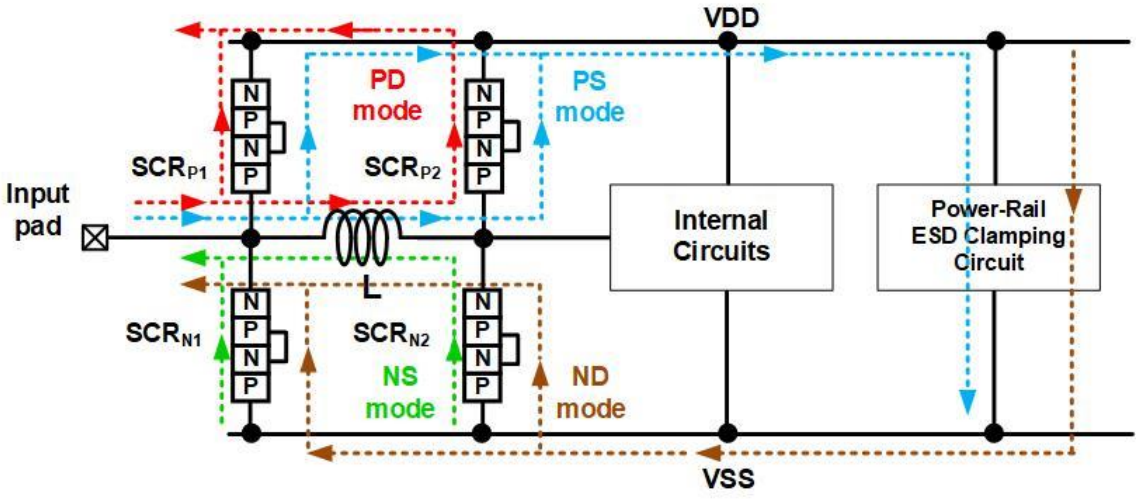
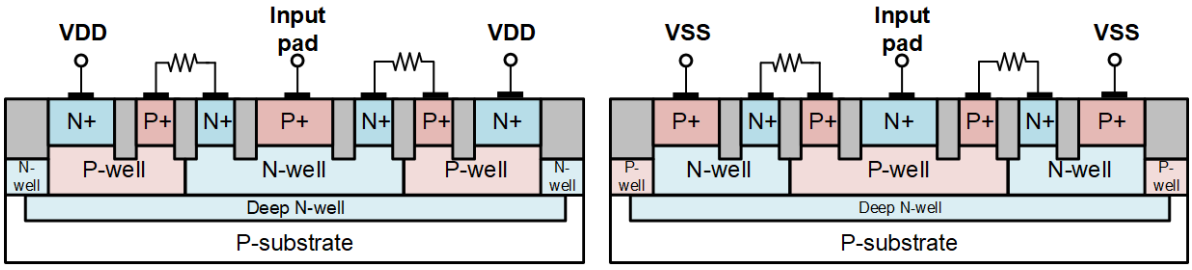


Fig. 3.8. The discharging path of whole-chip ESD protection with π-SDSCR.

3.4 Traditional π- shape RTSCR (π-RTSCR)

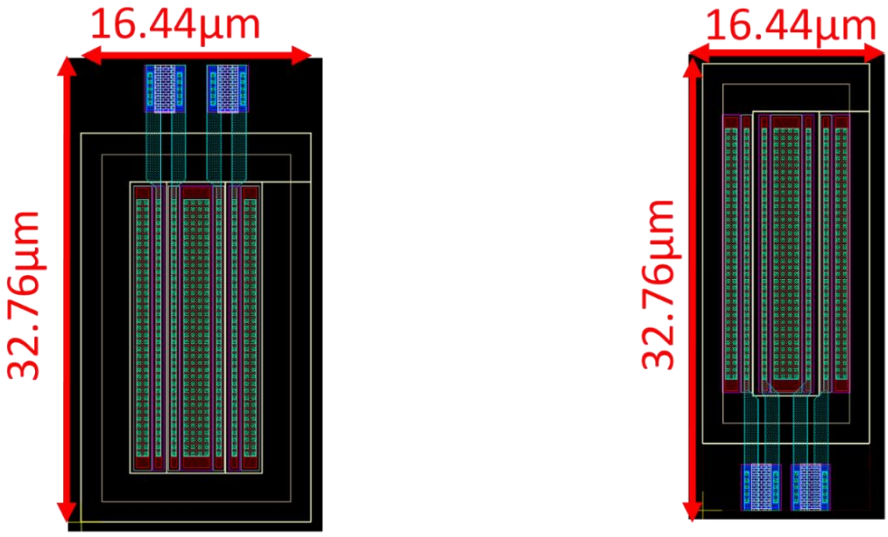
The cross-sectional view of p-type and n-type resistor-triggered SCR (RTSCR) is shown in Figures 3.9(a) and 3.9(b), respectively. These RTSCRs are connected with a small resistor between two P-N junctions of the SCR. To minimize parasitic capacitance, it is recommended to position the terminal connected to the input pad at the center of the device structure. In the p-type RTSCR depicted in Fig. 3.9(a), the P+ is linked to the input pad, and the N+ is connected to VDD. Conversely, in the n-type RTSCR illustrated

in Fig. 3.9(b), the N+ is connected to the input pad, and the P+ is linked to VSS. During an ESD event, the ESD current flows into the input pad. The small resistor helps prevent the current from damaging the stacked diodes and instead directs it into the embedded SCR. The embedded SCR then completes the discharge of the remaining ESD current. The top view of the P-RTSCR and N-RTSCR layout is visible in Fig. 3.10.



(a) (b)

Fig. 3.9. Cross-sectional view of (a) P-RTSCR (b) N-RTSCR.



(a) (b)

Fig. 3.10. layout top view of (a) P-RTSCR (b) N-RTSCR.

The matching inductor between two section is made by metal 6 with 6μm width in 0.18μm CMOS process. It can resonate with capacitance of RTSCR and reduce the signal loss at input pad.

As shown in Fig. 3.11, in the π-RTSCR structure of the whole-chip ESD

protection circuit, the ESD current under PD mode is discharged by $RTSCR_{P1}$ and $RTSCR_{P2}$, while the ESD current under NS mode is discharged by $RTSCR_{N1}$ and $RTSCR_{N2}$. The power-rail ESD clamp circuit is responsible for discharging ESD currents between VDD and VSS. The ESD current under ND mode is discharged by the power clamp circuit in series with $RTSCR_{N1}$ and $RTSCR_{N2}$, and the ESD current under PS mode is discharged by $RTSCR_{P1}$ and $RTSCR_{P2}$ in series with the power clamp circuit.

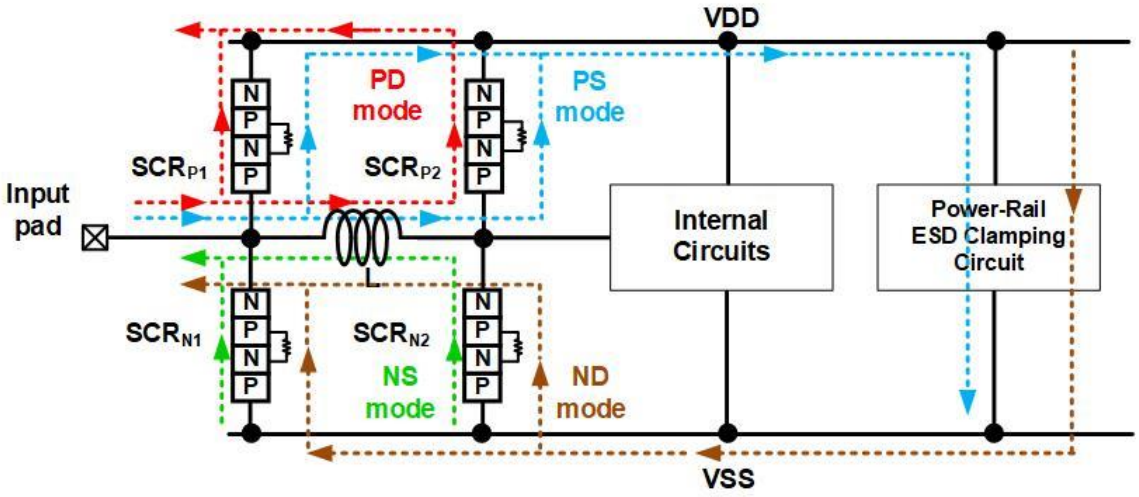


Fig. 3.11. The discharging path of whole-chip ESD protection with π-RTSCR.

3.5 Proposed π- shape PLTSCR (π-PLTSCR)

In this thesis, a novel power-line triggered SCR is proposed. As shown in Fig. 3.12, the PLTSCR is a normal SCR structure with a diode string used for triggering connected to either VDD or VSS. In the PLTSCR structure, it is able to discharge ESD current on its own and does not require assistance from a power clamp circuit. The p-type diode is chosen as the triggering diode string due to its small area cost. The diode string is able to conduct triggering current from either VDD or VSS when an ESD event occurs. In the π-PLTSCR structure, the ESD current under PD mode is discharged by the diode inside the SCR_n from VDD to input pad, while the ESD current under NS mode is discharged by the diode inside the SCR_p from VSS to input pad. The ESD current under PS mode is discharged by the SCR_n from input pad to VSS,

while the ESD current under ND mode is discharged by SCR_p from input pad to VDD.

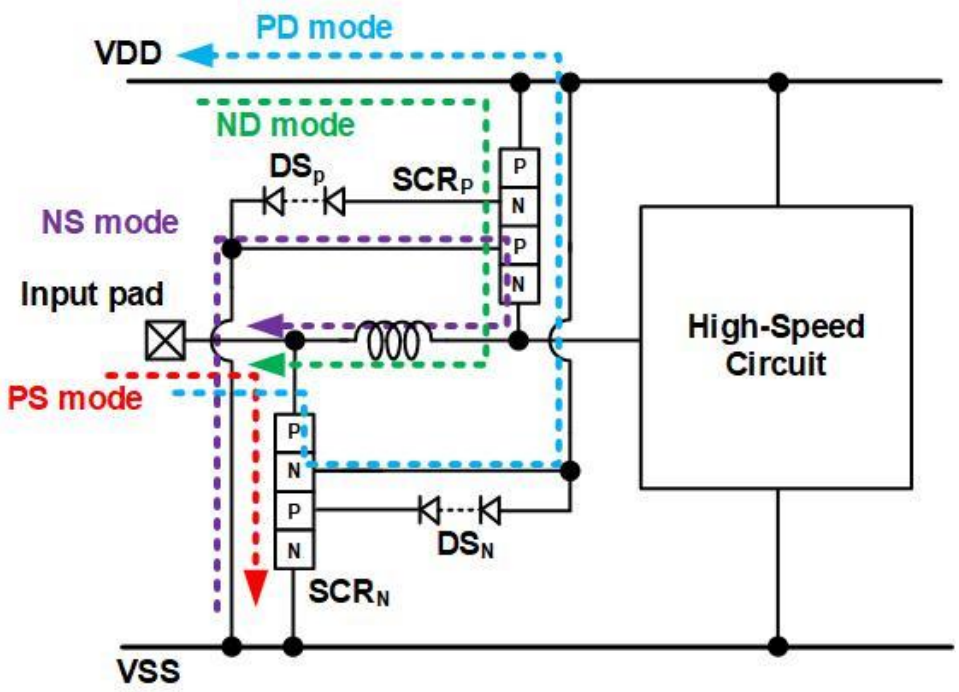
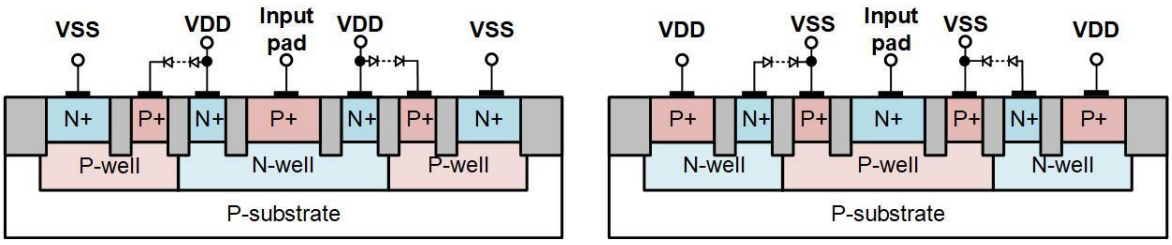


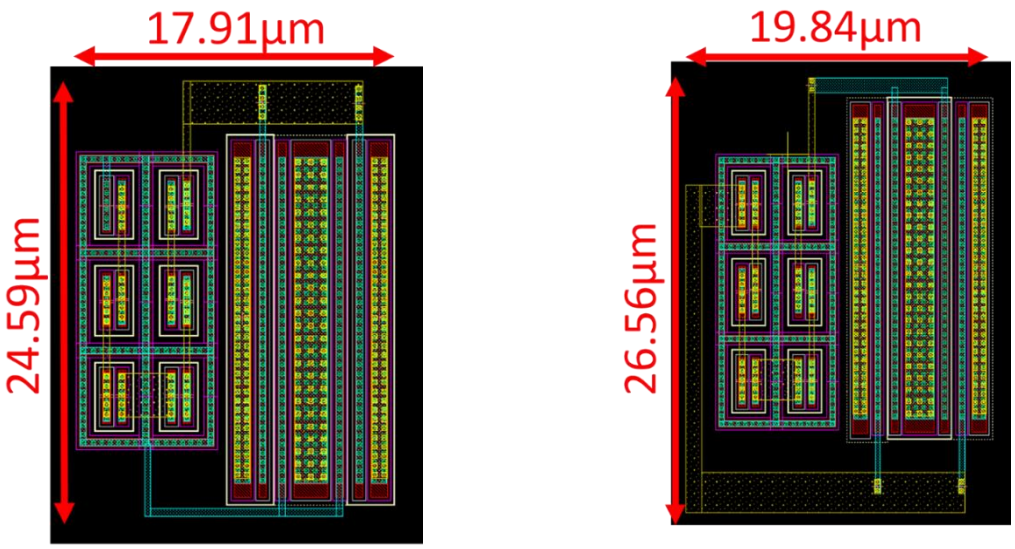
Fig. 3.12. The discharging path of π-PLTSCR.

Figures 3.13(a) and 3.13(b) display the cross-sectional view of p-type and n-type PLTSCR, respectively, which are connected with a diode string from VDD to SCR_n or SCR_p to VSS. To minimize parasitic capacitance, it's recommended to position the terminal connected to the input pad at the device structure's center. In the p-type PLTSCR presented in Fig. 3.13(a), the P+ is connected to VDD, and the N+ is linked to the input pad. Conversely, in the n-type PLTSCR shown in Fig. 3.13(b), the N+ is connected to the input pad, and the P+ is linked to VSS. During an ESD event, the ESD current flows into the input pad. The diode string conducts the current from VDD to SCR_n or SCR_p to VSS, reducing the triggered voltage of SCR. With the aid of the diode string, the PLTSCR can prevent ESD current damage. The top view of the P-PLTSCR and N-PLTSCR layout is visible in Fig. 3.14.



(a) (b)

Fig. 3.13. Cross-sectional view of (a) P-PLTSCR (b) N-PLTSCR.



(a) (b)

Fig. 3.14. layout top view of (a) P-PLTSCR (b) N-PLTSCR.

3.6 Simulation Results

The high-frequency performance of each π-shape proteciton device can be defined by S-parameters. The S_{21} represents the insertion loss and the S_{11} reprensents the return loss. With these parameter, the efficiency of each protection device can be quantified.

For high-frequency performance, the higher S_{21} means the less signal loss at another terminal of passive device and lower S_{11} means the signal that can be deliverd with less loss. The protection device should be designed to keep the S_{21} close to 0dB and S_{11} as small as possible.

The matching inductor should be simulated by electromaganetic (EM) software.

The matching inductor is drawn as octagon shape. The line width of inductor is 6μm line spacing is 2μm. The The 3D figure of matching inductor is shown in Fig. 3.15. All the ESD protection device is matched with a 0.38nH inductor. The conversion part consists of metal 3~5 to increase the equivalent thickness of metal. The layout top view of inductor is shown in Fig. 3.16.

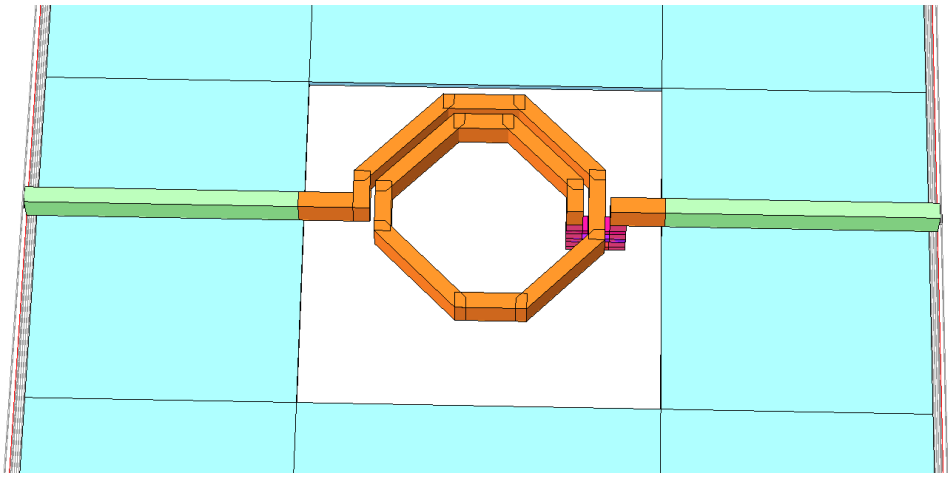


Fig. 3.15. The 3D firgure of matching inductor.

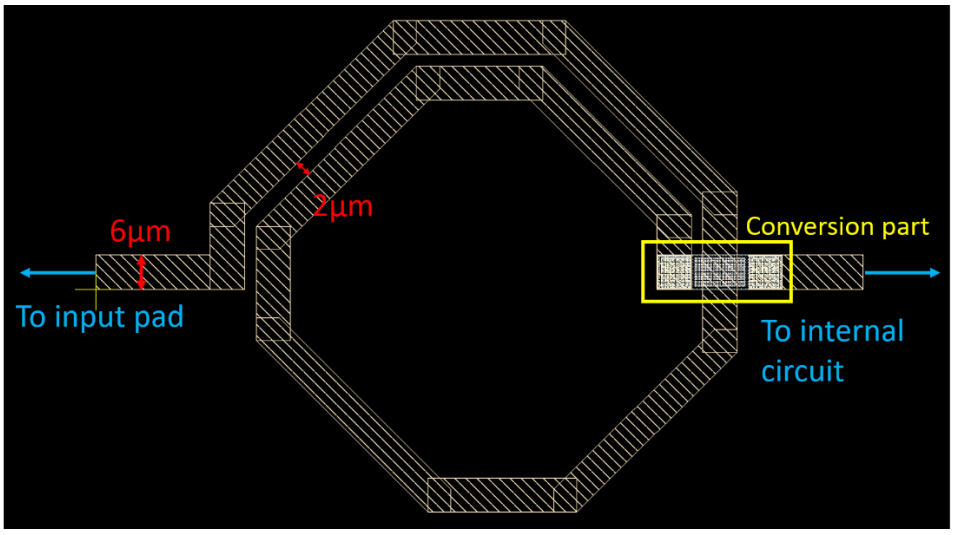


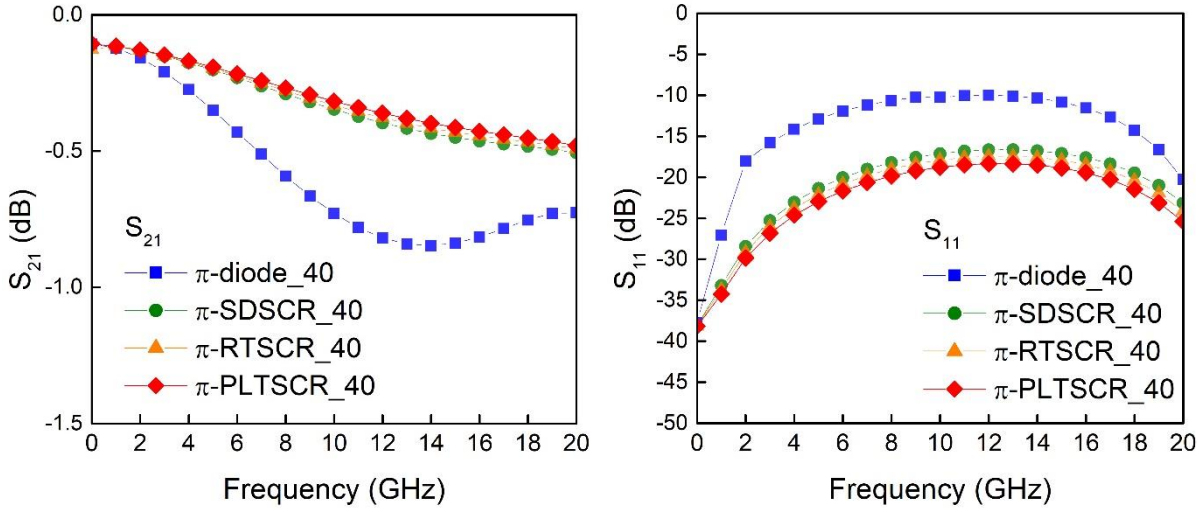
Fig. 3.16. The layout top view of matching inductor.

To verify the ESD robustness of each protection deivce, the width of deivce is selected as 20μm (per stage). For the proposed design, some experimental variable is designed for ESD test and high-frequency measurement such as width, number of triggering diode.

Simulated result of S-parameter of π-diode is compared with π-SDSCR, π-RTSCR

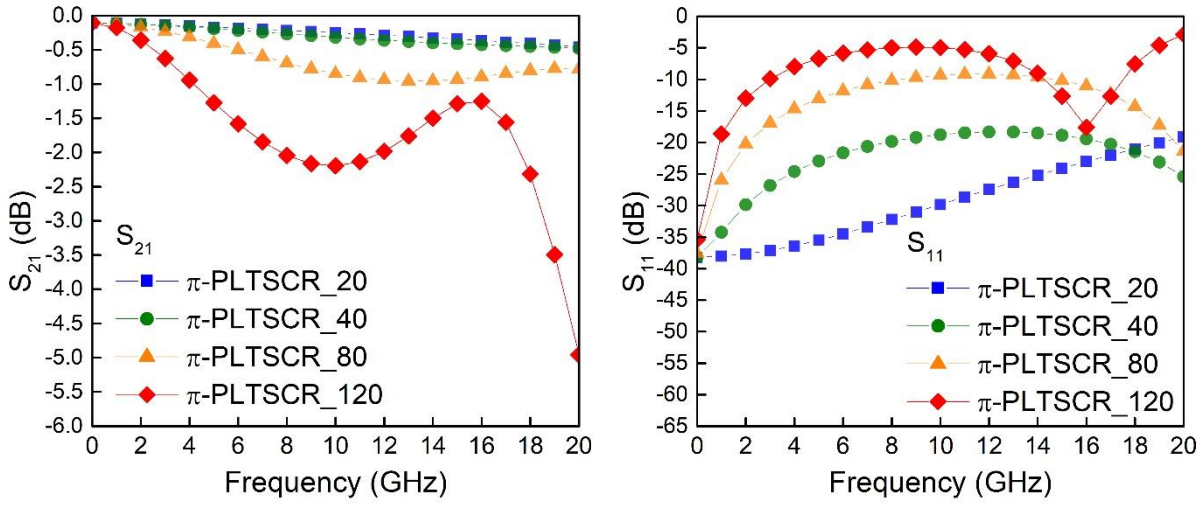
and π-PLTSCR in Fig. 3.17. All the total width of device is 40μm.

Another simulated result of π-PLTSCR with different device size is shown in Fig. 3.18. These size of π-PLTSCR is selected as 20, 40, 80, and 120μm.



(a) (b)

Fig. 3.17. The simulated S_{21} and S_{11} of different protection device (a) S_{21} (b) S_{11}.



(a) (b)

Fig. 3.18. The simulated S_{21} and S_{11} of π-PLTSCR with different size (a) S_{21} (b) S_{11}.

Table3.1 The simulation result of S-parameter at 20GHz

Cell Name	S_{21} (dB) at 20GHz	S_{11} (dB) at 20GHz
π-diode	-0.72	-20.25
π-SDSCR	-0.50	-23.15
π-RTSCR	-0.49	-24.16
π-PLTSCR	-0.48	-25.40
π-PLTSCR_20	-0.46	-19.09
π-PLTSCR_40	-0.48	-25.40
π-PLTSCR_80	-0.78	-21.39
π-PLTSCR_120	-4.95	-2.87

3.7 Measurement Results

All the test key of π-shape ESD protection device is implement in 0.18μm CMOS process. The test chip contains four type ESD protection including π-diode, π-SDSCR, π-RTSCR, and π-PLTSCR. The π-PLTSCRs with different size are also fabricated in the test chip. The measurement result of each device is introduced in next part.

3.7.1 High-Frequency Performance

In order to capture the S-parameter of each protection device, the 67GHz RFIC measurement system with 2-port GSG probes is used. [28] The measurement setup is shown in Fig. 3.19. In order to remove the impact of pad, the de-embedded method is used. After applying the de-embedding technique to eliminate the effects of the pad, the measured results are presented as follows, revealing the true characteristics of the devices. [29]

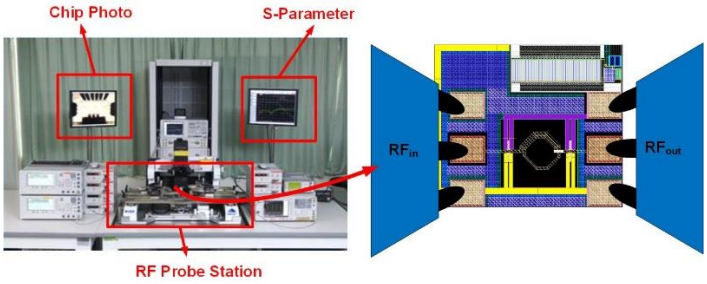


Fig. 3.19. The measurement setup of 67GHz RFIC measurement system.

The measurement result of π-diode is compared with π-SDSCR, π-RTSCR, and π-PLTSCR is shown in Fig. 3.20. The measurement result of π-PLTSCR_20 is compared with π-PLTSCR_40, π-PLTSCR_80, and π-PLTSCR_120 is shown in Fig. 3.21. The measurement result of S-parameter of each protection device at 20GHz is listed in Table 3.2.

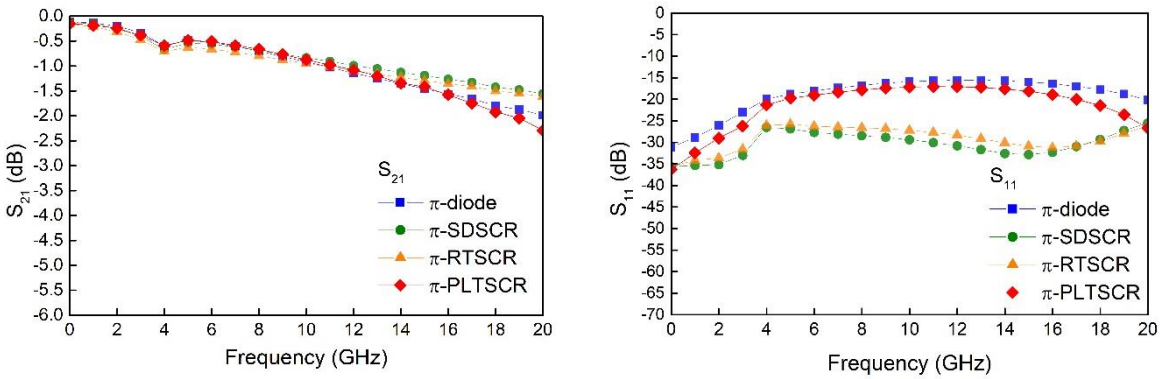


Fig. 3.20. The measured S_{21} and S_{11} of different protection device (a) S_{21} (b) S_{11}.

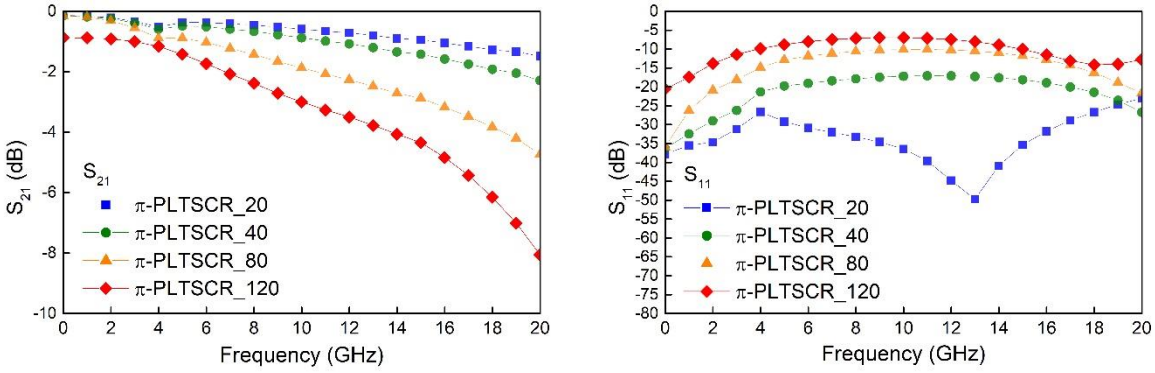


Fig. 3.21. The measured S_{21} and S_{11} of π-PLTSCR with different size (a) S_{21} (b) S_{11}

Table3.2 The measurement result of S-parameter at 20GHz

Cell Name	S_{21} (dB) at 20GHz	S_{11} (dB) at 20GHz
π-diode	-1.98	-20.16
π-SDSCR	-1.55	-25.53
π-RTSCR	-1.61	-26.21
π-PLTSCR	-2.28	-26.70
π-PLTSCR_20	-1.48	-23.05
π-PLTSCR_40	-2.28	-26.70
π-PLTSCR_80	-4.73	-21.71
π-PLTSCR_120	-8.05	-12.78

3.7.2 TLP Measurement

The I-V curve of ESD protection circuit can be measured by transmission-line-pulsing (TLP) generation system. The equipment can produce high-energy pulse to simulate ESD events. The voltage and current value of ESD protection circuit can be recorded after the pulse flow into the circuit. [30] The TLP measurement system used in this thesis is shown in Fig. 3.22. By using the TLP system, the characteristic of ESD protection device such as trigger voltage (V_{t1}), holding voltage (V_h), secondary breakdown current (I_{t2}) can be obtained from the measured I-V curve. The failure criterion of protection device is that the leakage current increases by 30%. All ESD protection devices undergo measurement in PS mode, PD mode, NS mode, and ND mode. Figures 3.23(a)-3.23(d) illustrate the TLP measurement outcomes of different ESD protection device in each mode. The second breakdown current (I_{t2}) is listed in Table 3.3. The TLP measurement results π-diode, π-SDSCR, π-RTSCR, and π-PLTSCR in the worst mode are 3.6A, 4.1 A, 3.9A, and 4.7A, respectively. Figures 3.24(a)-3.24(d)

illustrate the TLP measurement outcomes of π-PLTSCR with different sizes in each mode. The second breakdown current (I_{t2}) is listed in Table 3.3. The TLP measurement resultsπ-PLTSCR_20, π-PLTSCR_40, π-PLTSCR_120, and π-PLTSCR_120 in the worst mode are 1.8A, 4.7 A, 5.1A, and 6.7A, respectively. The I_{t2} of each protection circuit is listed in table 3.3.

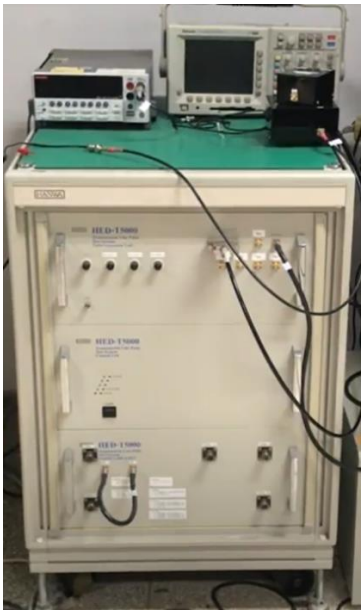
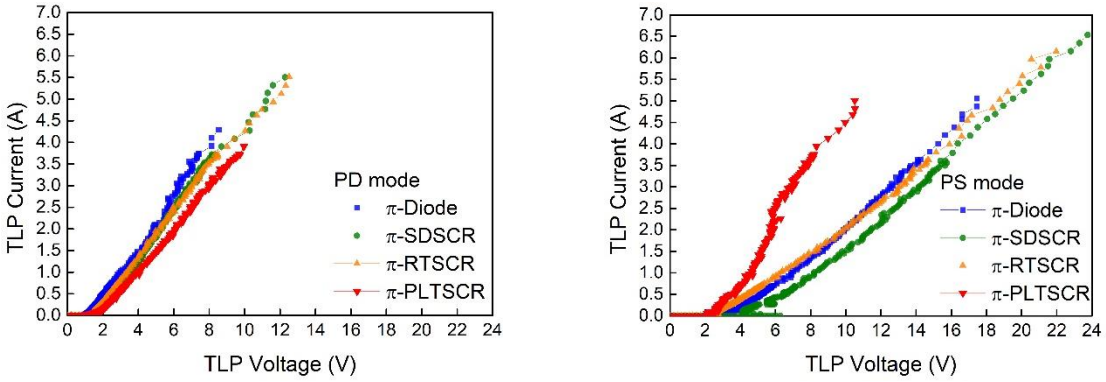
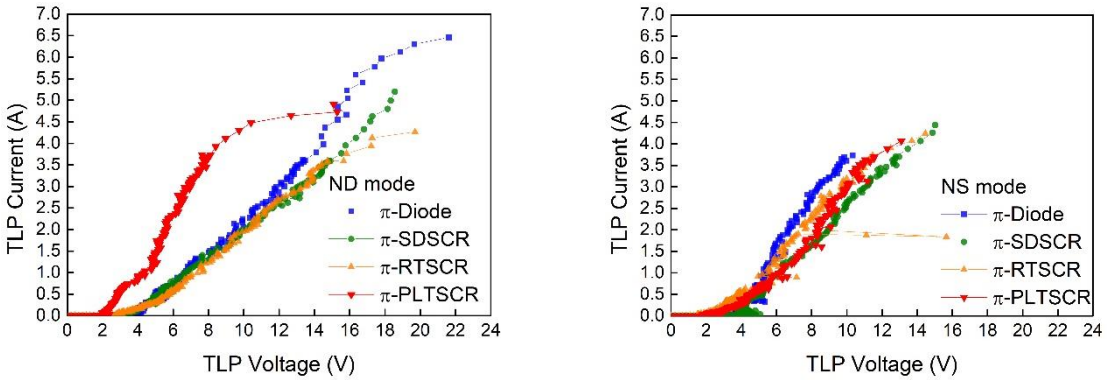


Fig. 3.22. Transmission-line pulsing (TLP) generation system. [30]

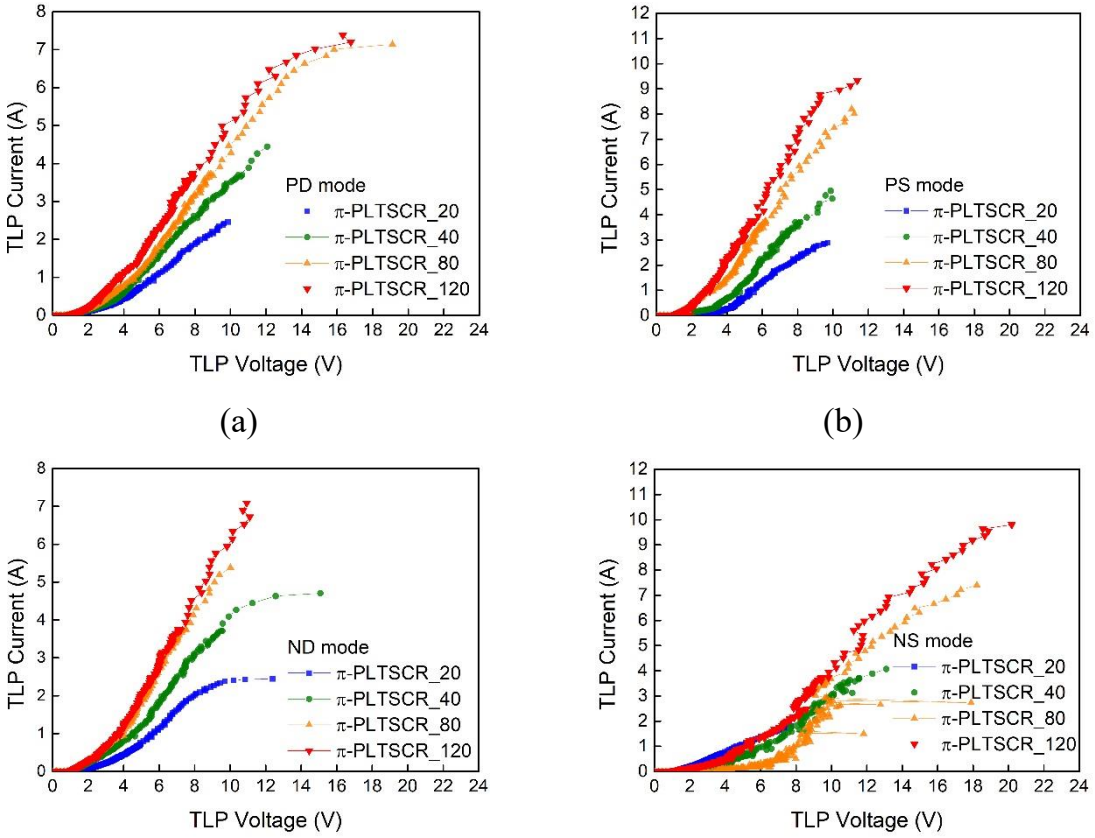


(a) (b)



(c) (d)

Fig. 3.23. TLP I-V curves of different test devices under PD, PS, ND, and NS mode



(a) (b)

(c) (d)

Fig. 3.24. TLP I-V curves of π-PLTSCR with different size under PD, PS, ND, and NS mode

Table 3.4 provides the measurement results for the parameter $V_{clamp@1.3A}$, which is defined as the voltage across the circuit when the ESD current reaches 1.3A. It can be

estimated that the HBM level is approximately 2kV when the ESD current reaches 1.3A, based on the equivalent resistor of HBM being 1.5k ohms.

Table 3.3. It_2 measurement result of each protection circuit.

Cell Name	It_2 (A)			
	PS mode	PD mode	NS mode	ND mode
π-diode	3.6	7.9	7.2	5.7
π-SDSCR	4.1	9.3	8.0	6.8
π-RTSCR	3.9	7.4	8.2	6.1
π-PLTSCR	4.7	5.0	4.7	7.0
π-PLTSCR_20	2.8	2.4	1.8	2.4
π-PLTSCR_40	4.7	5.0	4.7	7.0
π-PLTSCR_80	8.2	5.1	7.2	7.3
π-PLTSCR_120	9.9	6.7	9.8	9.5

Table 3.4. $V_{Clamp@1.3A}$ measurement result of different protection devices.

Cell Name	$V_{Clamp@1.3A}$ (V)			
	PS mode	PD mode	NS mode	ND mode
π-diode	7.9	3.7	5.8	7.3
π-SDSCR	9.3	4.2	6.9	8.1
π-RTSCR	7.4	4.0	6.1	8.2
π-PLTSCR	5.1	4.7	7.0	4.7

3.7.3 DC leakage current measurement

In order to confirm the ESD protection device will not cause extra power consumption, the DC leakage current should be measured. The measurement results of DC leakage current are listed in Table 3.3. The leakage current from VDD to input pad of π-diode, π-SDSCR, π-RTSCR and proposed π-PLTSCR is 212, 174, 154, and 85 pA, the leakage current from input pad to VSS of π-diode, π-SDSCR, π-RTSCR and proposed π-PLTSCR is 33, 12, 7, and 23 pA, and the leakage from VDD to VSS of π-diode, π-SDSCR, π-RTSCR, and π-PLTSCR are 12pA, 19pA, 14pA, and 45pA..

Table 3.5. The measurement result of DC leakage current.

Test Circuit	Leakage (pA)		
	VDD to input pad	Input pad to VSS	VDD to VSS
Traditional π-Diode	212	33	12
Traditional π-SDSCR	174	12	19
Traditional π-RTSCR	154	7	14
Proposed π-PLTSCR	85	23	45

3.7.4 HBM Test

From the TLP measurement result, the I-V curve of ESD protection devices can be obtained. But the real HBM robustness should be measured by HBM tester. The failure criterion is defined as an increase in the leakage current of over 30%. The HBM tester is shown in Fig. 3.25.

The HBM level of each ESD protection circuit is measured. The failure criterion is defined as an increase in the leakage current of over 30%. The test results of each ESD protection circuit are listed in table 3.4**.** The ESD robustness of π-diode, π-SDSCR, π-RTSCR, and π-PLTSCR are 6.3kV, >8kV, 7kV, and 7.5kV, respectively.

Fig. 3.25. HBM tester

Table 3.6. The measurement result of HBM test

Test Circuit	HBM (kV)			
	PD Mode	PS Mode	ND Mode	NS Mode
Traditional π-Diode	6.3	>8	>8	6.9
Traditional π-SDSCR	>8	>8	>8	>8
Traditional π-RTSCR	>8	>8	7	>8
Proposed π-PLTSCR	>8	>8	7.7	7.5
π-PLTSCR_20	4	4.5	4	4
π-PLTSCR_40	>8	>8	7.7	7.5
π-PLTSCR_80	>8	>8	>8	>8
π-PLTSCR_120	>8	>8	>8	>8

3.8 Comparison

The figure of merit (FOM) is defined to compare the performance of each ESD

protection circuit, and it is given by

$$FOM_1 = \frac{1}{Area * Insertion\ \ Loss * V_{clamp@1.3A}}$$

where the *Area* is the total layout area of ESD protection circuit, the *Insertion Loss* is the measured $|S_{21}|$ at 20GHz, and the $V_{clamp@1.3A}$ is the voltage cross the circuit when the current is 1.3A of four discharge modes. The comparison results of all ESD protection circuits are listed in table 3.5. The FOM of π-diode, π-SDSCR, π-RTSCR, and π-PLTSCR are 1.18, 1.22, 1.35, and 2.02 $(mm^2*dB*V)^{-1}$, respectively. From this result, the proposed π-PLTSCR is better than traditional designs.

Table 3.7. FOM_1 comparison of π-shape ESD protection circuits.

Test Circuit	Area (mm^2)	Insertion Loss @20 GHz (dB)	$V_{clamp@1.3A}$ (V)	FOM_1 $(mm^2*dB*V)^{-1}$
Traditional π-Diode	0.054	1.98	7.9	1.18
Traditional π-SDSCR	0.057	1.55	9.3	1.22
Traditional π-RTSCR	0.056	1.61	8.2	1.35
Proposed π-PLTSCR	0.031	2.28	7.0	2.02

3.9 Summary

In this chapter, the proposed PLTSCR can suit for the high-speed applications in CMOS technology. Based on the high-frequency measurement results, the proposed design exhibits an insertion loss of lower than 3dB, can achieve HBM ESD robustness up to 7.5kV, and occupies an area of only 0.031mm^2. The area cost is less than other

designs about 36% because the proposed design does not use the power clamp to discharge ESD current. Furthermore, the clamping voltage during ESD current discharging can be much lower. The worst $V_{clamp@1.3A}$ of the proposed design is 7V, while those of other designs are as high as 7.9V, 8.2V, and 9.3V. Considering the FOM of each ESD protection circuit, the performance of proposed design is better than traditional designs. Of course, the matching inductor of the proposed π-PLTSCR can be optimized to further improve the insertion loss.

Chapter 4

Verification of Proposed π-PLTSCR with Trans-Impedance Amplifier (TIA)

4.1 Background of TIA

Over the past few years, there has been a gradual rise in the need for high-speed transmission products. This has, in turn, driven the data rate of optical communication systems to new heights. In order to maintain such high operating speeds, circuits must be designed with a large bandwidth. The trans-impedance amplifier (TIA) is a crucial component in optical communications. Its main function is to convert photo current into a voltage signal, making it a necessary component for any optical receiver. The architecture of an optical receiver system is illustrated in Figure 4.1 [31].

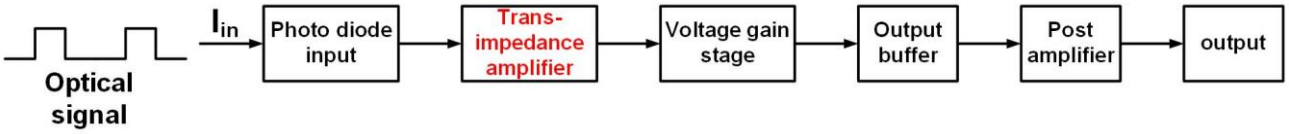


Fig. 4.1. The block diagram of optical receiver system.

4.2 Structure of TIA

The architecture of the TIA with a π-shape ESD protection circuit is illustrated in Figure 4.2. The π-shape ESD protection circuits are incorporated into the input and matched with the input-matching inductor. To achieve whole-chip ESD protection, a power clamp is placed between the power line (VDD) and the ground line (VSS). The TIA operates at a supply voltage of 1.8 V, and the input bias is 1 V. The drain resistors are chosen as 180 Ω, and the input resistors are selected as 100 Ω. The inductors L_1 and L_3 have a value of 0.46 nH, L_2 is 0.76 nH, L_4 is 1.6 nH, L_5 is 1.2 nH, and L_6 is 0.22 nH.

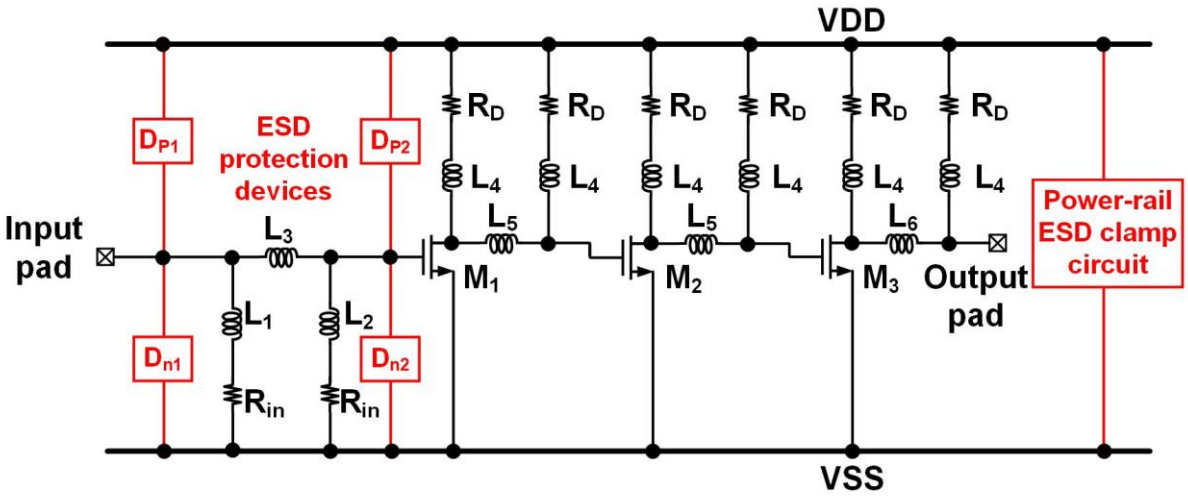


Fig. 4.2. The architecture of TIA with π-shape ESD protection circuit.

4.3 Simulation Results of TIA

TIA circuits are evaluated for their ability to provide ESD protection using different protection device, including traditional π-diodes, π-SDSCRs, π-RTSCRs, and the proposed π-PLTSCR. S-parameter simulations of all the test circuits are performed using Advanced Design System (ADS), while SONNET electromagnetic (EM) is used for electromagnetic simulations of the inductors and metal routing.

4.3.1 TIA w/o Protection

The circuit diagram of TIA without protection circuit is shown in Fig. 4.3. It combines three common-source (CS) stage amplifiers. The supply voltage (VDD) is 1.8V and the input bias is 1V.

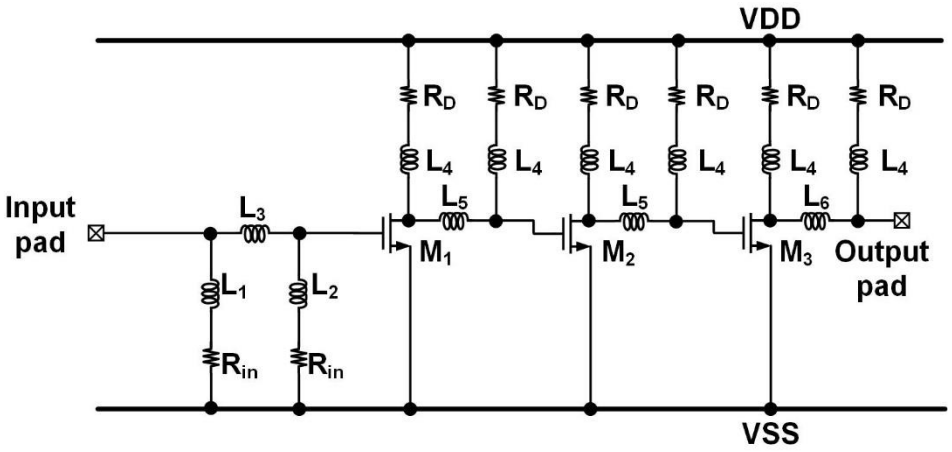
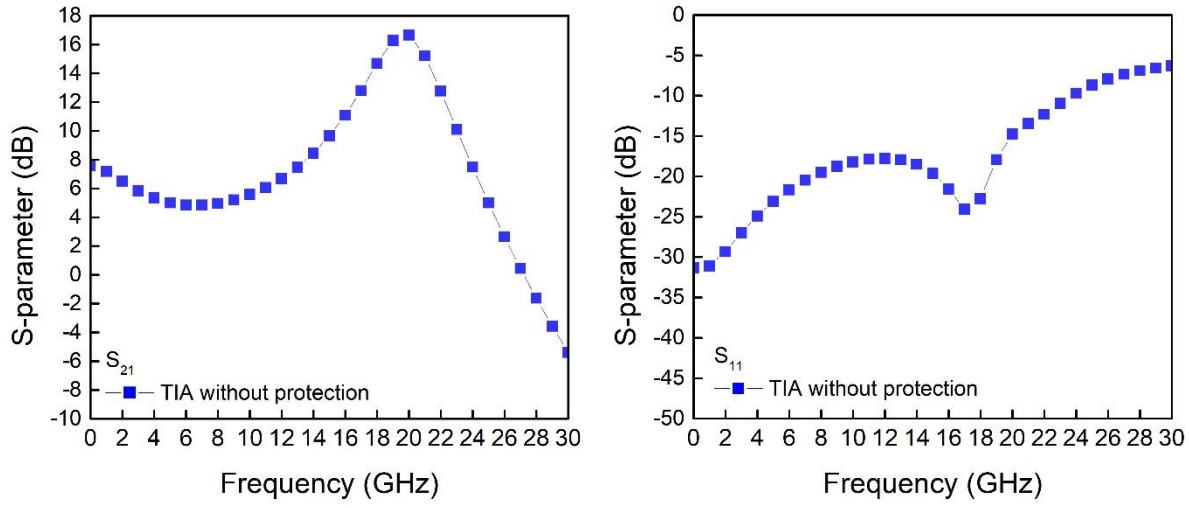


Fig. 4.3. The circuit diagram of TIA without ESD protection circuit.

As shown in Fig. 4.4 (a) and (b), simulated S_{21} is 9.65dB, and S_{11} is -19.63dB at 15GHz. Layout view of TIA is depicted in Fig. 4.5.



(a) (b)

Fig. 4.4. High-frequency simulation result of TIA without protection (a) S_{21} and (b) S_{11}.

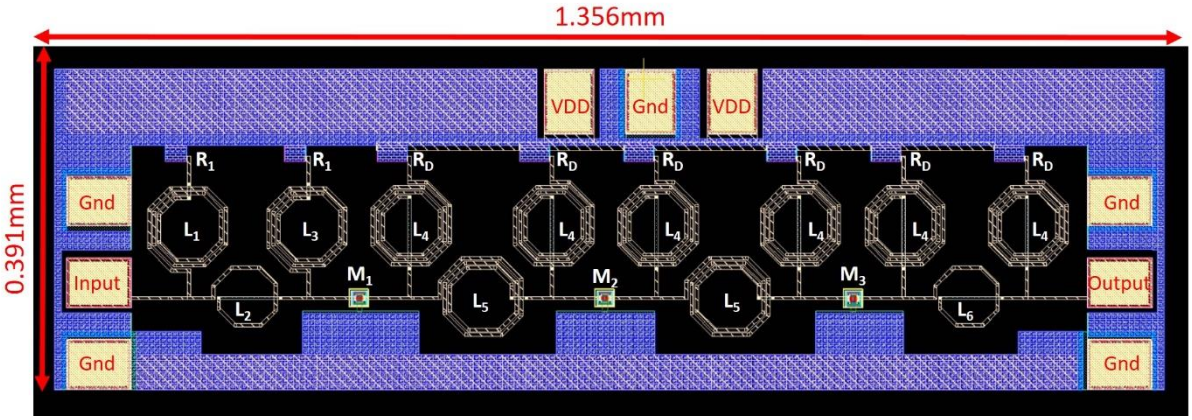


Fig. 4.5. Layout top view of TIA without protection.

4.3.2 TIA with Traditional π-Diode

The whole-chip ESD protection for TIA with π-diode input protection circuit is shown in Fig. 4.6. Different from TIA without protection, this TIA is equipped with π-diode protection circuit and power clamp circuit. The size of diode in each stage is

selected as 20μm.

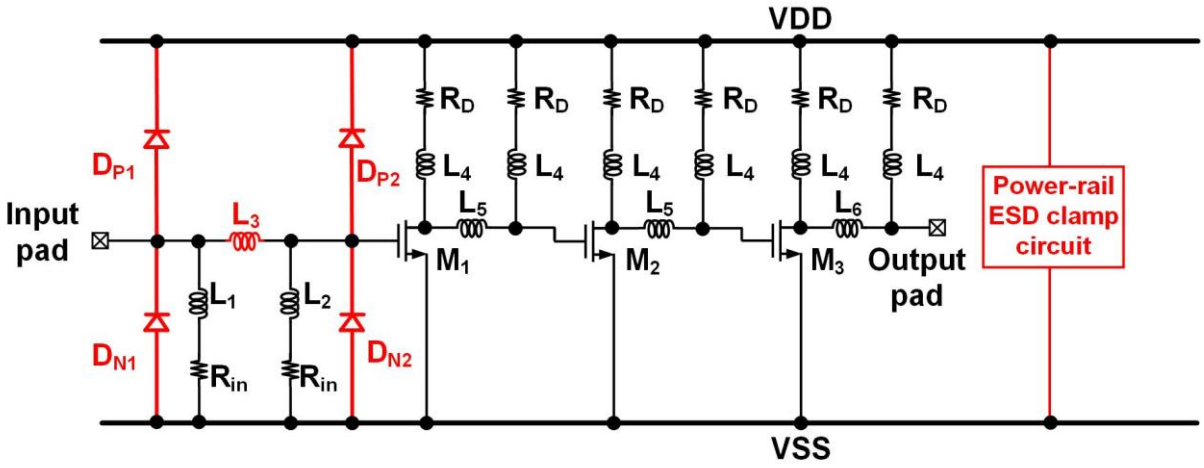
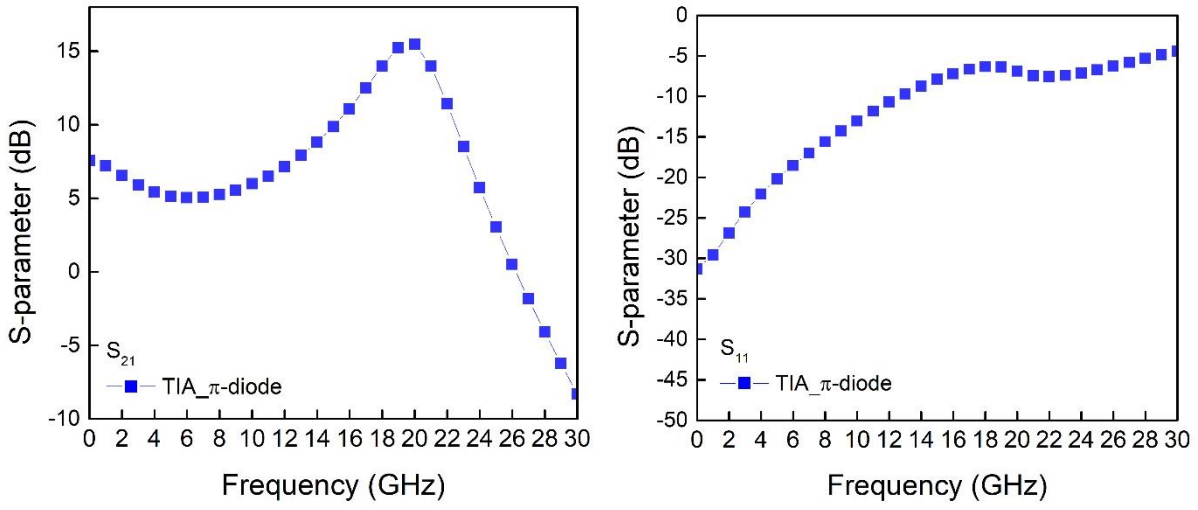


Fig. 4.6. The circuit diagram of TIA with π-diode.

As shown in Fig. 4.7 (a) and (b), simulated S_{21} is 9.86dB, and S_{11} is -7.89dB at 17GHz. Layout view of TIA with π-diode is depicted in Fig. 4.8.



(a) (b)

Fig. 4.7. High-frequency simulation result of TIA with π-diode (a) S_{21} and (b) S_{11}.

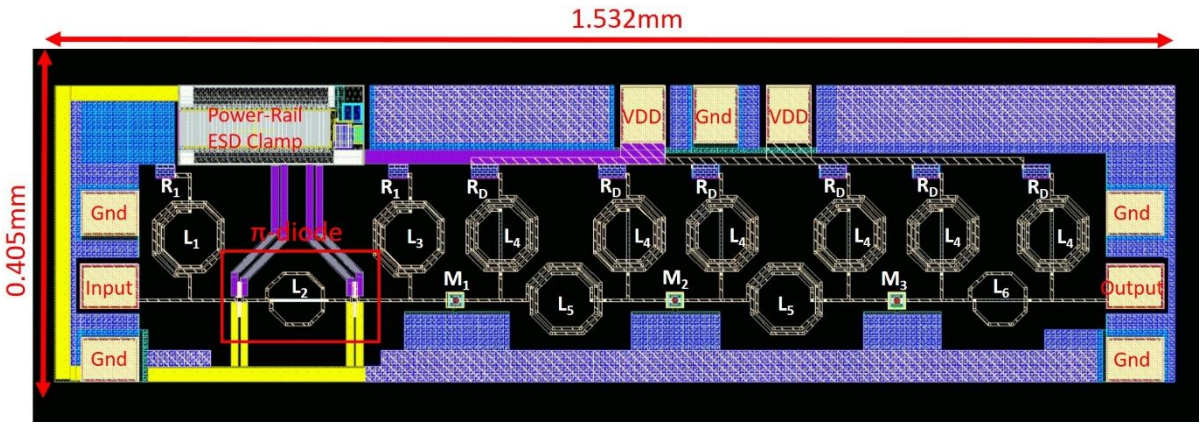


Fig. 4.8. Layout top view of TIA with π-diode.

4.3.3 TIA with Traditional π-SDSCR

The whole-chip ESD protection for TIA with π-SDSCR input protection circuit is shown in Fig. 4.9. Different from TIA without protection, this TIA is equipped with π-SDSCR protection circuit and power clamp circuit. The size of SDSCR in each stage is selected as 20μm.

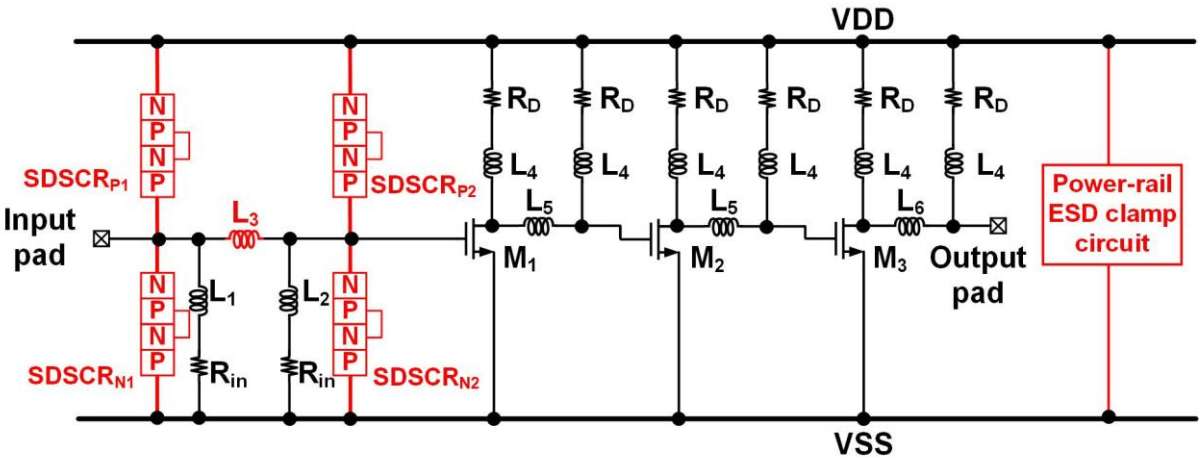
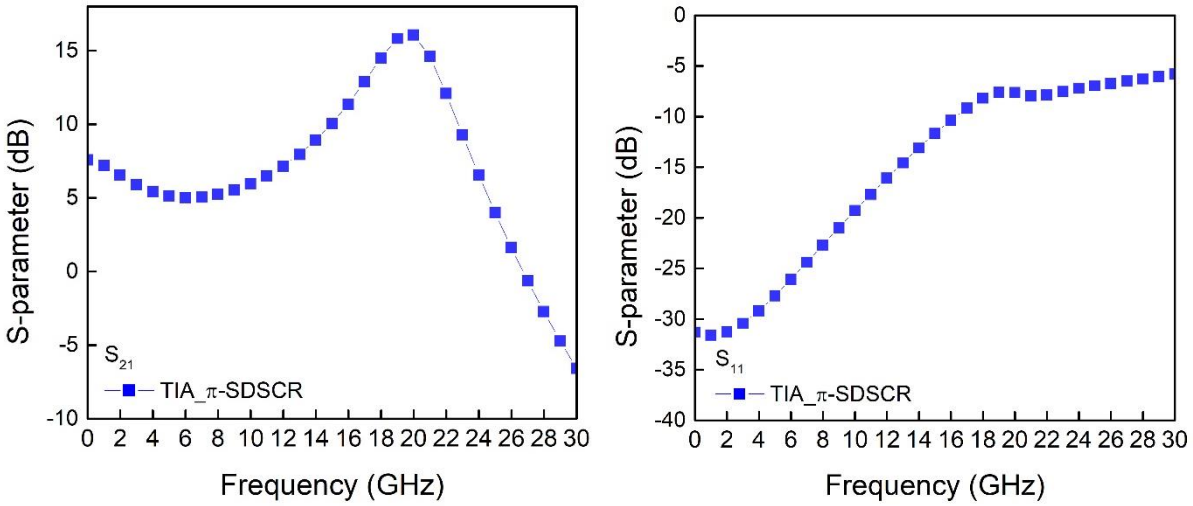


Fig. 4.9. The circuit diagram of TIA with π-SDSCR.

As shown in Fig. 4.10 (a) and (b), simulated S_{21} is 10.04dB, and S_{11} is -13.07dB at 15GHz. Layout view of TIA with π-SDSCR is depicted in Fig. 4.11.



(a) (b)

Fig. 4.10. High-frequency simulation result of TIA with π-SDSCR (a) S_{21} and (b) S_{11}.

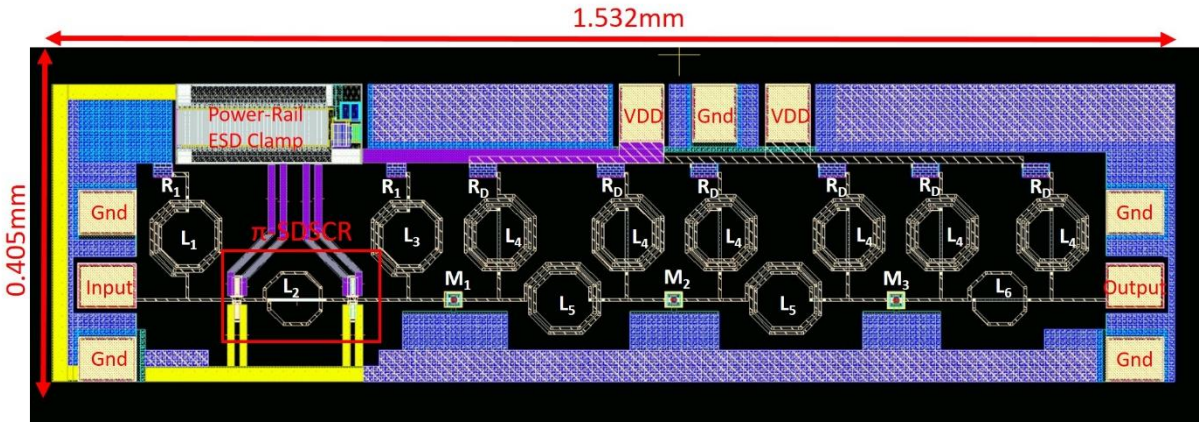


Fig. 4.11. Layout top view of TIA with π-SDSCR.

4.3.4 TIA with Traditional π-RTSCR

The whole-chip ESD protection for TIA with π-RTSCR input protection circuit is shown in Fig. 4.12. Different from TIA without protection, this TIA is equipped with π-RTSCR protection circuit and power clamp circuit. The size of RTSCR in each stage is selected as 20μm.

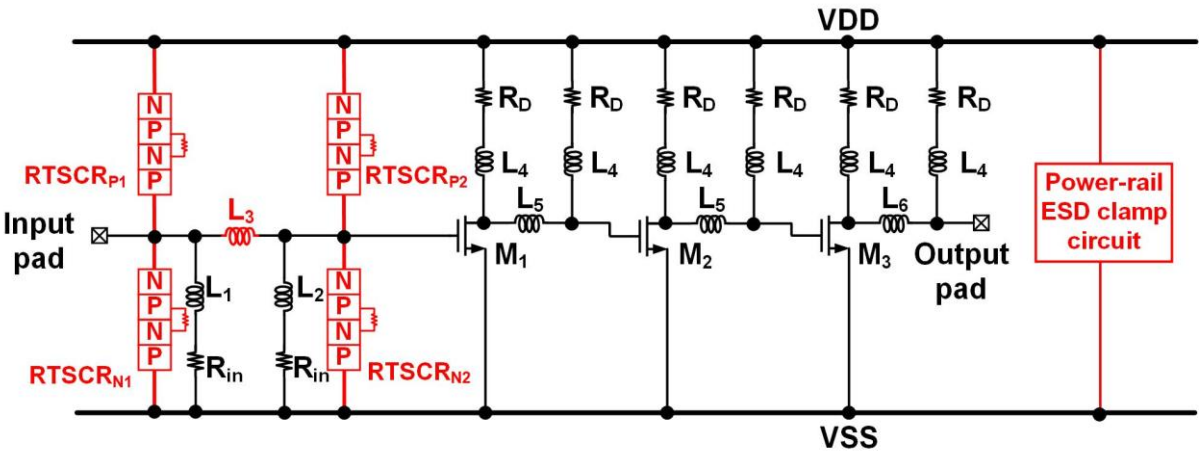
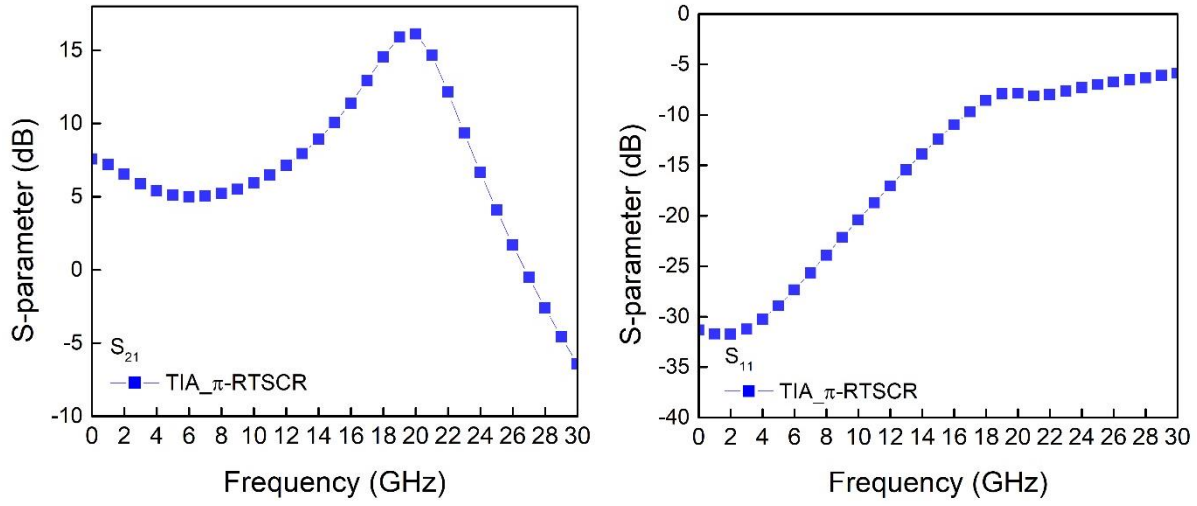


Fig. 4.12. The circuit diagram of TIA with π-RTSCR.

As shown in Fig. 4.13 (a) and (b), simulated S_{21} is 10.05dB, and S_{11} is -12.39dB at 15GHz. Layout view of TIA with π-RTSCR is depicted in Fig. 4.14.



(a) (b)

Fig. 4.13. High-frequency simulation result of TIA with π-RTSCR (a) S_{21} and (b) S_{11}.

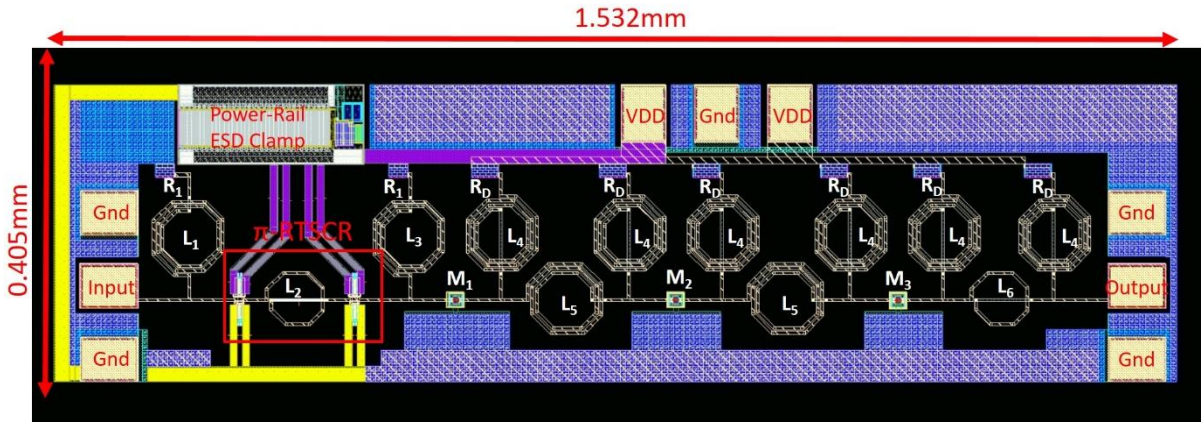


Fig. 4.14. Layout top view of TIA with π-RTSCR.

4.3.5 TIA with proposed π-PLTSCR

The whole-chip ESD protection for TIA with π-PLTSCR input protection circuit is shown in Fig. 4.15. Different from TIA without protection, this TIA is equipped with π-PLTSCR protection circuit and power clamp circuit. The size of PLTSCR in each stage is selected as 20μm.

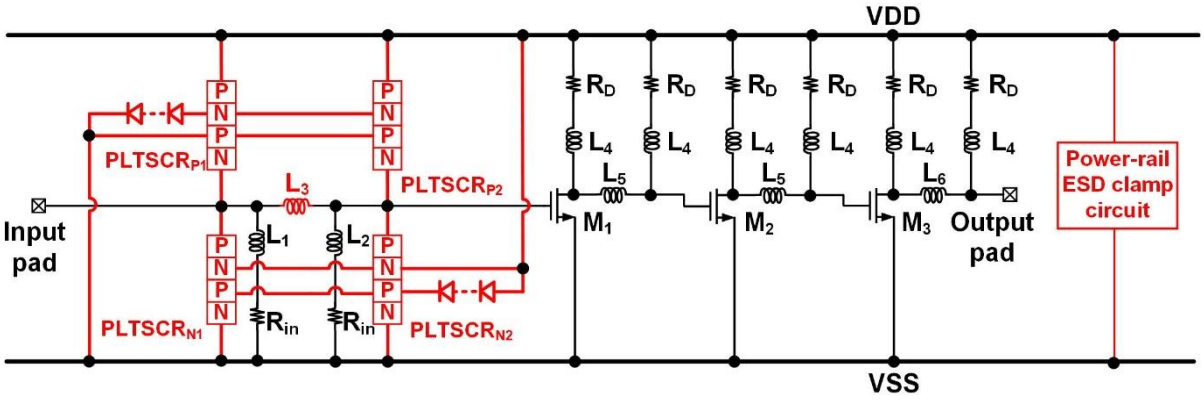
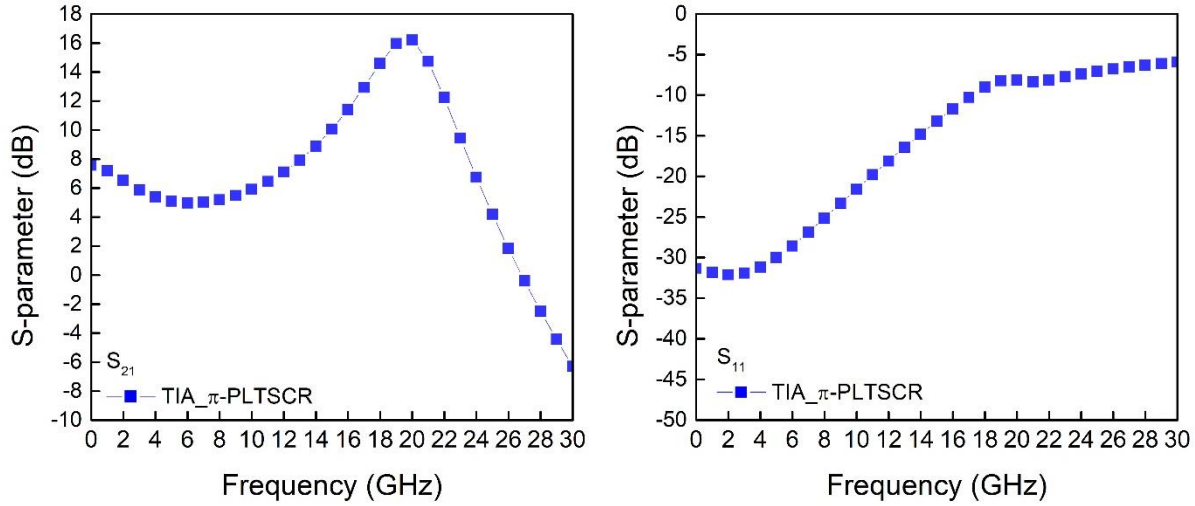


Fig. 4.15. The circuit diagram of TIA with π-PLTSCR.

As shown in Fig. 4.16 (a) and (b), simulated S_{21} is 10.04dB, and S_{11} is -13.20dB at 15GHz. Layout view of TIA with π-PLTSCR is depicted in Fig. 4.17.



(a) (b)

Fig. 4.16. High-frequency simulation result of TIA with π-PLTSCR (a) S_{21} and (b) S_{11}.

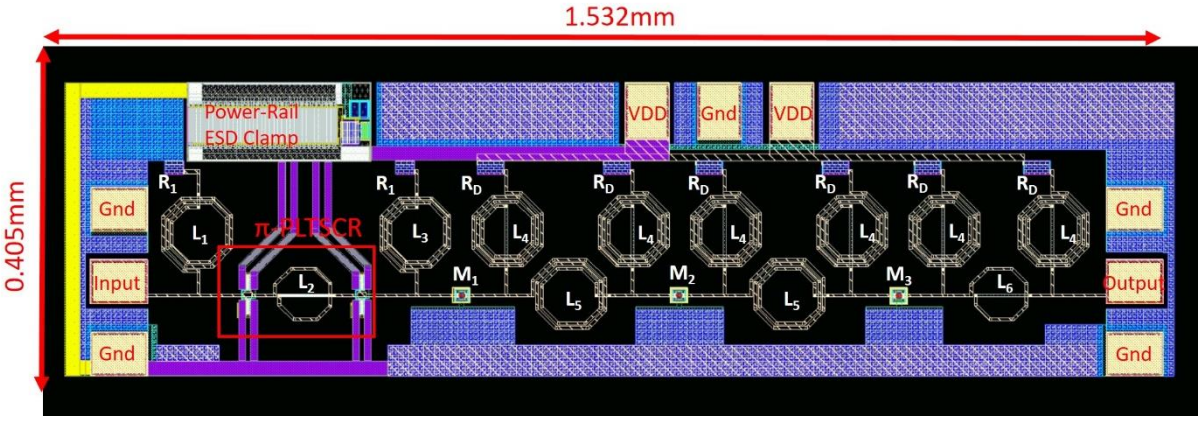


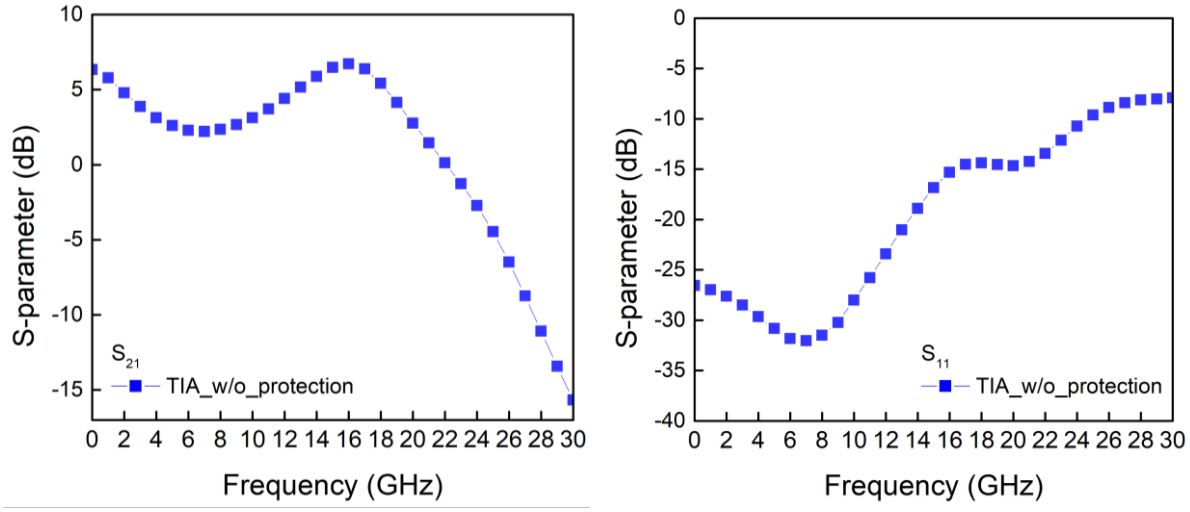
Fig. 4.17. Layout top view of TIA with π-PLTSCR.

4.4 Measurement Results of TIA

4.4.1 High-Frequency Performance

In order to verify the high-frequency performance, all the test circuits are measured by the 67GHz RFIC on-wafer measurement system.

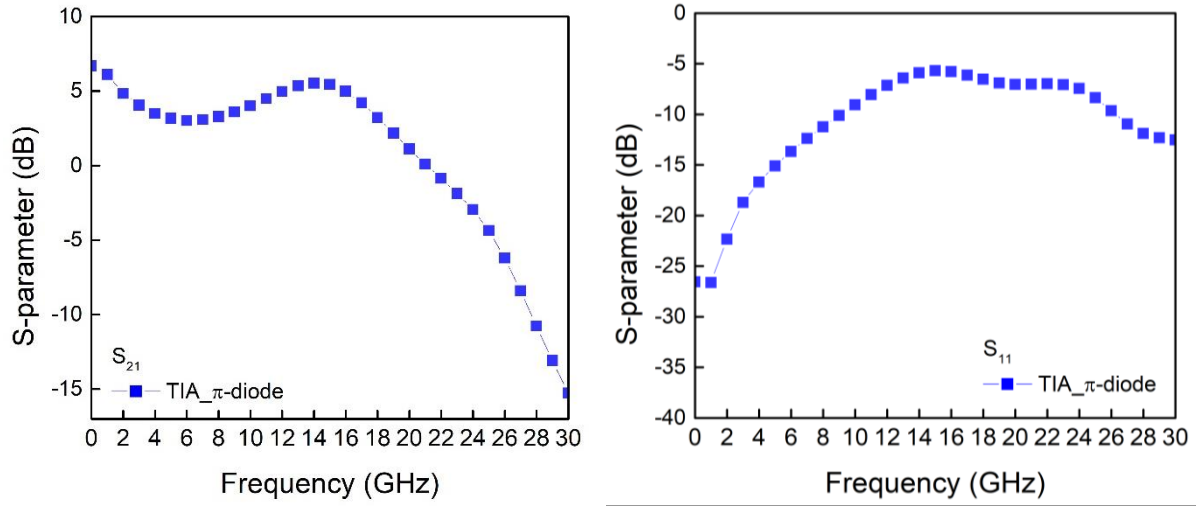
The S-parameter measurement result of TIA without protection circuit is shown in Fig. 4.18 (a) and (b). The measured S_{21} at 15GHz is 6.48dB and the S_{11} at 15GHz is -16.81dB.



(a) (b)

Fig. 4.18. High-frequency measurement result of TIA without protection (a) S_{21} and (b) S_{11}.

The S-parameter measurement result of TIA with π-diode ESD protection circuit is shown in Fig. 4.19 (a) and (b). The measured S_{21} at 15GHz is 5.43dB and the S_{11} at 15GHz is -5.68dB.

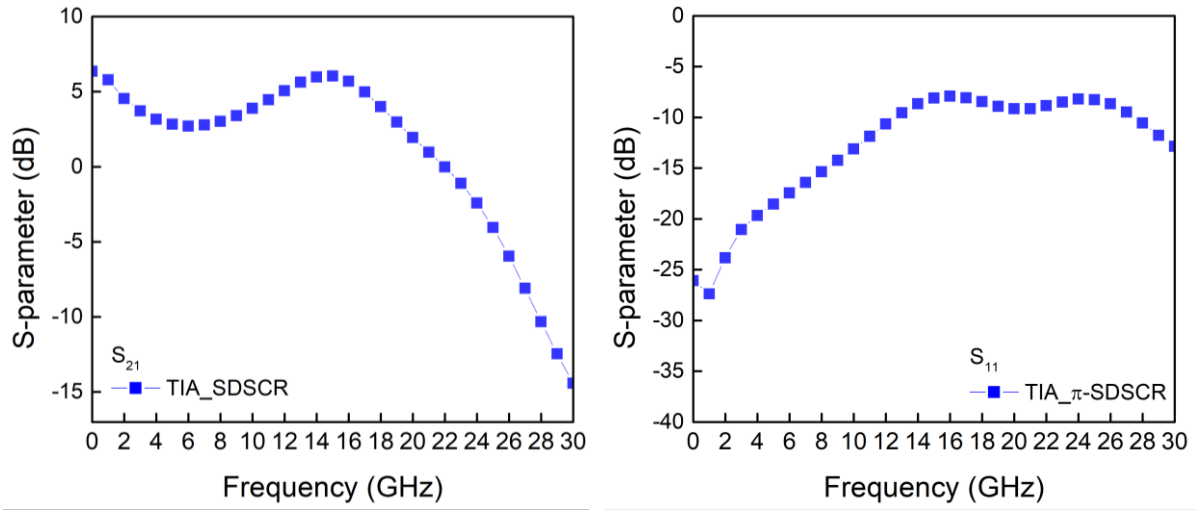


(a) (b)

Fig. 4.19. High-frequency measurement result of TIA with π-diode ESD protection circuit (a) S_{21} and (b) S_{11}.

The S-parameter measurement result of TIA with π-SDSCR ESD protection circuit is shown in Fig. 4.20 (a) and (b). The measured S_{21} at 15GHz is 6.09dB and the S_{11} at

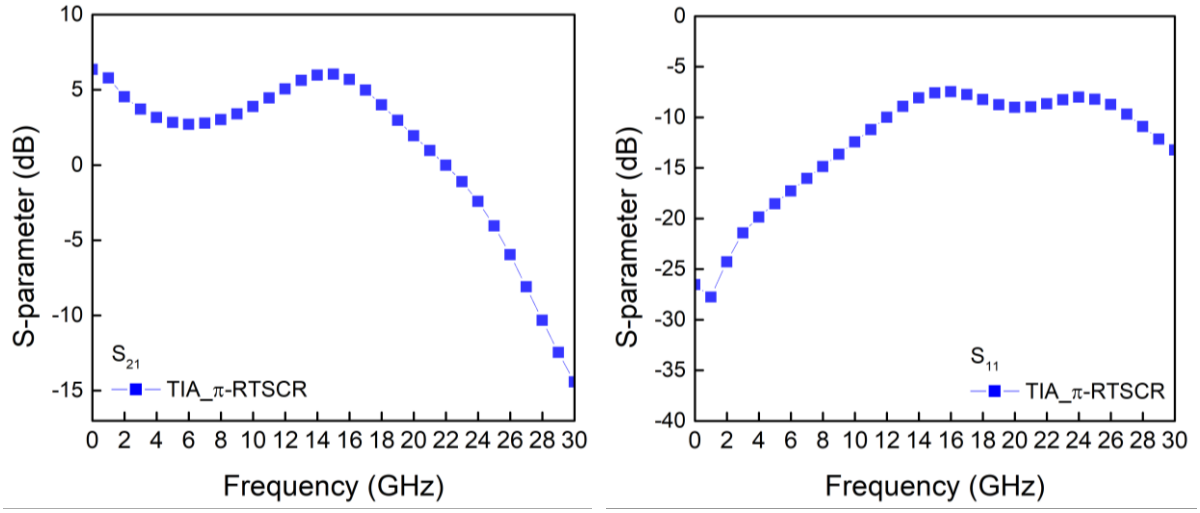
15GHz is -8.09dB.



(a) (b)

Fig. 4.20. High-frequency measurement result of TIA with π-SDSCR ESD protection circuit (a) S_{21} and (b) S_{11}.

The S-parameter measurement result of TIA with π-RTSCR ESD protection circuit is shown in Fig. 4.21 (a) and (b). The measured S_{21} at 15GHz is 6.03dB and the S_{11} at 15GHz is -7.57dB.

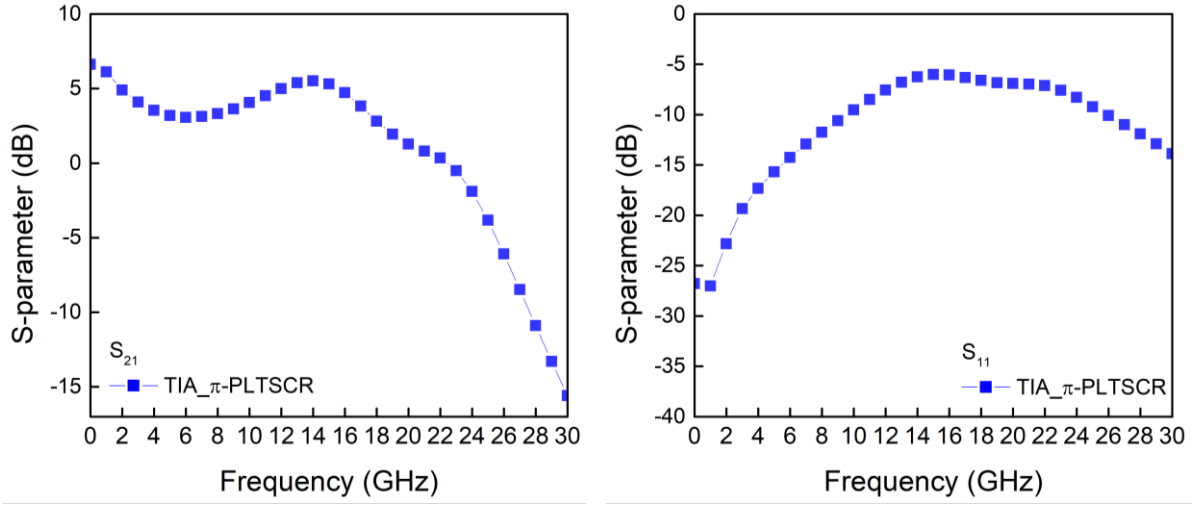


(a) (b)

Fig. 4.21. High-frequency measurement result of TIA with π-RTSCR ESD protection circuit (a) S_{21} and (b) S_{11}.

The S-parameter measurement result of TIA with π-PLTSCR ESD protection circuit

is shown in Fig. 4.22 (a) and (b). The measured S_{21} at 15GHz is 5.31dB and the S_{11} at 15GHz is -6.01dB. All the measurement results of high-frequency performance are listed in table 4.1.



(a) (b)

Fig. 4.22. High-frequency measurement result of TIA with π-PLTSCR ESD protection circuit (a) S_{21} and (b) S_{11}.

Table 4.1. The measurement result of S-parameter

Test Circuit	S_{21} (dB) @15GHz	S_{11} (dB) @15GHz
TIA without protection	6.48	-16.81
TIA with π-diode	5.43	-5.68
TIA with π-SDSCR	6.09	-8.09
TIA with π-RTSCR	6.03	-7.57
TIA with π-PLTSCR	5.31	-6.01

4.4.2 TLP I-V Measurement

To obtain the I-V curve of TIA with various ESD protection circuits, it is necessary to perform TLP testing. The TLP testing results for TIA under different protection circuits such as TIA without protection, TIA with traditional π-diode, TIA with

traditional π-SDSCR, TIA with traditional π-RTSCR, and TIA with proposed π-PLTSCR in the worst case are 0.16 A, 3.44 A, 3.45 A, 3.14 A, and 3.74 A, respectively. These results are presented in Fig. 4.23 and summarized in Table 4.2.

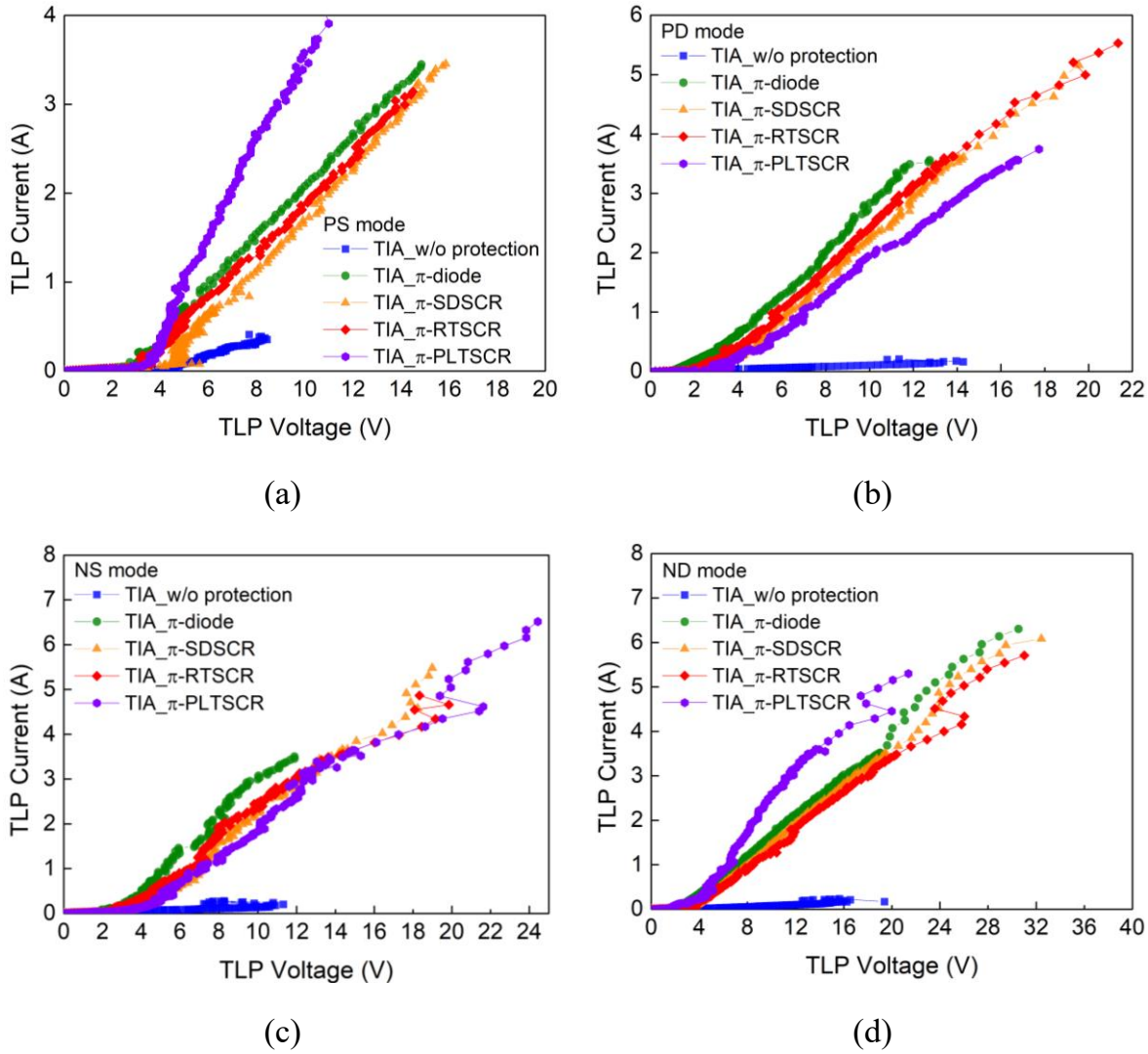


Fig. 4.23. TLP measurement result of test circuits under (a) PS mode, (b) PD mode, (c) NS mode, and (d) ND mode.

Table 4.2. The It_2 of each TIA with/without protection circuit.

Cell Name	It_2 (A)			
	PS mode	PD mode	NS mode	ND mode
TIA w/o protection	0.40	0.16	0.27	0.16
TIA with π-diode	3.44	3.55	3.45	6.30
TIA with π-SDSCR	3.45	5.15	5.30	6.08
TIA with π-RTSCR	3.14	5.52	4.65	5.71
TIA with π-PLTSCR	4.98	3.74	6.32	5.30

Another parameter $V_{clamp@1.3A}$ is defined as the voltage across the circuit when the ESD current achieve 1.3A. The measurement result of $V_{clamp@1.3A}$ is listed in Table 4.3. When the ESD current achieve 1.3A, the HBM level can be estimated about 2kV because the equivalent resistor of HBM is 1.5k ohm.

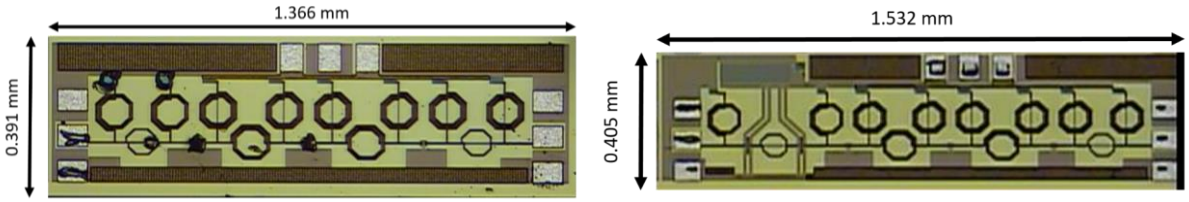
Table 4.3. Measured $V_{clamp@1.3A}$ of each test circuit under each discharge mode.

Cell Name	$V_{Clamp@1.3A}$ (V)			
	PS mode	PD mode	NS mode	ND mode
TIA w/o protection	-	-	-	-
TIA with π-diode	7.18	6.16	5.83	8.48
TIA with π-SDSCR	8.60	7.21	7.64	9.39
TIA with π-RTSCR	8.14	6.86	7.08	9.99
TIA with π-PLTSCR	5.73	8.10	8.15	6.91

4.4.3 HBM Test

To assess the ESD robustness of TIAs with or without protection circuits, the HBM test can be used. However, the failure criterion of leakage current may not clearly

indicate whether the circuit has been damaged or not, as TIA circuits often have large input stage leakage currents. Another approach involves taking a photo of the circuit under a microscope. In Fig. 4.24 (a), it is evident that the TIA without protection was damaged after the 1 kV HBM test. On the other hand, in Fig. 4.24 (b), the TIA with π-SDSCR ESD protection circuit did not show obvious damage under the microscope. To determine the correct HBM level, it is necessary to measure the high-frequency performance after the HBM test.



(a) (b)

Fig. 4.24. Photo of TIA circuit after HBM test: (a) TIA without protection; (b) TIA with π-SDSCR.

The HBM measurement result of TIA without protection circuit is shown in Fig. 4.25 (a) and Fig. 4.25 (b). The S_{21} and S_{11} are changed after 1kV HBM zap voltage. The TIA without protection circuit is broken obviously.

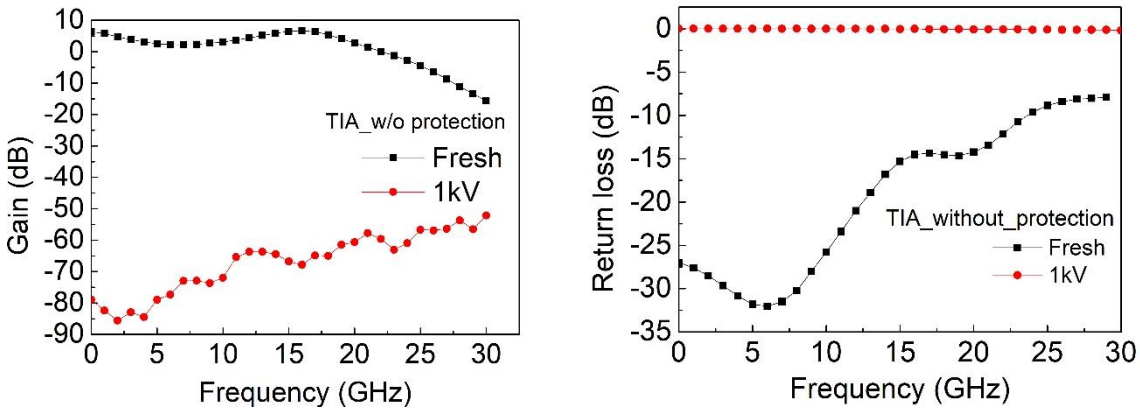


Fig. 4.25. The measured S_{21} and S_{11} of TIA without protection circuit (a) S_{21} (b) S_{11}.

The HBM measurement result of TIA with π-diode ESD protection circuit is shown

in Fig. 4.26 (a) and Fig. 4.26 (b). The S_{21} and S_{11} are changed after 6kV HBM zap voltage. The TIA with π-diode protection circuit is broken obviously.

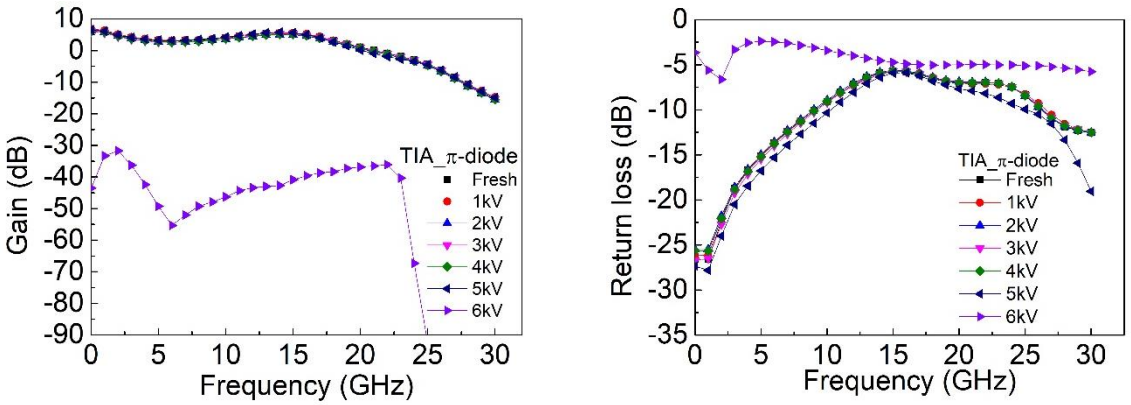


Fig. 4.26. The measured S_{21} and S_{11} of TIA with π-diode ESD protection circuit (a) S_{21} (b) S_{11}.

The HBM measurement result of TIA with π-SDSCR ESD protection circuit is shown in Fig. 4.27 (a) and Fig. 4.27 (b). The S_{21} and S_{11} are changed after 7kV HBM zap voltage. The TIA with π-SDSCR protection circuit is broken obviously.

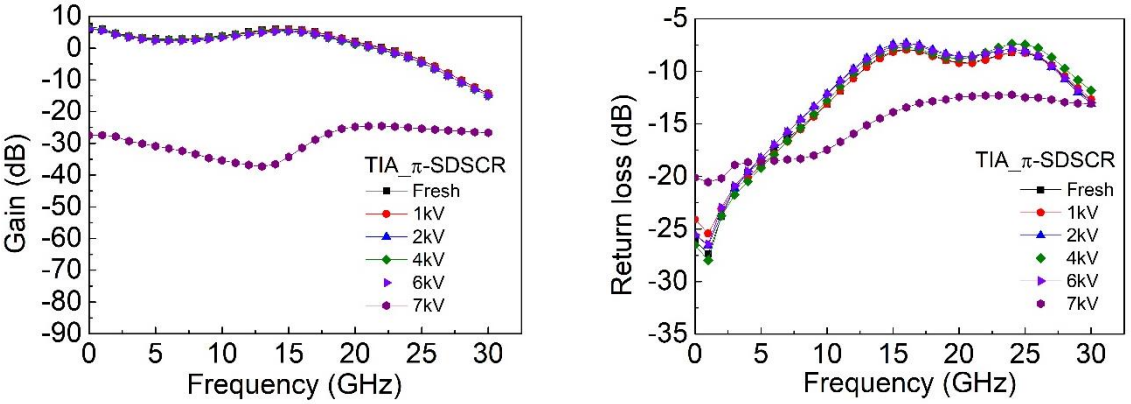


Fig. 4.27. The measured S_{21} and S_{11} of TIA with π-SDSCR ESD protection circuit (a) S_{21} (b) S_{11}.

The HBM measurement result of TIA with π-RTSCR ESD protection circuit is shown in Fig. 4.28 (a) and Fig. 4.28 (b). The S_{21} and S_{11} are changed after 6kV HBM

zap voltage. The TIA with π-RTSCR protection circuit is broken obviously.

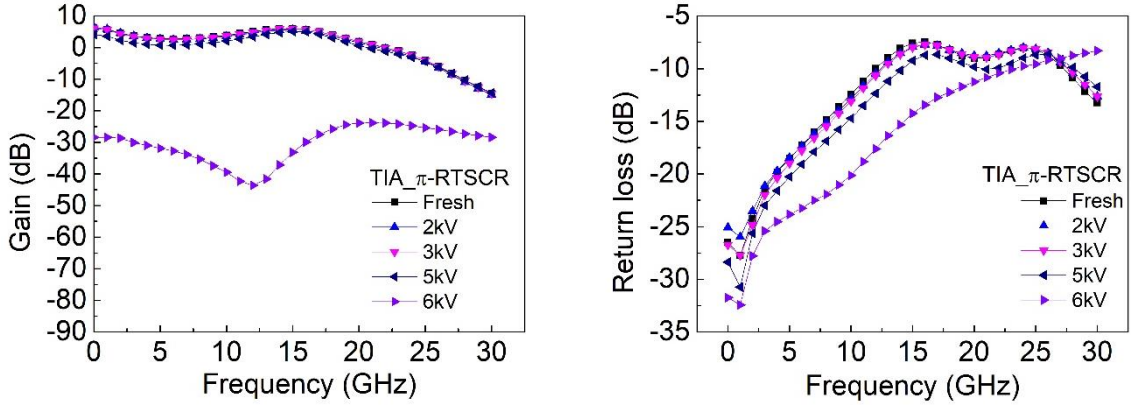


Fig. 4.28. The measured S_{21} and S_{11} of TIA with π-RTSCR ESD protection circuit (a) S_{21} (b) S_{11}.

The HBM measurement result of TIA with π-PLTSCR ESD protection circuit is shown in Fig. 4.29 (a) and Fig. 4.29 (b). The S_{21} and S_{11} are changed after 7kV HBM zap voltage. The TIA with π-PLTSCR protection circuit is broken obviously.

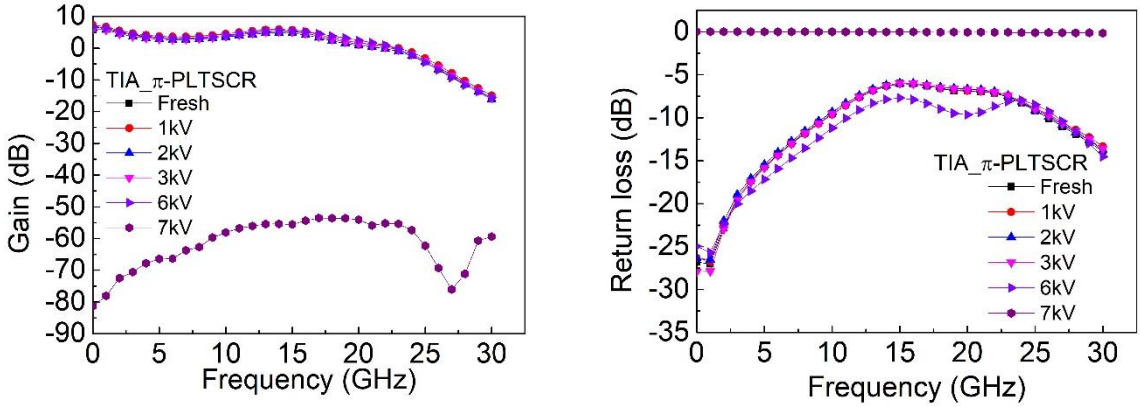


Fig. 4.29. The measured S_{21} and S_{11} of TIA with π-PLTSCR ESD protection circuit (a) S_{21} (b) S_{11}.

The test results of each TIA are listed in Table 4.4**.** The ESD robustness of TIA without protection, TIA with π-diode, TIA with π-SDSCR, TIA with π-RTSCR, and TIA with π-PLTSCR are <1kV, 5kV, 6kV, 5kV, and 6kV, respectively.

Table4.4. The HBM measurement result of TIAs by function confirmation

Test circuit	HBM (kV)
TIA w/o protection	<1kV
TIA with traditional π-diode	5kV
TIA with traditional π-SDSCR	6kV
TIA with traditional π-RTSCR	5kV
TIA with proposed π-PLTSCR	6kV

4.5 Comparison

As shown in Fig. 4.30, the high-frequency measurement result of TIA without protection circuits and TIA with different protection circuit are compared. Because the ESD protection is added to TIA circuit, the area of the whole circuit increased about 10%. The S_{21} of TIA without protection circuit is 6.48dB. The S_{21} of TIA with π-diode is 5.43dB. The S_{21} of TIA with π-SDSCR is 6.09dB. The S_{21} of TIA with π-RTSCR is 6.03dB. The S_{21} of TIA with π-PLTSCR is 5.31dB. The ESD protection circuit does not impact the performance of TIA too much and provides sufficient ESD robustness. In the HBM test, the measurement result of TIA without protection circuit is <1kV. This level cannot match the ESD standard for commercial applications. The HBM level of TIA with traditional π-diode, π-SDSCR, π-RTSCR, and π-PLTSCR is 5kV, 6kV, 5kV and 6kV respectively. These traditional designs can provide sufficient ESD robustness and cause less signal loss. But the traditional designs should use the power clamp circuit to discharge the ESD current under PS and ND modes. The proposed π-PLTSCR ESD protection circuit can discharge ESD current under four modes (PS, PD, NS, and ND mode). Due to the absence of the power clamp, the layout area can be reduced.

Compared to the TIA without protection, the TIA with the proposed π-PLTSCR just increases the layout area about 5%.

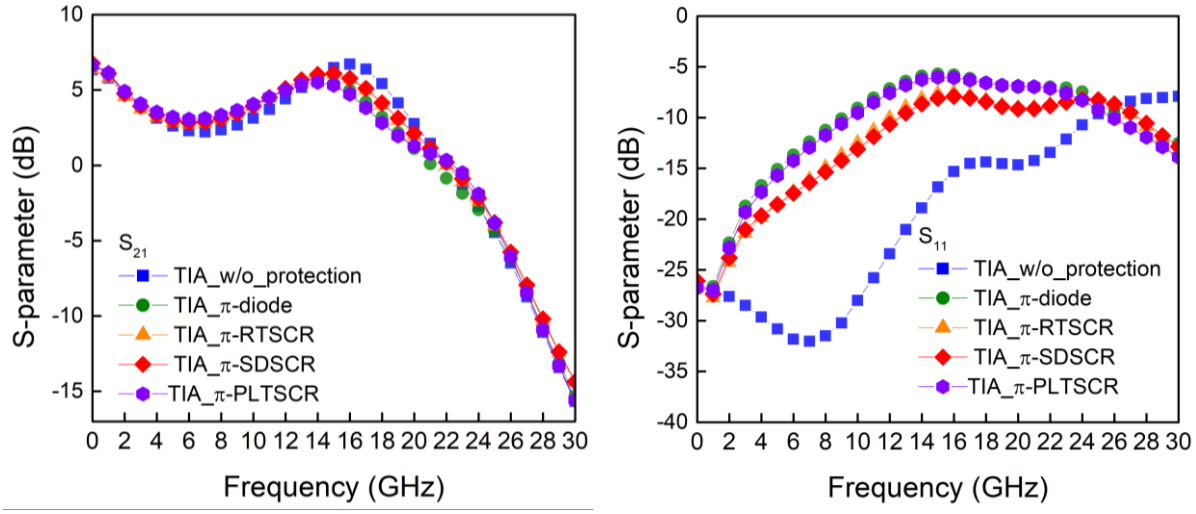


Fig. 4.30. The measured S_{21} and S_{11} of TIA with different ESD protection circuit (a) S_{21} (b) S_{11}.

From the TLP measurement result, the higher I_{t2} means the higher ESD robustness and another index $V_{clamp@1.3A}$ is measured. The lower $V_{clamp@1.3A}$ means the lower power consumption of ESD protection circuit when the ESD event occurred.

In order to compare these TIAs with different protection circuits, the FOM is defined as

$$FOM_2 = \frac{Gain}{Area * V_{clamp@1.3A}}$$

where the $V_{clamp@1.3A}$ is the highest voltage cross when the ESD current achieves 1.3A under four modes. The S_{21} is measured gain of TIA at 15GHz. The area is the area cost of the TIA with different ESD protection circuits. The HBM level is the weakest level under four mode tests. The comparison result of FOM_2 is listed in Table 4.5.

Table 4.5. Comparison table of FOM_2

Test Circuit	Area		S_{21} at 15GHz (dB)	$V_{clamp@1.3A}$ (V)	FOM_2
	ESD protection circuit (mm^2)	Total (mm^2)			
TIA with π-diode	0.054	0.588	5.43	8.48	1.08
TIA with π-SDSCR	0.057	0.591	6.09	9.99	1.03
TIA with π-RTSCR	0.056	0.587	6.03	9.39	1.09
TIA with π-PLTSCR	0.031	0.564	5.31	8.15	1.56

4.6 Summary

In this chapter, the three-stage CS TIA is equipped with four different ESD protection circuits. The simulation result is shown in section 4.3 and the measurement is also shown in section 4.4. The TIA without protection is damaged after 1kV HBM test. With the ESD protection circuit, the TIA can sustain more higher ESD voltage level but less signal loss. From the measurement result, the TIA with π-diode, π-SDSCR, π-RTSCR, and π-PLTSCR can provide 5kV, 6kV, 5kV, and 6kV ESD robustness respectively.

In this thesis, all the test circuits are fabricated in 180nm CMOS technology. From all measurement results, the proposed π-PLTSCR can provide the highest ESD robustness, save the chip area and cause less signal loss. The proposed design can suit high-speed applications and save the cost of chip fabrication.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

The first chapter of this thesis introduces the motivation behind the work, the concept of ESD, ESD test standards and specifications, and the design criteria for ESD protection circuits. In the second chapter, the parasitic effects of ESD protection circuits and prior art for high-speed ESD protection circuits are presented. To address the issue of parasitic effects, a two-stage distributed ESD protection circuit and a low parasitic capacitance protection device are utilized.

In the following chapter, the traditional π-diode, π-SDSCR, π-RTSCR, and proposed π-PLTSCR are presented. The proposed π-PLTSCR is compared with the traditional π-diode, π-SDSCR, and π-RTSCR. All the test circuits are implemented in 0.18μm CMOS technology. According to the measurement result, the proposed π-PLTSCR can provide sufficient ESD robustness of 6kV and does not distort the high-frequency performance too much. With the same size of protection device, the proposed can save the most layout area because the proposed design can discharge ESD current without power clamp circuit under PS, PD, NS, and ND modes. From the measurement result of proposed π-PLTSCR with different sizes, we can realize the ESD robustness will not increase when the size exceeds 80μm.

In chapter 4, all the π-shape ESD protection circuits are added to TIAs to provide the function of ESD protection. From the high-frequency measurement result, the proposed π-PLTSCR can provide the 6kV HBM level and distort the gain of TIA only about 1dB. Moreover, the proposed design can save the layout area from the absence of power clamp. The total area of TIA with π-PLTSCR only increases about 5%. The proposed design can be more suit for high-speed applications and save cost.

5.2 Future Work

The proposed design π-PLTSCR has been fabricated in this work. The proposed design provides a good ability of ESD protection and saves the area cost. But the proposed design still has some issues to solve. The S_{21} of π-PLTSCR is -2.28dB. It is a slightly high value. It may cause by the diode string. In the structure of SDSCR, only consists of a SCR and a metal line. The major difference between SDSCR and PLTSCR is the triggered method. The cross-section view of p-type SDSCR and PLTSCR are shown in Fig. 5.1 and Fig. 5.2. The diode string may cause the parasitic effect.

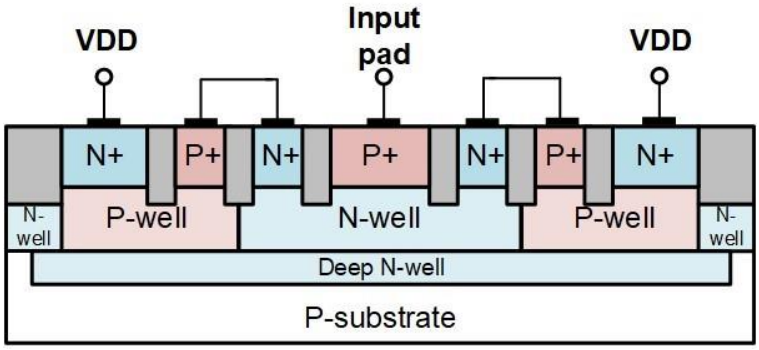


Fig. 5.1. Cross-sectional view of p-type SDSCR.

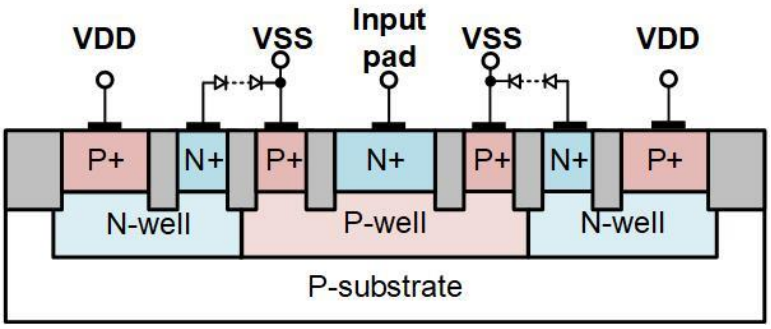
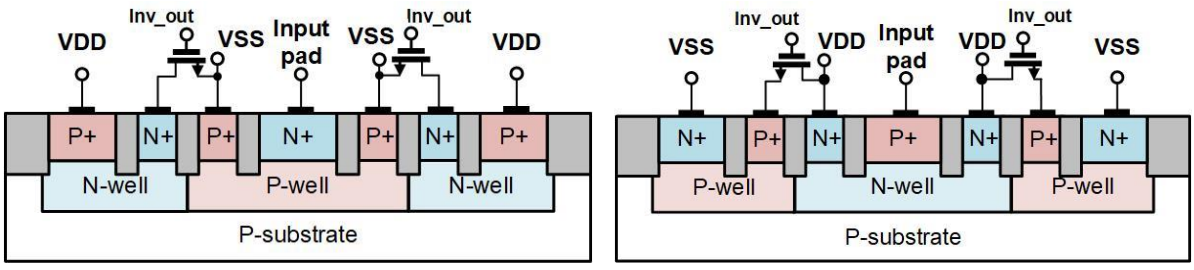


Fig. 5.2. Cross-sectional view of p-type PLTSCR.

Another method is trying to change the triggering element such as MOSFET. As shown in Fig. 5.3 (a) and (b), the cross-section view of MOS-triggered PLTSCR is illustrated. The gate of triggering MOS is connected to the of R-C inverter output. The R-C inverter control circuit is shown in Fig. 5.4. When the positive ESD event occurs, the output of R-C inverter will deliver a logic high and turn on the triggering NMOS of

PLTSCR. On the other hand, when the negative ESD event occurs, the triggering NMOS will conduct the triggering current from the parasitic diode in the NMOS structure. The triggering current can help the SCR turn on quickly like the conduction mechanism of diode string. The schematic of MOS-triggered π-PLTSCR is shown in Fig. 5.5. The discharge path of MOS-triggered π-PLTSCR under PS, PD, NS, and ND node is shown in Fig. 5.6. When ESD event occurs under PS and ND mode, the MOS-triggered π-PLTSCR will discharge the ESD current from input pad to VSS through SCR_n and SCR_p. When ESD event occurs under PD and NS mode, the MOS-triggered π-PLTSCR will discharge the ESD current from input to VDD via the embedded diode of SCR_n and SCR_p. The discharge path of MOS-triggered π-PLTSCR under VDD to VSS and VSS to VDD mode is shown in Fig. 5.7. When the positive ESD event occurs at the VDD pad and the ESD voltage exceeds the breakdown voltage of the p-n junction, the NPN BJT of SCR_n can discharge the positive ESD current from VDD. When the negative ESD event occurs at the VDD pad and the ESD voltage exceeds the breakdown voltage of the p-n junction, the PNP BJT of SCR_p can discharge the negative ESD current from VDD.



(a) (b)

Fig. 5.3. Cross-sectional view of MOS-triggered PLTSCR (a) p-type (b) n-type.

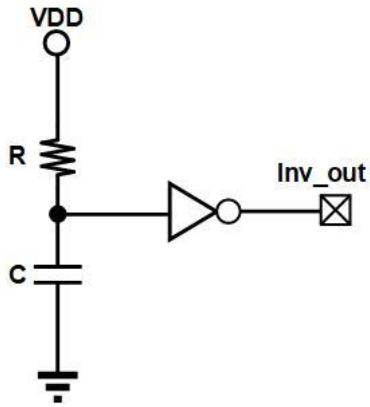


Fig. 5.4. The schematic of R-C inverter control cirucit.

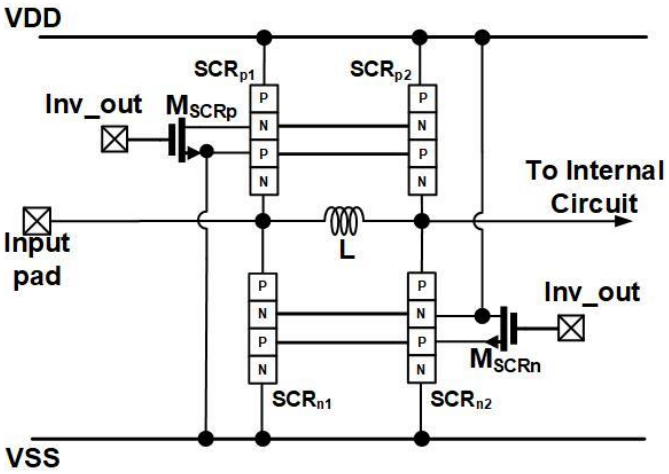


Fig. 5.5. The schematic of MOS-triggered π-PLTSCR.

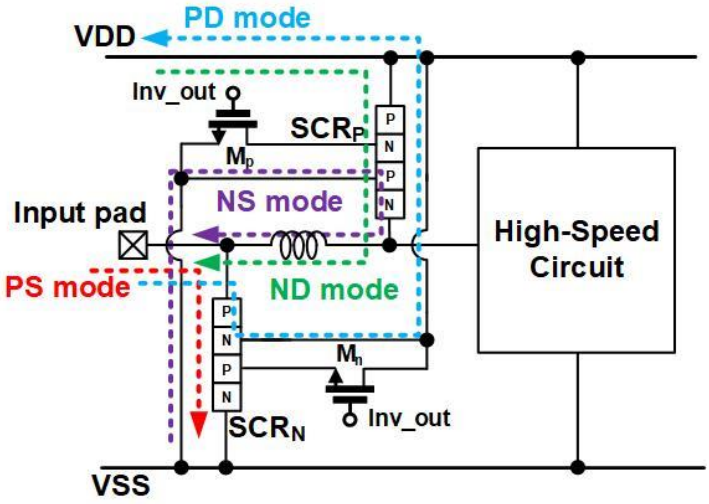


Fig. 5.6. The discharge path of MOS-triggered π-PLTSCR under PS, PD, NS, and ND mode.

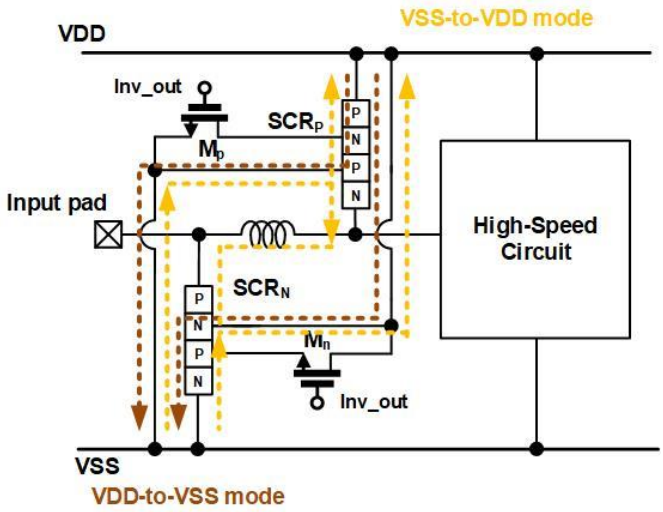
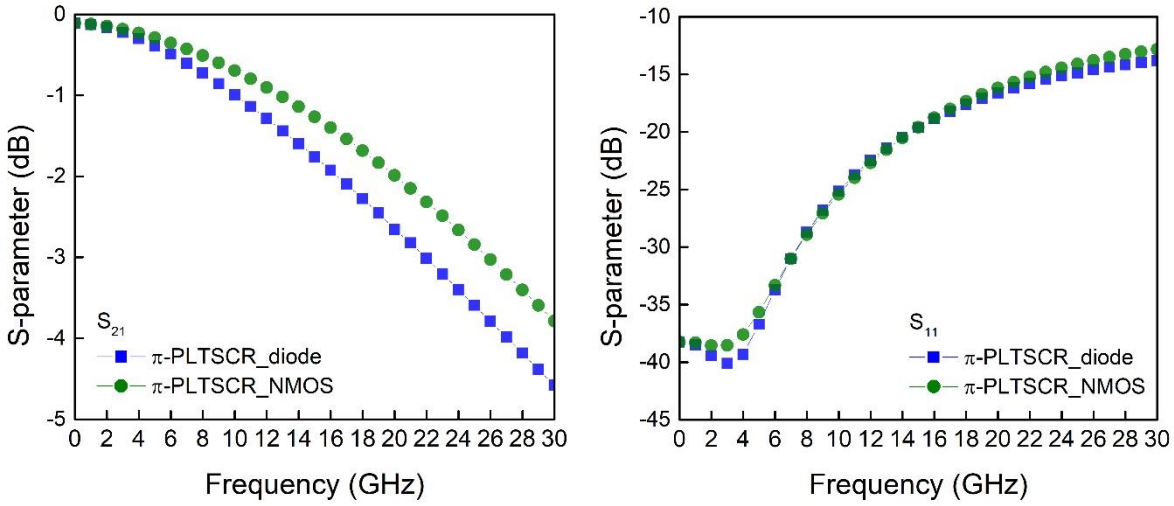


Fig. 5.7. The discharge path of MOS-triggered π-PLTSCR under VDD to VSS and VSS to VDD mode.

The simulated S_{21} and S_{11} are shown in Fig. 5.8. The S_{21} of π-PLTSCR with diode string triggering element at 20GHz is -2.63dB. In the contrast, the S_{21} of π-PLTSCR with NMOS string triggering element at 20GHz is -1.98dB. The S_{11} of π-PLTSCR with diode string triggering element at 20GHz is –16.60dB. Compared with diode string, the S_{11} of π-PLTSCR with NMOS string triggering element at 20GHz is -16.72dB. The design with NMOS string triggering element can further improve the performance of π-PLTSCR.



(a) (b)

Fig. 5.8. High-frequency simulation result of π-PLTSCR with different triggering element (a) S_{21} and (b) S_{11}.

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書報討論（二）	許陳鑑、王嘉斌
數位通訊系統	黃政吉
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半導體元件物理	劉傳璽
半導體元件物理導論（二）	駱芳鈺

Publication List

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