Nano-CMOS Circuit and Physical Design

Chapter 5 ELECTROSTATIC DISCHARGE PROTECTION DESIGN

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CHAPTER 5

ELECTROSTATIC DISCHARGE PROTECTION DESIGN

5.1 INTRODUCTION

Electrostatic discharge (ESD) protection has been implemented on integrated circuits (ICs) for more than 30 years. ESD design has faced three significant problems related to scaling processes. First, the gate oxide of the core devices has continued to shrink, reducing the oxide breakdown voltage to a level that makes it difficult to protect. This is shown in Figure 5.1, where the breakdown voltage of the thin oxide devices is less than 5 V and the operating supply may be as high as 1.5 V. The ESD protection device must operate between these two voltages, which becomes progressively more difficult to achieve as the two boundaries move closer together. A second effect has been the ever-increasing I/O speed, making large-I/O-buffer ESD devices impractical because of the high capacitive loading. A final effect is the introduction of several supply voltages, which makes the overall ESD protection scheme more complicated. Some supplies may be lightly loaded, making it difficult for the ESD protection to turn on fast enough to prevent damaging some of the devices. In this chapter, various ESD protection schemes are presented that have been implemented for several process generations and are still applicable to the 90-nm technology node and beyond.

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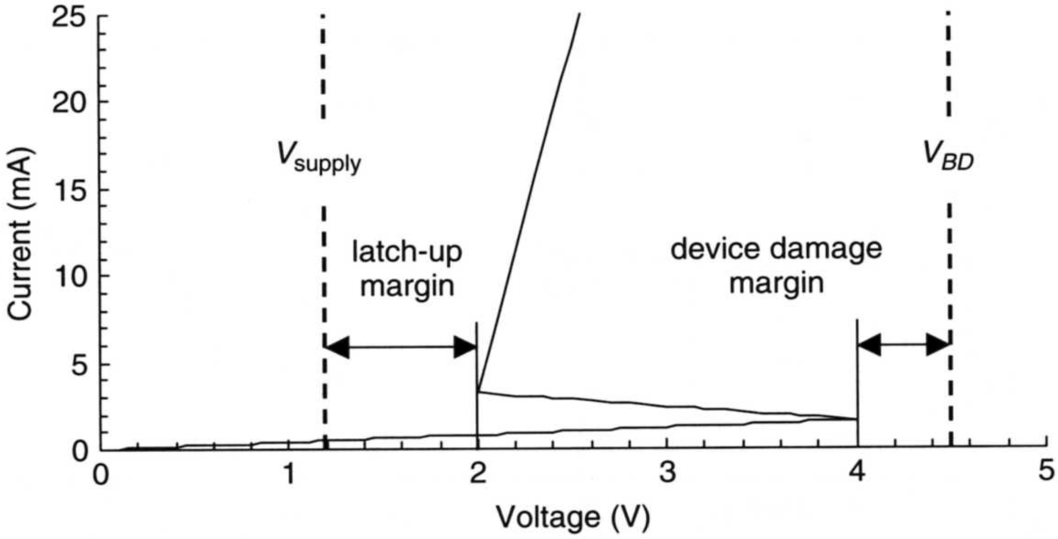


Figure 5.1 ESD protection scaling issue for deep-submicron processes.

5.2 ESD STANDARDS AND MODELS

The ESD phenomenon often happens between two or more objects with different electrostatic potentials. The ESD phenomenon is known to be a serious problem for IC products fabricated by advanced deep-submicron semiconductor process technologies. In scaled-down CMOS processes, MOS devices with shallower junction depth, thinner gate oxide, lightly doped drain (LDD) structure, and silicided diffusion have higher operating speed and lower operating power, but they become weaker to ESD stresses. Devices are usually damaged by ESD due to the rapidly generated heat or the rapidly created high electrical field. To predict the ESD immunity level or to find the ESD-sensitive (weak) point of the ICs, there are several organizations that make ESD standards. They are ESDA (Electrostatic Discharge Association), AEC (Automotive Electronics Council), EIA/JEDEC (Electronic Industries Alliance/Joint Electron Device Engineering Council), and MIL-STD (U.S. Military Standards). The dominant ESD test methods on component-level IC products are known as HBM (human body model) [1], MM (machine model) [2], and CDM (charged device model) [3].

5.3 ESD PROTECTION DESIGN

5.3.1 ESD Protection Scheme

The concept of on-chip ESD protection design, shown in Figure 5.2, is used to avoid damage from the HBM/MM ESD stresses under almost-random pin combinations. For every input or output pin, there are ESD clamp devices placed from the pad to VDD and VSS power lines to discharge the four modes of ESD stresses on the I/O pin. To overcome the ESD stresses in pin-to-pin ESD stresses and VDD-to-VSS ESD stresses, the power-rail ESD clamp circuit must be placed between the VDD and VSS power lines of the IC [4,5]. For most logic

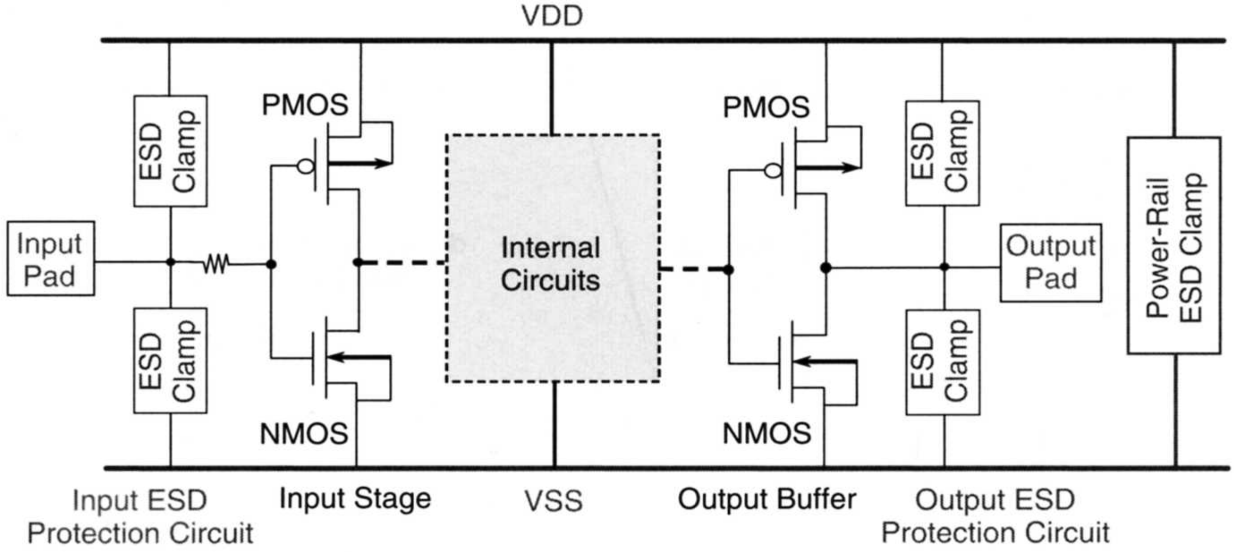


Figure 5.2 Concept of on-chip ESD protection design.

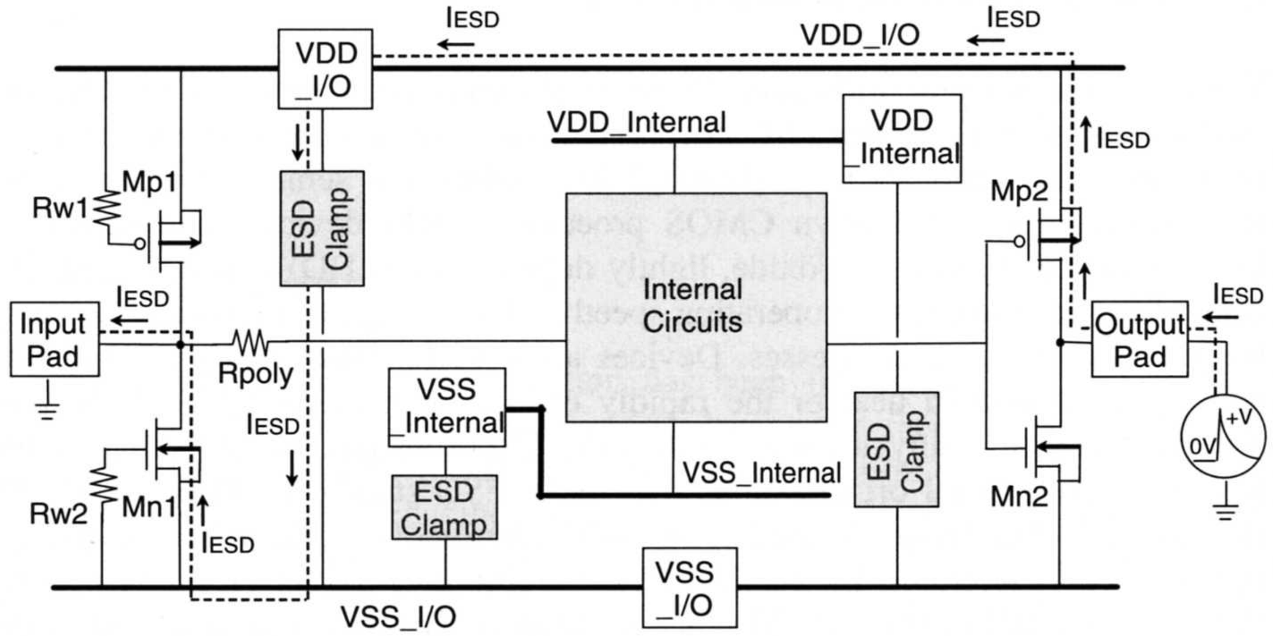


Figure 5.3 Whole-chip ESD protection scheme for an IC with separated power pins for I/O circuits and internal circuits.

ICs, the power pins for I/O circuits are often separated from the power pins of the core circuits to avoid noise coupling issues and to reduce ground bounce. With the separated power pins, the typical whole-chip ESD protection scheme is shown in Figure 5.3. Besides the ESD clamp devices at the input and output pads, the most important design to achieve whole-chip ESD protection for all devices and circuits in an IC against ESD damage (especially against pin-to-pin and VDD-to-VSS ESD stresses) is the arrangement on the power lines and the power-rail ESD clamp circuits between the separated power lines. As shown by the dashed lines in Figure 5.3, the ESD current discharging path or the IC under pin-to-pin ESD zapping can be built up by using I/O ESD devices, power metal lines, and power-rail ESD clamp circuits. Only by having a successful whole-chip

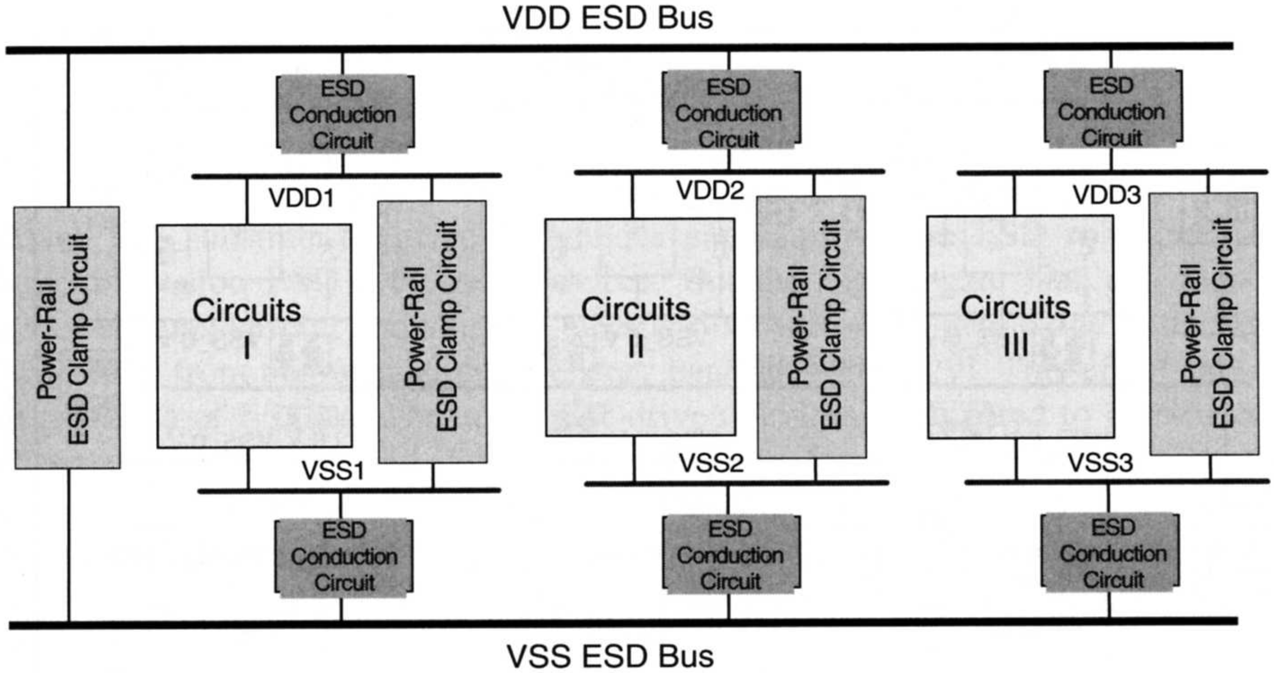


Figure 5.4 Suggested whole-chip ESD protection scheme for an IC with more separated power lines. (From Ref. 6.)

ESD protection scheme can the internal (core) circuits be protected effectively by ESD clamp devices located at the I/O pads and ESD clamp circuits located between the power rails.

Most traditional ESD protection designs were focused on ESD protection circuits or devices for I/O pins, which can provide protection against ESD stresses on an I/O pin under the four modes of pin combination. But ESD protection circuits or devices located at I/O pads cannot provide enough protection for internal circuits against pin-to-pin and VDD-to-VSS ESD stresses, which often cause an ESD failure located in the internal circuits but not on I/O ESD devices. For ICs with more independent power supplies, the whole-chip ESD protection scheme suggested is shown in Figure 5.4, which has been included in the design rules of one famous semiconductor foundry. The ESD conduction circuits between the VDD ESD bus and the separated power supplies (VDD1, VDD2, VDD3) can be realized by using stacked diodes [7] or even bidirectional silicon-controlled rectifier (SCR) devices [8,9]. For an IC [such as a system on a chip (SoC)] with more complex power supplies with different voltage levels, a whole-chip ESD protection scheme with multiple ESD buses is shown in Figure 5.5. With successful arrangement of the whole-chip ESD protection scheme, the internal circuits can still be safely protected by ESD clamp devices located at I/O pads and between the power rails.

5.3.2 Turn-on Uniformity of ESD Protection Devices

The devices that can be realized in general CMOS processes are the resistor, diode, NMOS/PMOS, field oxide device (FOD), vertical/lateral bipolar junction transistor (BJT), SCR device (p-n-p-n structure), capacitor, and inductor. ESD

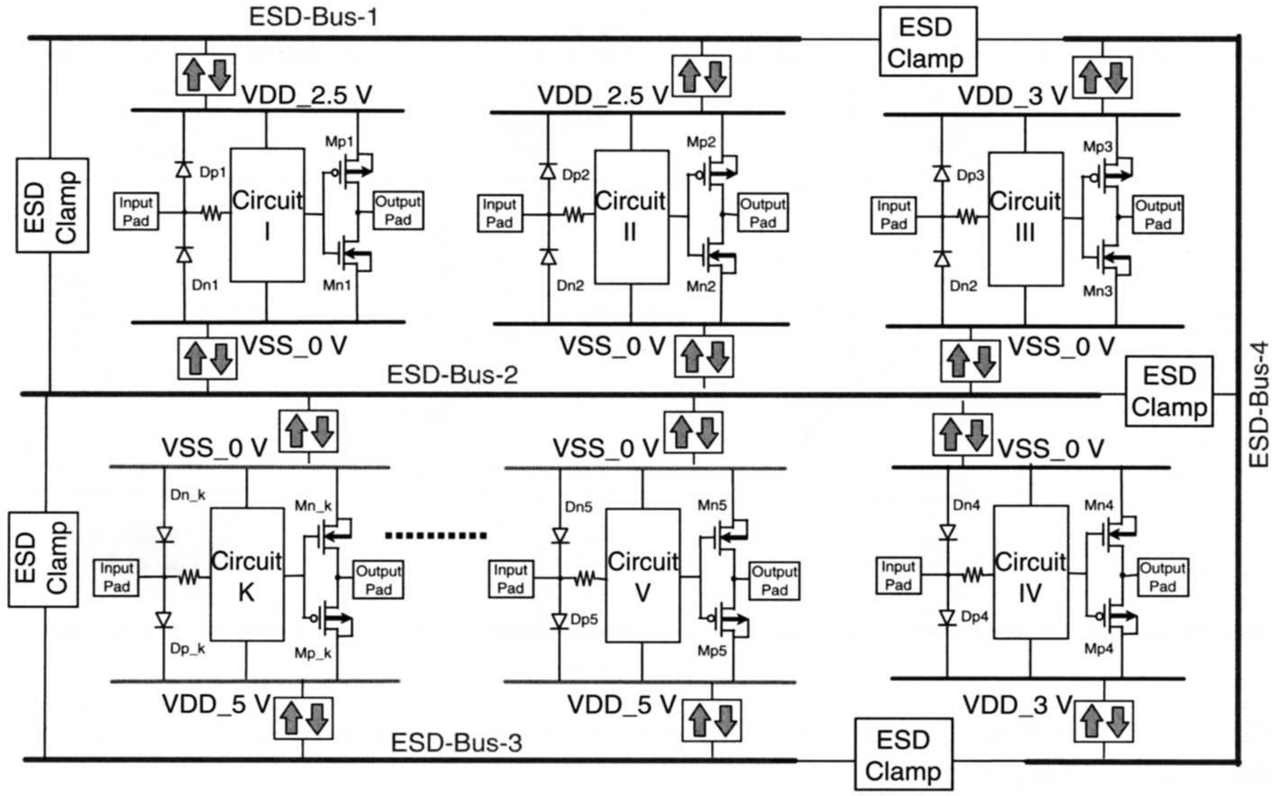


Figure 5.5 Whole-chip ESD protection scheme with multiple ESD buses for an IC with a more complex power supply configuration and different voltage levels.

clamp devices or circuits are therefore built up with those devices to sustain the ESD levels requested (such as an HBM of 2000 V, an MM of 200 V, and a CDM of 1000 V). To sustain a high-enough ESD level, the devices used in ESD clamp circuits should be drawn with a corresponding large-enough device dimension or size to sustain the ESD-induced heat without causing burnout or damage. However, the layout skill needed to draw ESD clamp devices in a reasonable silicon area to sustain a high-enough ESD level must be optimized [10–12]. Some advanced area-efficient designs for the layout of ESD clamp devices to have a high-enough ESD level within a smaller layout area had been reported in [13–16].

PMOS and NMOS devices in the output buffers are also often working as the ESD clamp devices to protect the I/O pin without adding an extra ESD clamp device to the pad. To provide enough driving current to the external load and to withstand high-enough ESD stresses, the NMOS/PMOS of output buffers are often designed with a channel width of several hundreds of micrometers. Such ESD protection devices with larger device dimensions are often realized with multiple fingers to reduce the total layout area [17]. But during ESD stress, the multiple fingers of an ESD protection MOSFET cannot be turned on uniformly. If only some MOSFET fingers are turned on, the device can be damaged by the ESD event [18]. This often causes a low ESD level in an ESD protection circuit, even if the MOSFET has large device dimensions. To improve the turn-on uniformity among multiple fingers, gate-driven design [19–22] and substrate-triggered design [24–28] were reported to increase the ESD robustness of the large-device-dimension NMOS. Recently, the ESD robustness of gate-driven NMOS has been found to decrease dramatically when the gate voltage is somewhat increased [16,22]. The gate-driven design causes large ESD current discharging through the strong-inversion channel of NMOS [29]; therefore, the NMOS device is easily burned out by ESD energy. Gate-driven and substrate-triggered techniques can improve the ESD robustness of large-dimension ESD protection devices. But the higher gate bias can induce larger channel current and a higher electric field across the gate oxide to damage MOSFETs from the explication of energy band diagrams [29]. This effect causes degradation of ESD robustness in gate-driven devices. Compared to gate-driven design, substrate-triggered design can avoid the formation of channel current and enhance the space-charge region to sustain higher ESD current far away from the channel surface. Therefore, substrate-triggered design can be one of the most effective solutions for improving the ESD robustness of CMOS devices in nanoscale-CMOS technologies [30].

5.3.3 ESD Implantation and Silicide Blocking

In addition to the layout or triggering techniques used to improve the ESD robustness of ESD clamp devices within a limited layout area, some process modifications had been developed with extra masking layers to further improve the ESD robustness of I/O. To enhance ESD robustness of these clamp devices, ESD implantations had been reported for inclusion into process flow to modify device structures for ESD protection [31–37]. N-type ESD implantation was used to cover the LDD peak structure and to make a deeper junction in NMOS devices for ESD protection [31,32]. P-type ESD implantation under the drain junction of the NMOS was used to reduce the reverse junction breakdown voltage and to turn on the parasitic lateral bipolar of the NMOS device earlier [33,34]. With higher doping concentration, P-type ESD implantation can also be used to reduce the reverse junction breakdown voltage of diode or field oxide devices and to allow the devices to sustain higher ESD stresses under reverse-biased conditions [35]. Moreover, both N- and P-type ESD implantations were used in NMOS devices to ensure higher ESD robustness [36]. Experimental comparisons among various ESD implantations for ESD protection in the same CMOS process have been made [37]. A modified design of ESD implantation for NMOS to improve, especially, MM ESD robustness has been reported [38,39].

Another process modification for improving ESD robustness of I/O devices is to use extra mask layers to block the formation of silicided diffusion in the drain regions of devices connected to an I/O pad [40–46]. A similar approach has been implemented without the additional mask layers by drawing an N-well into the drain region of NMOS to block the formation of silicided diffusion in the drain regions of I/O devices to improve ESD robustness [47,48]. Recently, a dummy gate has also been used to block formation of silicided diffusion in the drain regions of I/O devices without using an extra masking layer [49,50].

5.3.4 ESD Protection Guidelines

Some guidelines in the design of ESD clamp devices or circuits for I/O pins or power pins follow.

1. Provide the IC with an efficient ESD protection scheme to bypass any ESD stress while the IC is under ESD stress conditions.
2. Pass the normal I/O signals and keep inactive while the IC is operating under normal conditions.
3. Reduce (to the minimum possible) the input capacitance and resistance to permit acceptable I/O signal delay.
4. Have a high ESD robustness within a reasonable (as small as possible) layout area.
5. Maintain a high latch-up immunity in CMOS ICs (all the I/O devices and ESD protection devices have to be surrounded by guard rings). Fabrication of such ESD protection devices should be compatible with the process technology (without additional mask layers or modified process steps, if possible).
6. ESD circuits must not affect I/O circuit functionality during normal operation (such as high-voltage-tolerant I/O applications or power-down operations).

5.4 LOW-*C* ESD PROTECTION DESIGN FOR HIGH-SPEED I/O

5.4.1 ESD Protection for High-Speed I/O or Analog Pins

Conventional ESD protection design with a two-stage structure for a digital input pin is shown in Figure 5.6, where a gate-grounded short-channel NMOS is used as a secondary protection device to clamp the overstress voltage across the gate oxide of the input circuits. To provide a high ESD level, a robust device (such as an SCR, field oxide device, or long-channel NMOS) is used as the main discharge element in the primary protection stage to bypass ESD current on the input pad. Between the primary and secondary stages of the input ESD protection circuit, a resistor is added to limit ESD current flowing through short-channel NMOS in the secondary stage. The resistance value of this resistor depends on the turn-on voltage of the ESD clamp device in the primary stage and the secondary breakdown current of the short-channel NMOS in the secondary stage. The primary ESD clamp device must be triggered on to bypass ESD current before the gate-grounded NMOS (ggNMOS) in the secondary stage is damaged by the overstress ESD current. If the primary ESD clamp device has a high turn-on voltage, the resistance should be large enough: on the order of several hundreds of ohms. Such two-stage ESD protection design can provide a high ESD tolerance level for digital input pins. But the large series resistance and large junction capacitance in ESD clamp devices cause

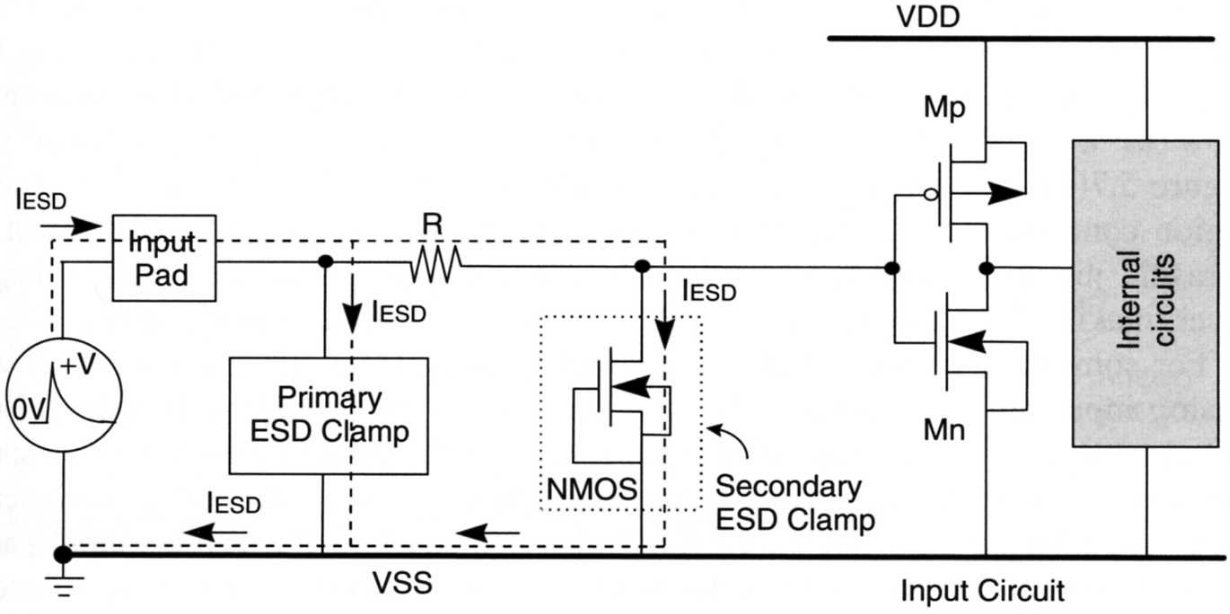


Figure 5.6 Conventional two-stage ESD protection circuit for digital input pin in CMOS ICs.

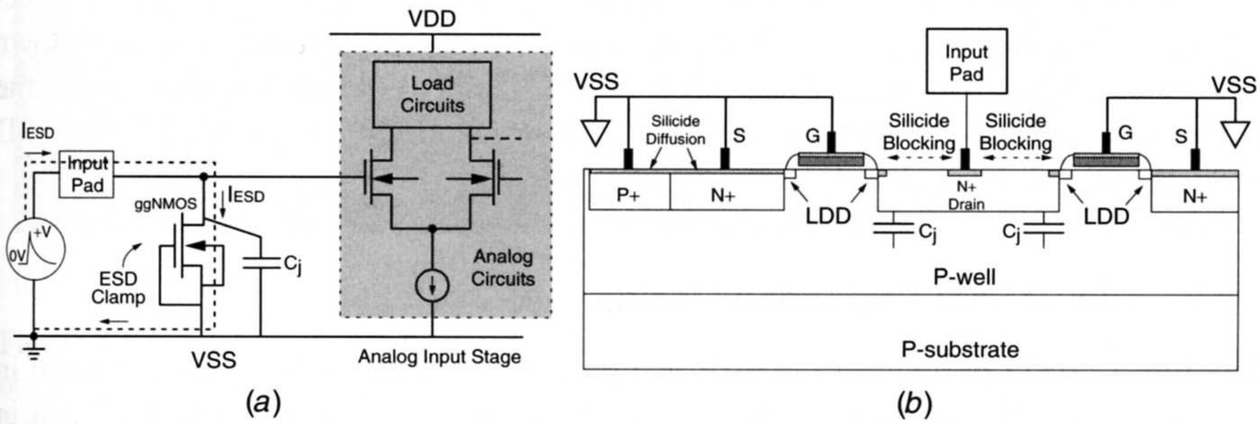


Figure 5.7 (*a*) Single-stage ESD protection circuit for an analog input pin in CMOS ICs; (*b*) cross-sectional view of a ggNMOS with a silicide-blocking drain region.

a long *RC* delay to the input signal. It is not suitable for analog signals or high-speed I/O applications, which are becoming much more prevalent in the more advanced processes.

For analog input signal or high-speed I/O applications, series resistance between the input pad and internal circuits is typically forbidden. Therefore, the two-stage ESD protection design in Figure 5.6 is no longer suitable for analog or high-speed I/O pins. To protect the analog or high-speed I/O pin, an ESD protection circuit with a single-stage ESD protection design is used, as shown in Figure 5.7(*a*), where a ggNMOS is used as the ESD clamp device. Lack of series resistance to limit ESD current toward the ggNMOS, as well as the ESD robustness of the NMOS device, seriously degrade ESD protection on advanced deep-submicron CMOS technologies [51,52]. A ggNMOS is often designed with large device dimensions and wide drain-contact-to-poly-gate layout spacing to sustain an acceptable ESD level [16,52,53]. The additional silicide-blocking masks [40–44] have been included in the deep-submicron CMOS process to increase the robustness of the ESD clamp device. A schematic cross-sectional view of a ggNMOS with a silicide-blocking drain region is illustrated in Figure 5.7(*b*). But a ggNMOS with larger device dimensions and a wider drain region contributes a larger parasitic drain capacitance to the input pad. Such a parasitic junction capacitance is nonlinear and dependent on the input voltage level, making it unacceptable for truly high-speed I/O and analog inputs.

For some high-resolution data converter circuits, the input capacitance of an analog input pin is required to be kept as constant as possible within the input voltage range. A major source of distortion in high-speed analog circuits, especially in single-ended input implementations, is the voltage-dependent nonlinear input capacitance associated with ESD clamp devices at the analog input pad. Typical degradation on circuit performance due to the nonlinear input capacitance of the input ESD clamp devices has been reported in Ref. 65, where the input capacitance varies from 4 to 2 pF due to the input voltage swing from 0 to 2 V. This capacitance variation caused an increase in harmonic distortion in an analog-to-digital converter (ADC) and therefore degraded the precision of the ADC from 14 bits to 10 bits. Thus, it has been an emerging challenge to design an effective ESD protection circuit for high-precision analog applications in scaled-down CMOS technologies. In Section 5.4.2, low-*C* ESD protection design, with the advantages of small input capacitance, no series resistance, and a high ESD level, is described in detail.

5.4.2 Low-*C* ESD Protection Design

The low-*C* ESD protection circuit for high-speed I/O or analog pins is shown in Figure 5.8(*a*). The corresponding layout of this low-*C* ESD protection circuit in a 0.35-μm silicided CMOS cell library is shown in Figure 5.8(*b*) for reference. In Figure 5.8(*a*), the Dp1 (Dn1) is the parasitic junction diode in the drain region of an Mp1 (Mn1) device. To reduce the input capacitance of a high-speed I/O or analog pin, Mn1 and Mp1 are both designed with much smaller device dimensions (W/L): only 50/0.5 (μm/μm). The HBM ESD level of a stand-alone NMOS with a device dimension of 50/0.5 (μm/μm) is less than 500 V in the typical 0.35-μm silicided CMOS process when an NMOS is zapped in PS-mode ESD stress. But such a small NMOS can sustain an HBM ESD level of 8000 V in the same 0.35-μm silicided CMOS process, while the NMOS is zapped in NS-mode ESD stress. In PS-mode (NS-mode) ESD stress, NMOS is operated in its drain-breakdown condition (drain diode forward-bias condition) to bypass ESD current. The power dissipation located on the ESD clamp device is equal to the product of ESD current and the operating voltage of the device during ESD events. Therefore, an NMOS has a significantly different ESD stress level between PS and NS modes. Similarly, a stand-alone PMOS with a small device dimension also has a high ESD stress level in the PD mode but a much lower ESD stress level in ND-mode ESD stress.

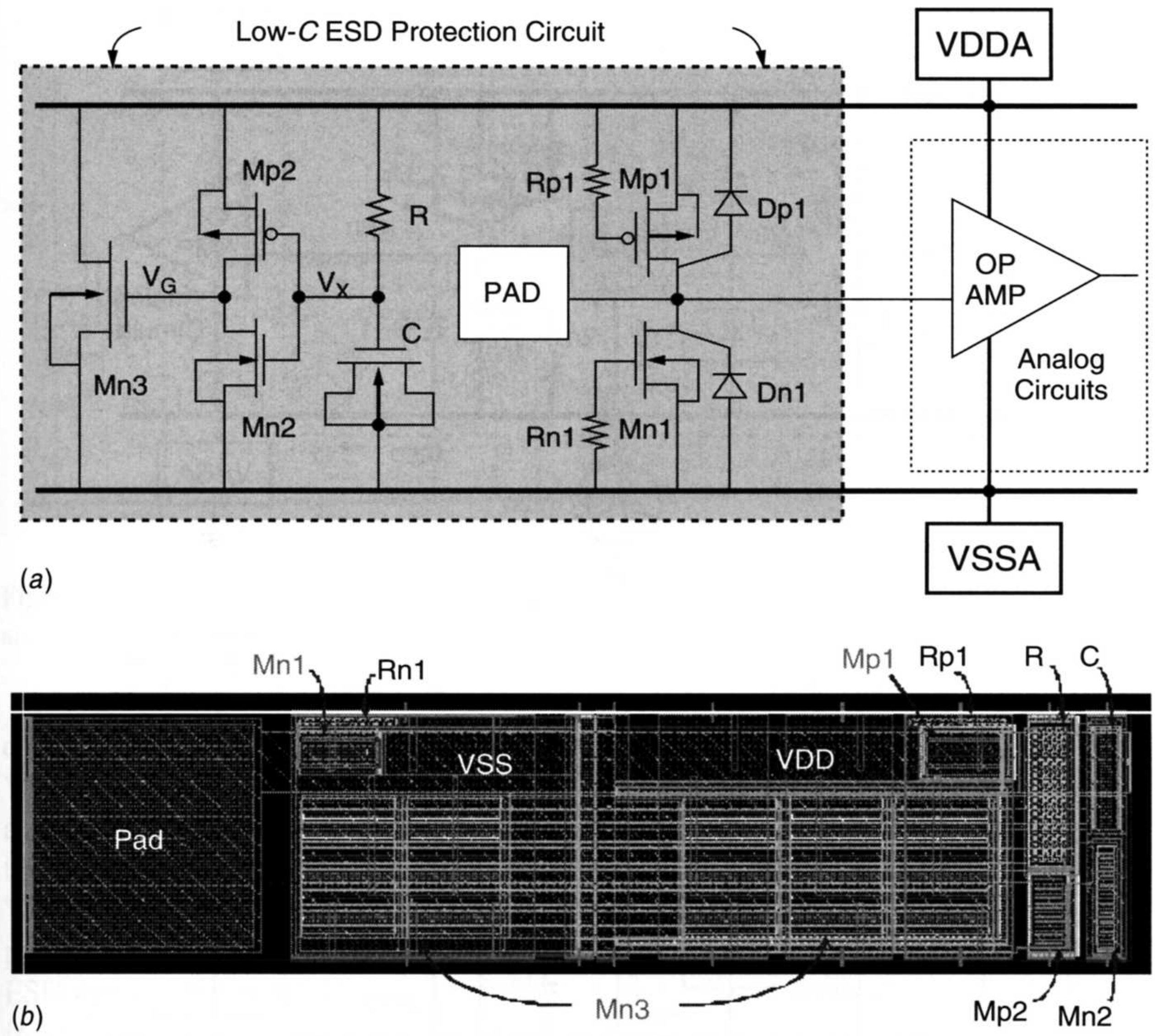


Figure 5.8 (*a*) Low-*C* ESD protection circuit for high-speed I/O or analog pins; (*b*) layout example of a low-*C* ESD protection circuit for high-speed I/O or analog pins in a 0.35-μm silicided CMOS process. [Part (*a*) from Ref. 55.].

To avoid the small-dimension Mn1 and Mp1 going into the drain-breakdown condition during PS- and ND-mode ESD stresses, an efficient ESD clamp circuit between the power rails is co-constructed into an analog ESD protection circuit to increase the overall ESD protection level. In Figure 5.8(*a*), the *RC*-based ESD detection circuit [5] is used to trigger on the Mn3 device when the pad is zapped in PS- or ND-mode ESD stresses. The ESD current paths in this analog ESD protection circuit are illustrated by the dashed lines in Figure 5.9(*a*) and

different voltage level. But the input capacitance of this low-C ESD protection circuit [Figure 5.8(a)] with a complementary PMOS and NMOS structure can be kept almost constant even if the input signal has a voltage swing from 0 V to V_{dd} (3 V). The total input junction capacitance of the low-C ESD protection circuit with different device dimensions are accurately calculated in the frequency domain by using pin-capacitance-measurement simulation [56] in the STAR-HSPICE CAD tool.

The simulated results are shown in Figure 5.11, where the channel widths of Mn1 and Mp1 vary from 50 to 400 μm with a fixed channel length of 0.5 μm under different voltage levels on the input pad. The drain-contact-to-poly-gate spacing in both Mn1 and Mp1 is drawn as 3.4 μm, whereas the source-side spacing is drawn as 1.55 μm. With device dimensions of 50/0.5 (μm/μm) in both Mn1 and Mp1, the input capacitance of the low-C ESD protection circuit is varying from 0.37 to 0.4 pF for an input voltage swing of 0 to 3 V. But the input capacitance of the traditional ESD protection circuit in Figure 5.7(a) with a ggNMOS of $W/L = 400/0.5$ (μm/μm) varies from 1.83 to 1.12 pF for an input voltage swing of 0 to 3 V.

The layout size of the metal bond pad for wire bonding in the 0.35-μm CMOS process is specified as $96 \times 96\ \mu m^2$, which contributes a parasitic C_{pad} value of 0.67 pF. So the total input capacitance of this low-C ESD protection circuit, including the bond pad, is only about 1.04 to 1.07 pF, even if the input signal has a voltage swing from 0 to 3 V. With such a small and almost constant

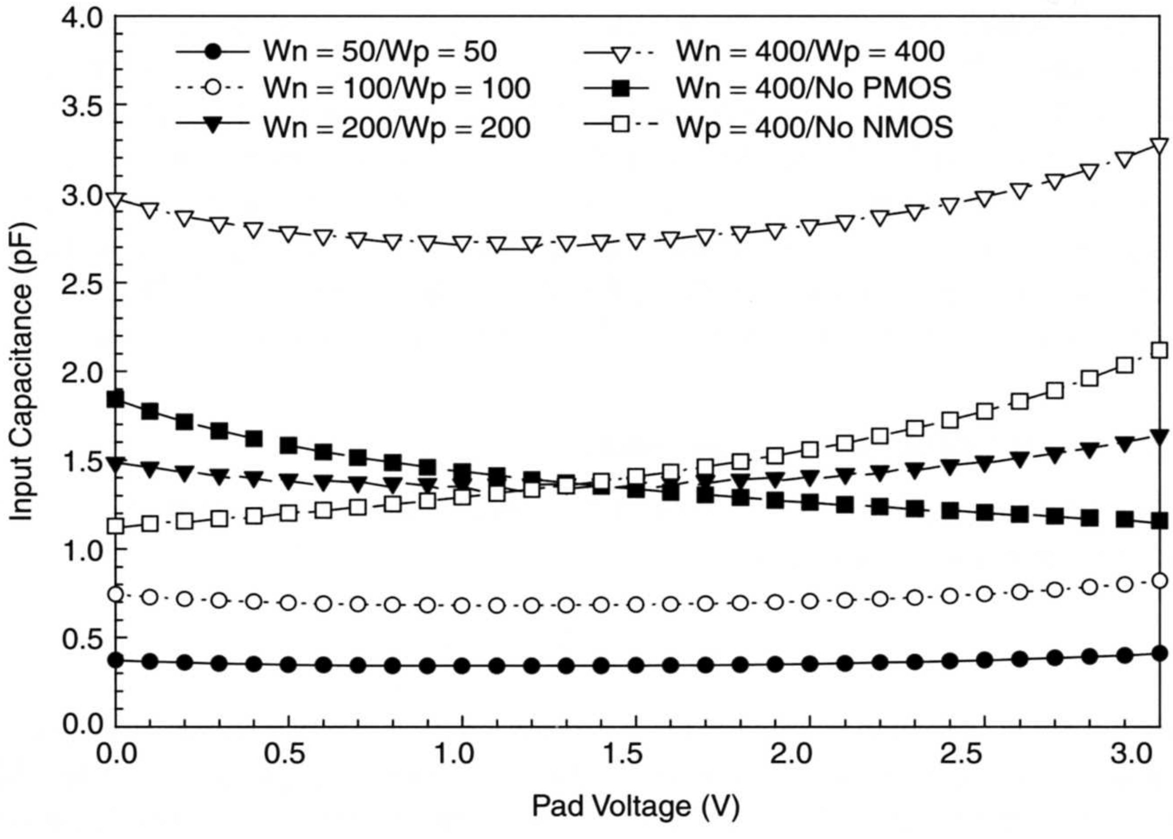


Figure 5.11 Input junction capacitance of the low-C ESD protection circuit with different device dimensions in Mn1 and Mp1 during different input voltage levels on the pad.

input capacitance, this low-C analog ESD protection circuit is more suitable for high-precision and high-speed I/O applications in both analog and digital pins. To further reduce the parasitic capacitance generated from the bond pad, low-C bond pad structures have been developed [57]. An additional reduction in the capacitance can be achieved by adding diodes between the ESD devices (Mn1 and Mp1) and the input pad. Polysilicon diodes with a stacked configuration have been developed in a 0.25-μm CMOS process to protect the RF input pin of a RF low-noise amplifier (LNA) operating at 2.4 GHz [58].

The main nonlinear source in the input capacitance is the bias-dependent junction capacitance at the drain regions of Mn1 and Mp1 of the low-C ESD protection circuit shown in Figure 5.5(a). When the input signal at the input pad has an increasing voltage, the drain junction capacitance of Mn1 decreases but the drain junction capacitance of Mp1 increases. On the contrary, the drain junction capacitance of Mn1 increases but the drain junction capacitance of Mp1 decreases when the input signal at the input pad has a decreasing voltage. From the complementary structure of this low-C ESD protection circuit, the input capacitance can be kept almost constant if suitable layout dimensions and spacings are selected to draw the Mn1 and Mp1 devices. A design model to optimize the layout dimensions and spacing of ESD clamp devices had been developed to keep the input capacitance almost constant for this low-C ESD protection circuit [70]. Variation on the total input capacitance of this low-C ESD protection circuit can be designed below 1%. The absolute error must be determined by considering the difference in the doping densities of NMOS and PMOS devices. Mismatches between assumed and actual doping densities will result in an increase in capacitance nonlinearity.

5.4.4 ESD Robustness

The low-C ESD protection circuit has been practically fabricated in a 0.35-μm silicided CMOS process with an operational amplifier as its input circuit. In this test chip, both the inverting and noninverting input pins are protected by the analog ESD protection circuit proposed. The silicide-blocking mask is also used on the device's Mn1, Mp1, and Mn3 to improve their ESD robustness, but without using the extra ESD implantation process modification.

The fabricated analog ESD protection circuits are zapped by an ESD simulator in both the HBM (human-body model) and MM (machine model) ESD stresses. The ESD test results of the maximum sustaining voltage are summarized in Table 5.1 which includes the analog pin-to-pin ESD stress. The failure criterion is defined as leakage current at the pad that exceeds 1 μA under 5-V voltage bias after any ESD zapping. As shown in Table 5.1, the low-C ESD protection circuit can successfully provide the analog pins with an HBM (MM) ESD level above 6000 V (400 V) in all ESD stress conditions but without adding a series resistor between the pad and the internal circuits.

The conventional ESD protection design shown in Figure 5.7(a) with a ggNMOS of $W/L = 480/0.5$ (μm/μm) for an analog input pin is also fabricated in

TABLE 5.1 ESD Level of a Low-*C* ESD Protection Circuit in HBM and MM ESD Testing

	Pin Combination in ESD Test				
	PS Mode	NS Mode	PD Mode	ND Mode	Pin-to-Pin
HBM (V)	6000	−8000	7000	−7000	6000
MM (V)	400	−400	400	−400	400

the same test chip as a reference. The HBM PS-mode ESD level of the design in Figure 5.7(*a*) is about 3 kV, but its analog pin-to-pin HBM ESD level is below 500 V. The pin-to-pin ESD damage location is founded on the poly gate of the first input stage in the operational amplifier circuit. So the conventional ESD protection design cannot protect the thinner gate oxide of the differential input stage in deep-submicron CMOS technologies during pin-to-pin ESD stress.

Although this test structure has been fabricated on a 0.35-μm process, it is still applicable to more advanced processes. The primary difference will be the physical device sizes necessary to match the diffusion capacitance of the NMOS and PMOS devices.

5.4.5 Turn-on Verification

To verify the turn-on efficiency of the low-*C* ESD protection circuit during pin-to-pin ESD stress, a square-wave voltage pulse generated from a pulse generator (HP 8118A) is applied to the inverting pin of an operational amplifier, while the noninverting pin of the operational amplifier is grounded and both the VDDA and VSSA pins are floating. The experimental setup to verify the turn-on efficiency in the positive and negative pin-to-pin ESD stress conditions is shown in Figure 5.12(*a*) and (*b*), respectively.

The measured voltage waveforms in positive pin-to-pin ESD stress conditions are shown in Figure 5.13(*a*) and (*b*). The voltage waveform in Figure 5.13(*a*) is the original voltage pulse generated from a HP 8118A pulse generator with a pulse height of 8 V and a pulse width of 200 ns. The 8-V voltage pulse has a rise time of about 10 ns, which is similar to the rise time of an HBM ESD pulse. The drain breakdown voltage of the NMOS Mn1 in the 0.35-μm silicide CMOS process without an extra ESD implantation process modification is about 8.5 V. Therefore, the voltage pulse with a pulse height of 8 V does not cause the drain breakdown in Mn1 in an analog ESD protection circuit. By applying such a voltage pulse to the analog pin, the turn-on efficiency of the proposed analog ESD protection circuit can be practically verified. Although this positive voltage pulse is applied to the input pin as shown in Figure 5.12(*a*), the low-*C* ESD protection circuit clamps it, and the degraded voltage waveform is shown in Figure 5.13(*b*). The voltage waveforms in the negative pin-to-pin ESD stress condition are also measured and shown in Figure 5.14(*a*) and (*b*).

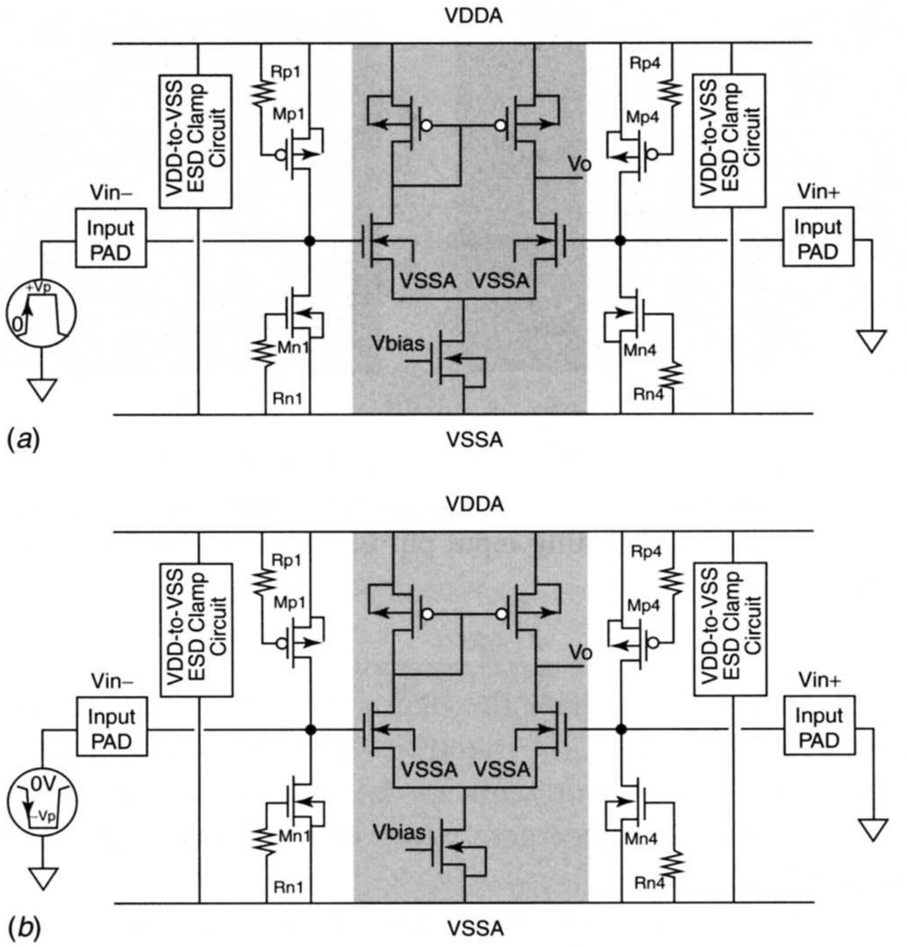


Figure 5.12 Experimental setup to verify the turn-on efficiency of the low-*C* ESD protection circuit during (*a*) positive and (*b*) negative pin-to-pin ESD stress conditions.

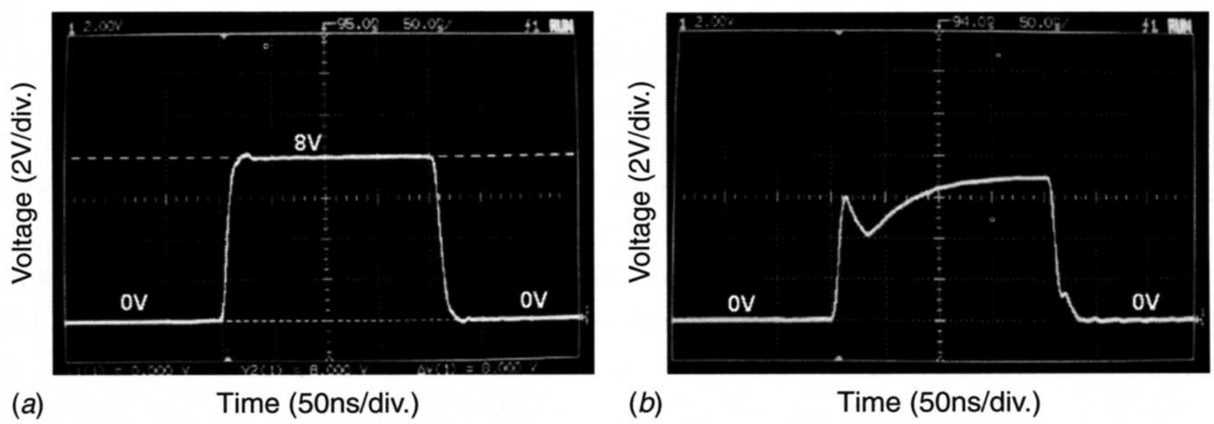


Figure 5.13 (*a*) Measured voltage waveform of the original 8-V voltage pulse generated from a pulse generator; (*b*) degraded voltage waveform when the 8-V voltage pulse is applied to the analog inverting input pin in the pin-to-pin stress condition shown in Figure 5.12(*a*).

The voltage waveform in Figure 5.14(*a*) is the original negative voltage pulse generated from the pulse generator with a pulse height of −8 V and a pulse width of 200 ns. When this negative voltage pulse is applied to the input pin as shown in Figure 5.12(*b*), it is clamped by the analog ESD protection circuit to a

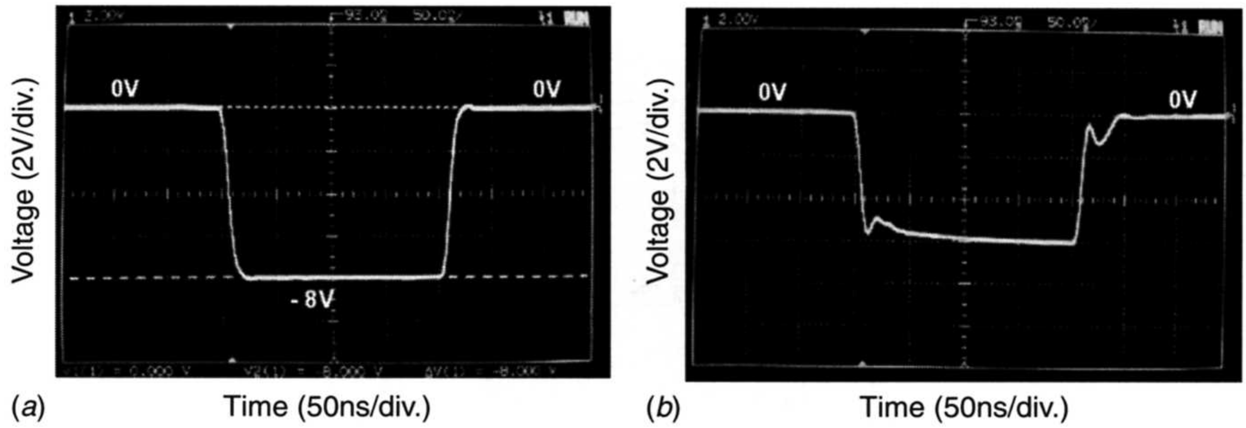


Figure 5.14 (*a*) Measured voltage waveform of the original negative (−8 V) voltage pulse generated from a pulse generator; (*b*) degraded voltage waveform when the voltage pulse is applied to an analog inverting input pin in the pin-to-pin stress condition shown in Figure 5.12(*b*).

voltage level of only −5 V, where the degraded voltage waveform is shown in Figure 5.14(*b*). From Figures 5.13(*b*) and 5.14(*b*), the voltage pulses are actually clamped by the low-*C* ESD protection circuit during the pin-to-pin ESD stress conditions. Therefore, the thinner gate oxide of the input stage can be protected during pin-to-pin ESD stress.

The turn-on efficiency of the low-*C* ESD protection circuit during PS- and ND-mode ESD stresses are also verified. The experimental setups are shown in Figure 5.15(*a*) and (*b*) for the PS and ND modes, respectively. When a positive voltage pulse with a voltage level of 8 V [shown in Figure 5.15(*a*)] is applied to the input pin in the PS-mode condition, the low-*C* ESD protection circuit clamps the positive voltage pulse and the degraded voltage waveform on the pad is as shown in Figure 5.16(*a*). While the negative voltage pulse shown in Figure 5.15(*b*) is applied to the input pin in the ND-mode condition, the negative (−8 V) voltage pulse is clamped by the low-*C* ESD protection circuit and the degraded voltage waveform on the pad is as shown in Figure 5.16(*b*). This has practically verified the turn-on efficiency of the low-*C* ESD protection circuit.

From the experimental verification above, positive or negative voltage pulses are clamped by the low-*C* ESD protection circuit through the VDD-to-VSS ESD clamp device Mn3. Mn1 and Mp1 in the low-*C* ESD protection circuit are operated in the junction diode forward-based condition rather than the drain-breakdown condition; therefore, the proposed analog ESD protection circuit can sustain a much higher ESD level even though the Mn1 and Mp1 devices have much smaller dimensions than those of traditional protection devices. This low-*C* ESD protection circuit without the series resistance between the pad and the internal circuits can safely protect the thinner gate oxide of the input stage. With much smaller device dimensions in Mn1 and Mp1, the total input junction capacitance connected to the pad can be reduced for high-frequency analog I/O or high-speed digital I/O applications.

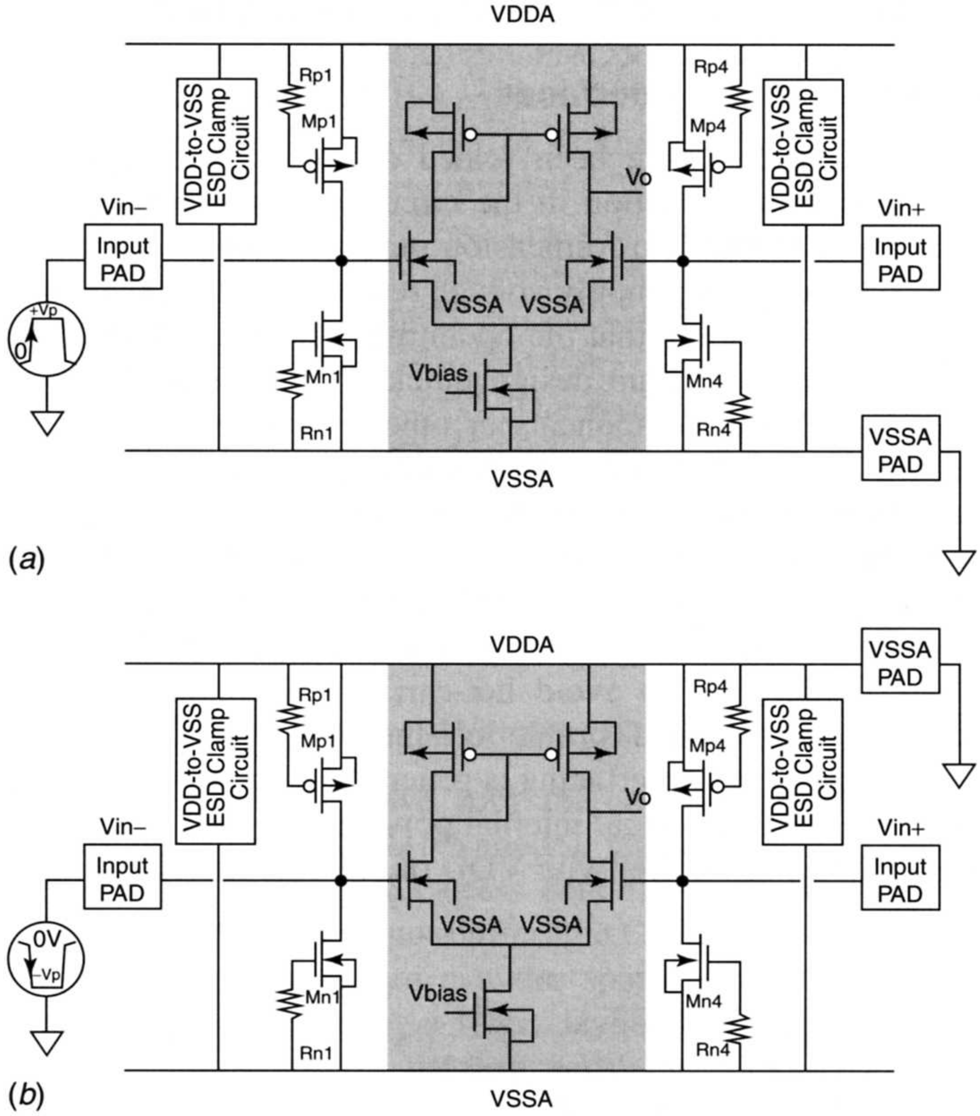


Figure 5.15 Experimental setup to verify the turn-on efficiency of the low-*C* ESD protection circuit during (*a*) PS- and (*b*) ND-mode ESD stress.

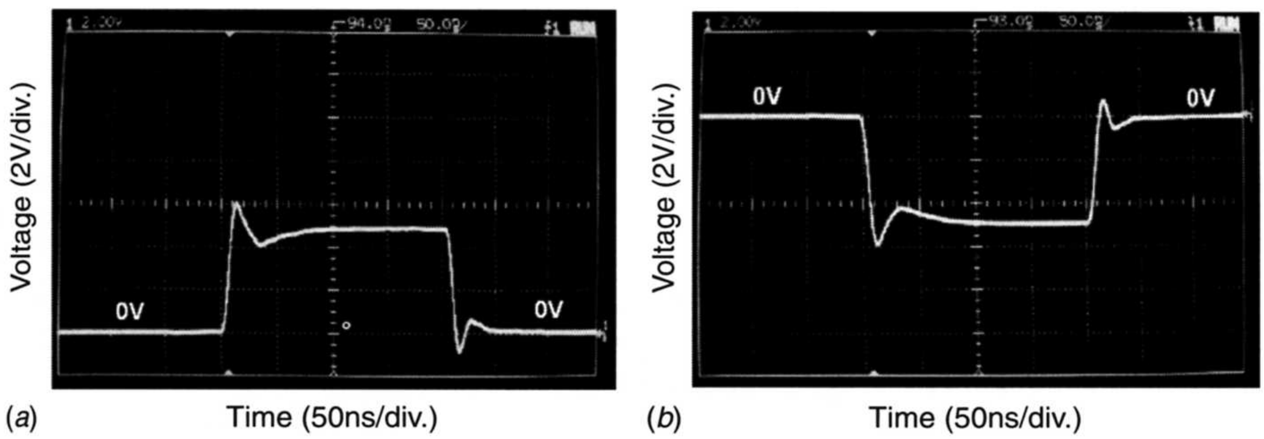


Figure 5.16 (*a*) Degraded voltage waveform when a positive 8-V voltage pulse is applied to the input pin in the PS-mode ESD stress condition; (*b*) degraded voltage waveform when a negative −8-V voltage pulse is applied to the input pin in the ND-mode ESD stress condition.

5.5 ESD PROTECTION DESIGN FOR MIXED-VOLTAGE I/O

5.5.1 Mixed-Voltage I/O Interfaces

The transistor dimensions have been scaled down into the nanometer region, resulting in a significant reduction in the circuit power supply voltage as well. Obviously, the smaller transistor dimension makes the chip area smaller, saving silicon cost. The lower power supply voltage results in lower power consumption (or reduced increase assuming that the operating increases). With the advance of modern CMOS technology, chip design quickly migrates to the lower voltage level, but some peripheral components or other ICs are still operated at higher voltage levels (3.3 or 5 V). In other words, chips with different supply voltages coexist in a system. Because of this mixture of supply voltages, most microelectronic systems require interfacing of semiconductor chips or subsystems with different internal power supply voltages. With the mix of power supply voltages, chip-to-chip interface I/O circuits must be designed to avoid electrical overstress across the gate oxide [60], to avoid hot-carrier degradation [61] on the output devices, and to prevent undesirable leakage current paths between the chips [62,63]. For example, 3.3-V interfacing is generally required for ICs implemented in CMOS processes with a normal internal power supply voltage of 1.0 or 1.5 V. The traditional CMOS I/O buffer with VDD of 3.3 V is shown in Figure 5.17(*a*),

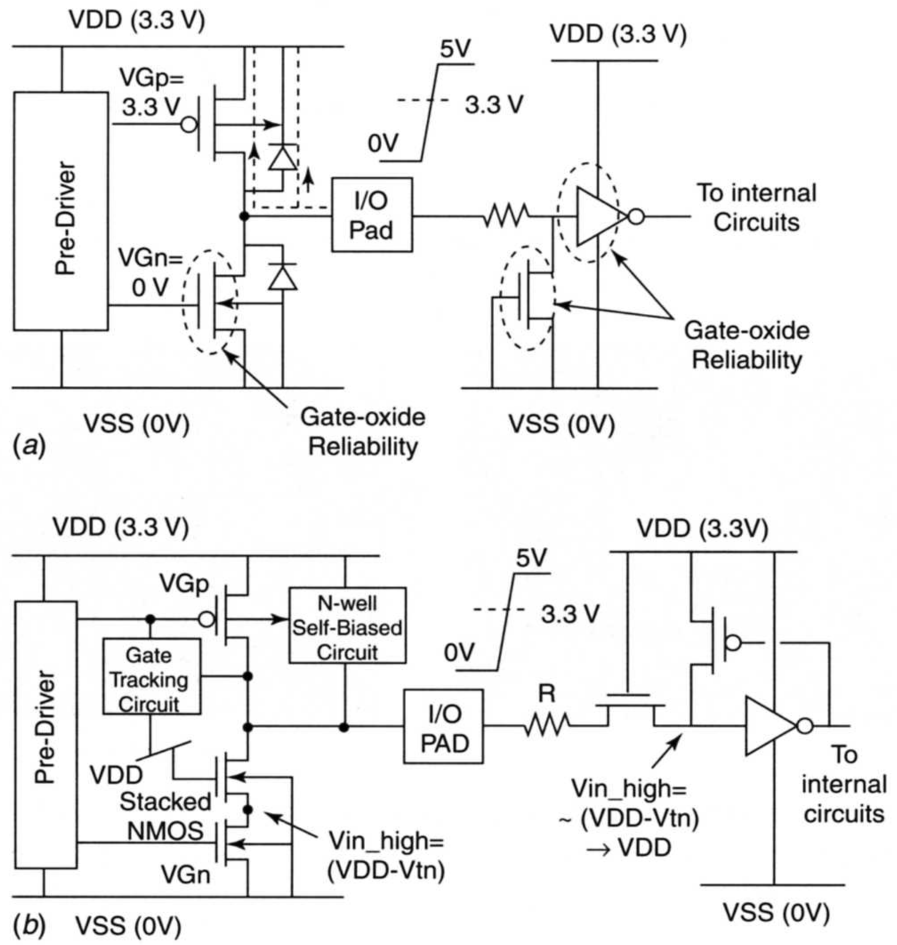


Figure 5.17 Typical circuit diagram for (*a*) a traditional CMOS I/O buffer and (*b*) a mixed-voltage I/O buffer with stacked NMOS and the self-biased-well PMOS.

where there is an output stage and an input stage. When a 5-V signal is applied to the I/O pad, the channel of the output PMOS and the parasitic drain-to-well junction diode in the output PMOS generate leakage current paths from the I/O pad to VDD [the dashed lines shown in Figure 5.17(*a*)]. Moreover, the gate oxides of the output NMOS, gate-grounded NMOS for input ESD protection, and input inverter stage are overstressed by the 5-V input signal. To solve the gate oxide reliability issue without using the additional thick gate oxide process (called dual-gate oxide in some CMOS processes [64,65]), the stacked-MOS configuration had been widely used in mixed-voltage I/O buffers [66–72] or even in power-rail ESD clamp circuits [73]. The basic circuit diagram of a typical 3 V/5 V-tolerant mixed-voltage I/O circuit is shown in Figure 5.17(*b*) [67]. The pull-up PMOS, connected from the I/O pad to VDD power line, has self-biased circuits for tracking its gate and n-well voltages, when the 5-V input signals enter the I/O pad. A detailed diagram of a circuit that implements the gate-tracking function and the n-well self-biased circuit block is shown in [72].

5.5.2 ESD Concerns for Mixed-Voltage I/O Interfaces

ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS mode), negative-to-VSS (NS mode), positive-to-VDD (PD mode), and negative-to-VDD (ND mode) ESD stress conditions. To have sufficiently high ESD robustness of the CMOS output buffer, the CMOS buffer is generally drawn with larger device dimensions and a wider spacing from the drain contact to the poly gate, which often occupy a larger layout area in the I/O cell. Without increasing device dimensions in the I/O cells, the VDD-to-VSS ESD clamp circuits across the power lines of CMOS ICs had been used successfully to improve ESD robustness of CMOS I/O buffers [55]. The ESD current paths for a traditional CMOS output buffer under the positive-to-VSS ESD stress condition is illustrated by the dashed lines in Figure 5.18(*a*), where most ESD current is

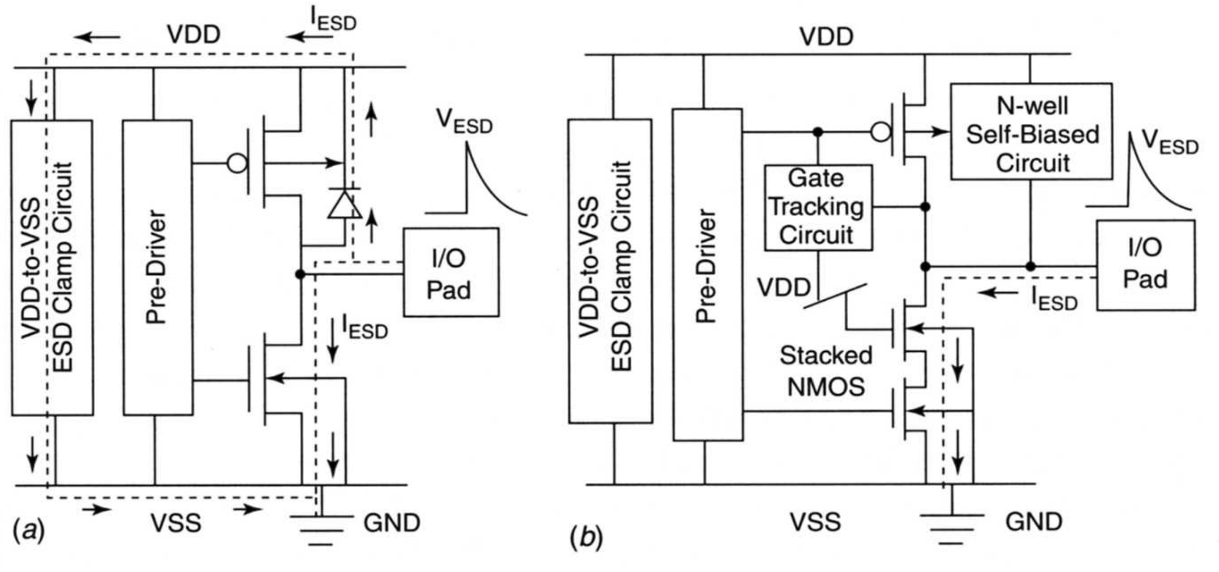


Figure 5.18 ESD current paths along (*a*) a traditional CMOS output buffer and (*b*) a mixed-voltage output buffer, under positive-to-VSS ESD stress conditions.

discharged through the parasitic diode of PMOS and the VDD-to-VSS ESD camp circuit to ground. Therefore, the traditional CMOS output buffer can sustain a high ESD stress. But due to the leakage current issue in the mixed-voltage I/O buffer, there is no any parasitic diode connected from the I/O pad to the VDD power line. Because of the limitation of placing a diode from the pad to VDD in mixed-voltage I/O circuits, the positive-to-VSS ESD voltage zapping on the I/O pad cannot be diverted from the pad to the VDD power line, and cannot be discharged through the additional power-rail (VDD-to-VSS) ESD clamp circuit. Such positive-to-VSS ESD current on the I/O pad is totally discharged through the stacked NMOS in the snapback breakdown condition. The ESD current under this positive-to-VSS ESD stress condition along the mixed-voltage output buffer is shown by the dashed line in Figure 5.18(*b*). The NMOS devices in a stacked configuration have a higher trigger voltage (V_{t1}), a higher snapback holding voltage (V_{sb}), and a lower secondary breakdown current (I_{t2}) than that of the single NMOS [74]. Therefore, such mixed-voltage I/O circuits with stacked NMOS often have a much lower ESD level than that of I/O circuits with a single NMOS [74,75]. So the mixed-voltage I/O circuit often has the lowest ESD level (often <2 kV in the human-body-model ESD test) under a positive-to-VSS ESD stress condition. Without the parasitic diode connected from the I/O pad to the VDD power line, the mixed-voltage I/O circuit also has a lower ESD level under a positive-to-VDD ESD stress condition. Therefore, ESD protection design on the mixed-voltage I/O circuits is mainly focused to improve the ESD level under positive ESD stress conditions.

To increase the ESD level of such mixed-voltage I/O circuits, some designs with extra multiple diodes in stacked configuration had been added from the I/O pad to the VDD power line [63,64]. However, while mixed-voltage I/O circuits are operating in a high-temperature environment with a high-voltage input, the forward-biased leakage current from the pad to V_{DD} through the stacked diodes must be reduced by additional circuit designs [76–79].

5.5.3 ESD Protection Device for a Mixed-Voltage I/O Interface

In this section, a new ESD protection design is presented to improve the ESD robustness of mixed-voltage I/O buffers significantly by using a stacked-NMOS triggered SCR device [80,81]. The new ESD protection circuit for mixed-voltage I/O circuits, which combines a stacked-NMOS structure with the gate-coupling circuit technique into the SCR device, is fully process-compatible to general CMOS processes without causing a gate oxide reliability problem. Without using thick gate oxide, the new ESD protection design for a 3 V/5 V-tolerant mixed-voltage I/O buffer has been verified successfully in a 0.35-μm CMOS process and should be applicable to the smaller geometry processes.

The cross-sectional view and corresponding layout pattern of a stacked-NMOS triggered silicon-controlled rectifier (SNTSCR) device are shown in Figure 5.19(*a*) and (*b*), respectively. This SNTSCR device structure can be realized in general CMOS processes without extra process modification. The

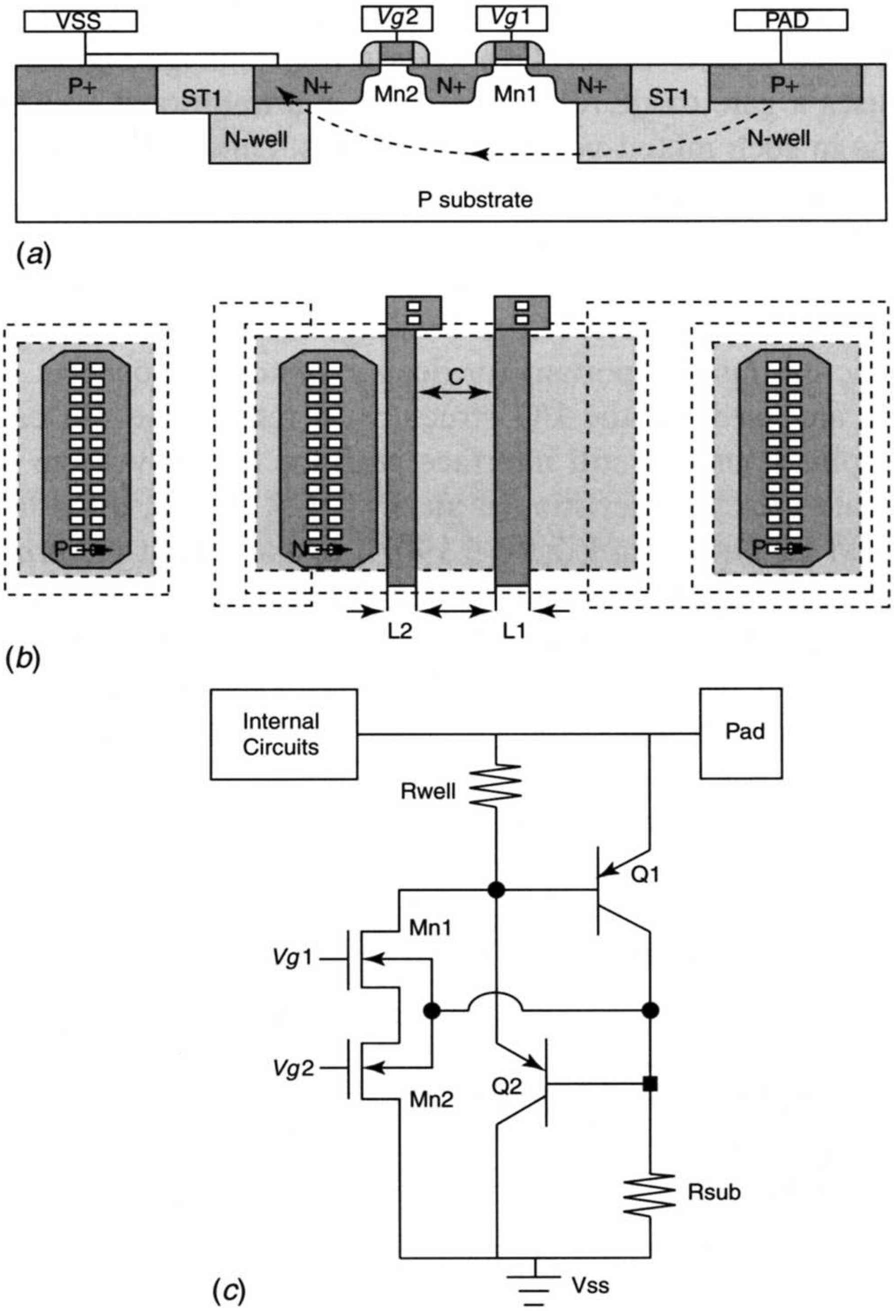


Figure 5.19 (*a*) Cross-sectional view, (*b*) corresponding layout pattern, and (*c*) equivalent circuit of a proposed SNTSCR device in a p-substrate CMOS process.

SNTSCR device is disposed on a bond pad to protect mixed-voltage I/O circuits from ESD damage. The corresponding equivalent circuit of this SNTSCR device is shown in Figure 5.19(*c*).

In the SNTSCR device, two NMOS transistors (Mn1 and Mn2) are stacked in the cascoded configuration, where the drain of Mn1 is across the junction between an N-well region and the p-substrate. The p^+ diffusion, N-well, p-substrate, and n^+ diffusion to form a lateral SCR device between the I/O pad and VSS is indicated by the dashed line in Figure 5.19(*a*). The purpose of Mn1 and Mn2 connected in stacked configuration is to sustain the high voltage level of input signals without causing a gate oxide reliability issue in the SNTSCR device under normal circuit operating conditions. If a single NMOS is inserted in the lateral SCR device, such as the traditional LVTSCR [82], the voltage across gate oxide will be greater than VDD when a high-voltage signal enters the I/O pad. This causes a gate oxide reliability issue in a traditional LVTSCR for long-term operation in such mixed-voltage I/O circuits. During ESD stress conditions, Mn1 and Mn2 are both turned on by a suitable gate-biased design, triggering the lateral SCR on for discharging ESD current. Without using thick gate oxide in the CMOS process, the proposed SNTSCR device has no gate oxide reliability issue when used to protect mixed-voltage I/O circuits. This ESD structure has become increasingly important for deep-submicron processes where thinner oxide devices are used for the I/O structure to reduce the pin capacitance for high-speed applications and still interface with the higher-voltage ICs.

To investigate the characteristics of an SNTSCR device, three layout parameters [C, L1, and L2 shown in Figure 5.19(*b*)] of the layout pattern are adjusted. C is the poly-to-poly spacing across the center common n+ diffusion; L1 and L2 are the channel lengths of Mn1 and Mn2, respectively. Such SNTSCR devices with different layout parameters but with a fixed channel width of 60 μm have been fabricated in a 0.35-μm CMOS process. The measured $I-V$ characteristics of an SNTSCR device with C = 0.5 μm and L1 = L2 = 0.35 μm under different gate biases of V_{g1} and V_{g2} are shown in Figure 5.20. The trigger voltage (V_t) of the SNTSCR device decreases from 10 V to 6 V when the gate bias increases from $V_{g1} = V_{g2} = 0$ V to $V_{g1} = V_{g2} = 0.5$ V. As $V_{g1} = V_{g2} > 0.6$ V, both Mn1 and Mn2 are turned on to trigger SNTSCR on; therefore, V_t decreases to around

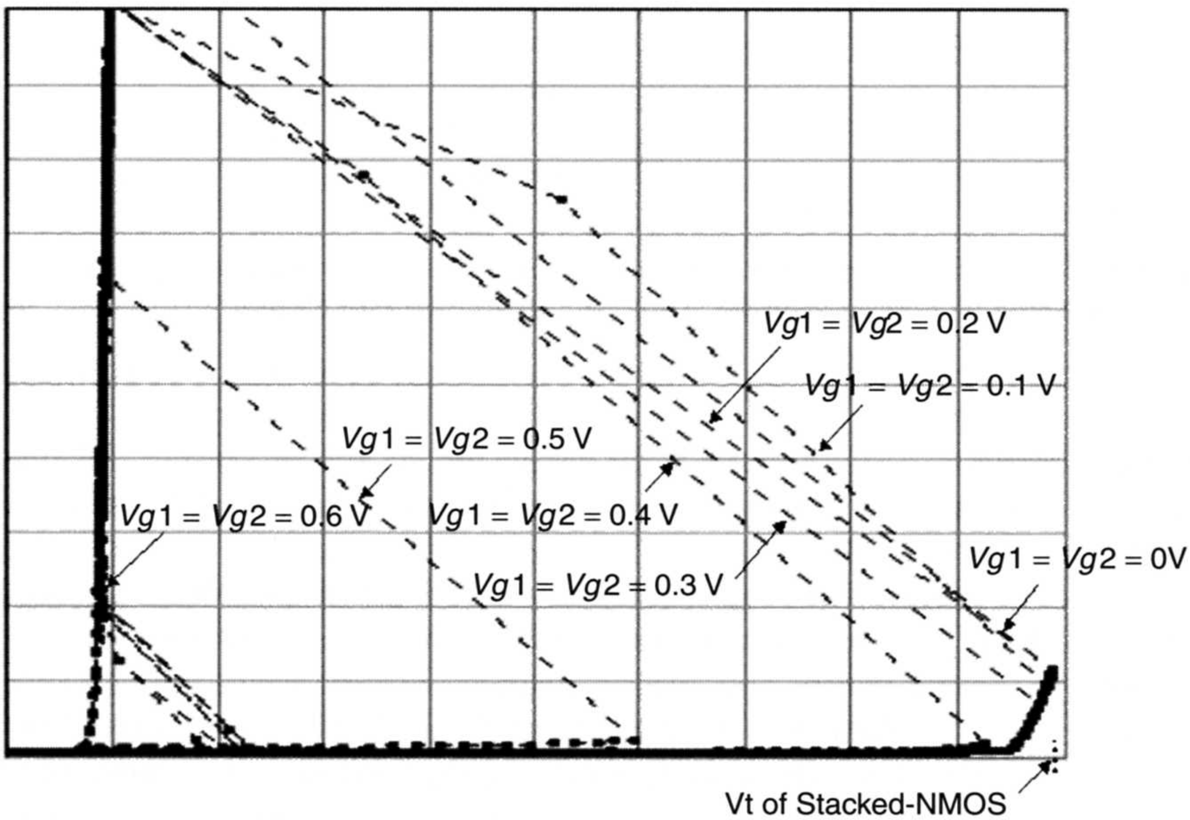


Figure 5.20 Measured $I-V$ curves of fabricated SNTSCR devices with C = 0.5 μm and L1 = L2 = 0.35 μm under different gate biases (x-axis: 1 V/div.; y-axis: 1 mA/div.).

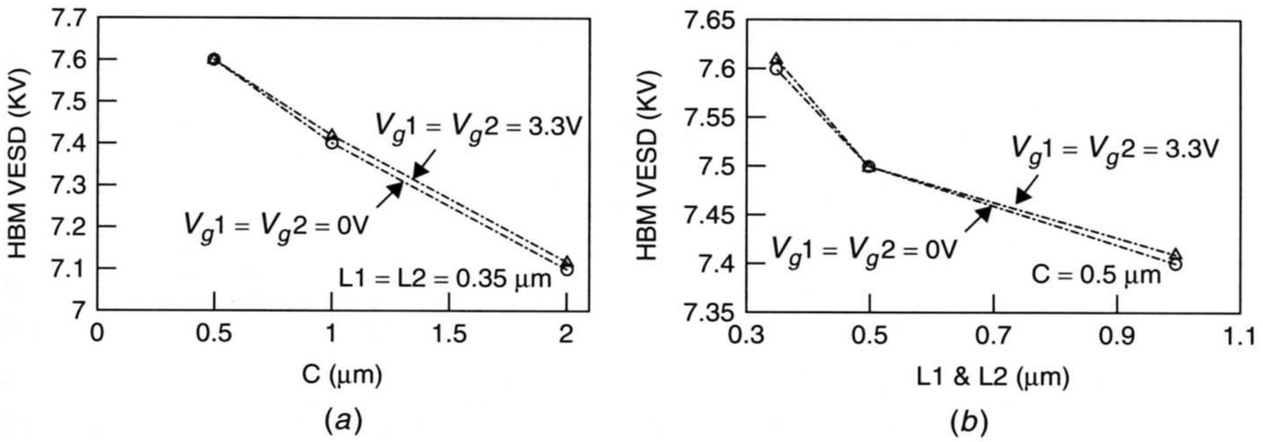


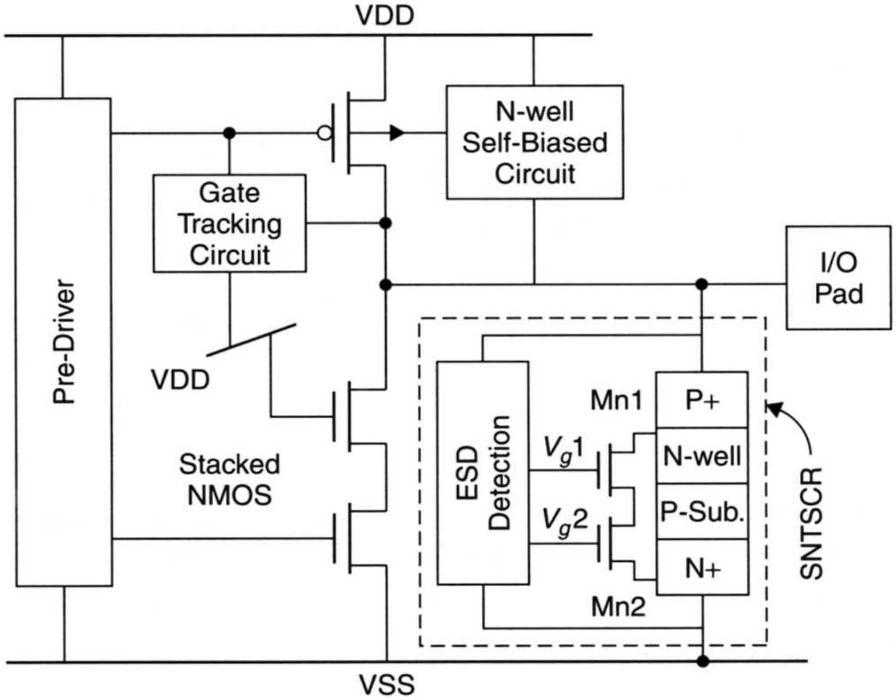
Figure 5.21 (*a*) Dependence of the HBM ESD level on the layout parameter C of SNTSCR devices under different gate biases ($V_{g1} = V_{g2}$). Failure criterion: $I_{\text{leakage}} > 1\ \mu A$ at $V_{\text{bias}} = 5$ V. (*b*) Dependence of the HBM ESD level on layout parameters L1 and L2 of SNTSCR devices under different gate biases ($V_{g1} = V_{g2}$). Failure criterion: $I_{\text{leakage}} > 1\ \mu A$ at $V_{\text{bias}} = 5$ V.

1 to 2 V. With suitable gate biases on Mn1 and Mn2, the trigger voltage of an SNTSCR device can be reduced lower than the snapback breakdown voltage of the stacked NMOS (about 10 V) in the mixed-voltage I/O buffer. Therefore, the new proposed ESD protection circuit with a SNTSCR device can effectively protect mixed-voltage I/O buffers.

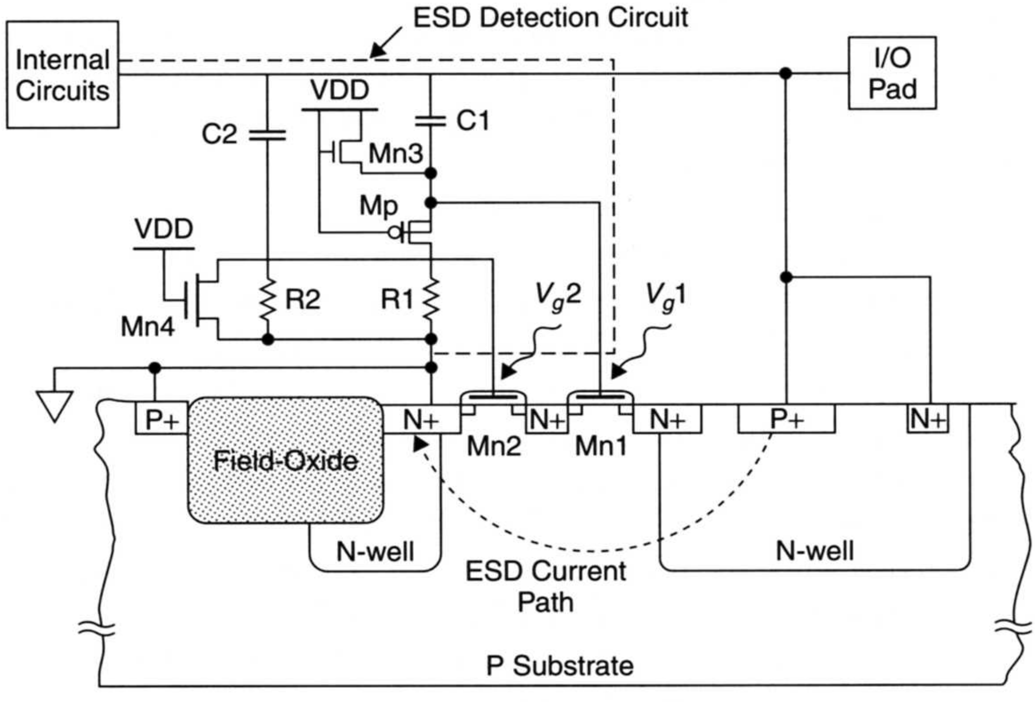
The impact of layout parameters and gate biases on the positive-to-VSS HBM ESD level of an SNTSCR device are shown in Figure 5.21(*a*) and (*b*). Figure 5.21(*a*) shows the dependence of the HBM ESD level on layout parameter C with fixed channel lengths of L1 = L2 = 0.35 μm in an SNTSCR device. Figure 5.21(*b*) shows the dependence of the HBM ESD level on the channel lengths of L1 and L2 with a fixed layout parameter C = 0.5 μm in an SNTSCR device. The failure criterion is defined at the leakage current greater than 1 μA under the voltage bias of 5 V. The HBM ESD robustness of an SNTSCR device is slightly degraded when the layout parameters C, L1, and L2 are increased. With shorter layout parameters (C, L1, and L2), an SNTSCR device has a narrower anode-to-cathode spacing, which implies a smaller turn-on resistance. Therefore, an SNTSCR device drawn with shorter layout parameters (C, L1, and L2) has a higher ESD level. The gate biases on V_{g1} and V_{g2} do not obviously improve the ESD level of an SNTSCR device (Figure 5.21), but it can trigger on the SNTSCR earlier to discharge ESD current. Thus, an SNTSCR device with a suitable gate-biased design can effectively protect mixed-voltage I/O buffers of CMOS ICs.

5.5.4 ESD Protection Circuit Design for a Mixed-Voltage I/O Interface

Based on experimental investigation on SNTSCR devices, an ESD protection design with an SNTSCR for protecting mixed-voltage I/O buffers is shown in Figure 5.22(*a*). An ESD detection circuit is designed to provide suitable gate



(*a*)



(*b*)

Figure 5.22 (*a*) ESD protection circuit with an SNTSCR device to protect the mixed-voltage I/O buffer; (*b*) design of an ESD detection circuit with an SNTSCR device with a larger design region on the sustaining resistance and coupling capacitance for protecting mixed-voltage I/O buffers.

biases to trigger on the SNTSCR device during ESD stress conditions. On the contrary, this ESD detection circuit must keep the SNTSCR off when the IC is under normal circuit operating conditions. An ESD detection circuit designed using a gate-coupling technique with consideration of gate oxide reliability issues is shown in Figure 5.22(*b*).

In normal circuit operating conditions the SNTSCR is kept off so that it does not interfere with the voltage levels of signals on the I/O pad. In this normal operating state, Mn3 in Figure 5.22(*b*) acts as a resistor to bias the gate voltage (V_{g1}) of Mn1 at VDD. But the gate of Mn2 is grounded through resistor R_2. When the I/O pad is applied with a high input voltage (5 V), the center common n+ region between the Mn1 and Mn2 transistors has a voltage level about VDD − Vthn (Vthn is the threshold voltage of an NMOS). So all the devices in the ESD protection circuit can meet the limited electrical-field constraint of gate oxide reliability during normal circuit operating conditions. The coupled voltage through capacitor C_1 could also increase the gate voltage of Mn1 when the voltage on I/O pad transfers from 0 V to 5 V. The PMOS device (Mp) in Figure 5.22(*b*) is therefore designed to clamp the excessive voltage once the voltage of Mn1's gate increases to VDD + V_{thp} (V_{thp} is the magnitude of the threshold voltage of Mp). Proper design of an ESD detection circuit ensures that the SNTSCR structure can be kept off under normal circuit operating conditions. Moreover, the PMOS (Mp) can further clamp the gate voltage of Mn1 to ensure gate oxide reliability on Mn1 even if the I/O pad has a high input voltage level.

The capacitors (C_1 and C_2), resistors (R_1 and R_2), Mp, and Mn3 compose an ESD detection circuit for providing suitable gate biases to the SNTSCR device. Capacitor C_1 (C_2) is designed to couple the ESD transient voltage to the gate of Mn1 (Mn2) to lower the trigger voltage of the SNTSCR device. Resistor R_1 (R_2) is designed to maintain the coupled voltage longer on the gate of Mn1 (Mn2) for triggering the SNTSCR device into its holding region. To further improve the design region for easily choosing the suitable sustaining resistance and coupling capacitance in general CMOS processes, device Mn4 is added across the sustaining resistor R_2, which is located between the gate of Mn2 and VSS. The gate of Mn4 is biased at VDD, but it is better to connect the gate to the VDD power line through a diffusion resistor for consideration of the antenna rule issue associated with the process. Under the normal circuit operating condition, Mn4 is always turned on to clamp the coupling voltage V_{g2} below the threshold voltage (V_{thn}), and to keep Mn2 off. Therefore, the SNTSCR can be guaranteed off under normal circuit operating conditions.

During positive-to-VSS ESD stress conditions, a positive high ESD voltage is applied to the I/O pad with VSS grounded but VDD floating. In this ESD stress condition, the gate of Mp is grounded since the initial voltage level on the floating VDD power line is zero. So Mp is turned on, but Mn3 is off. The capacitors, C_1 and C_2, are designed to couple the ESD transient voltage from the I/O pad to the gates of Mn1 and Mn2, respectively. The coupled voltage should be designed higher than the threshold voltage to turn on Mn1 and Mn2 for triggering the SNTSCR device on before the devices in the mixed-voltage I/O circuit are damaged by ESD energy. Under ESD stress conditions, Mn4 is off since the initial voltage level on the floating VDD power line is zero. The voltage (V_{g2}) coupled to the gate of Mn2 is determined by the sustaining resistance (R_2) and the coupling capacitance (C_2). When the SNTSCR is triggered on, the ESD current is discharged primarily from the I/O pad to VSS through this SNTSCR device. The characteristics of lower trigger voltage and low holding voltage of the gate-coupling SNTSCR device can safely protect the thin gate oxide of mixed-voltage I/O circuits as well as sustaining a high ESD level within a smaller silicon area.

The purpose of the ESD detection circuit is to provide suitable gate biases for an SNTSCR device under the normal circuit operating conditions and ESD stress conditions. To obtain suitable gate biases, it is important to determine the values of the coupling capacitors (C_1 and C_2) and sustaining resistors (R_1 and R_2). Based on the foregoing operating principles, suitable values of C_1, C_2, R_1, and R_2 to meet the circuit operations desired in various CMOS processes can be adjusted and finely tuned using HSPICE simulation.

5.5.5 ESD Robustness

Positive-to-V_{SS} human-body-model (HBM) ESD levels of mixed-voltage I/O buffers with or without an ESD protection circuit are measured and compared in Figure 5.23(*a*). Mixed-voltage I/O buffers with different stacked-NMOS channel widths are also tested as a reference. The HBM ESD level of mixed-voltage I/O buffers (with a stacked-NMOS channel width of 120 μm) can obviously be improved from the original ~2 kV to become greater than 8 kV using the proposed ESD protection circuit with an SNTSCR device. In Figure 5.23(*a*), all the mixed-voltage I/O buffers protected by the proposed ESD protection circuit have the same SNTSCR device width of 60 μm.

The positive-to-VSS machine-model (MM) ESD levels of mixed-voltage I/O buffers with or without an ESD protection circuit are measured and compared in Figure 5.23(*b*). Mixed-voltage I/O buffers with various stacked-NMOS channel widths are also tested as a reference. From the measured results, the MM

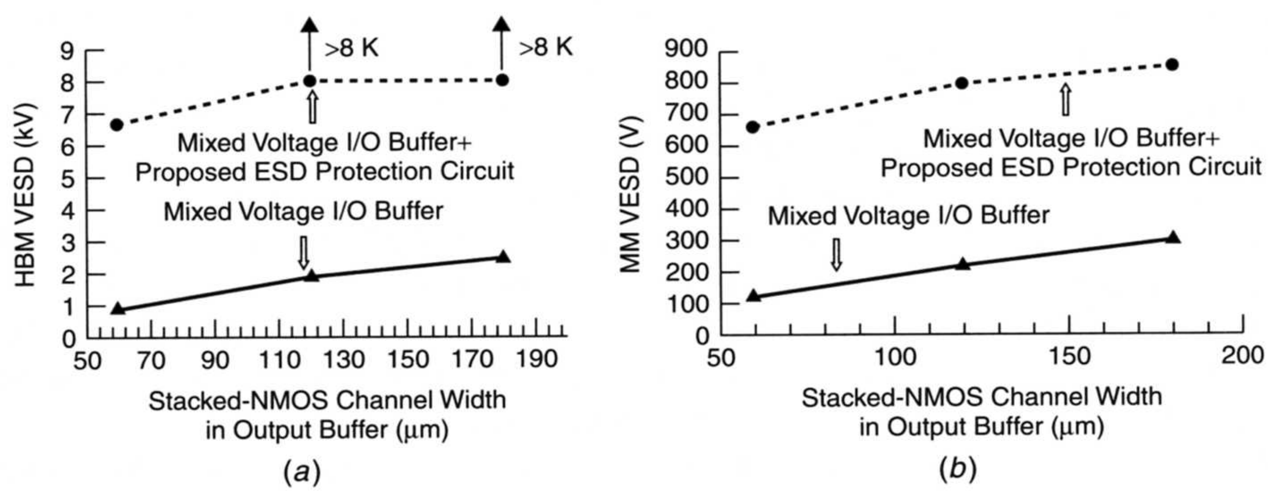


Figure 5.23 (*a*) Comparison of the positive-to-VSS HBM ESD robustness of mixed-voltage I/O buffers with or without an ESD protection circuit under various channel widths of a stacked NMOS in mixed-voltage I/O buffers. (*b*) Comparison of the positive-to-VSS MM ESD robustness of mixed-voltage I/O buffers with or without an ESD protection circuit under various channel widths of a stacked NMOS in mixed-voltage I/O buffers.

ESD level of a mixed-voltage I/O buffer with a channel width of 120 μm in a stacked NMOS can be improved significantly from the original ~200 V to become ~800 V by an ESD protection circuit with an SNTSCR device width of only 60 μm.

5.5.6 Turn-on Verification

To verify the turn-on efficiency of an ESD protection circuit for mixed-voltage I/O, a 0- to 8-V sharply rising voltage pulse with a rise time of 10 ns is applied to the I/O pad when VSS is relatively grounded but VDD is floating (to simulate the positive-to-VSS ESD stress condition). The stacked NMOS in the output buffer has a snapback breakdown voltage of about 10 V. Such a 0- to 8-V pulse applied to the I/O pad does not break down the stacked NMOS of the mixed-voltage output buffer. But the 0- to 8-V pulse can trigger on the ESD protection circuit to cause a degraded voltage waveform such as that shown in Figure 5.24(*a*), where the applied 0- to 8-V voltage pulse is clamped to about

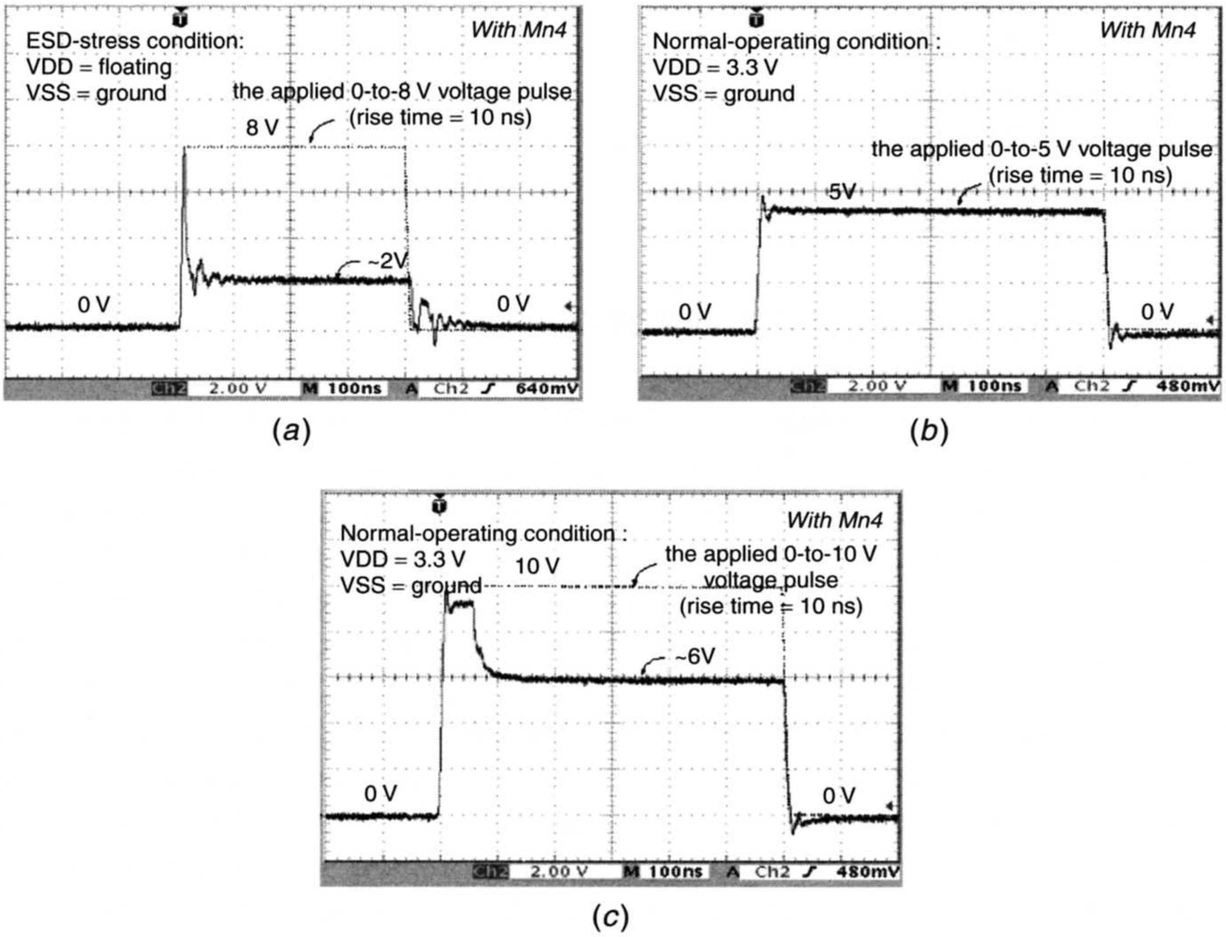


Figure 5.24 (*a*) Measured voltage waveform on the I/O pad triggered by a 0-to-8 V voltage pulse with a rise time of 10 ns, under positive-to-VSS ESD stress conditions (y-axis: 2 V/div.; x-axis: 100 ns/div.); and the measured voltage waveforms on the I/O pad triggered by (*b*) 0- to 5-V and (*c*) 0- to 10-V voltage pulses with a rise time of 10 ns under normal operating conditions with VDD = 3.3 V and VSS = 0 V (y-axis: 2 V/div.; x-axis: 100 ns/div.).

2 V by the SNTSCR device. The transition time of about 10 ns from 8 V to 2 V in Figure 5.24(a) is the corresponding turn-on speed of the SNTSCR device realized in this 0.35-μm CMOS process.

In the normal circuit operating condition with VDD (VSS) biased at 3.3 V (0 V), a 0- to 5-V input voltage pulse with a rise time of 10 ns is applied to the I/O pad while a digital oscilloscope monitors voltage on the I/O pad. The applied 0- to 5-V waveform is not degraded, as shown in Figure 5.24(b). During normal circuit operating conditions, the gate of Mn4 is biased at VDD (3.3 V). The coupled gate voltage of Mn2 through capacitor C_2 is discharged to ground by the turned-on Mn4, so the SNTSCR device is not triggered on by normal input signals of 5 V. If the applied voltage pulse is increased further, to 10 V, under normal circuit operating conditions, the measured voltage waveform on the I/O pad is as shown in Figure 5.24(c). The applied 0- to 10-V pulse is clamped to about ~6 V in Figure 5.24(c), but not to the voltage level of about 2 V as that shown in Figure 5.24(a). The stacked NMOS has a snapback breakdown of about 10 V and a snapback holding voltage of about 6 V in this 0.35-μm CMOS process. Therefore, the degraded voltage level of about 6 V in Figure 5.24(c) is clamped by the stacked NMOS of the mixed-voltage I/O buffer in the snapback region. If the SNTSCR device in the ESD protection circuit is triggered on, the voltage level should be clamped to its holding voltage of about 2 V. This result has further confirmed that the Mn4 device in the ESD detection circuit can safely apply the SNTSCR device to protect the mixed-voltage I/O buffer without being unexpectedly triggering under the normal circuit operating condition.

5.6 SCR DEVICES FOR ESD PROTECTION

Due to the low holding voltage (V_h, about 1.5 V in general CMOS processes) of a silicon-controlled rectifier (SCR) device, the power dissipation (power $\simeq I_{\mathrm{ESD}} \times V_h$) located on the SCR device during ESD stress is significantly less than that located on other ESD protection devices compared to a diode, MOS, BJT, or field-oxide device. The SCR device can sustain a much higher ESD level within a smaller layout area in CMOS ICs, so it has been used to protect internal circuits against ESD damage for a long time. But the SCR device still has a higher switching voltage (i.e., trigger voltage, about 22 V) in the sub-$\frac{1}{4}-\mu$m CMOS technology, which is generally greater than the gate oxide breakdown voltage of the input stages. Furthermore, gate oxide thickness, time to breakdown (t_{BD}), or charge-to-breakdown (Q_{BD}) will also be decreased with shrinking CMOS technologies. This trend makes it imperative to reduce the switching voltage of SCRs and to enhance their turn-on speed for efficient protection of ultrathin gate oxide from latent damage or rupture, especially against fast charged-device-model (CDM) ESD events, which is becoming the most difficult specification to meet in deep-submicron processes.

An overview of SCR-based devices for on-chip ESD protection is given in this section. In addition, solutions to avoid the transient-induced latch-up issue of SCR-based devices in CMOS IC products with a maximum voltage supply greater than 1.5 V are also discussed. However, such latch-up problems will certainly vanish when the maximum voltage supply of IC products is smaller than the holding voltage of SCR devices. For example, a single SCR with a holding voltage of about 1.6 V can safely be used as ESD protection without latch-up danger in a 0.13-μm CMOS process with a maximum voltage supply of 1.2 V.

5.6.1 Turn-on Mechanism of SCR Devices

The equivalent circuit schematic of a SCR device is shown in Figure 5.25(*a*). The SCR device consists of a lateral NPN and a vertical PNP bipolar transistor and forms a two-terminal, four-layer PNPN (P+/N-well/P-well/N+) structure, which is inherent in CMOS processes. The switching voltage of the SCR device is dominated by the avalanche breakdown voltage of an N-well/P-well junction, which is about 22 V in a 0.25-μm CMOS process or 18 V in a 0.13-μm CMOS process. When a positive voltage applied to an SCR anode is greater than the breakdown voltage and its cathode is grounded, for example, the hole and electron current will be generated through the avalanche breakdown mechanism. The hole current will flow through the P-well to P+ diffusion connected to ground, whereas the electron current will flow through the N-well to N+ diffusion connected to the SCR anode. As long as the voltage drop across the P-well resistor (R_{pwell}) [N-well resistor (R_{nwell})] is greater than 0.7 V, the NPN (PNP) transistor will be turned on to inject the electron (hole) current to further bias the PNP (NPN) transistor and initiate SCR latching action. Finally, the SCR will successfully be triggered

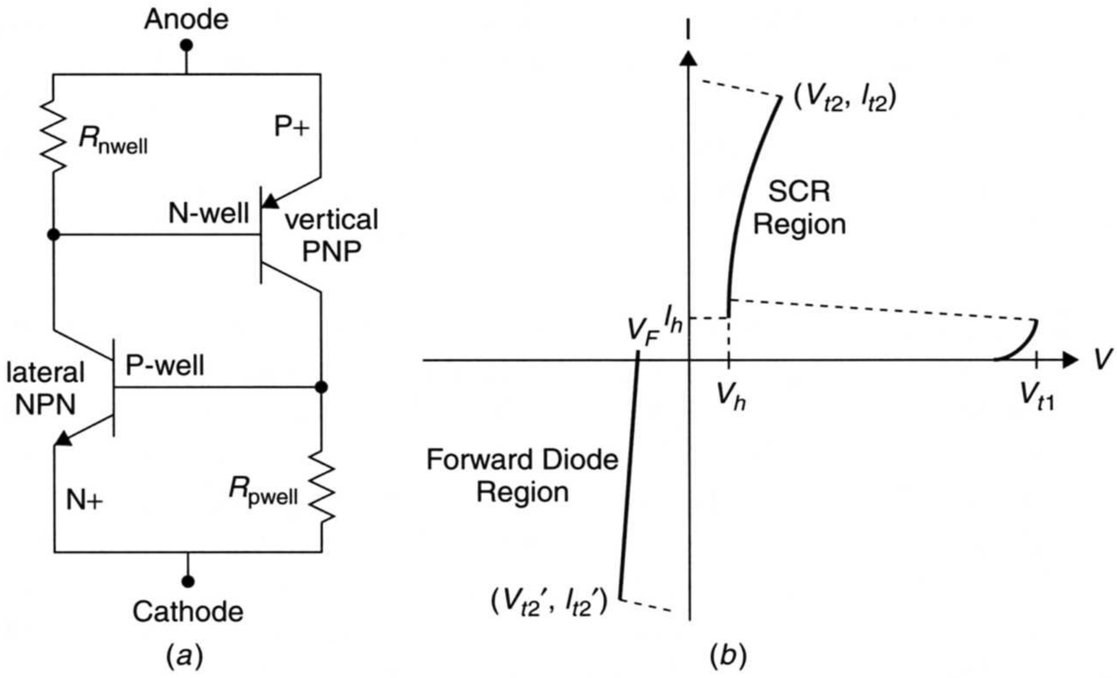


Figure 5.25 (*a*) Equivalent circuit schematic of a SCR device. (*b*) $I-V$ characteristics of an SCR device in a CMOS process under positive and negative voltage biases.

on into its latching state to discharge ESD current through the positive-feedback regenerative mechanism [94,95].

The dc $I-V$ characteristic of SCR device is shown in Figure 5.25(b). Once the SCR is triggered on, the required holding current to keep the NPN and PNP transistors on can be generated through the positive-feedback regenerative mechanism of latch-up without involving the avalanche breakdown mechanism. So the holding voltage (V_h) of an SCR can be reduced to a lower voltage level of about 1.5 V, typically. When negative voltage is applied on the anode terminal of SCR, the parasitic diode (N-well/P-well junction) inherent in SCR structure will be forward biased to clamp the negative voltage at a lower voltage level of about 1 V (cut-in voltage of a diode). Whether the ESD energy is positive or negative, the SCR device can clamp ESD overstresses to a lower voltage level, so the SCR device can sustain the highest ESD robustness within a smaller layout area in CMOS ICs.

5.6.2 SCR-Based Devices for CMOS On-Chip ESD Protection

Low-Voltage Triggering SCRs [82,85] To protect input and even output stages more effectively, a low-voltage triggering SCR (LVTSCR) has been developed. The device structure of the LVTSCR is illustrated in Figure 5.26(a) and the corresponding $I-V$ characteristic of the LVTSCR in a 0.25-μm CMOS process is shown in Figure 5.26(b). An example of using the LVTSCR device as the input ESD protection circuit is shown in Figure 5.26(c). In some applications, the N-well of an LVTSCR is connected to the input pad. The switching voltage of the LVTSCR (about 7 V) is equivalent to the drain breakdown or punch-through voltage of a short-channel NMOS device, which is inserted into the LSCR structure rather than the original switching voltage of the LSCR device (about 22 V). With such a low switching voltage, the LVTSCR can provide effective ESD protection for the input or output stages of CMOS ICs without a secondary ESD protection circuit. Therefore, the total layout area of the ESD protection circuits with the LVTSCR can be saved. Furthermore, to protect both PMOSs and NMOSs in the input or output stages of CMOS ICs, a complementary LVTSCR structure [99] has been invented to provide better ESD protection.

Gate-Coupled LVTSCRs [86] To effective protect ultrathin gate oxide in a deep-submicron CMOS process, the gate-coupling technique was applied to further reduce the switching voltage of the LVTSCR without involving avalanche breakdown mechanism. The ESD protection circuit for an input or output pad with complementary gate-coupled LVTSCR devices [NMOS-triggered LSCR (NTLSCR) and PMOS-triggered LSCR (PTLSCR)] is shown in Figure 5.27(a). The device structure of a complementary gate-coupled LVTSCR is illustrated in Figure 5.27(b), and the $I-V$ characteristics of a gate-coupled LVTSCR in a 0.25-μm CMOS process is shown in Figure 5.27(c). The dependence of the switching voltage of an SCR device on the gate bias voltage of an NTLSCR device is shown in Figure 5.27(d). The capacitances (C_n and C_p) in Figure 5.27(a) must

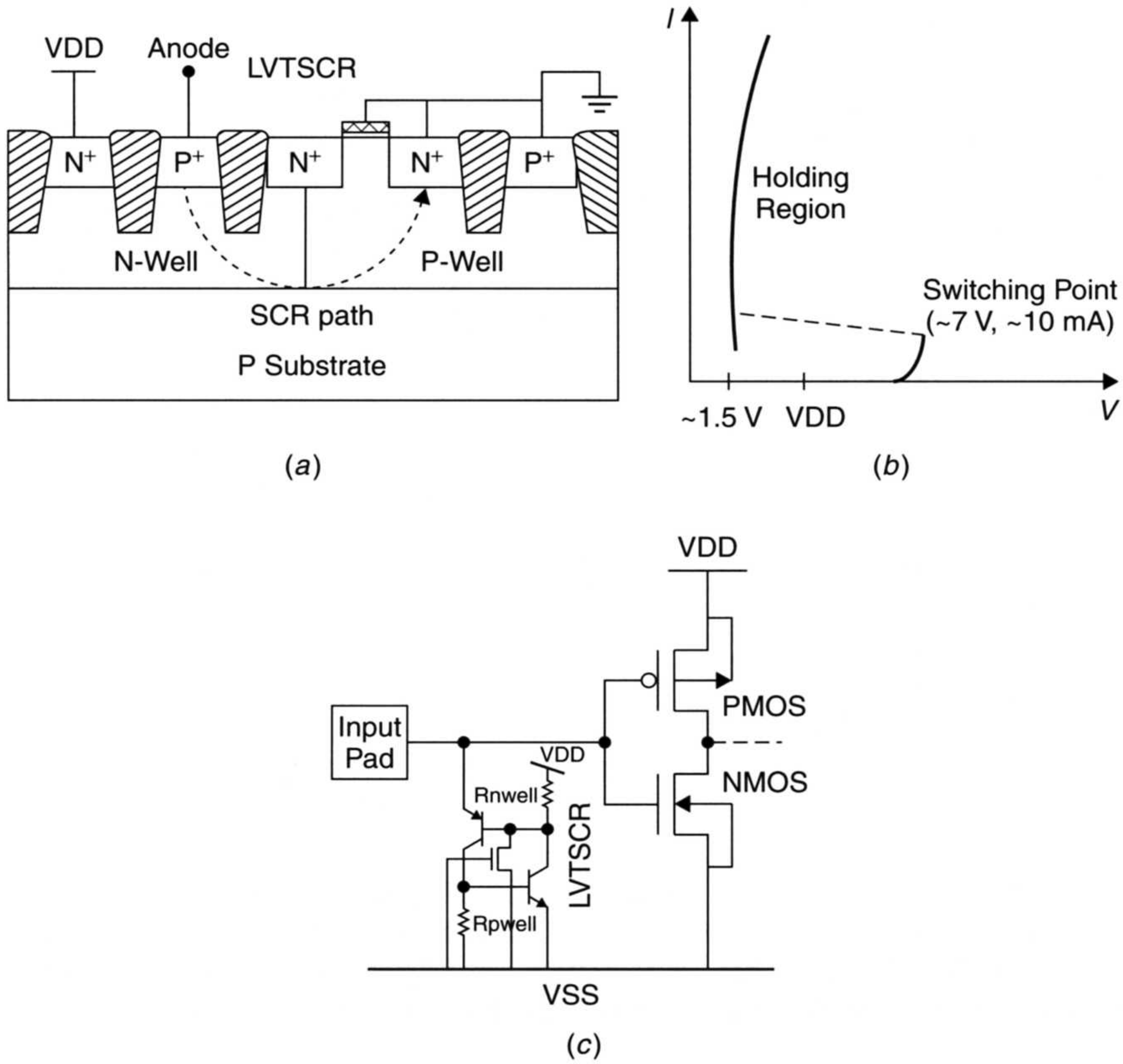


Figure 5.26 (*a*) Device structure of a low-voltage triggering SCR (LVTSCR) in a CMOS process. (*b*) $I-V$ characteristics of an LVTSCR in a 0.25-μm CMOS process. (*c*) Input ESD protection circuit with an LVTSCR device.

be designed at a suitable value where the coupled voltage under normal circuit operating conditions is smaller than the threshold voltage of NMOS/PMOS but greater than the threshold voltage of NMOS/PMOS under ESD zapping conditions [20]. The switching voltage of a gate-coupled NTLSCR (PTLSCR) can be adjusted using the coupled voltage on the gate of the short-channel NMOS (PMOS) in the SCR device structure. The higher coupled voltage on the gate of the short-channel NMOS/PMOS in the LVTSCR leads to lower switching voltage in the LVTSCR. Therefore, gate-coupled LVTSCR devices can quickly discharge ESD current to protect the ultrathin gate oxide of the input or output stages more effectively.

Grounded-Gate NMOS Triggered SCRs [88,89] A grounded-gate NMOS triggered SCR (GGSCR) is another choice for on-chip ESD protection circuit. A NMOS transistor, which resembles a GGNMOS configuration, is used as an external trigger device to trigger on the GGSCR. In contrast to the LVTSCR, the

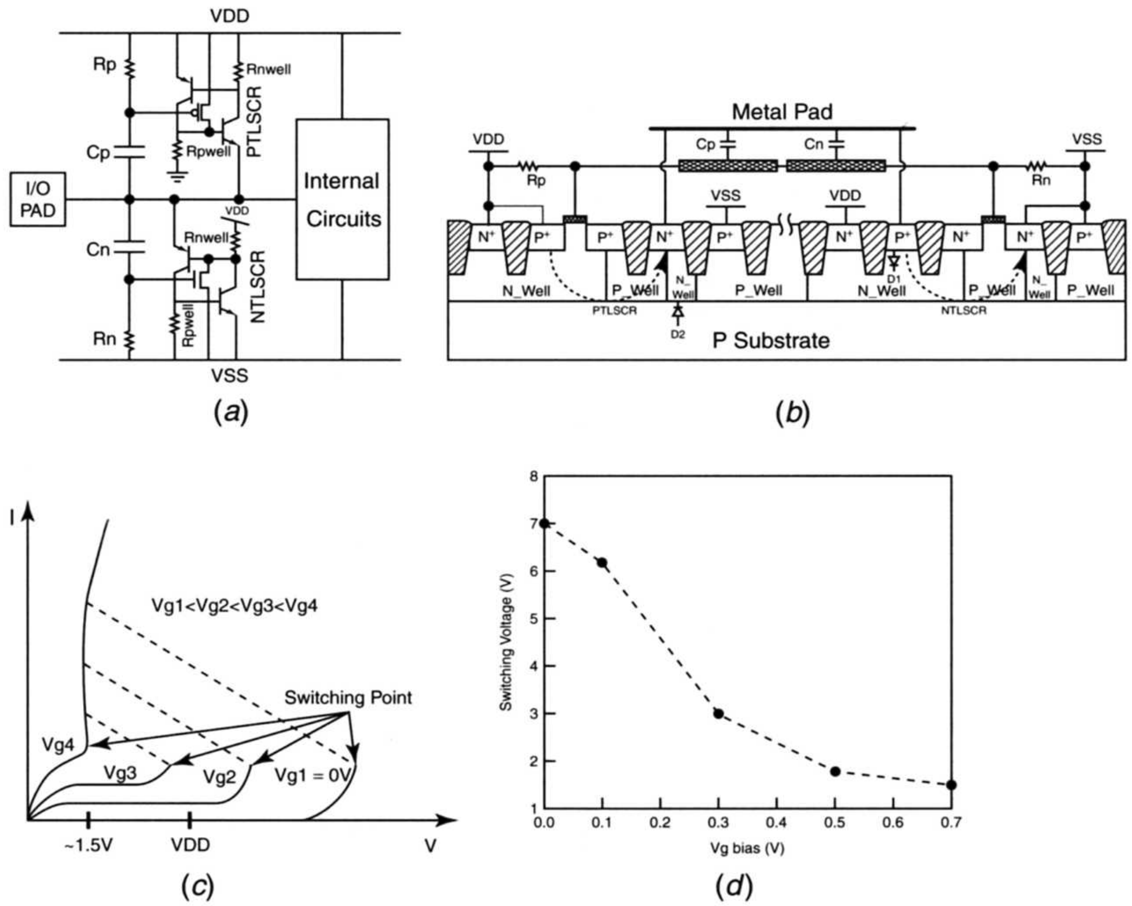
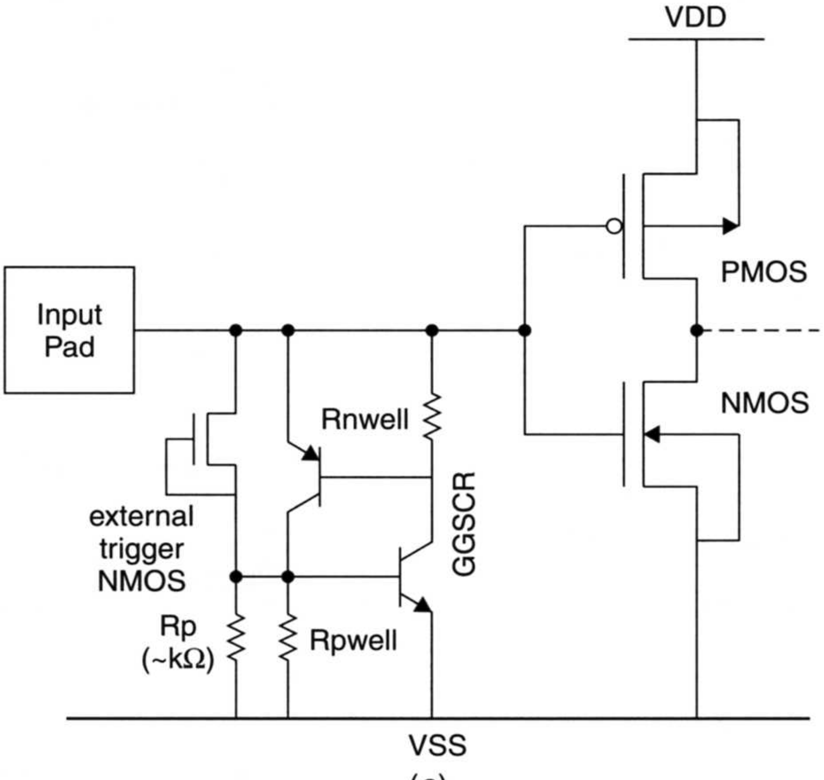


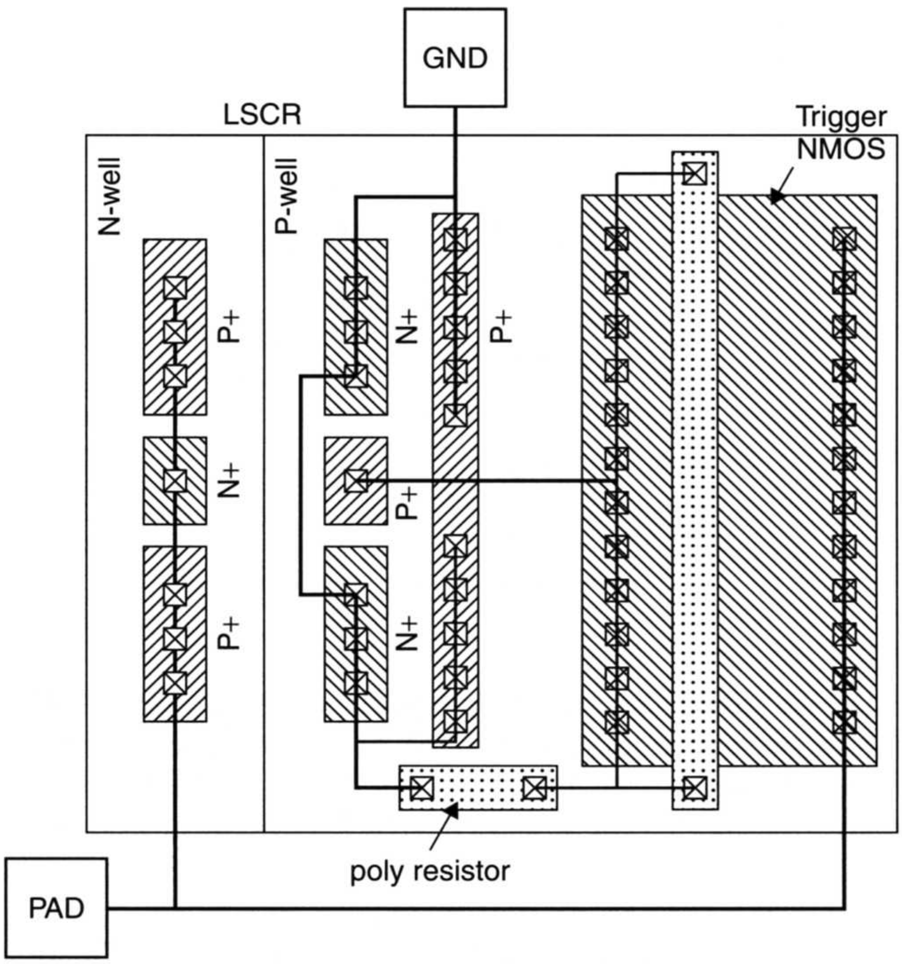
Figure 5.27 (*a*) ESD protection circuit with gate-coupled LVTSCR devices. (*b*) Device structure of a gate-coupled LVTSCR device in a CMOS process. (*c*) I–V characteristics of a gate-coupled LVTSCR device in a 0.25-μm CMOS process. (*d*) Dependence of switching voltage of an SCR device on the gate bias voltage of an NTLSCR device.

drain of the external trigger NMOS in GGSCR is coupled directly to the pad, and its gate and source are coupled into the P-substrate (the base of the NPN). An example of using a GGSCR device as an input ESD protection circuit is shown in Figure 5.28(*a*). The layout top view of the GGSCR is illustrated in Figure 5.28(*b*) [105]. When an ESD event is applied to the I/O pad in Figure 5.28(*a*), the external trigger NMOS will enter avalanche breakdown first to inject the triggering current into the P-substrate and poly resistor. As long as the base voltage of NPN is greater than 0.7 V, the GGSCR will be triggered on. The poly resistor in Figure 5.28(*b*) controls the triggering and holding current and prevents false triggering of the GGSCR. From the experimental results, a GGSCR designed with a shorter anode-to-cathode spacing will have a lower holding voltage, higher I_{t2}, better dV/dt triggering ability, and faster turn-on speed than those of an LVTSCR with longer anode-to-cathode spacing.

Substrate-Triggered SCRs [90,91] The turn-on mechanism of an SCR device is essentially a current triggering event. While a current is applied to the base or substrate of an SCR device, it can be quickly triggered into its latching state. With the substrate-triggered technique, p-type substrate-triggered SCR (P_STSCR) and n-type substrate-triggered SCR (N_STSCR) devices for ESD protection were



(*a*)



(*b*)

Figure 5.28 (*a*) Input ESD protection circuit with GGSCR device. (*b*) Layout top view of GGSCR in a CMOS process.

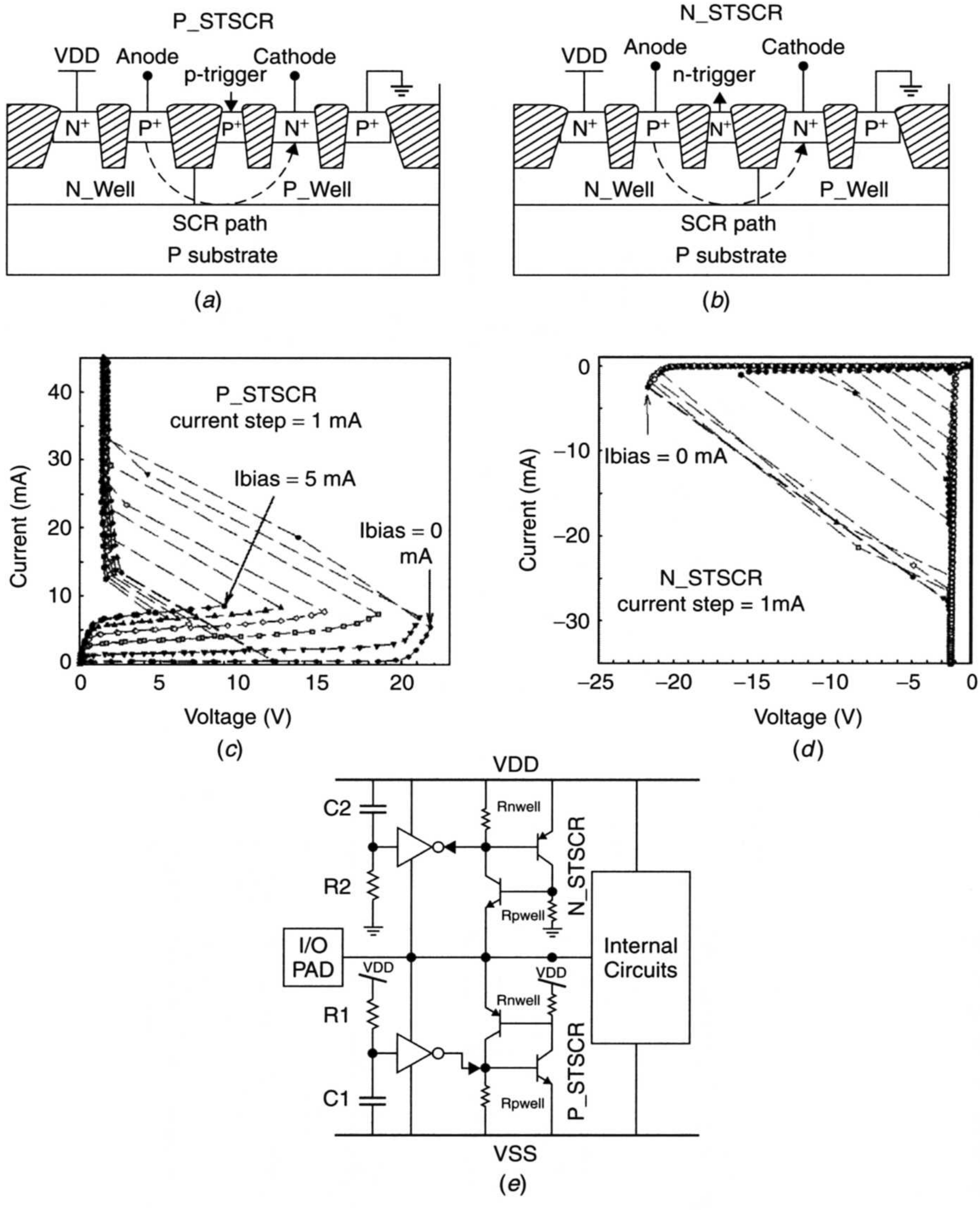


Figure 5.29 Device structures of (*a*) the p-type substrate-triggered SCR (P_STSCR) and (b) the n-type substrate-triggered SCR (N_STSCR) devices. The I-V characteristics of (c) the P_STSCR and (d) the N_STSCR devices in a 0.25-μm CMOS process. (e) The ESD protection circuit with the P_STSCR and N_STSCR devices for I/O pad.

reported. The device structures of the P_STSCR and N_STSCR are illustrated in Figure 5.29(*a*) and (*b*), respectively. Comparing this structure to the traditional lateral SCR device structure, an extra P+ diffusion is inserted into the P-well of the P_STSCR device structure and connected out as the p-trigger node of the P_STSCR device. For the N_STSCR, an extra N+ diffusion is inserted into the

N-well of the N_STSCR device structure and connected out as the n-trigger node of the N_STSCR device. The I–V characteristics of the P_STSCR and N_STSCR are shown in Figure 5.29(*c*) and (*d*), respectively. With the increase in substrate-/well-triggered current, the switching voltage of the P_STSCR/N_STSCR device can be reduced to its holding voltage. The turn-on time of the STSCR can be also reduced to about 10 ns under a 5-V voltage pulse with a 10-ns rise time in a 0.25-μm CMOS process. With the lower switching voltage, the STSCR device can clamp the ESD voltage to a lower voltage level more quickly, to fully protect the ultrathin gate oxide of input stages from ESD overstress. The ESD protection circuit for an input or output pad with P_STSCR and N_STSCR devices is shown in Figure 5.29(*e*). In normal circuit operating conditions with VDD and VSS power supplies, the input of inv_1 (inv_2) is biased at VDD (VSS). Therefore, the output of the inv_1 (inv_2) is biased at VSS (VDD), due to the turn-on of NMOS (PMOS) in the inv_1 (inv_2), whenever the input signal is logic high or logic low. The p-trigger (n-trigger) node of the P_STSCR (N_STSCR) device is kept at VSS (VDD) by the output of the inv_1 (inv_2), so the P_STSCR and N_STSCR devices are guaranteed off under normal circuit operating conditions. Under the positive-to-VSS (PS) ESD-zapping condition (with grounded VSS but floating VDD) shown in Figure 5.29(*e*), the input of the inv_1 is initially floating with a zero voltage level; therefore, the PMOS of the inv_1 will be turned on due to the positive ESD voltage on the pad. So the output of the inv_1 is charged up by the ESD energy to generate the trigger current into the p-trigger node of the P_STSCR device. Therefore, the P_STSCR device is triggered on, and the ESD current is discharged from the I/O pad to the grounded VSS pin through the P_STSCR device. A similar operating principle can be applied to N_STSCR under the negative-to-VDD (ND) ESD-zapping condition (with grounded VDD but floating VSS). Furthermore, an STSCR device with a dummy-gate structure has been invented [108,109] to further reduce the switching voltage and to improve the turn-on speed of STSCR. The bipolar current gain of an STSCR with a dummy-gate structure is larger than that of STSCR with a shallow trench isolation (STI) structure, so the triggering efficiency of STSCR with a dummy-gate structure is better than that of STSCR with STI.

Double-Triggered SCRs [94] Another method to reduce the switching voltage of an LSCR device and to further enhance the turn-on speed of an LSCR device more efficiently is the double-triggered technique. The device structure of a double-triggered SCR (DTSCR) is shown in Figure 5.30(*a*). The extra P+ and N+ diffusions are inserted into the P-well and N-well of a DTSCR device structure and connected out as the p- and n-trigger nodes of the DTSCR device. The dependence of the switching voltage of the DTSCR device on the substrate-triggered current under different N-well triggered currents is summarized in Figure 5.30(*b*). The switching voltage of the DTSCR can be reduced to a lower voltage level more efficiently if the substrate and N-well triggered currents are applied synchronously to the p- and n-trigger nodes, respectively. The I/O ESD protection circuit realized with DTSCR devices is shown in Figure 5.30(*c*).

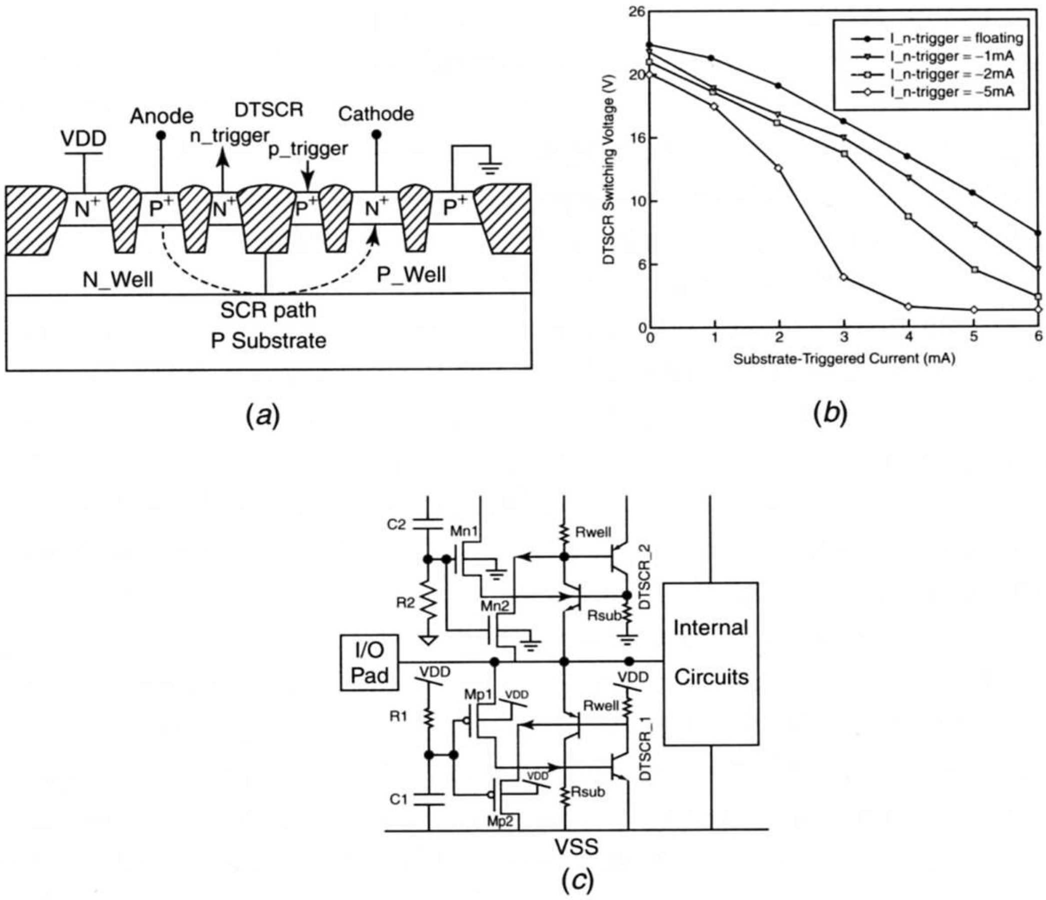


Figure 5.30 (*a*) Device structure of a double-triggered SCR (DTSCR). (*b*) Dependence of the switching voltage of a DTSCR device on substrate-triggered current under different N-well triggered currents in a 0.25-μm CMOS process. (*c*) ESD protection circuit with DTSCR devices for an I/O pad.

Based on the *RC* delay principle, the substrate and N-well triggered currents can be generated by Mp1 and Mp2 (Mn1 and Mn2), respectively, under PS (ND) ESD-zapping conditions. Therefore, the DTSCR with the double-triggered currents shown in Figure 5.30(*c*) can be triggered on more quickly to discharge ESD current. In normal circuit operating conditions with VDD and VSS power supplies, the gates of Mp1 and Mp2 (Mn1 and Mn2) are biased at VDD (VSS) through the resistor R_1 (R_2). Therefore, the Mp1, Mp2, Mn1, and Mn2 are all in the off state whenever the input signal is high or low. The p-trigger (n-trigger) node of the DTSCR device is kept at VSS (VDD) through the parasitic resistor R_{sub} (R_{well}), so such DTSCR is guaranteed to be kept off under normal circuit operating conditions. From the experimental results in a 0.25-μm CMOS process, when a 0- to 5-V voltage pulse is applied to the anode of DTSCR, the turn-on time of the DTSCR is about 37 ns under a positive voltage pulse of 1.5 V at the p-trigger node of the DTSCR. But the turn-on time of the DTSCR can be further reduced, to about 12 ns, while a negative voltage pulse of −5 V is synchronously applied to its n-trigger node. The dummy-gate structure used to block the STI in the SCR device can be applied to the DTSCR structure to further reduce the switching voltage and to enhance the turn-on speed of the DTSCR more efficiently.

Native-NMOS-Triggered SCRs [95] Native NMOS is built directly in a lightly doped p-type substrate in a sub-$\frac{1}{4}$-μm CMOS process, whereas normal NMOS (PMOS) is in a heavily doped P-well (N-well) in P-substrate twin-well CMOS technology. The native NMOS and lateral SCR can be merged to form a new ESD protection device, native-NMOS-triggered SCR (NANSCR), which has the advantages of lower switching voltage and faster turn-on speed. The device structure of an NANSCR is illustrated in Figure 5.31(*a*). The gate of native NMOS is connected to a negative bias circuit (NBC) [96] to turn off the NANSCR under normal circuit operating conditions. A comparison of dc $I-V$ curves between NANSCR and LVTSCR is shown in Figure 5.31(*b*). The switching voltage (about 4 V) of an NANSCR with a channel length of 0.3 μm is smaller than that (about 5 V) of an LVTSCR with a channel length of 0.13 μm in a 0.13-μm silicide CMOS process under the same channel width. With the substrate-triggered technique, the switching voltage of an NANSCR can be reduced further with an increase in the W/L ratio of native NMOS. The ESD protection circuit for an input or output pad with NANSCR devices is shown in Figure 5.31(*c*). In normal circuit operating conditions, the gates of native NMOS in all NANSCR devices are biased by the same NBC to turn off the NANSCR devices. So the NANSCR devices NANSCR_1 and NANSCR_2 will not

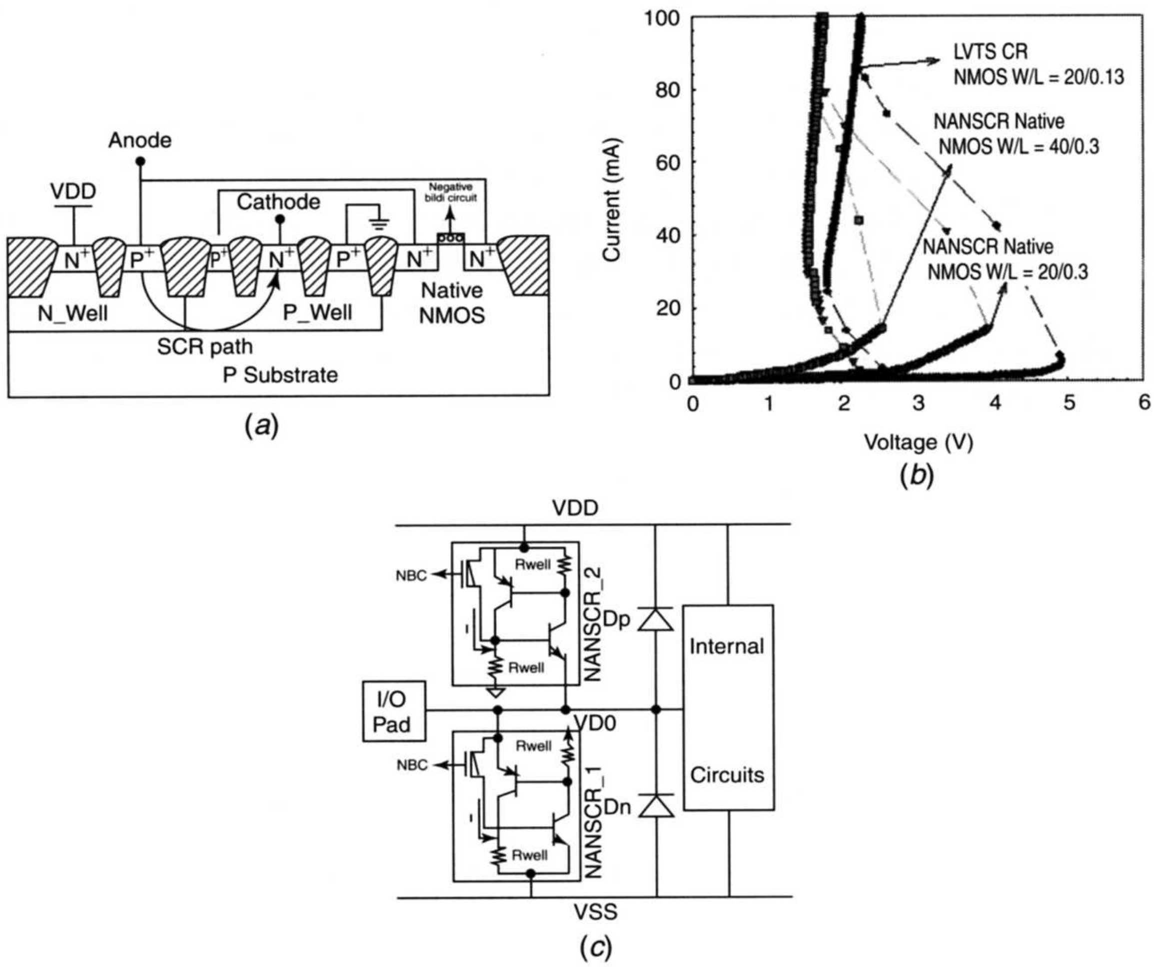


Figure 5.31 (*a*) Device structure of native-NMOS-triggered SCR (NANSCR). (*b*) Comparison of dc $I-V$ curves between NANSCR and LVTSCR in a 0.13-μm CMOS process. (*c*) ESD protection circuit with NANSCR devices.

interfere with the functions of I/O circuits. Under PS ESD-zapping conditions, the gate of native NMOS in NANSCR_1 is floating. NANSCR_1 is triggered on quickly by the substrate-triggering current generated from the already-on native NMOS. So the positive ESD current can be discharged quickly from the I/O pad through NANSCR_1 to the grounded VSS line. From the experimental results in a 0.13-μm CMOS process, the turn-on speed of NANSCR is faster than that of LVTSCR. Moreover, NANSCR can sustain a higher CDM ESD level (5 V/μm^2) than that (2.33 V/μm^2) of an LVTSCR. So it is more suitable for protecting the ultrathin gate oxide in nanoscale CMOS technologies.

5.6.3 SCR Latch-up Engineering

To make SCR-based devices with low enough switching voltage for effective ESD protection, transient-induced latch-up problems [87] must be avoided. There are two solutions to avoid having SCR-based devices with low switching voltage triggered on accidentally by a noise pulse when the CMOS ICs are under normal circuit operating conditions. Figure 5.32(*a*) shows one method for avoiding latch-up by increasing the triggering current of low-voltage-triggered SCR-based devices, but the switching and holding voltages are kept the same. With a higher triggering current, low-voltage-triggered SCR-based devices such as LVTSCRs have enough noise margin against overshooting or undershooting noise pulses on the pads. A high-current NMOS-triggered lateral SCR (HINTSCR) [99] device has been designed successfully by adding a bypass diode to the LVTSCR structure to increase its triggering current up to 218.5 mA in an 0.6-μm CMOS process. Such an HINTSCR has a noise margin greater than VDD + 12 V in 3-V applications. In addition, a high-holding-current SCR (HHI-SCR) device [89] modified from a GGSCR was reported with a holding current of about 70 mA in a 0.1-μm CMOS process by adjusting the external poly resistance from kilohms in a GGSCR to only about 10 Ω in an HHI-SCR.

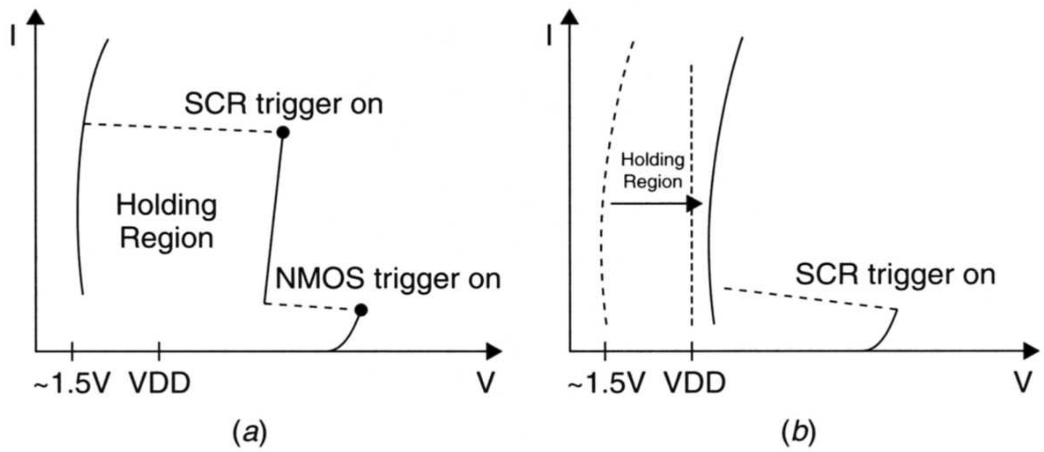


Figure 5.32 Two solutions to overcome latch-up issue in the ESD protection design with SCR-based device: (*a*) increasing the trigger current; (*b*) increasing holding voltage to avoid the SCR-based devices being accidentally triggered on by noise pulse.

Another method immune from latch-up is to increase the holding voltage of SCR-based devices to be greater than the maximum VDD voltage supply, as shown in Figure 5.32(*b*). By using an epitaxial substrate, the holding voltage of an SCR device can be increased to avoid latch-up problems [116]. But the fabrication cost of the CMOS wafer will also be increased. By stacking the voltage drop elements (such as diodes or SCR devices), an SCR-based device can elevate its total holding voltage in a bulk CMOS process. The switching voltage and current can still be kept at a lower voltage level by suitable trigger-assisted circuit design. A cascaded-LVTSCR [117] structure was designed to increase the holding voltage (>VDD) without degrading its ESD robustness in a 0.35-μm silicided CMOS technology. In addition, ESD protection circuits designed with stacked STSCR devices [90] or designed with an STSCR device and a stacked diode string [91] have been reported to have a 7-kV HBM ESD level and are free of latch-up problems in a 0.25-μm silicided CMOS technology. Recently, the holding voltage of a single SCR device has been adjusted dynamically for ESD protection (with a low holding voltage) and for normal circuit operations (with a higher holding voltage) [102]. A dynamic holding voltage SCR (DHVSCR) was reported to be an ESD protection device with high latch-up immunity. The device structure of an DHVSCR is shown in Figure 5.33(*a*). A PMOS and a NMOS are inserted into a DHVSCR device structure rather than an LSCR structure. The $I-V$ characteristics of the DHVSCR under normal circuit operating conditions and ESD-zapping conditions in a 0.25-μm CMOS process are shown in Figure 5.33(*b*). Under normal circuit operating conditions, the gates (V_{g1} and V_{g2}) of the PMOS and NMOS are biased at 2.5 V (VDD), but are biased at 0 V under ESD-zapping conditions. The holding voltage and holding current of the DHVSCR under normal circuit operating conditions are 2.8 V and 172 mA, respectively. Thus, the DHVSCR will not be kept in the latch-up state under normal circuit operating conditions. However, the holding voltage and holding current of the DHVSCR under ESD-zapping conditions drop to 2.2 V and 91 mA,

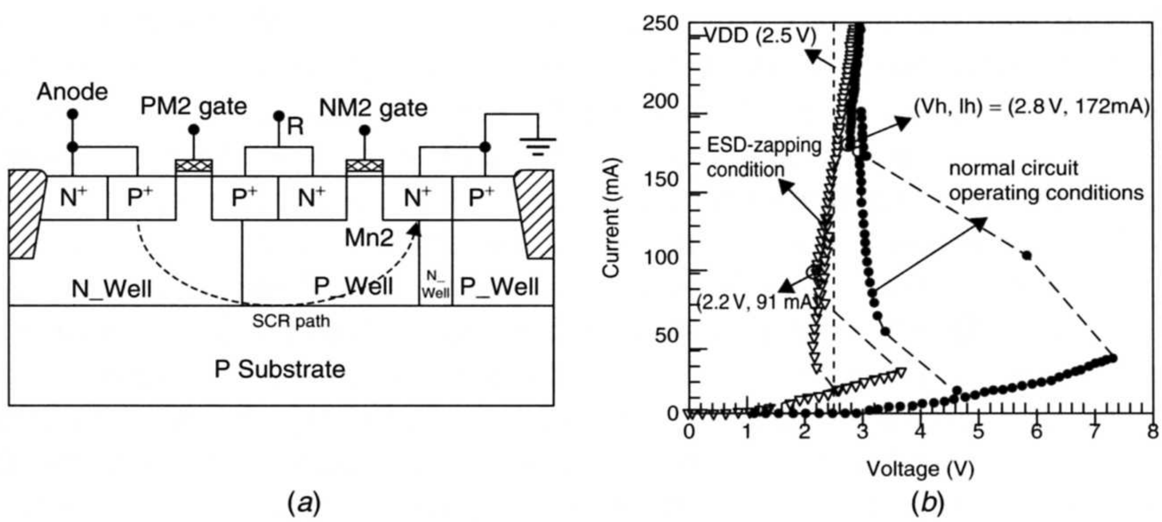


Figure 5.33 (*a*) Device structure of a dynamic holding voltage SCR (DHVSCR) in a CMOS process. (*b*) $I-V$ characteristics of the DHVSCR under normal circuit operating conditions and ESD-zapping conditions in a 0.25-μm CMOS process.

respectively. So the DHVSCR can also clamp the ESD overstress to a lower voltage level to sustain the higher ESD levels. The holding voltage and holding current of the DHVSCR can be adjusted by controlling the gate voltages of the PMOS and NMOS, which are merged with the SCR structure.

However, with scaled-down CMOS technologies, the power supply voltages in CMOS ICs have also been scaled down to follow the constant-field scaling requirement and to reduce power consumption. For CMOS IC products realized in a 0.13-μm silicided CMOS process, the maximum supply voltage for the internal circuit has been reduced to 1.2 V, so the latch-up concern inherent in SCR-based devices will certainly vanish. Therefore, SCR-based devices with lower switching voltages can be a great candidate for on-chip ESD protection, due to its highest ESD robustness, smallest layout area, and lack of latch-up danger compared with other ESD protection devices. However, in such a 0.13-μm CMOS process with ultrathin gate oxide, the turn-on speed of SCR devices should be enhanced to discharge ESD overstress voltage quickly for protecting such thinner gate oxide. Use of the NANSCR [95] and dummy-gate structure [92] to improve the turn-on speed of SCR-based devices will be a better choice to protect such an ultrathin gate oxide in nanoscale CMOS processes.

The switching voltage and turn-on speed of SCR-based devices must be suitably designed to fully and effectively protect the ultrathin gate oxide of input stages, especially against fast CDM ESD events. The switching voltage and turn-on speed of SCR-based devices will be the dominate factors in the overall performance of on-chip ESD protection circuits with SCR-based devices in nanoscale CMOS processes with a maximum voltage supply below 1.2 V. For a nanoscale CMOS process, SCR-based devices with a low-enough switching voltage and fast-enough turn-on speed are required to protect the ultrathin gate oxide of I/O circuits.

5.7 SUMMARY

With continued scaling of CMOS technologies into nanoscale dimensions, more circuits and functions have been integrated into a chip, such as the system on a chip (SoC). With scaled-down CMOS processes, the gate oxide becomes much thinner, which is more easily ruptured by ESD overstress. An SoC integrates more circuits and functions into a chip and often has a larger die size, which provides a larger body capacitance for storing CDM charges in the body of the IC. Additionally, SoCs often have a pin count of several hundreds. The layout area for each I/O cell in a high-pin-count SoC is significantly limited, which also limits the layout area for drawing ESD protection devices in such a high-pin-count SoC. An SoC often has multiple separated power pins, which cause unexpected ESD failures at the interface circuits between circuit blocks. Therefore, the ESD issue will become worst as we scale to deep-submicron processes, especially for CDM ESD events.

To effectively protect SoCs fabricated in nanoscale CMOS processes, the turn-on speed of ESD protection devices must be enhanced to discharge ESD current quickly before the internal circuits are damaged by ESD stresses. If an on-chip ESD clamp device (NMOS) has a negative threshold voltage (or a near-0-V threshold voltage), the ESD clamp device can stay in the already-on condition to discharge ESD current when the IC is being zapped by ESD pulses. But during normal circuit operating conditions, an extra negative bias can be used to turn off the ESD clamp device. With the already-on characteristics, the ultrathin gate oxide of SoCs in nanoscale CMOS processes can still be safely protected.

For an SoC with multiple separated power pins, a whole-chip ESD protection scheme is very important to avoid ESD failure located at internal or interface circuits of the SoC. The layout arrangement of power lines will have a strong impact on the ESD level of an SoC. Some suitable ESD connecting cells should be used to connect the separated power lines in the chip. Among ESD protection devices the SCR has the highest area efficiency to sustain ESD overstress. But an SCR with a four-layer structure often has a slow turn-on speed, which could be too slow to protect an SoC with ultrathin gate oxide. If an SCR device with some modified design or triggering circuits can have a fast enough turn-on speed, it will be the best choice for ESD protection in the SoC with VDD voltage levels below 1.2 V, without causing latch-up danger.

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