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Chapter 7

ESD (Electrostatic Discharge) Protection Design for Nanoelectronics in CMOS Technology

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Abstract. *In this tutorial, we teach useful on-chip ESD protection designs for CMOS integrated circuits. The contents include (1) Introduction to Electrostatic Discharge, (2) Design Techniques of ESD Protection Circuit, (3) Whole-Chip ESD Protection Design, and (4) ESD Protection for Mixed-Voltage I/O Interface. The clear ESD protection design concepts and detailed circuit implementations are presented in this course. ESD protection design is more important in the nanoscale CMOS technology. High ESD robustness can not be achieved with only process solutions. The circuit design solutions should be added into the chips with suitable layout arrangement to achieve the purpose of whole-chip ESD protection for IC products.*

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7.1 Introduction to Electrostatic Discharge (ESD)

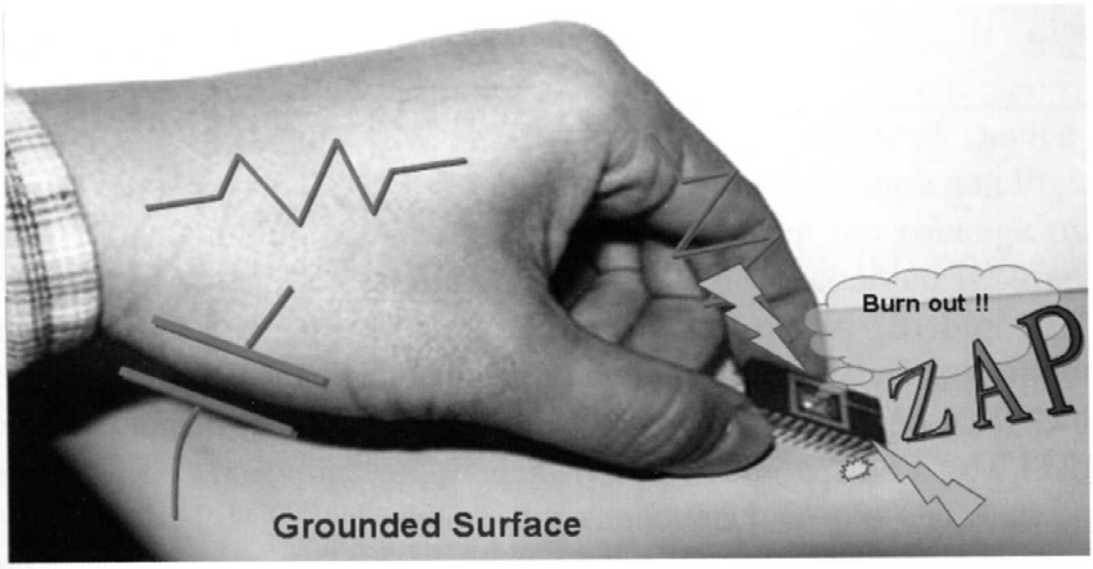
Electrostatic discharge (ESD) phenomenon often happens between two or more objects with different electrostatic potentials. ESD phenomenon has been known as a serious problem for IC products fabricated by the advanced deep-submicron and nanoscale semiconductor process technologies. In the scaled-down CMOS processes, the MOS devices with shallower junction depth, thinner gate oxide, lightly-doped drain (LDD) structure, and slicided diffusion have better circuit performance of higher operating speed and lower operating power, but they become weaker to ESD stresses. Devices are usually damaged by ESD due to the rapidly generated heat or the rapidly created strong electrical field. To predict the ESD immunity level, or to find the ESD sensitive (weak) point of the ICs, there are several organizations to issue ESD test standards. They are ESDA (Electrostatic Discharge Association), AEC (Automotive Electronics Council), EIA/JEDEC (Electronic Industries Alliance / Joint Electron Device Engineering Council), and MIL-STD (US Military Standard). The dominant ESD test methods on component-level IC products are known as HBM (Human Body Model) [1], MM (Machine Model) [2], and CDM (Charged Device Model) [3].

7.1.1 ESD Standards and Models

7.1.1.1 Human Body Model (HBM)

The actual ESD event from the charged human body to the IC is shown in Fig. 7.1(a). A person with electrostatic potential to handle the IC to a grounded surface will cause the ESD current through the fingers of human body to the IC, and then to the grounded surface. The circuit diagram used to model this ESD event (called as Human Body Model, HBM) is shown in Fig. 7.1(b). The equivalent capacitance in the HBM to store the electrostatic charges is standardized as 100 pF, and the resistance in the HBM to discharge the electrostatic charges through human's finger is standardized as 1.5 kohm. The typical current peak of 2-kV HBM ESD event is $\sim$1.3Amp with a rise time of 5$\sim$10ns. With such fast ESD current discharging through the IC, it easily causes some serious damages on the I/O devices of the ICs, if there is no suitable ESD protection design in the ICs. The typical HBM ESD failure on the I/O devices of a 0.18-μm CMOS IC is shown in Fig. 7.1(c), where the I/O pin is zapped by a 1-kV HBM ESD stress. The obvious damages locate along the poly-gate between the

drain and source regions of an NMOS to cause the I/O pin shorting to ground.



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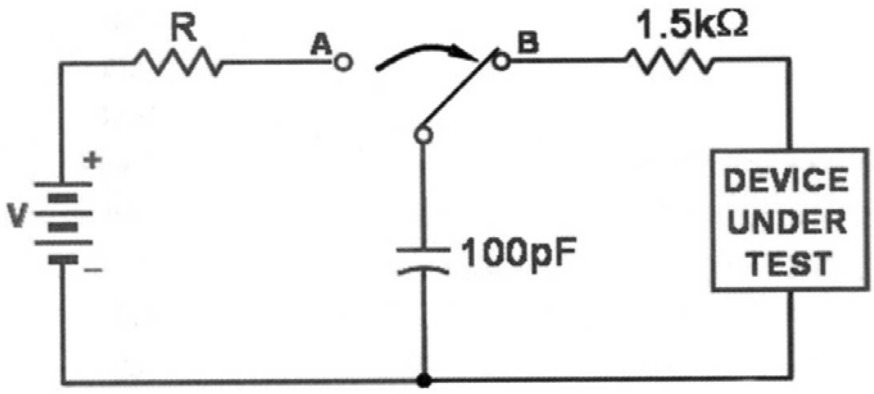

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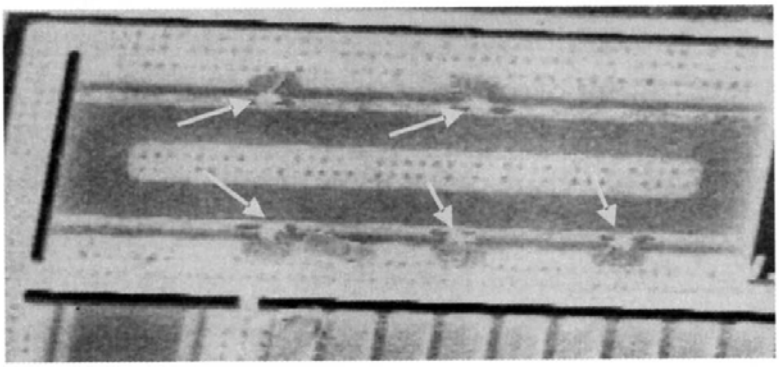
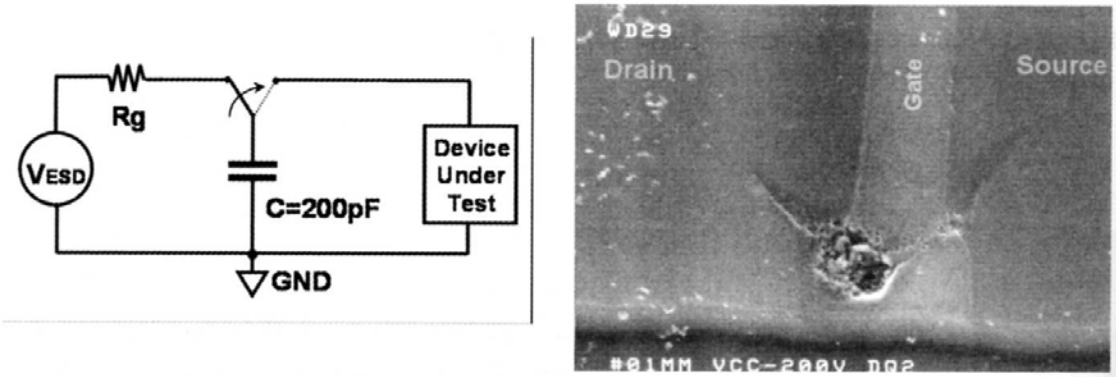


(c)

Figure 7.1: (a) ESD event from the charged human body to the IC. (b) The equivalent circuit of human body model (HBM) ESD event. (c) The typical ESD failure caused by HBM ESD stress on the I/O devices of CMOS IC.



(a) (b)

Figure 7.2: (a) The equivalent circuit of machine model (MM) ESD event. (b) The typical ESD failure caused by MM ESD stress on the output NMOS of CMOS IC.

7.1.1.2 Machine Model (MM)

The IC products often have huge volume for mass production. To handle such huge production volume, the automatic machines are used to process IC products during fabrication, assembly, and testing. The automatic machines could generate the ESD event to cause the ESD stress on the IC products. The circuit diagram for the Machine Model (MM) ESD event is shown in Fig. 7.2(a). The equivalent capacitance in the MM to store the electrostatic charges is standardized as 200 pF, and the resistance in the MM to discharge the electrostatic charges is ideally zero. But, actually, the parasitic resistance of several ohm and the parasitic inductance of several nH along the connection line from the capacitor (200 pF) to the device under test (DUT) will cause little ringing in the MM ESD current waveform. The typical current peak of 200-V MM ESD event is ~3.8Amp with a current ringing frequency of ~16MHz. The rise time (1~3ns) of MM ESD event is slightly faster than that of HBM ESD event, due to the absence of the discharging resistance of 1.5 kohm (HBM). With such faster ESD current discharging through the IC, it easily causes more serious damages on the I/O devices of the ICs. The typical ESD failure on the I/O devices of a 0.18-μm CMOS IC is shown in Fig. 7.2(b), where the I/O pin is zapped by a 200-V MM ESD stress. The obvious damage locates across the finger's end of the poly-gate between the drain and source regions of an output NMOS to cause the I/O pin shorting to ground.

7.1.1.3 Charged-Device Model (CDM)

The electrostatic charges could be also stored in the floating IC during the fabrication/assembly/testing processes. If the charged IC touches to the grounded surface, the electrostatic charges will be discharged from the body of IC to the external ground to cause the Charged Device Model (CDM) ESD event. The typical CDM ESD events are shown in Figs. 7.3(a) and 7.3(b). In Fig. 7.3(a), the IC dropping from the package tube will be charged with electrostatic charges. When the charged IC touches the grounded surface, the CDM ESD event will occur. In Fig. 7.3(b), the charged IC is isolated on the grounded surface. When a grounded tool or human's finger touches to this charged IC, the CDM ESD event will also occur. The typical equivalent model to show this CDM ESD event is shown in Fig. 7.3(c), where the capacitance in the CDM to store the electrostatic charges is dependent on the IC (with package) itself. For an IC with large die size or package, it will often have a large equivalent capacitance in this CDM ESD event. The charges (Q) stored in the CDM is Q=CxV. For a specified ESD voltage level of CDM, the larger capacitance (C) will cause the more charges stored in the IC body, which in turn causes a larger ESD current discharging from the pin that first touches to ground. So, the equivalent capacitance of CDM ESD event can not be standardized but dependent on the IC itself. The typical current peak of 1000-V CDM ESD event discharged from a capacitance of 4 pF is as large as ~15Amp with a rise time of only ~200ps. The discharging speed of CDM ESD event is much faster than those of HBM and MM ESD events. With such a very fast discharging, the gate oxide of I/O devices is easily damaged before the ESD protection device to effectively clamp the ESD overstress voltage on the I/O devices. The turn-on speed of ESD clamp device on the I/O pins will be a key issue for CDM ESD protection in the nanoscale CMOS processes with the ultra thinner gate oxide. With such a very fast CDM ESD current discharging through the IC, it easily causes serious damages on the gate oxide of I/O devices of the ICs. The typical ESD failure on the I/O devices of a 0.18-μm CMOS IC is shown in Fig. 7.3(d), where the IC is zapped by a 1000-V CDM ESD stress. The obvious damages locate on the poly-gate near to the drain side of an output NMOS to cause the gate of output NMOS shorting to its substrate.

The equivalent circuit of CDM event in an IC product with input buffer and input ESD protection circuit at the input pad is shown in Fig. 7.4(a), which is corresponding to the diagram shown in Fig. 7.3(c). The ESD clamp devices located around the input pad can provide ESD protection to the gate oxide of input buffer against HBM or MM ESD stresses. How-

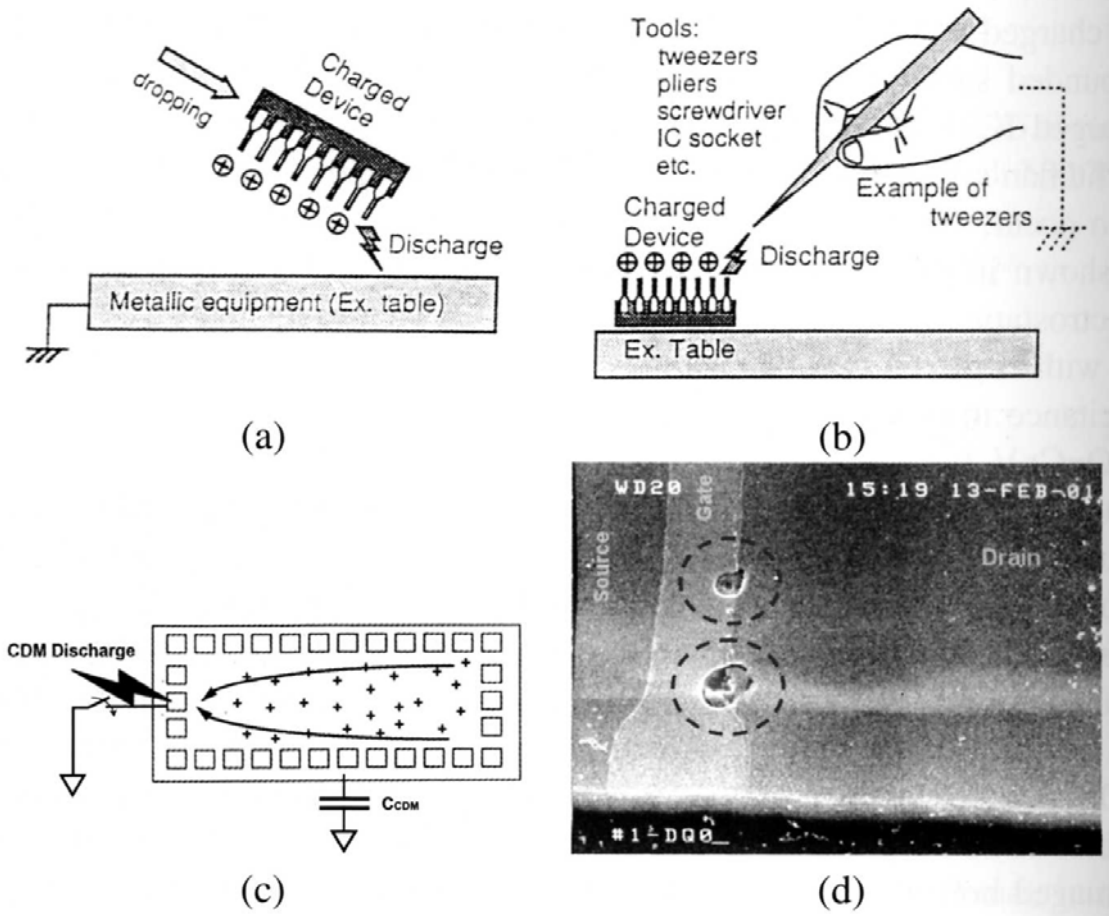


Figure 7.3: (a) The typical charged device model (CDM) ESD event caused by IC dropping from the package tube. (b) The typical CDM ESD event caused by a grounded tool or human's finger touching to the charged IC. (c) The equivalent model to show the CDM ESD event. (d) The typical ESD failure caused by CDM ESD stress on the output NMOS of CMOS IC.

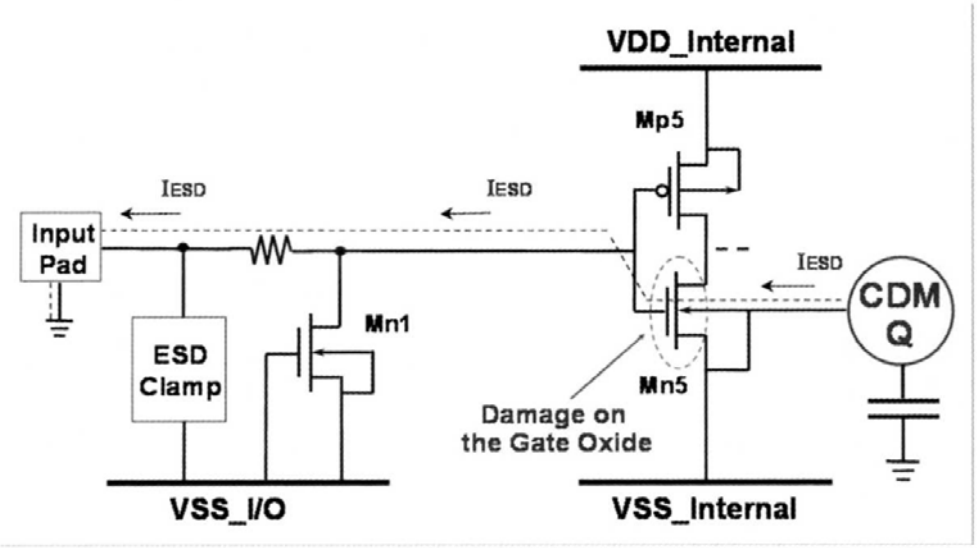
ever, in CDM ESD event, the static charges are initially stored in the body (substrate) of the IC. When the input pin is touched to external ground, the CDM charges are discharged from the body of chip to the external ground. For modern IC design with noise consideration, the VSS power line of I/O cells is often separated from the VSS power line of core logics to avoid switch noise coupling issue. With such separated VSS power lines in the chip, the CDM charges are mainly discharged as the dashed line shown in Fig. 7.4(a) to cause serious gate oxide rupture on the input device Mn5. A typical case of CDM ESD damage on an IC product is shown in Fig. 7.4(b), which is retuned from field application. In Fig. 7.4(b), the melting part is located just at the poly gate of Mn5 which is directly connected to the input pad. For the large scale CMOS IC (with a large capacitance for CDM charges storing in its body) fabricated in nanoscale CMOS processes (with the ultra thinner gate oxide), it will be more sensitive to such CDM ESD event.

7.1.2 ESD Testing

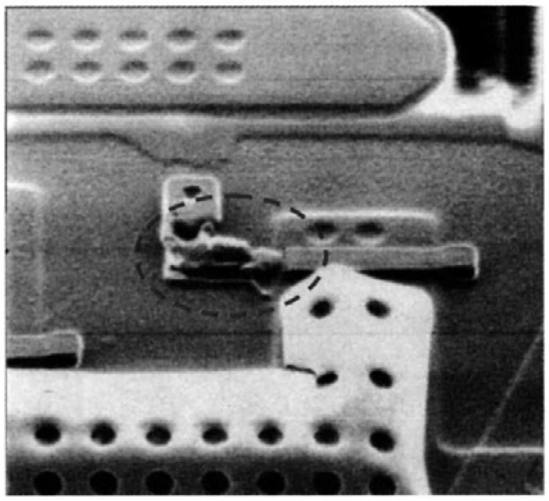
The ESD zapping to the pin of IC and the relatively grounded pin of IC during handling as that shown in Fig. 7.1(a) is random. Basically, the ESD could enters into some pin of the IC with some another pin relatively grounded. There is a lot of pin combination between the ESD-zapped pin and the relatively-grounded pin, during ESD occurrence to the IC. If every possible pin combination needs to be zapped by ESD stresses, it will waste too many time and IC samples to verify the ESD robustness of an IC product. To reduce the all possible pin combination for ESD verification, some ESD testing methods have been specified in the standards [1]–[3]. In the following subsection, the ESD testing methods will be described. The ESD simulators to generate the ESD waveforms for using to zap the IC products have been commercially produced.

7.1.3 ESD Testing for HBM / MM

Since the electrostatic charges stored on the human body or machine could be positive or negative relatively to the grounded surface. The HBM/MM ESD stress may have positive or negative voltage on an input (or output) pin of an IC, when the VDD or VSS pins is relatively grounded. In the worst case, the HBM/MM ESD is zapping to only one I/O pin of the IC when only one of the VDD or VSS pins is relatively grounded. So, there are four pin-combination modes for HBM/MM ESD zapping to an input (or output) pin. The four pin-combination modes for HBM/MM



(a)



(b)

Figure 7.4: (a) The equivalent circuit of CDM event in an IC product with input buffer and input ESD protection circuit at the input pad. (b) The typical CDM ESD failure on the input NMOS, where the melting part is located just at the poly gate of Mn5 which is directly connected to the input pad.

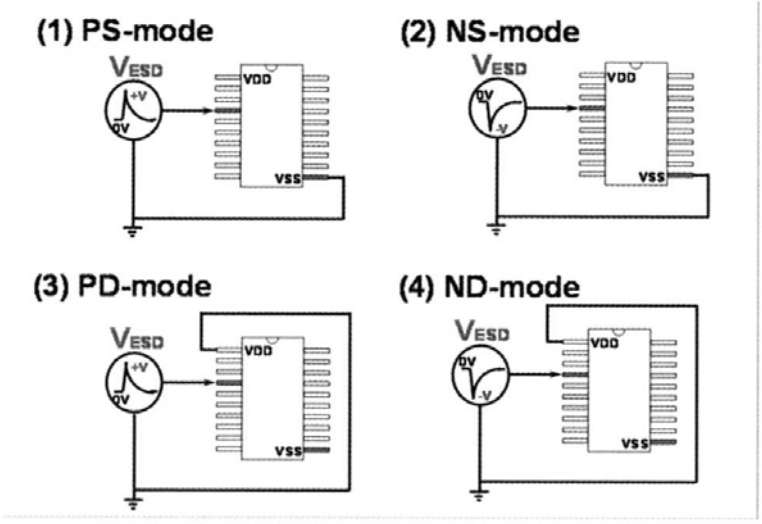


Figure 7.5: The four pin-combination modes for HBM/MM ESD zapping on the input or output pins, which are positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) ESD stresses on one I/O pin.

ESD zapping on the input or output pins are illustrated in Fig. 7.5, which are positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) ESD stresses on one I/O pin. The input or output ESD protection circuits are therefore designed to bypass the ESD current from the stressed pin to the VDD or VSS pins. With the different relatively grounded VDD or VSS pins, the ESD levels of one I/O pin under these four modes of ESD stresses will be different. The typical example of HBM ESD test report on an IC product is shown in Table 7.1 for the I/O pins during these four modes of pin combination. The ESD level of one I/O pin under some ESD stress of pin combination is often defined at the ESD voltage that causes the voltage point at 1-μA of the I-V curve (seen from the I/O pin to VDD or VSS) shifting more than 20% (or 30%) from its original I-V curve (before ESD zapping). Or, in some applications, the ESD level of one I/O pin under some ESD stress of pin combination is defined at the ESD voltage that causes the I/O pin out of its specifications (such as the leakage current of 1μA, or some circuit performances). The OK mark in the Table 7.1 means that the pin under the HBM ESD stress can pass the highest 8kV level (the maximum voltage level that the ESD simulator can apply).

As seen in the Table 7.1, for example the pin #5, it can sustain the HBM ESD levels of 4250V, -500V, 4000V, and -5750V, when this pin #5 is zapped in the PD-, ND-, PS-, and NS-mode ESD stresses, respectively. Even if this pin #5 can sustain the HBM ESD stress of greater than 4000V

Table 7.1: The HBM ESD test report for the I/O pins of an IC product during the four modes of pin combination.

Zapping Mode / Test Pin	VDD(+) PD-Mode	VDD(-) ND-Mode	VSS(+) PS-Mode	VSS(-) NS-Mode
Pin #2	2500	-1000	500	OK
Pin #3	1750	-500	500	OK
Pin #4	7250	OK	7000	OK
Pin #5	4250	-500	4000	-5750
Pin #6	5000	-2500	4500	-3000
Pin #7	3000	OK	4500	-7000
Pin #8	7250	OK	7250	OK
Pin #9	2000	-1000	500	OK
Pin #10	2250	OK	750	OK
Pin #11	6500	-750	500	OK
Pin #12	1500	OK	500	OK

OK: > 8000

in some pin-combination modes, it has an ESD robustness of only 500V in the ND-mode ESD stress. However, the HBM ESD level of this pin #5 in the Table 7.1 is defined at only 500V, but not 4000V. The lowest absolute magnitude of ESD voltages zapping to this I/O pin to cause any damage in this IC is defined as the ESD robustness of this I/O pin. With different pin-combination of ESD stresses (PD-, ND-, PS-, and NS-modes) at the same I/O pin, the ESD current flowing paths in the IC will be different. The different ESD current paths flow through the IC often to cause ESD damages at different locations or different devices. Therefore, the HBM/MM ESD levels of an I/O pin under these four pin-combination modes should be different, as those shown in Table 7.1. So, each I/O pin could have the different HBM/MM ESD level in the same IC product.

Besides the four modes of ESD stresses on one I/O pin, the ESD current may enter into any pin and go out from another pin (not the VDD or VSS pins) of the IC. The ESD voltage may cross any two pins of the IC and cause some unexpected ESD damages in the internal circuits. To verify such ESD stress, two additional pin-combinations for ESD testing, the pin-to-pin ESD stress and the VDD-to-VSS ESD stress, had been specified in the HBM/MM ESD testing standards [1]–[2]. These two additional pin-combinations for ESD testing are illustrated in Figs. 7.6 and 7.7. In the pin-to-pin ESD stress of Fig. 7.6, the positive or negative ESD voltage is zapped to the selected one I/O pin with all other I/O pins grounded,

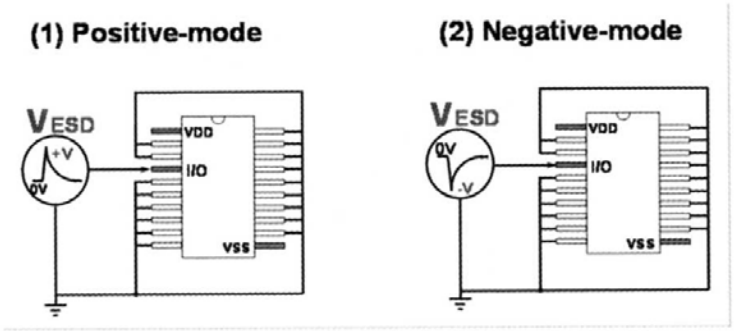


Figure 7.6: The pin-to-pin ESD stress, the positive or negative ESD voltage zapped to the selected one I/O pin with all other I/O pins grounded, whereas the power pins (VDD and VSS) are floating.

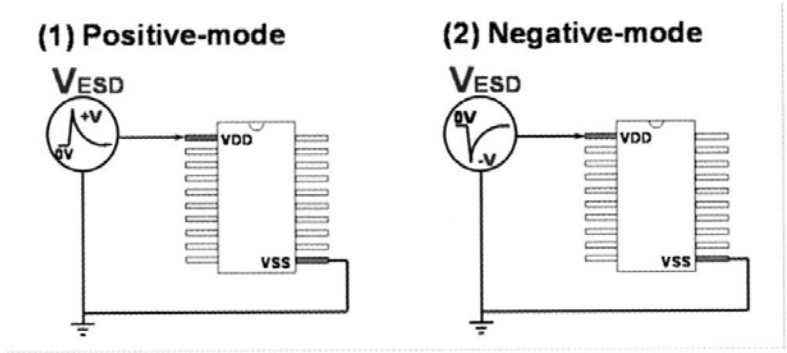


Figure 7.7: The VDD-to-VSS ESD stress, the positive or negative ESD voltage zapped to the VDD pin with the VSS pin grounded, whereas all I/O pins (non-power pins) are floating.

whereas the power pins (VDD and VSS) are all floating. In the VDD-to-VSS ESD stress of Fig. 7.7, the positive or negative ESD voltage is zapped to the VDD pin with the VSS pin grounded, whereas all I/O pins (non-power pins) are floating.

In these two additional pin-combinations for ESD testing, the internal circuits are more vulnerable to ESD damage even if there is input or output ESD protection circuits in the ICs [4]–[9]. The ESD damages located in the internal circuits (not on the I/O circuits) are more difficult to be found by only measuring the leakage current on the input or output pins. Complex failure analyses with full function verification are often required to find the failure location. To avoid ESD damages in the ICs during these two additional pin-combination ESD stresses, the power-rail (VDD-to-VSS) ESD clamp will play the key important role to achieve the whole-chip ESD protection design [10]. For the IC with more than one VDD or VSS pins, the more detailed pin combinations for ESD test on the IC with multiple power pins have been specified in the standards [1]-[3]. The ESD protec-

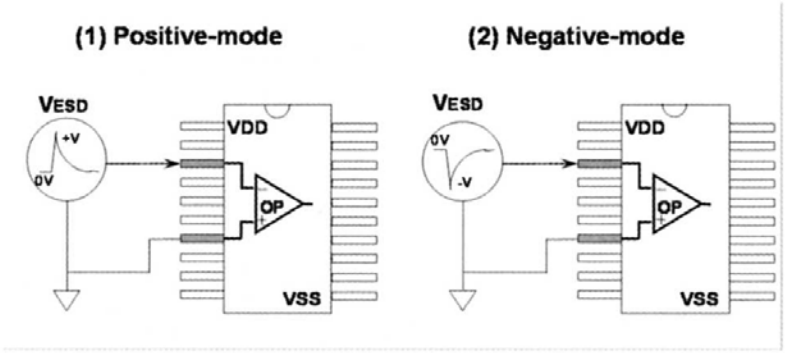


Figure 7.8: The pin combination of the additional analog pin-to-pin ESD stress to verify the ESD level of analog circuits with the operational amplifier or differential input stage.

tion design for the IC with multiple power supply pins (or even with power pins of different voltage levels) become more complex and difficult. One of the effective solutions for designing the IC with multiple power pins to have good enough ESD robustness is to use the ESD buses [11]. For more details, please see the papers in the references list.

Except for the above ESD-zapping pin combinations, an additional pin-to-pin ESD stress had been especially specified in some earlier standard for the analog circuits with operational amplifiers or differential input stages to verify the ESD level of analog pins. The analog pin-to-pin ESD stress for the differential input pins of an operational amplifier is illustrated in Fig. 7.8, where the positive or negative ESD voltage is applied to the inverting input pin with the corresponding non-inverting input pin relatively grounded. During such an analog pin-to-pin ESD stress, all the other pins including both the VDD and VSS pins are floating. The ESD current during such an analog pin-to-pin ESD stress is illustrated in Fig. 7.9 with the differential input stage of an operational amplifier. Because of the lack of series resistor between the analog input pad and the internal circuits (for the most analog signal request), the overstress ESD current easily reaches to the thinner gate oxide of the differential input stage with a common-source circuit structure. If the VSSA power connection between the inverting input pin and the non-inverting input pin has a long metal line in the IC layout, the gate oxide of the differential input stage is easily ruptured by the ESD voltage to cause a discharging current path as the dashed line shown in Fig. 7.9. The ESD clamp device (such as the large-dimension gate-grounded NMOS) between the inverting input pad and the VSSA power line can not provide effective ESD protection against this additional analog pin-to-pin ESD stress. Therefore, some modified ESD protection designs should be included into the analog ESD protection circuit to overcome this

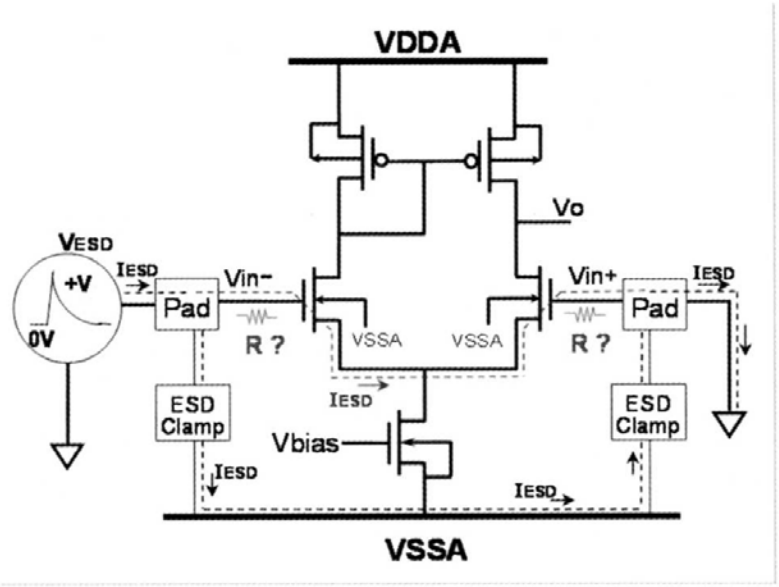


Figure 7.9: The ESD current path during the analog pin-to-pin ESD stress.

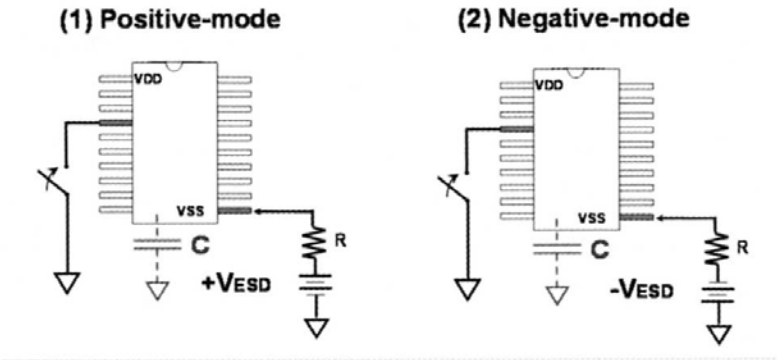


Figure 7.10: The ESD testing to verify CDM ESD level of IC product.

analog pin-to-pin ESD-stress issue.

7.1.3.1 ESD Testing for CDM

In the HBM/MM ESD events, the electrostatic charges are initially stored in the human body / machine, which are not stored in the IC. But, in the CDM ESD event, the electrostatic charges are initially stored in the body of IC itself. So, the pin combination for verifying ESD robustness of IC product in CDM ESD stress is quite different to that in HBM/MM ESD stresses. The ESD testing to verify CDM ESD level of IC product is shown in Fig. 7.10. The positive or negative ESD voltage (generated from a high-voltage generator) is initially installed into the body of IC through a resistor (in the order of Mega-ohm). The pin to be charged with ESD voltage is the pin that directly connected to the body (substrate) of the IC, which is often

Table 7.2: The ESD levels of an IC product in the three ESD models are briefly classified into three grades.

	HBM	MM	CDM
Okay	+/- 2kV	+/- 200V	+/- 1kV
Safe	+/- 4kV	+/- 400V	+/- 1.5kV
Super	+/- 10kV	+/- 1kV	+/- 2kV

the VSS (or GND) pin of the most logic IC with the p-type substrate. After the IC is charged up to the specified voltage level, some of the I/O pins is touching to ground. The charges stored in the IC body will be discharged out from the IC through the selected I/O pin (that is touching to ground) to simulate the CDM ESD events. Every I/O pin and the power (VDD) pin are requested to be discharged to verify the CDM ESD level of the IC product. The equipment to provide CDM ESD testing had been developed. Because the CDM ESD discharging way is quite different to that of HBM/MM ESD events, the on-chip ESD protection design for CDM ESD [12]-[16] is different to that for HBM/MM ESD protection.

The typical ESD levels of an IC product among these three ESD models are briefly classified into three grades in Table 7.2. For different ESD standards, there are more detailed classified grades. For commercial IC products, the HBM, MM, and CDM ESD levels are often specified as $\pm$2000V, $\pm$200V, and $\pm$1000V for the okay grade. For an IC with HBM ESD level of $\pm$2000V, this implies that the HBM ESD stresses of $\pm$2000V zapping to the pins of IC among all different pin combinations of ESD stresses do not cause any failure to the IC (including I/O leakage and circuit static/dynamic functions). So, how to design effective on-chip ESD protection with high enough ESD robustness to against these three (HBM, MM, and CDM) ESD stresses under almost-random pin combinations is a very challenging task to IC designers, especially when the IC is fabricated by the nanoscale CMOS processes with the more ESD-weak MOS devices.

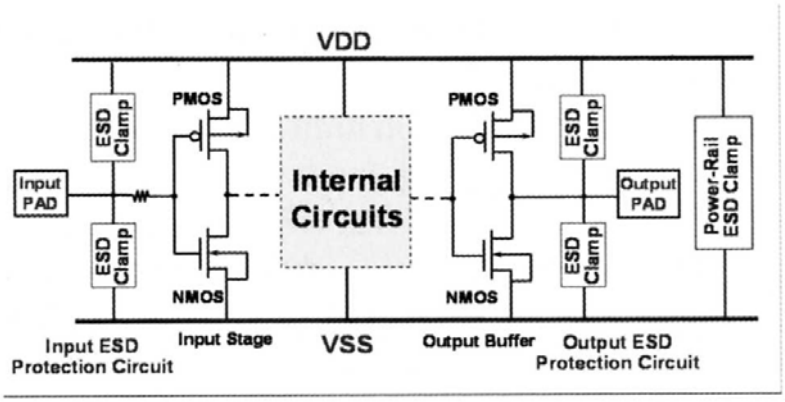


Figure 7.11: The concept of on-chip ESD protection design.

7.2 Design Techniques of ESD Protection Circuit

7.2.1 Basic ESD Protection Concept

To avoid the damages from the HBM/MM ESD stresses under almost-random pin combinations, the concept of on-chip ESD protection design is shown in Fig. 7.11. For every input or output pin, there are ESD clamp devices placed from the pad to VDD and VSS power lines to discharge the four modes of ESD stresses (shown in Fig. 7.5) on the I/O pin. To overcome the ESD stresses in the pin-to-pin ESD stresses (shown in Fig. 7.6) and in the VDD-to-VSS ESD stresses (shown in Fig. 7.7), the power-rail ESD clamp circuit must be placed between the VDD and VSS power lines of the IC [10]. The devices those can be realized in general CMOS processes are the resistor, diode, NMOS/PMOS, field-oxide device (FOD), vertical/lateral bipolar junction transistor (BJT), SCR device (p-n-p-n structure), and capacitor/inductor. The ESD clamp devices or circuits are therefore built up with those devices to sustain the requested ESD levels (such as HBM of 2000V, MM of 200V, and CDM of 1000V). The typical I-V curves among those devices are shown in Figs. 7.12(a) $\sim$ 7.12(d). The ESD generated power (= heat/time) can be theoretically calculated as Power= I_{ESD} x V_{op}, where the I_{ESD} is the ESD current conducted through the device, and the V_{op} is the operating voltage of the device under ESD stress. I_{ESD} is related to ESD specification, which is defined by product request. However, the V_{op} of device can be different in the forward-biased condition and reverse-biased condition. The ESD-generated heat will burn out the junction or cause contact spiking. To have a minimum ESD-generated heat under the specified ESD level, only the diode in forward-biased condition

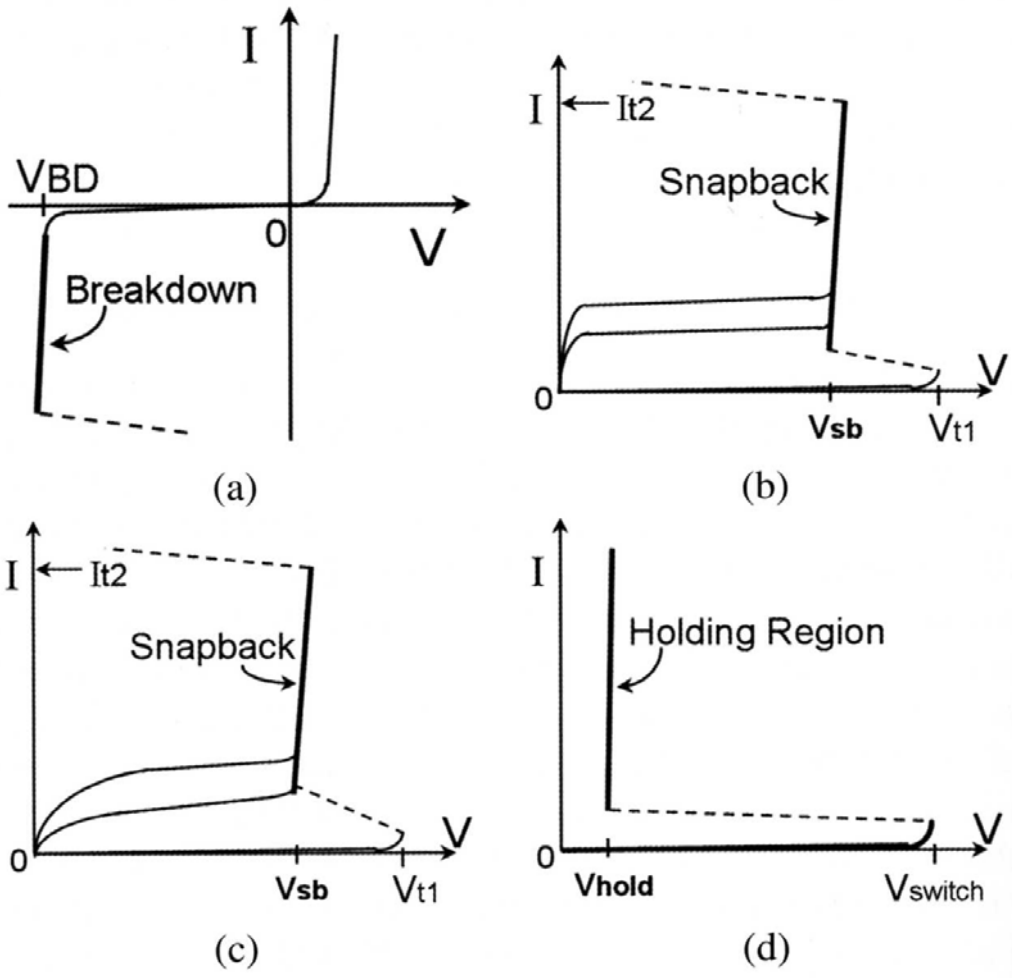


Figure 7.12: The I-V characteristics of ESD protection devices in (a) diode, (b) NMOS, (c) field-oxide device (lateral n-p-n BJT), and (d) SCR (p-n-p-n structure) in CMOS technology. The device, which has a lower operating voltage during ESD stress, can sustain a higher ESD level.

and the SCR in holding region have the smallest V_{op} of 1~2 V. Therefore, the diode in forward-biased condition and the SCR in holding region can sustain the highest ESD level within minimum silicon area among the ESD protection devices in CMOS technology.

To sustain a high enough ESD level, the devices used in the ESD clamp circuits should be drawn with the corresponding large enough device dimension or size to sustain the ESD-induced heat without causing burn-out or damage. However, the layout skill to draw the ESD clamp devices in a reasonable silicon area to sustain high enough ESD level must be optimized [17]-[19]. Some advanced area-efficient designs on the layout of ESD clamp devices to have high enough ESD level within a smaller layout area had been reported in [20]-[23].

7.2.2 Turn-on Uniformity of ESD Protection Devices

The PMOS and NMOS devices in the output buffers are also often working as the ESD clamp devices to protect the I/O pin without adding extra ESD clamp device to the pad. To provide the enough driving current to the external loading and to sustain the high enough ESD stresses, the NMOS / PMOS of output buffers are often designed with a channel width of several hundreds micrometer. Such ESD protection devices with larger device dimensions are often realized with multiple fingers to reduce total layout area [17]. But, during ESD stress, the multiple fingers of ESD protection MOSFET cannot be uniformly turned on. Only several fingers of the MOSFET were turned on and therefore damaged by ESD [24]. This often causes a low ESD level in ESD protection circuit, even if the MOSFET has a large device dimension. To improve the turn-on uniformity among those multiple fingers, the gate-driven technique [25]-[28] or substrate-triggered technique [29]-[34] had been reported to increase ESD robustness of the large-device-dimension NMOS. The circuit schematics for gate-driven design and substrate-triggered design are shown in Figs. 7.13(a) and 7.13(b), respectively. Recently, ESD robustness of the gate-driven NMOS had been found to be decreased dramatically when the gate voltage is somewhat increased [23], [28]. The gate-driven design causes large ESD current discharging through the strong-inversion channel of NMOS [35], therefore NMOS is easily burned out by ESD energy. The gate-driven and substrate-triggered techniques can improve the turn-on uniformity of the large-dimension ESD protection devices. But, the higher gate bias can induce larger channel current and higher electric field across gate oxide to damage MOSFET from the explication of energy band diagrams [35]. This effect causes the degradation of ESD robustness in gate-driven de-

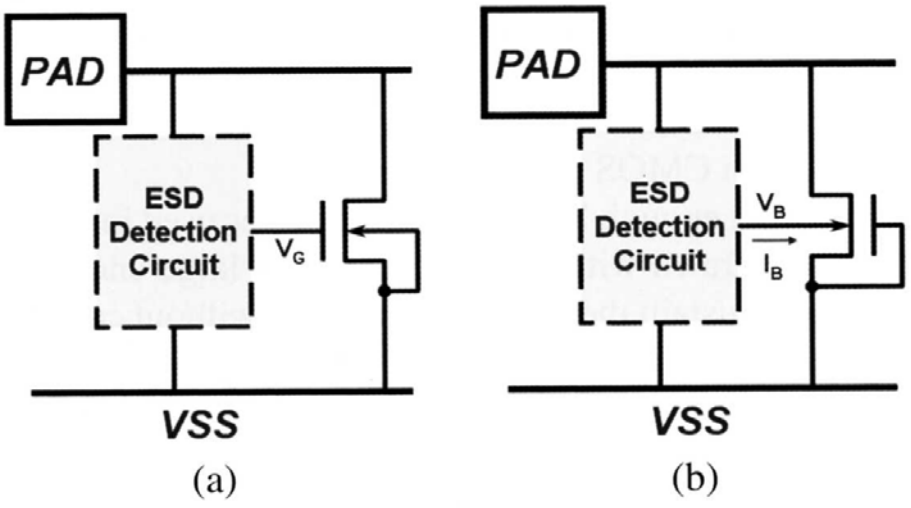


Figure 7.13: To improve turn-on uniformity among the multiple fingers of NMOS for ESD protection by (a) gate-driven design and (b) substrate-triggered design.

vices. Comparing to the gate-driven design, the substrate-triggered design can avoid the forming of channel current and enhance the space-charge region to sustain higher ESD current far away from the channel surface. Therefore, the substrate-triggered design can be one of the most effective solutions to improve ESD robustness of CMOS devices in nanoscale CMOS technologies [36].

The typical circuit design to realize the output NMOS with substrate-triggered technique is shown in Fig. 7.14 [34], where the gate of output NMOS Mn3 is controlled by the pre-buffer circuit. The R3, C3, and Mp4 form the substrate-triggered circuit to the bulk of Mn3. The Rsub is the parasitic substrate resistance from the triggering node in the layout to the guard ring (P+ diffusion) of the output NMOS. During normal circuit operating (with VDD and VSS biases), the gate of Mp4 is biased at VDD through R3. So, the Mp4 is kept off and the bulk of Mn3 is biased at VSS by the guard ring (P+ diffusion) that is often drawn to surround the NMOS in chip layout. With Mp4 kept off, there is no influence to the output function of this output buffer. During PS-mode ESD stress (VDD floating, VSS grounded), the positive ESD voltage is zapping on the output pad. The floating VDD in PS-mode ESD stress has an initial voltage level of $\sim$0V when the VSS is grounded. So, the gate of Mp4 is initially with a voltage level of $\sim$0V. When the positive ESD voltage appears on the output pad, the Mp4 with an initial low voltage level will be turned on to conduct some ESD current through Mp4 and inject into the bulk of Mn3. Therefore, the Mn3 is triggered on by this substrate-triggered cur-

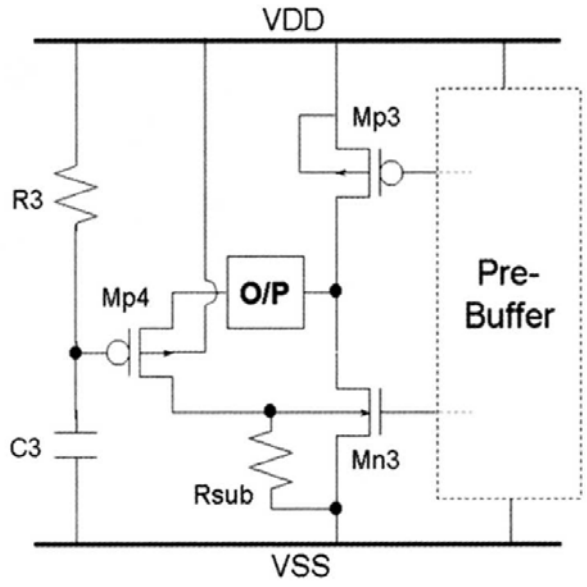


Figure 7.14: The circuit design to realize the output NMOS with substrate-triggered technique, where the gate of output NMOS Mn3 is controlled by the pre-buffer circuit. The R3, C3, and Mp4 form the substrate-triggered circuit to the bulk of Mn3. The Rsub is the parasitic substrate resistance from the triggering node in the layout to the guard ring (P+ diffusion) of the output NMOS.

rent to discharge ESD current from the output pad to grounded VSS. The turn-on time of Mp4 during such PS-mode ESD stress can be adjusted by the RC time constant of R3 and C3. From the experimental result verified in a 0.18-μm CMOS process, the HBM ESD robustness of output NMOS (W/L=200μm/0.3μm) can be significantly improved from the original ~0.5 kV to ~3 kV by this substrate-triggered design. The improvements of HBM ESD levels on the device channel widths of output NMOS with or without this substrate-triggered design are shown in Fig. 7.15.

7.2.3 ESD Implantation and Silicide Blocking

Besides the layout or triggering techniques to improve ESD robustness of the ESD clamp devices within a limited layout area, some process modifications had been developed with extra masking layers to increase ESD robustness of I/O devices for ESD protection. To enhance ESD robustness of these clamp devices, ESD implantations had been reported for including into process flow to modify device structures for ESD protection [37]-[43]. The N-type ESD implantation was used to cover the LDD peak structure and to make a deeper junction in NMOS device for ESD protection [37], [38]. The P-type ESD implantation located under the drain junction of the

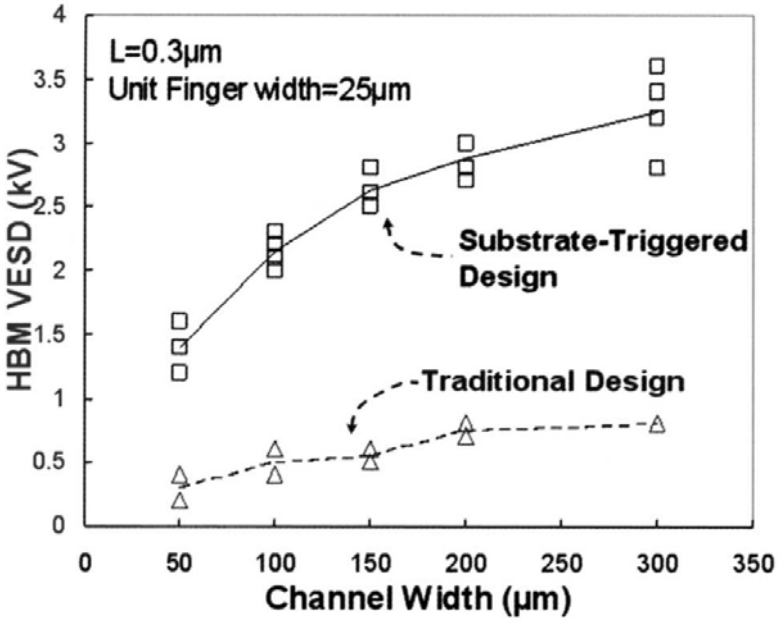


Figure 7.15: The improvements of HBM ESD levels on the device channel widths of output NMOS with or without the substrate-triggered design. This result was verified in a 0.18-μm CMOS process with 1.8-V gate oxide.

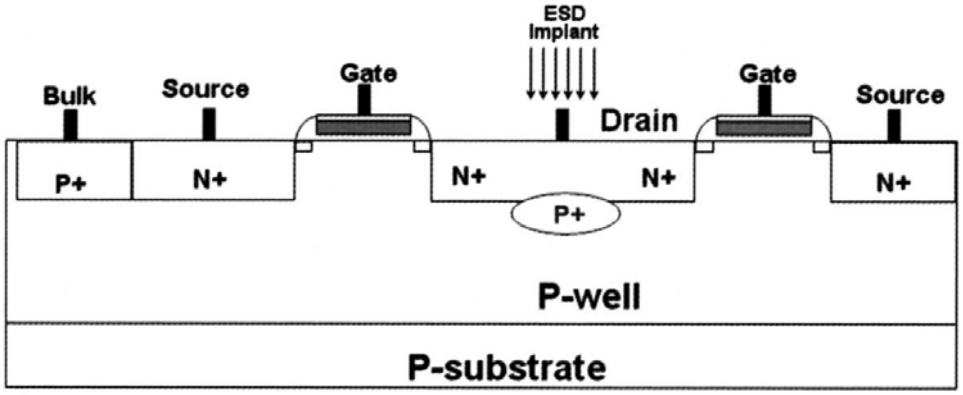
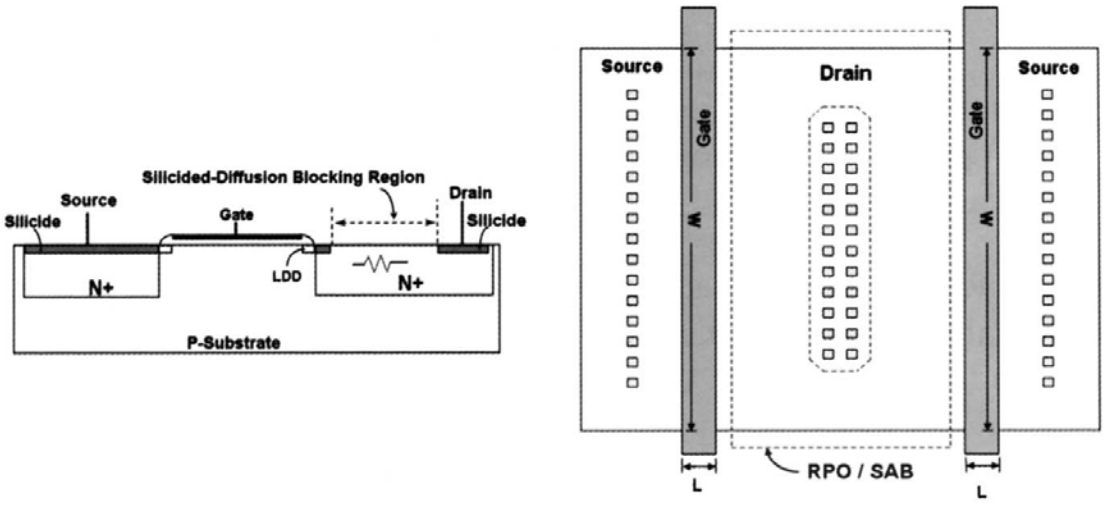


Figure 7.16: The device structure of NMOS with p-type ESD implantation under the drain junction to improve ESD robustness.

NMOS was used to reduce the reverse junction breakdown voltage, and to earlier turn on the parasitic lateral bipolar of NMOS [39], [40]. The device structure with this additional p-type ESD implantation is shown in Fig. 7.16. With higher doping concentration, the P-type ESD implantation can be also used to reduce the reverse junction breakdown voltage of diode or field-oxide device, and to sustain higher ESD robustness under reverse-biased condition [41]. Moreover, both of the N-type and P-type ESD implantations were used in NMOS device to wish a higher ESD robustness [42]. The experimental comparison among those different ESD implantations for ESD protection in the same CMOS process had been in-



(a) (b)

Figure 7.17: (a) The device structure of NMOS with silicide blocking at the drain diffusion to improve ESD robustness. (b) The corresponding layout pattern on NMOS with silicide blocking mask layer (called as RPO or SAB in some foundry's design rules.

vestigated in [43]. A modified design on ESD implantation for NMOS to improve, especially, MM ESD robustness was reported in [44]-[45].

Another process solution for improving ESD robustness of I/O devices for ESD protection is to use extra masking layer to block the formation of silicided diffusion on the drain regions of the output devices those connected to the I/O pad [46]-[52]. The device structure with silicide blocking is shown in Fig. 7.17(a), and the corresponding layout style to realize the silicide blocking mask is shown in Fig. 7.17(b) with a mask layer name of RPO or SAB in some foundry's design rules. Without using the extra masking layer to block the silicided diffusion, the layout design by drawing the N-well into the drain region of NMOS had been developed to block the formation of silicided diffusion in the drain regions of I/O devices to improve ESD robustness [53]-[54]. Recently, the dummy gate has been also used to block the formation of silicided diffusion in the drain regions of I/O devices without using the extra masking layer [55]-[56].

7.2.4 Some ESD Protection Guidelines

Some of guidelines to design the ESD clamp devices or circuits for the I/O pins or power pins are listed in the following :

1. Provide the IC with efficient ESD protection scheme to bypass any ESD stress while the IC is in the ESD-stress conditions;

2. Pass the normal I/O signals and keep inactive while the IC is in normal operating conditions;

3. Reduce the input capacitance and resistance to meet acceptable I/O signal delay (as small as possible);

4. Have a high ESD robustness within a reasonable layout area (layout area as small as possible);

5. Maintain a high latchup immunity in the CMOS IC's (all the I/O devices and ESD protection devices have to be surrounded by guard rings);

6. Fabrication of such ESD protection devices can be compatible to the process technology (without increasing the additional mask layers or modifying the process steps as possible);

7. Without interrupting the I/O circuit applications (such as high-voltage-tolerant I/O applications, or power-down operations).

7.3 Whole-Chip ESD Protection Design

In the pin-to-pin ESD stress of Fig. 7.6, the ESD voltage across the two pins can be transferred to become across the VDD and VSS power lines of the IC. The ESD current discharging paths in the IC under the pin-to-pin ESD stress condition are illustrated in Fig. 7.18, where a positive ESD voltage is applied to an input pin with some output pin relatively grounded, but both the VDD and VSS pins are floating. The positive ESD voltage on the input pad may be discharged through the input protection diode Dn1 to the floating VSS power line, and then discharged through the output NMOS to the grounded output pin. But, before the diode Dn1 breaks down to discharge the ESD current, the ESD current is transferred into the floating VDD power line through the forward-biased diode Dp1 in the input ESD protection circuit. The ESD current is therefore conducted into the internal circuits through the VDD power line and discharged through the internal

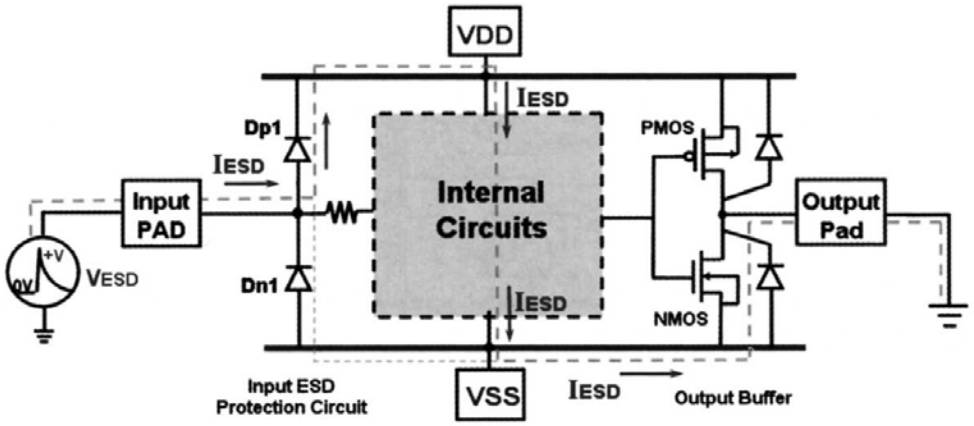


Figure 7.18: The ESD current paths through the IC under the pin-to-pin ESD test condition, where a positive ESD voltage is applied to some input pin while another output pin is grounded.

circuits to VSS. In the VDD-to-VSS ESD testing condition of Fig. 7.7, the ESD voltage is directly applied to the VDD pin with the VSS pin grounded but all input and output pins are floating. The ESD current discharging path in this VDD-to-VSS ESD stress condition is illustrated in Fig. 7.19, where the ESD current is directly conducted into the internal circuits to cause some ESD damages in the internal circuits. The ESD damages in the internal circuits are difficult to be found by only measuring the leakage current on the input or output pins. Complex failure analyses with full function verification are often required to find the failure location.

In order to clamp the ESD overstress voltage across the power lines, the gate-grounded NMOS was used as the ESD clamp device between the VDD and VSS power lines, as shown in Fig. 7.20. In the pin-to-pin or the VDD-to-VSS ESD stresses, the ESD voltage across the VDD and VSS power lines of the IC is clamped by the gate-grounded NMOS in its snapback-breakdown condition. Because the ESD current is discharged through the gate-grounded NMOS, this gate-grounded NMOS has to be drawn with a larger channel length and width to protect itself. But, the device dimensions and layout spacings of the internal circuits are further reduced in the scaled-down CMOS technology. During the pin-to-pin or the VDD-to-VSS ESD stresses, the internal circuits with minimum device dimensions and spacings are easily damaged by the ESD overstress voltage before the gate-grounded NMOS with larger device dimension is broken down to bypass the ESD current. So, to really protect all the circuits in an IC, a suitable ESD protection circuit has to be placed between the VDD and VSS power lines of the IC to clamp the ESD overstress voltage across the power lines [10].

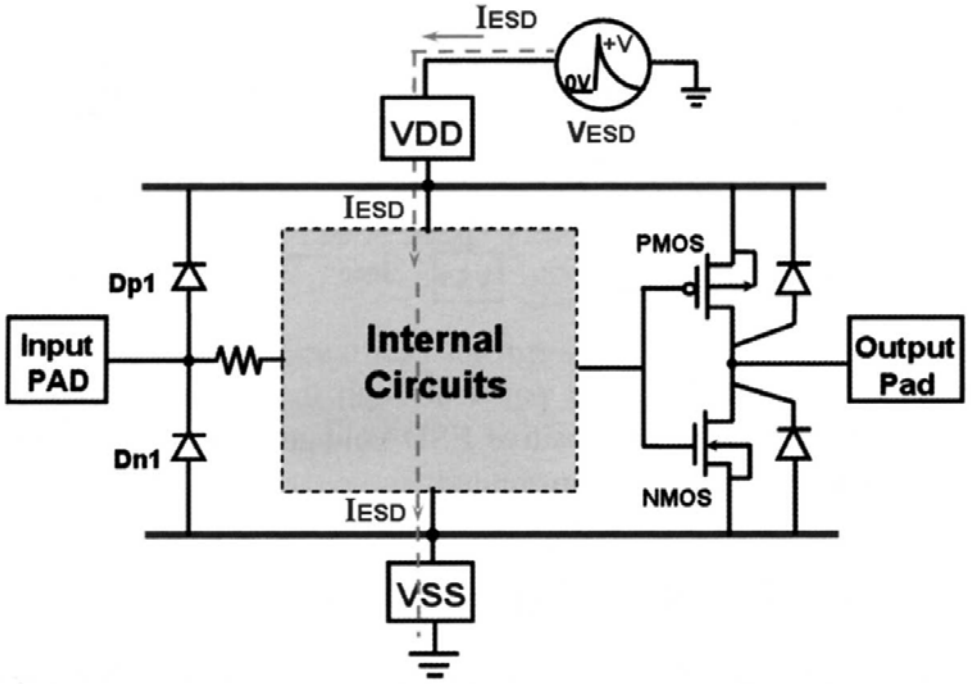


Figure 7.19: The ESD current discharging path through the IC under the VDD-to-VSS ESD test condition.

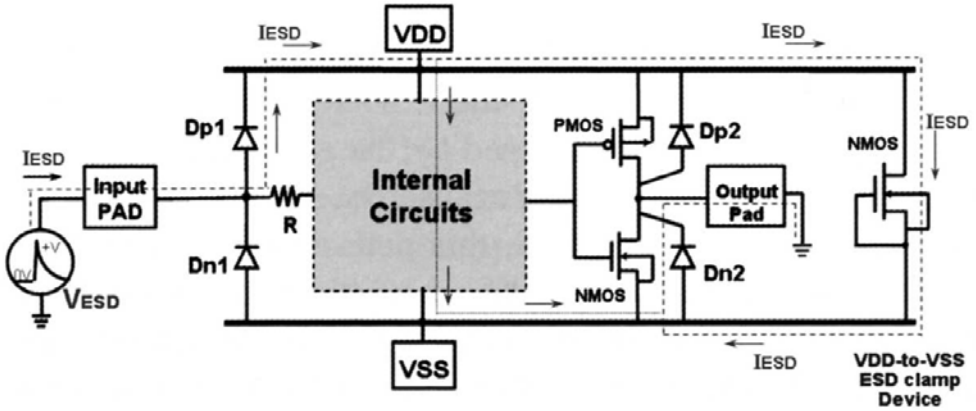


Figure 7.20: The ESD current discharging path through the IC under the pin-to-pin ESD test condition with a gate-grounded NMOS as the ESD clamp device between the VDD and VSS power lines.

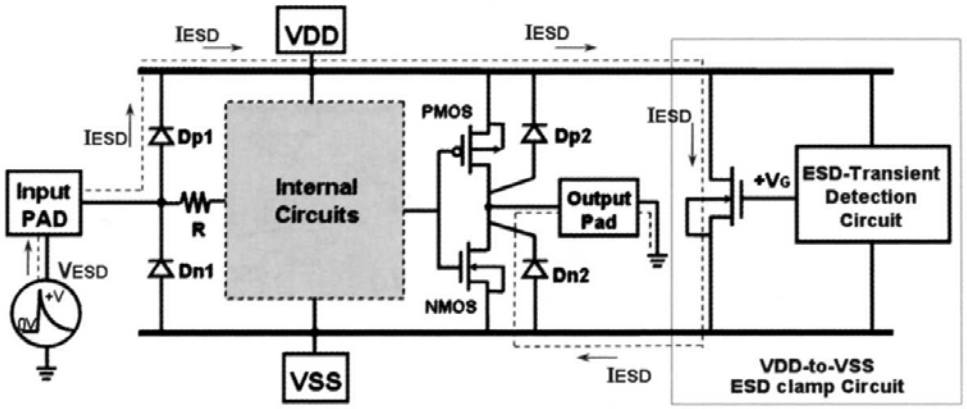


Figure 7.21: The ESD current discharging path through the IC under the pin-to-pin ESD test condition, where an effective VDD-to-VSS ESD clamp circuit is designed to achieve the whole-chip ESD protection.

7.3.1 Power-Rail ESD Clamp Circuit

To efficiently clamp the ESD voltage across the VDD and VSS power lines before the internal circuits are damaged, an ESD-transient detection circuit is used to turn on the VDD-to-VSS ESD-clamping NMOS, as illustrated in Fig. 7.21. The ESD-transient detection circuit is designed to detect the ESD event and sends a control voltage to the gate of the ESD-clamping NMOS. Because the ESD-clamping NMOS is turned on by a positive gate voltage rather than by the drain snapback breakdown, the NMOS can be turned on in time to bypass the ESD current before the internal circuits are damaged by the ESD overstress voltage. In the pin-to-pin ESD stress condition, the ESD current is diverted from the input pin into the floating VDD power line, as dashed line shown in Fig. 7.21. The floating VSS power line is initially biased at a ground level through the parasitic diode Dn2 in the output NMOS with a grounded output pin. Therefore, the ESD-transient detection circuit is biased by the ESD energy and turns on the ESD-clamping NMOS to provide a short-circuit path between the VDD and VSS power lines to bypass the ESD current. Thus, the ESD current can be efficiently discharged through the forward-biased diode Dp1, ESD-clamping NMOS, and the diode Dn2. The devices operating in the forward-biased conditions can sustain much higher ESD current than they operating in the reverse-biased breakdown conditions. But, when the IC is in the normal operating condition with the power supplies, this ESD clamp NMOS must be kept off to avoid the power loss from VDD to VSS.

To realize the aforementioned ESD-transient detection function, a simple *RC*-based VDD-to-VSS ESD clamp circuit is shown in Fig. 7.22. This ESD clamp circuit is designed to be turned on when the ESD voltage ap-

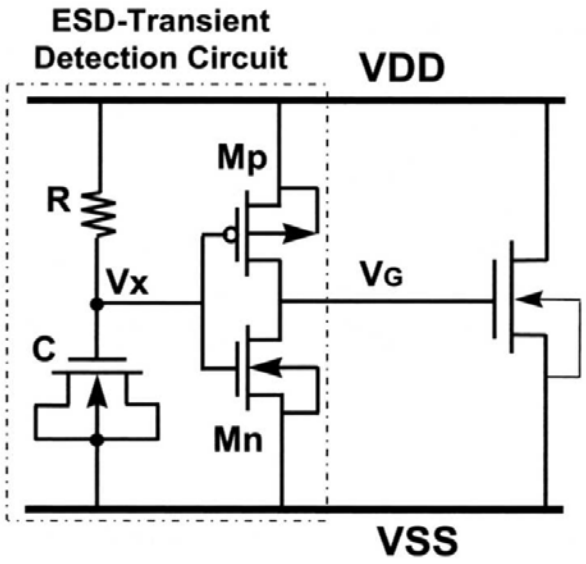
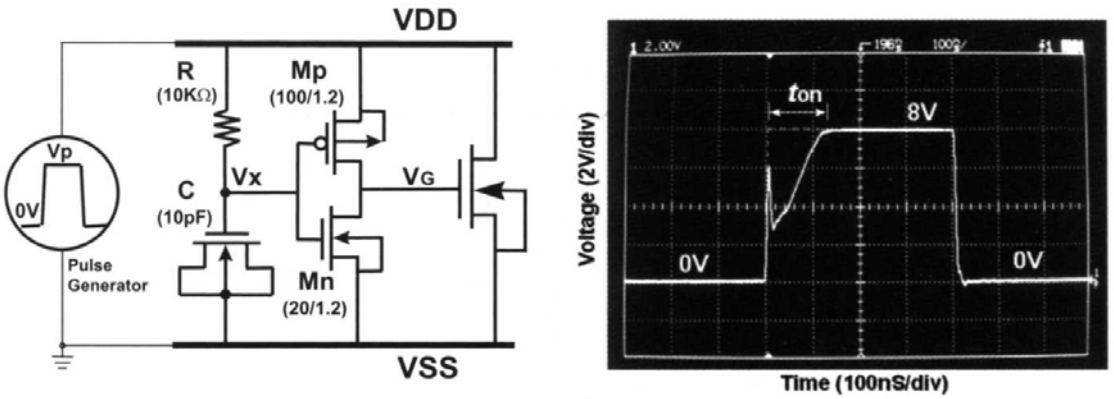


Figure 7.22: The efficient VDD-to-VSS ESD clamp circuit with RC-based ESD detection circuit.

pears across the VDD and VSS power lines. But, this ESD protection circuit is kept off when the IC is under the normal power-on condition. To meet these requirements, the *RC* time constant in the proposed VDD-to-VSS ESD clamp circuit is designed about 0.1 $\sim$ 1 μs to achieve the aforementioned operations.

Initially, the nodes Vx and VG have the voltage levels the same as the VSS level because the IC is in the floating condition without power supplies. The ESD voltage across the VDD and VSS power line will charge the capacitor C to rise up the voltage level of Vx in Fig. 7.22. The ESD voltage has a rise time about $\sim$10 ns. The voltage level of Vx is increased much slower than the voltage level on the VDD power line, because the RC circuit has a time constant in the order of μs. Due to the delay of the voltage increase on the node Vx, the Mp device is biased by the ESD voltage on the VDD power line and conducts a high voltage to the gate of the ESD-clamping NMOS. As the voltage on the node VG is greater than the NMOS threshold voltage, the ESD-clamping NMOS is turned on to bypass the ESD current from the VDD to the VSS power lines. The turned-on NMOS, which provides a short-circuit path between the VDD and VSS power lines, can clamp the ESD voltage across the VDD and VSS power lines to a very low voltage level. So, the internal circuits can be effectively protected without any ESD damage. The turn-on time ($t$on) of the ESD clamp NMOS can be adjusted by the RC time constant in the ESD-transient detection circuit.



(a) (b)

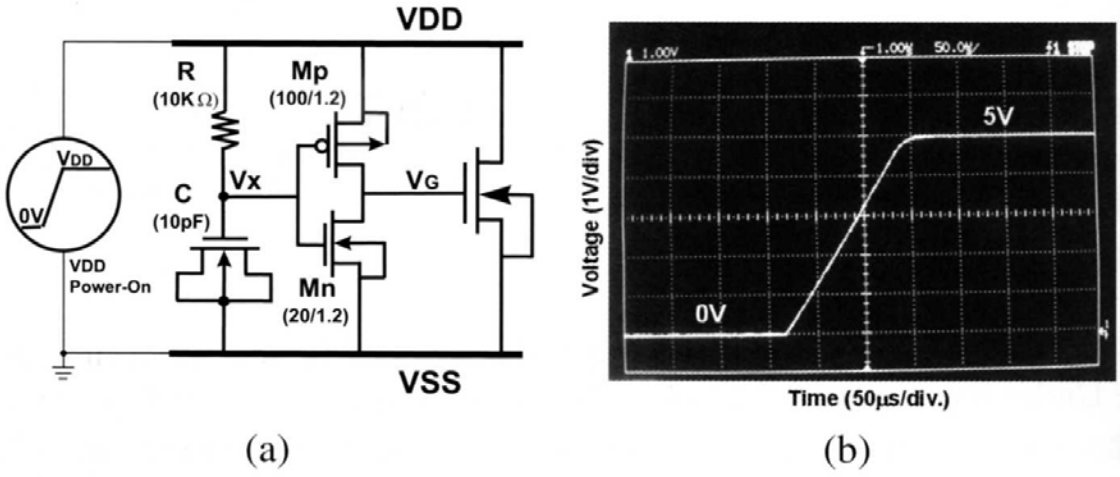
Figure 7.23: Turn-on verification on the VDD-to-VSS ESD clamp circuit with RC-based ESD detection circuit under the ESD stress condition. (a) The experimental setup used to simulate the ESD-stress condition, (b) the measured voltage waveform on the VDD power line.

Under the normal VDD power-on condition, the VDD power-on voltage waveform has a rise time in the order of milli-second (ms). With such a slow rise time of ms, the voltage level on the node Vx in the ESD-transient detection circuit with a RC time constant of μs can follow the VDD voltage in time to keep the Mp off. Because the Vx is simultaneously increased to the VDD voltage level in the VDD power-on condition, the Mn is turned on to keep the VG at a voltage level of 0V. So, the ESD clamp NMOS is guaranteed to be kept off when the IC is under the VDD power-on condition or in the normal operating conditions.

Due to the difference on the rise times between the ESD voltage and VDD power-on voltage, the VDD-to-VSS ESD clamp circuit provides a short-circuit path between the VDD and VSS power lines in the ESD-stress conditions, but it becomes a open circuit between the power lines in the VDD power-on condition. The device dimension of the ESD clamp NMOS is designed as large as possible to provide a much low turn-on resistance between the VDD and VSS power lines to quickly bypass the ESD current. But, an NMOS with a large device dimension also occupies a larger layout area. So, the device dimension of the ESD clamp NMOS is strongly dependent on the required ESD level and the specified layout area of the IC.

To verify the aforementioned ESD-transient detection function, an experimental setup is shown in Fig. 7.23(a), where a voltage pulse generated from the pulse generator is used to simulate the ESD pulse. The voltage pulse generated from the pulse generator initially has a square-type voltage

waveform with a rise time about 5ns. When the voltage pulse is applied to the VDD power line with the VSS grounded, the sharp-rising edge of the ESD-like voltage pulse will trigger on the ESD-clamping NMOS to provide a short-circuit path between the VDD and VSS power lines. Due to the limited driving current of the pulse generator, the voltage waveform on the VDD power line will be degraded by the turned-on ESD clamp NMOS. The degraded voltage waveform on the VDD power line is shown in Fig. 7.25(b), where a voltage pulse with a pulse height of 8V and a pulse



(a) (b)

Figure 7.24: Turn-on verification on the VDD-to-VSS ESD clamp circuit with RC-based ESD detection circuit during VDD power-on condition. (a) The experimental setup used to simulate the normal VDD power-on condition, (b) the measured voltage waveform on the VDD power line.

width of 400ns is applied to the VDD power line. The voltage waveform is degraded at the rising edge because the ESD clamp NMOS is simultaneously turned on when the ESD-like voltage pulse is applied to the VDD power line. The degradation on the voltage waveform is dependent on the turned-on resistance of the ESD clamp NMOS and the output resistance of the pulse generator. The maximum voltage drop from the 8-V voltage level in Fig. 7.23(b) is 5.2V. A larger device dimension of the ESD clamp NMOS leads to a more degradation on the voltage waveform. When the node Vx is charged up greater than the logic threshold voltage of the inverter (Mp and Mn) in the ESD-transient detection circuit, the ESD clamp NMOS will be turned off and the voltage waveform will be restored to the original voltage level. In Fig. 7.23(b), the applied 8-V voltage pulse has a degradation period about $\sim$135 ns, which is corresponding to the turn-on time of the ESD clamp NMOS.

To verify the action of the VDD-to-VSS ESD clamp circuit in the normal VDD power-on condition, an experimental setup is shown in

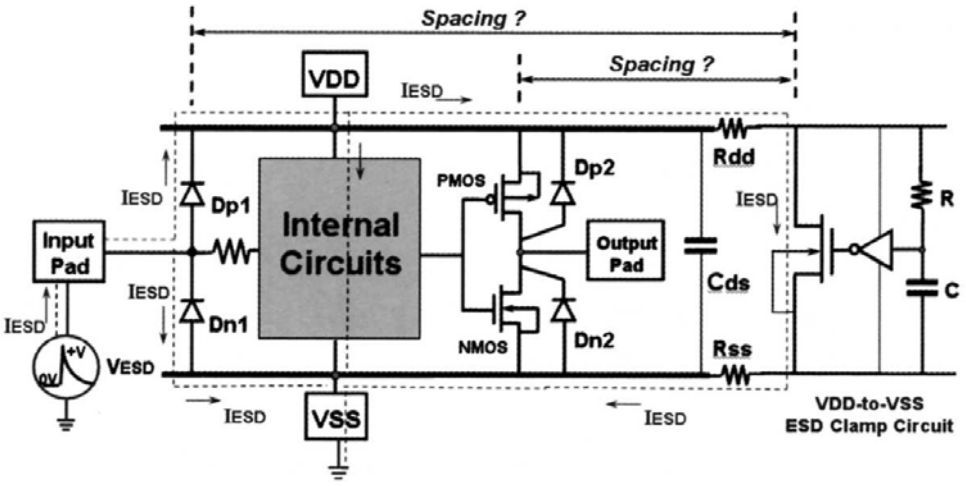


Figure 7.25: A schematic diagram to show the spacing effect on the ESD protection of a chip due to the parasitic resistance and capacitance along the VDD and VSS power lines.

Fig. 7.24(a). A ramp voltage with a rise time of 0.1ms and a high-level voltage of 5V is applied to the VDD power line with the VSS power line grounded to simulate the VDD power-on condition. The voltage waveform on the VDD power line is monitored and shown in Fig. 7.24(b), where the voltage waveform is still remained as a ramp voltage without any degradation on the waveform. So, the ESD clamp NMOS in the VDD-to-VSS ESD clamp circuit is indeed kept off in the normal VDD power-on condition.

7.3.2 Location of Power-Rail ESD Clamp Circuit

The operation of pin-to-pin ESD protection with the efficient VDD-to-VSS ESD clamp circuit has been explained in Fig. 7.21. With suitable design on the ESD-transient detection circuit, the ESD clamp NMOS can provide an effective discharging path between VDD and VSS power lines to bypass the ESD current away from the internal circuits of the IC. However, the modern VLSI (or ULSI) often has a very large die size, which has much longer VDD and VSS power lines to surround the whole chip and to connect the I/O circuits. Such longer power lines had been reported to have a negative impact on the ESD protection of IC's [8]. The negative impact on the pin-to-VSS ESD protection owing to the longer VDD and VSS power lines is illustrated in Fig. 7.25, where the VDD-to-VSS ESD clamp circuit is placed far from the stressed input and VSS pads. The longer VDD and VSS power lines generally generate the higher series resistance (Rdd and Rss) along the power lines or a larger VDD-to-VSS parasitic capacitance (Cds) across the power lines. The parasitic Rdd, Rss, and Cds along the

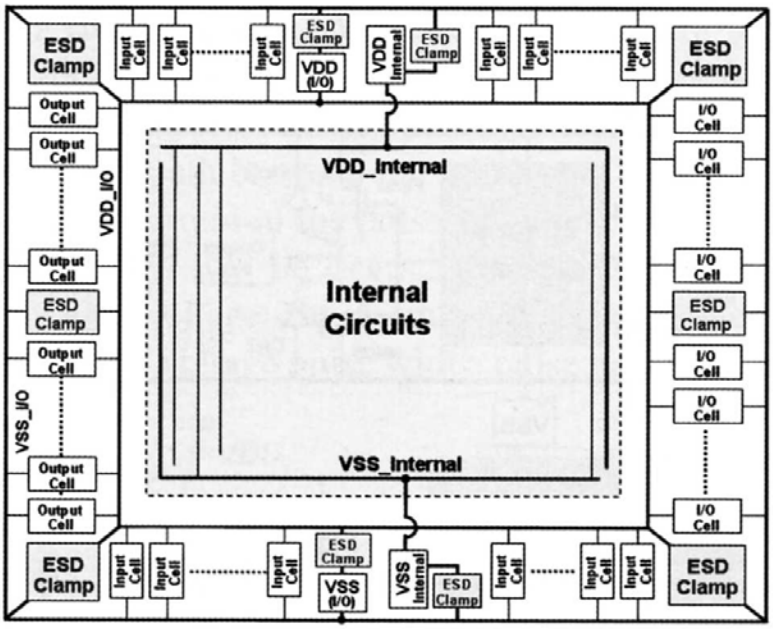


Figure 7.26: A schematic diagram to show the concept of whole-chip ESD protection design with multiple efficient power-rail ESD clamp circuits between the VDD and VSS power lines in a CMOS chip.

VDD and VSS power lines contribute a time delay to limit the ESD current discharging through the ESD clamp NMOS. The equivalent parasitic Rdd, Rss, and Cds along the VDD and VSS power lines are strongly dependent on the location of the stressed pad and the grounded pad in the IC. If the VDD-to-VSS ESD clamp circuit is located too far from the stressed pad and the relatively grounded pad, as shown in Fig. 7.25, the speed and efficiency to bypass the ESD current through the VDD-to-VSS ESD clamp circuit is seriously delayed and degraded by the parasitic resistance and capacitance along the power lines. Some ESD current is still discharged through the internal circuits and causes some ESD damages on the internal circuits. So, the pins of the IC may have different ESD levels, even if the pins have the same ESD protection circuits. The stressed pin has a higher ESD level if the stressed pin is closer to the VDD-to-VSS ESD clamp circuit. Therefore, a special design rule to specify the spacing from the input or output pins to the VDD-to-VSS ESD clamp circuit for effective whole-chip ESD protection has to be established.

The design concept with the efficient VDD-to-VSS ESD clamp circuit is illustrated in Fig. 7.26 to provide a real whole-chip ESD protection without the unexpected ESD damage in the internal circuits under any ESD-stress condition. Four VDD-to-VSS ESD clamp circuits are inserted in the four sides of the chip with the VDD and VSS power lines surrounding the whole chip. For a larger die size with a much longer VDD and VSS

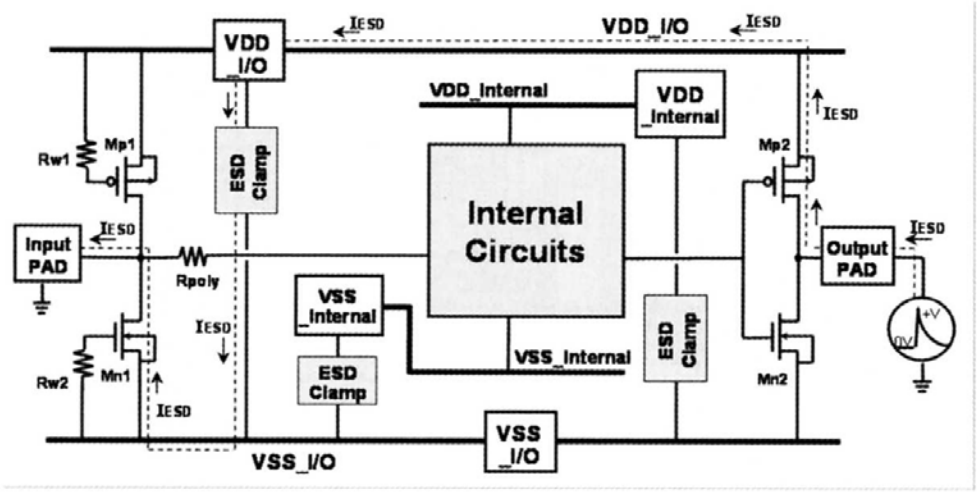


Figure 7.27: The whole-chip ESD protection scheme for the IC with separated power pins for I/O circuits and internal circuits.

power lines, the numbers of the VDD-to-VSS ESD clamp circuits inserted between the power lines of the chip should be increased. The VDD-to-VSS ESD clamp circuits can be also placed in the four corners of the chip without increasing the total layout area of the chip, where the corners are often empty without any device in the most IC's.

7.3.3 Protection for ICs with Separated Power Lines

Most of the traditional ESD protection designs were focused on the ESD protection circuits or devices for the I/O pins, which can provide protection against ESD stresses on the I/O pin under the four modes of pin combination. But, only with the ESD protection circuits or devices located at the I/O pads can not provide the enough protection for internal circuits against the pin-to-pin and VDD-to-VSS ESD stresses, which often causes the ESD failure located in the internal circuits but not on the I/O ESD devices. In the modern logic ICs, the power pins for I/O circuits are often separated from the power pins of the core circuits to avoid noise coupling issue and to reduce the ground bounce. With the separated power pins, the typical whole-chip ESD protection scheme is shown in Fig. 7.27. Besides the ESD clamp devices at the input and output pads, the most important design to achieve the whole-chip ESD protection for all devices and circuits in the IC against ESD damages (especially against the pin-to-pin and VDD-to-VSS ESD stresses) is the arrangement on the power lines and the power-rail ESD clamp circuits between the separated power lines. As shown by the dashed lines in Fig. 7.27, the ESD current discharging path or the IC under pin-to-pin ESD zapping can be built up by using the I/O ESD devices, the

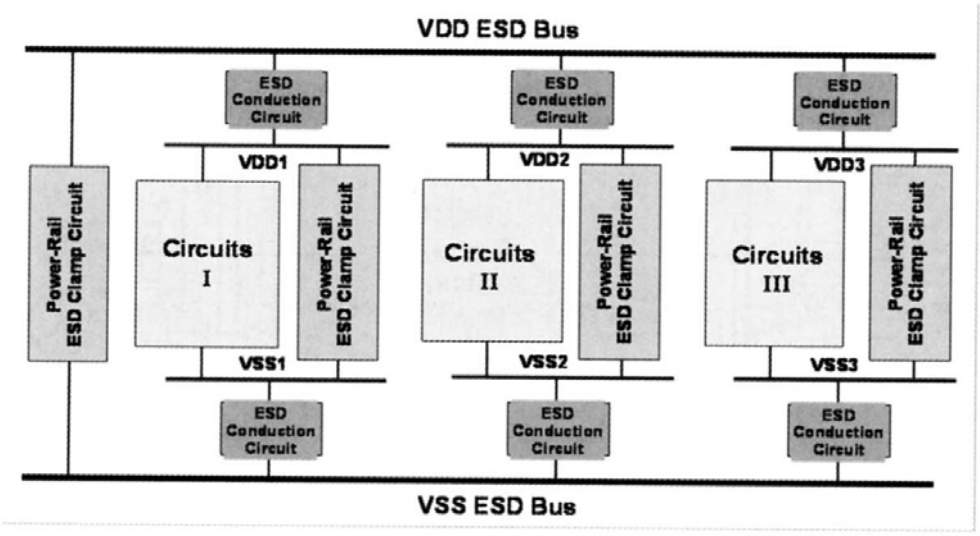


Figure 7.28: The suggested whole-chip ESD protection scheme for the IC with more separated power lines.

power metal lines, and the power-rail ESD clamp circuits. Only having a successful whole-chip ESD protection scheme, the internal (core) circuits can be effectively protected by the ESD clamp devices located at the I/O pads and the ESD clamp circuits located between the power rails.

For the IC with more separated power lines, the suggested whole-chip ESD protection scheme is shown in Fig. 7.28 [57], which has been included in the Design Rules of one famous semiconductor foundry. The ESD conduction circuits between the VDD ESD bus and the separated power lines (VDD1, VDD2, VDD3) can be realized by the stacked diodes [58] or even the bi-directional SCR devices [59]-[60]. If the IC (such as system on a chip, SoC) with more complex power supplies with different voltage levels, the whole-chip ESD protection scheme with the multiple ESD buses is shown in Fig. 7.29 [11]. With a successful arrangement for the whole-chip ESD protection scheme, the internal circuits can be safely protected by the ESD clamp devices located at the I/O pads and between the power domains.

7.4 ESD Protection for Mixed-Voltage I/O Interface

7.4.1 Mixed-Voltage I/O

To improve circuit operating speed and performance, the device dimension of MOSFET has been shrunk in the advanced CMOS integrated circuits

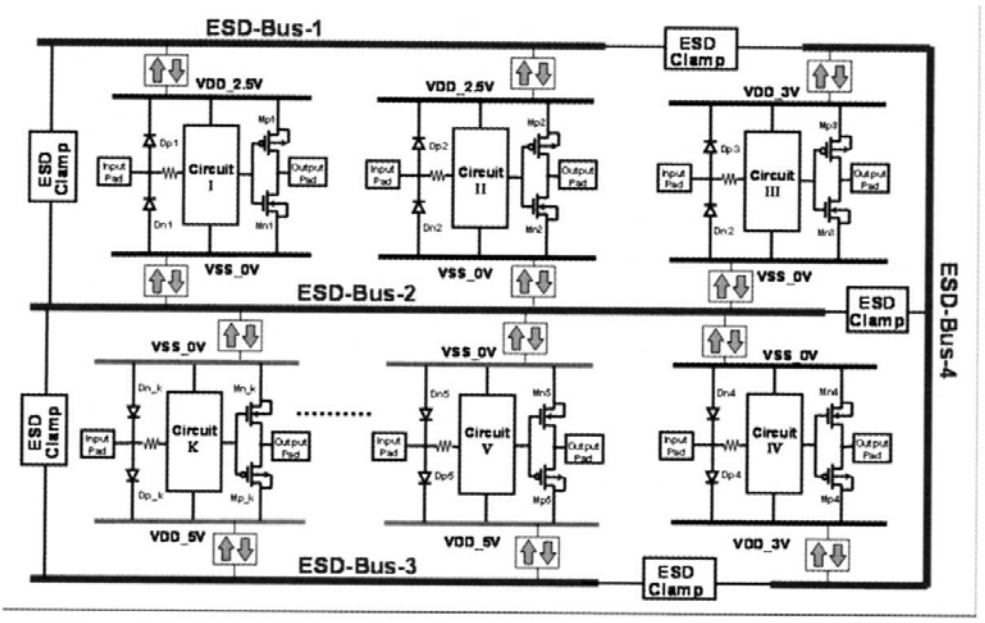
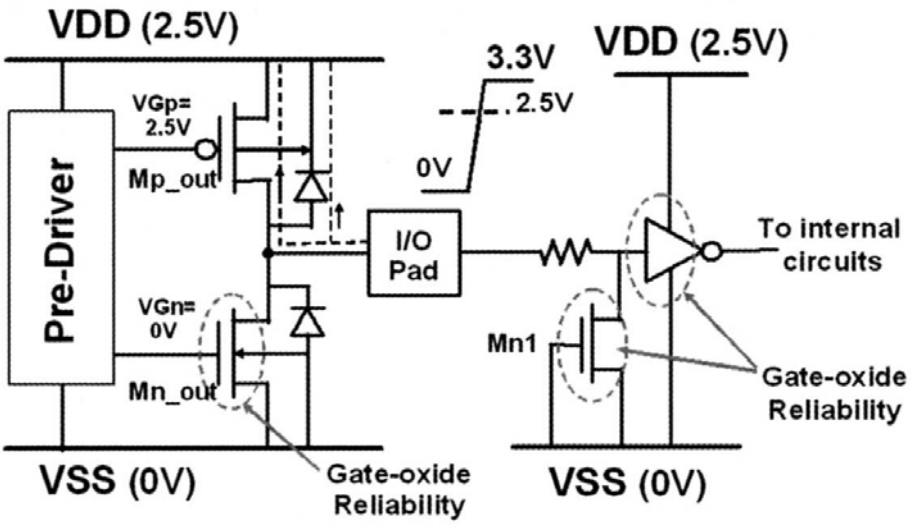
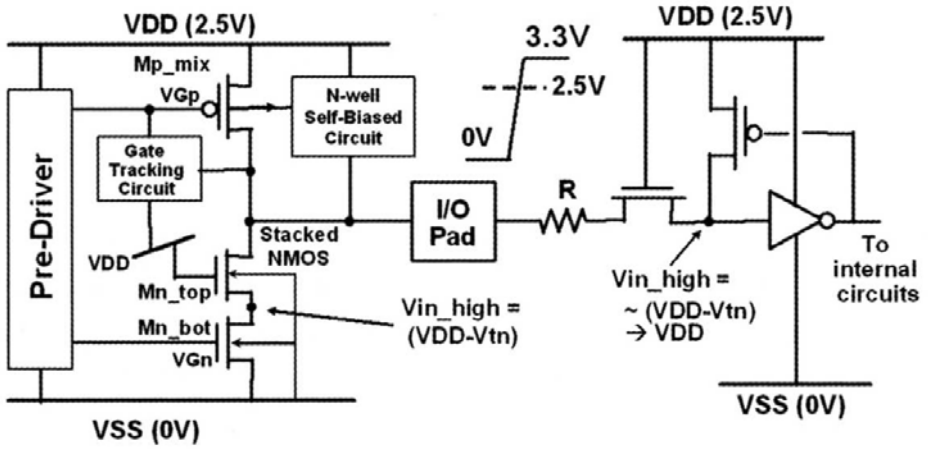


Figure 7.29: The whole-chip ESD protection scheme with the multiple ESD buses for the IC with more complex power supplies with different voltage levels.

(ICs). With the scaled-down device dimension in advanced CMOS technology, the power supply voltage is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. However, most microelectronic systems nowadays consist of mix semiconductor chips fabricated in different CMOS technologies. Therefore, the microelectronic systems often require the interfaces between semiconductor chips or subsystems which have different internal power supply voltages. With the different power supply voltages in a microelectronic system, chip-to-chip I/O interface circuits must be designed to avoid electrical overstress across the gate oxide [61], to avoid hot-carrier degradation [62] on the output devices, and to prevent the undesired leakage current paths between the chips [63], [64]. For example, a 3.3-V I/O interface is generally required by the ICs realized in CMOS processes with the normal internal power-supply voltage of 2.5V or 1.8V. The traditional CMOS I/O buffer with VDD of 2.5V is shown in Fig. 7.30(a) with both output and input stages. When an external 3.3-V signal is applied to the I/O pad, the channel of the output pMOS (Mp_out) and the parasitic drain-to-well junction diode in the Mp_out cause the leakage current paths from the I/O pad to VDD, as the dashed lines shown in Fig. 7.30(a). Moreover, the gate oxides of the output nMOS (Mn_out), the gate-grounded nMOS (Mn1) for input electrostatic discharge (ESD) protection, and the input inverter stage are over-stressed by the 3.3-V input signal to suffer the gate-oxide reliability issue. By us-



(a)



(b)

Figure 7.30: Typical circuit diagrams for (a) the traditional CMOS I/O buffer, and (b) the mixed-voltage I/O circuits with the stacked-nMOS and the N-well self-biased pMOS.

ing the additional thick gate-oxide process (or called as dual gate-oxide CMOS process [65], [66]), the gate-oxide reliability issue can be avoided. However, the process complexity and fabrication cost are increased.

To solve the gate-oxide reliability issue without using the additional thick gate-oxide process, the stacked-MOS configuration has been widely used in the mixed-voltage I/O circuits [67]-[73]. The typical 2.5V/3.3V-tolerant mixed-voltage I/O circuit is shown in Fig. 7.30(b) [68]. The independent control on the top and bottom gates of stacked-nMOS device allows the devices to meet reliability limitations during normal circuit op-

eration. The gate of top nMOS (Mn_top) in the stacked-nMOS device is biased at VDD (e.g. 2.5V in a 2.5V/3.3V mixed-voltage I/O interface). The gate of bottom nMOS (Mn_bot) is biased at VSS by the pre-driver circuit to avoid leakage current through the stacked-nMOS structure, when the I/O circuit has a high-voltage input signal. With a high-voltage input signal at the pad (e.g. 3.3V in a 2.5V/3.3V mixed-voltage I/O interface), the common node between the Mn_top and Mn_bot in the stacked-nMOS structure has approximately a voltage level of VDD-Vth ($\sim$ 1.9V), where Vth ($\sim$ 0.6V) is the threshold voltage of nMOS device. Therefore, the stacked-nMOS can be operated within the safe range for both dielectric and hot-carrier reliability limitations. The pull-up pMOS (Mp_mix), connected from the I/O pad to the VDD power line, has the gate tracking circuits for tracking the gate voltage and the n-well self-biased circuits for tracking n-well voltage, which are designed to ensure that the Mp_mix does not conduct current when the 3.3-V input signals enter the I/O pad. In such mixed-voltage I/O circuits, the on-chip ESD protection circuits will meet more design constraints and difficulty.

The on-chip ESD protection circuit for mixed-voltage I/O interfaces should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit should be quickly triggered on to discharge ESD current. In this subsection, an overview on the ESD protection designs for mixed-voltage I/O interface circuits without using the additional thick gate-oxide process is presented. The content covers the ESD design constraints in mixed-voltage I/O circuits, the classification and analysis of the proposed ESD protection designs for mixed-voltage I/O circuits, and the designs for high-voltage-tolerant power-rail ESD clamp circuit.

7.4.2 ESD Design Constraints in Mixed-Voltage I/O

The ESD protection design of traditional I/O pad cooperating with power-rail ESD clamp circuit has been shown in Fig. 7.31(a), where a PS-mode ESD pulse is applied to the I/O pad. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS from I/O pad to VDD, and then through the VDD-to-VSS ESD clamp circuit to ground. Such traditional I/O circuits cooperating with the VDD-to-VSS ESD clamp circuit can achieve a higher ESD level [10]. But, due to the leakage current issue in the mixed-voltage I/O circuits, there is no diode connected from the I/O pad to VDD power line in the mixed-voltage I/O circuits. Without the diode connected from the I/O pad

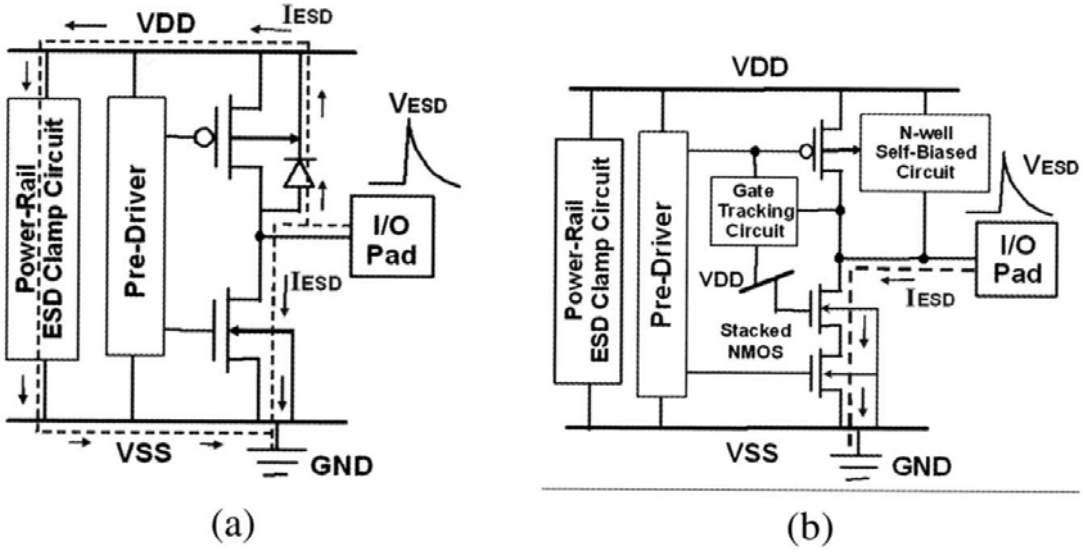


Figure 7.31: The ESD current paths of (a) the traditional I/O pad with power-rail ESD clamp circuit, and (b) the mixed-voltage I/O pad with power-rail ESD clamp circuit, under the positive-to-VSS (PS-mode) ESD stress. The ESD current paths are indicated by the dashed lines.

to VDD in the mixed-voltage I/O circuits, the ESD current at I/O pad under PS-mode ESD stress cannot be discharged from the I/O pad to VDD power line, and cannot be discharged through the additional VDD-to-VSS ESD clamp circuit. Therefore, the power-rail ESD clamp circuit did not help to pull up ESD level of the mixed-voltage I/O pad under the PS-mode ESD stress. The ESD current path in the mixed-voltage I/O circuits with power-rail ESD clamp circuit under PS-mode ESD stress in illustrated in Fig. 7.31(b). Such ESD current at the I/O pad is mainly discharged through the stacked-nMOS by snapback breakdown. However, the nMOS in stacked configuration has a higher trigger voltage and a higher snapback holding voltage, but a lower secondary breakdown current (It2), as compared to that of the single nMOS [74], [75]. Therefore, such mixed-voltage I/O circuits with stacked nMOS often have much lower ESD level under PS-mode ESD stress, as compared to the traditional I/O circuits with a single nMOS [74]. In addition, without the diode connected from the I/O pad to VDD, the mixed-voltage I/O circuit also has a lower ESD level for I/O pad under PD-mode ESD stress. The absence of the diode between I/O pad and VDD power line in the mixed-voltage I/O circuits will seriously degrade ESD performance of the I/O pad under the PS-mode and PD-mode ESD stresses.

The finger-type layout pattern and the corresponding cross-sectional view of stacked-nMOS device in mixed-voltage I/O circuits are shown in Figs. 7.32(a) and 7.32(b). The stacked-nMOS device can be used as both

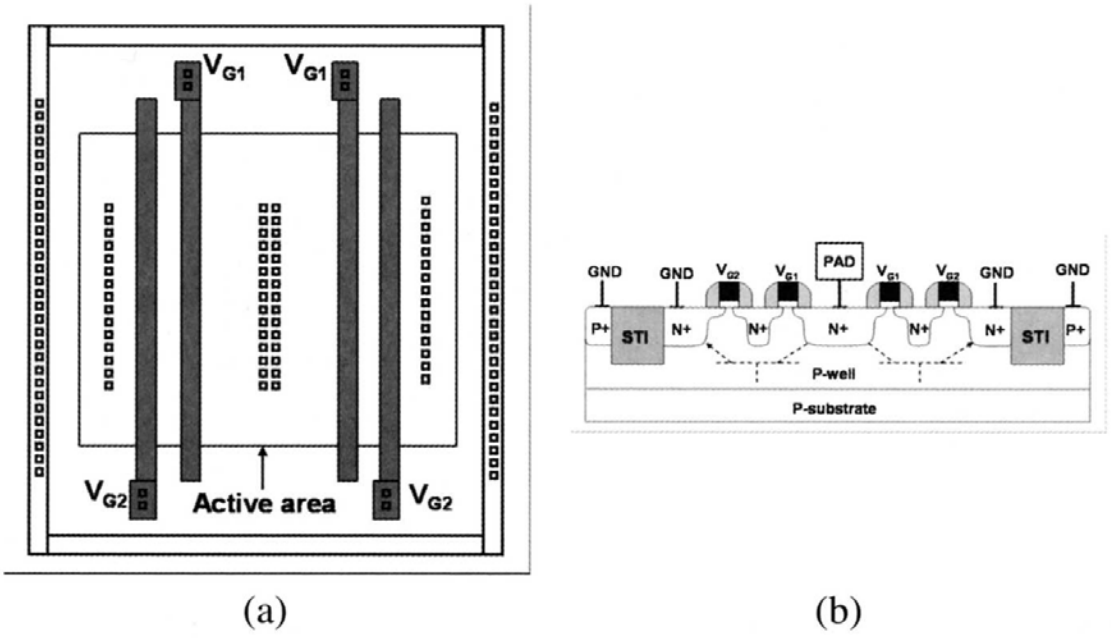
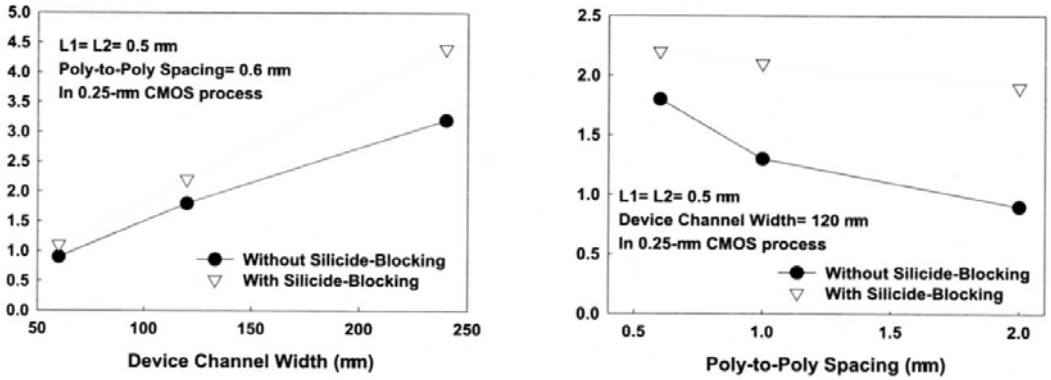


Figure 7.32: (a) Finger-type layout pattern, and (b) the corresponding cross-sectional view, of the stacked-nMOS device with the shared active configuration for the mixed-voltage I/O circuits in a p-substrate CMOS process.

of the pull-down device and ESD protection device in the mixed-voltage I/O circuits. The stacked-nMOS structure includes a first transistor (top nMOS), having a drain connected to an I/O pad, and a gate (V_{G1}) connected to the VDD power supply. A second transistor (bottom nMOS) is merged into the same active area of the first transistor, having a gate (V_{G2}) connected to the pre-driver of the mixed-voltage I/O circuits. The source of the top nMOS and the drain of the bottom nMOS are constructed together by sharing the common n+ diffusion region. Under the PS-mode ESD stress condition, the stacked nMOS is operated in snapback breakdown, where the bipolar effect taking place between the drain of the top nMOS and the source of the bottom nMOS. These two diffusions act as the emitter and collector of the parasitic lateral n-p-n bipolar junction transistor (BJT), respectively. The snapback mechanism of stacked-nMOS device for conducting large amounts of ESD current involves both avalanche breakdown and the parasitic n-p-n bipolar junction transistor.

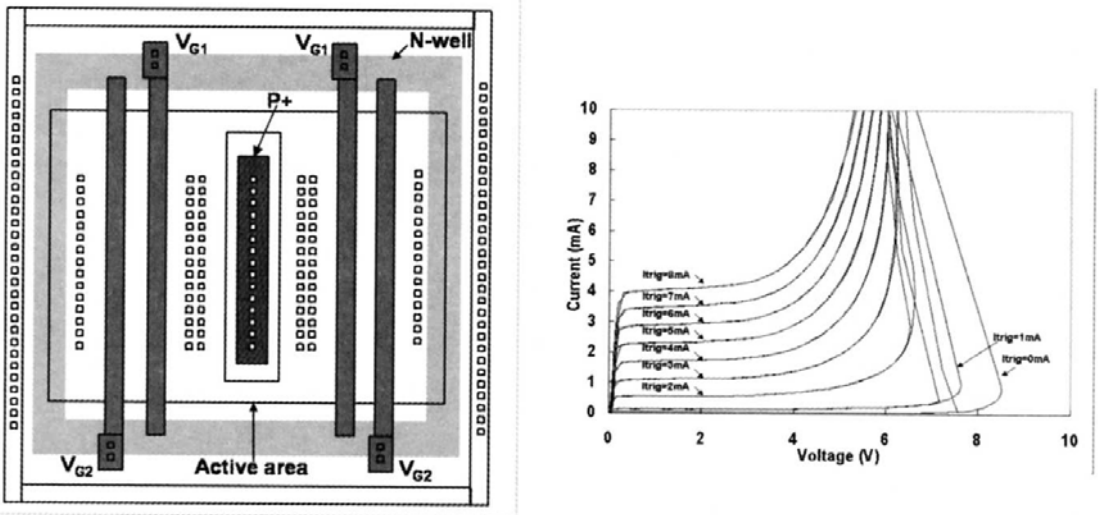
The dependencies of human-body-model (HBM) ESD level on the device channel width and poly-to-poly spacing (common n+ diffusion spacing) of stacked-nMOS device in a 0.25-μm CMOS process are shown in Fig. 7.33. In Fig. 7.33(a), the HBM ESD level of the stacked-nMOS device is increased while the device channel width is increased. Moreover, the stacked-nMOS device with silicide-blocking process can sustain higher ESD level than that with fully silicided process. The non-uniform turn-on



(a) (b)

Figure 7.33: Comparisons of HBM ESD robustness of the stacked-nMOS device with or without the silicide-blocking process, under (a) different channel widths, and (b) different poly-to-poly spacings, of the stacked-nMOS device fabricated in a 0.25-μm CMOS process.

issue of the parasitic n-p-n BJT in stacked-nMOS device can be improved by the silicide-blocking process. In Fig. 7.33(b), the HBM ESD level of stacked-nMOS device with fully silicided process is decreased obviously while the poly-to-poly spacing is increased. However, the HBM ESD level of stacked-nMOS device with silicide-blocking process is only decreased slightly. The turn-on efficiency and performance of the parasitic n-p-n BJT in stacked-nMOS device can be improved by reducing the poly-to-poly spacing. Although the ESD robustness of stacked-nMOS device can be somewhat improved by layout optimization, the stacked-nMOS device by snapback breakdown still cannot provide efficient ESD protection in the mixed-voltage I/O circuits. By using extra process modification such as ESD implantation, the ESD robustness of stacked-nMOS device can be further improved [45], [76], but the process complexity and fabrication cost are increased. In addition, the induced high voltage on the gate of top nMOS transistor under ESD stress will cause high-current crowding effect in the channel region to seriously degrade ESD robustness of stacked-nMOS device in the mixed-voltage I/O circuits [77]. Therefore, effective ESD protection design without increasing process complexity is strongly requested by the mixed-voltage I/O circuits in the scaled-down CMOS processes.



(a) (b)

Figure 7.34: (a) Finger-type layout pattern of the substrate-triggered stacked-nMOS device for mixed-voltage I/O circuits. (b) Measured I-V characteristics of the substrate-triggered stacked-nMOS device with different substrate-triggered currents (Itrig).

7.4.3 ESD Protection Design for Mixed-Voltage I/O

7.4.3.1 Substrate-Triggered Stacked-nMOS Device

The snapback operation of the parasitic n-p-n BJT in the stacked-nMOS structure can be controlled by its substrate potential. Therefore, the substrate resistance (Rsub) and substrate current are the important design parameters for ESD protection [78]. The substrate-triggered technique [34] can be used to generate the substrate current in ESD protection circuits. With the substrate-triggered current, the trigger voltage of the stacked-nMOS device in mixed-voltage I/O circuits can be reduced for more effective ESD protection [79], [80]. The finger-type layout pattern of the substrate-triggered stacked-nMOS device is shown in Fig. 7.34(a). As shown in the layout top view, an additional p+ diffusion is inserted into the center drain region of stacked-nMOS device as the substrate-triggered node. The trigger current is provided by the substrate-triggered circuit. An n-well structure is further diffused under the source region, which is also surrounding the whole device, to form a higher equivalent substrate resistance for improving turn-on efficiency of the parasitic lateral BJT in the stacked-nMOS device. The measured current-voltage (I-V) characteristics of the substrate-triggered stacked-nMOS device with different substrate-triggered currents (measured by a Tek370A curve tracer) are shown in Fig. 7.34(b). The trigger voltage of the parasitic n-p-n BJT in the stacked-

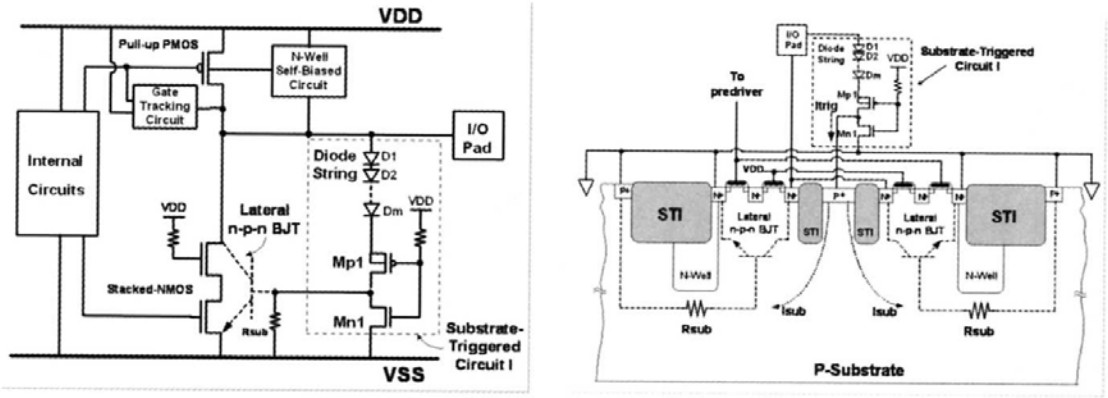


Figure 7.35: (a) Schematic circuit diagram of the substrate-triggered stacked-nMOS device with substrate-triggered circuit I for the mixed-voltage I/O circuits. (b) Cross-sectional view of the substrate-triggered stacked-nMOS device cooperating with substrate-triggered circuit I.

nMOS device can be effectively decreased while the substrate-triggered current is increased. The substrate-triggered circuit should be designed to avoid electrical overstress on the gate oxide and to prevent the undesired leakage current paths during normal circuit operating condition. During ESD stress condition, the substrate-triggered circuit should generate large enough trigger current to effectively improve the turn-on efficiency of parasitic n-p-n BJT in stacked-nMOS device. The substrate-triggered circuit should meet above constraints for providing effective ESD protection to the mixed-voltage I/O interface.

The substrate-triggered circuit I for stacked-nMOS device in the mixed-voltage I/O circuits is shown in Fig. 7.35(a) [79]. The cross-sectional view of the substrate-triggered stacked-nMOS device with such a substrate triggered circuit I is shown in Fig. 7.35(b). The substrate-triggered circuit I is composed of the diode string, a pMOS Mp1, and an nMOS Mn1, to provide the substrate current for triggering on the parasitic n-p-n BJT in the stacked-nMOS device during ESD stress. Under normal circuit operating condition, the turn-on voltage of the substrate-triggered circuit roughly equals to Vpad $\approx V_{\text{string}}(I) + |V_{\text{tp}}| + VDD$, where $V_{\text{string}}(I)$ is the total voltage drop across the diodes and V_{tp} is the threshold voltage of the pMOS. The turn-on voltage can be adjusted by varying the numbers of the diodes in the diode string. To satisfy the requirement in the 2.5V/3.3V mixed-voltage application, the number of the diodes in the diode string should be adjusted to make the turn-on voltage greater than 3.3V. When a 3.3-V input voltage is applied at I/O pad, Mp1 is kept off, and the local substrate of the stacked nMOS is biased at VSS by the turn-on of Mn1. With

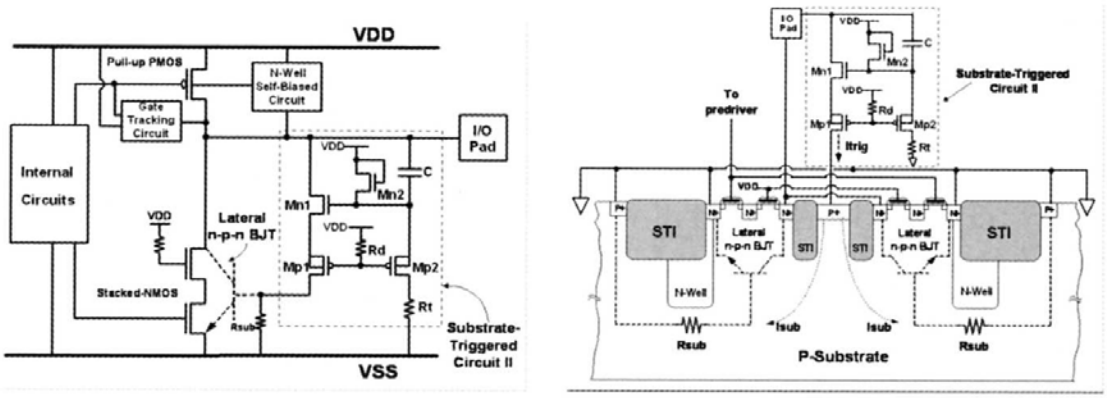


Figure 7.36: (a) Schematic circuit diagram of the substrate-triggered stacked-nMOS device with substrate-triggered circuit II for the mixed-voltage I/O circuits. (b) Cross-sectional view of the substrate-triggered stacked-nMOS device cooperating with substrate-triggered circuit II.

the diode string to block the 3.3-V input voltage at the I/O pad, the Mp1 with thin gate oxide has no gate-oxide reliability issue under normal circuit operating condition. The Mp1 in conjunction with the diode string is used to reduce the leakage current through the substrate-triggered circuit in normal operating condition. The choice of a particular diode string is also determined by the specified pin leakage current at a given temperature. If a lower input leakage is desired, the numbers of the diodes in the diode string should be increased. Under PS-mode ESD stress condition, the gate of the Mp1 has an initial voltage level of ~0V, while the VSS pin is grounded but the VDD pin is floating. The substrate-triggered circuit will provide the trigger current flowing through the diode string and the Mp1 into the p-substrate, when Vpad $\geq V_{\text{string}}(I) + |V_{\text{tp}}|$. The trigger current provided by the substrate-triggered circuit is determined by the diode string and the size of Mp1. Once the parasitic n-p-n BJT in the stacked-nMOS device is triggered on, the ESD current will be discharged from the I/O pad to VSS. In this design, the HBM ESD level of the mixed-voltage I/O circuits has been improved from the original 3.4kV to 5.6kV in a 0.25-μm CMOS process.

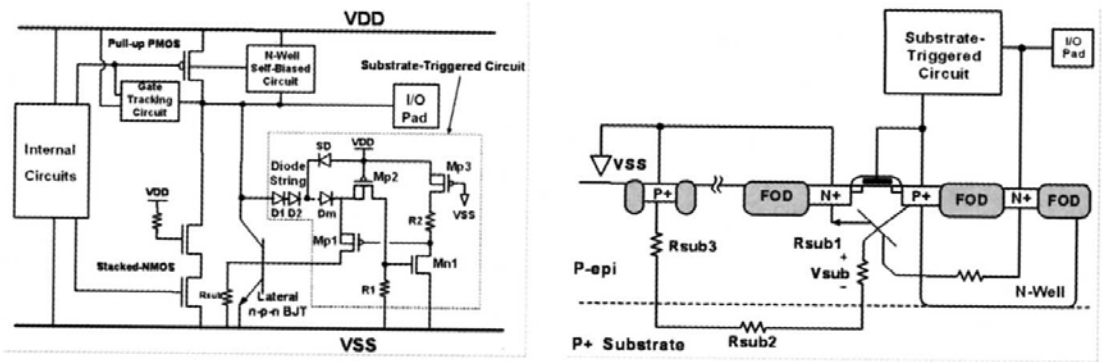
Another substrate-triggered circuit II for stacked-nMOS device in the mixed-voltage I/O circuits is shown in Fig. 7.36(a) [80]. The cross-sectional view of the substrate-triggered stacked-nMOS device with such a substrate-triggered circuit II is shown in Fig. 7.36(b). The substrate-triggered circuit II is composed of the pMOS Mp1, pMOS Mp2, nMOS Mn1, and nMOS Mn2, to provide the substrate current for triggering on the parasitic n-p-n BJT in the stacked-nMOS device during ESD stress. The gates of Mp1

and Mp2 are connected together to VDD through a resistor Rd. In the 2.5V/3.3V mixed-voltage IC application, the gates of Mp1 and Mp2 are biased at 2.5-V VDD supply under normal circuit operating condition. When the input voltage transfers from 0V to 3.3V at the I/O pad, the gate voltage of Mn1 could be increased through the coupling capacitor C. However, the Mn2 and Mp2 can clamp the gate voltage of Mn1 between VDD-Vtn and VDD+$|V_{tp}|$, where Vtn is the threshold voltage of nMOS. Once the gate voltage of Mn1 is over VDD+$|V_{tp}|$, the Mp2 will turn on to discharge the over-coupled voltage and to keep the gate voltage within VDD+$|V_{tp}|$. Since the upper boundary on the gate voltage of Mn1 is within VDD+$|V_{tp}|$, the source voltage of Mp1 is clamping below VDD, which keeps the Mp1 always off under normal circuit operation condition. The Mn2 and Mp2 can further clamp the gate voltage of Mn1 to avoid gate-oxide reliability issue in the substrate-triggered circuit, even if the I/O pad has a high input voltage level. Under PS-mode ESD-stress condition, the gates of Mp1 and Mp2 have an initial voltage level of $\sim$0V, while the VSS pin is grounded but the VDD pin is floating. The positive ESD transient voltage on the I/O pad is coupled through the capacitor C to the gate of Mn1. In this situation, both of the Mn1 and Mp1 are operated in the turn-on state. Therefore, the substrate-triggered circuit II will conduct some ESD current flowing from I/O pad through Mn1 and Mp1 into the p-substrate. The trigger current provided by the substrate-triggered circuit II is determined by the size of Mn1, Mp1, and the capacitor C. Once the parasitic n-p-n BJT in the stacked-nMOS device is triggered on, the ESD current will be mainly discharged from the I/O pad to VSS. In this design, the HBM ESD level of the mixed-voltage I/O circuits has been improved from the original 3.5kV to 5.5kV in a 0.25-μm CMOS process.

Both two substrate-triggered designs can significantly reduce the trigger voltage and ensure effective ESD protection for the mixed-voltage I/O circuits. By using such substrate-triggered designs, the gates of stacked-nMOS in the mixed-voltage I/O circuits can be fully controlled by the pre-driver of I/O circuits without conflict to the ESD protection circuits. The main ESD discharge device is the parasitic n-p-n BJT in the stacked-nMOS device. Therefore, the ESD robustness of mixed-voltage I/O circuits can be effectively improved without occupying extra silicon area to realize the additional stand-alone ESD protection device into the I/O cells.

7.4.3.2 Extra ESD Device between I/O pad and VSS

To improve ESD level of the mixed-voltage I/O circuits, the extra ESD device was added between I/O pad and VSS power line [81], [82]. The

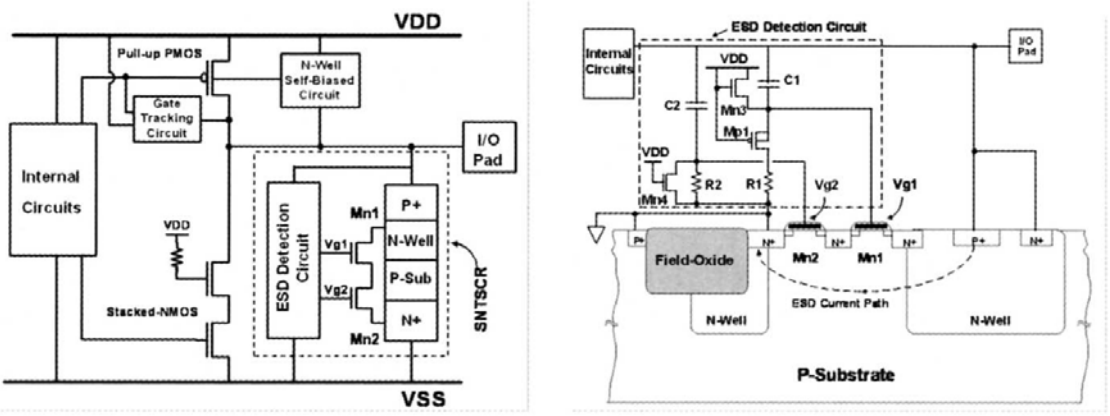


(a) (b)

Figure 7.37: (a) ESD protection design with substrate-triggered lateral n-p-n BJT device to protect the mixed-voltage I/O circuits. (b) Cross-sectional view of the lateral n-p-n BJT device in a thin-epi CMOS process.

ESD current at the I/O pad under PS-mode ESD stress is designed to be directly discharged through this additional ESD device to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be discharged through this ESD device to VSS power line, and then through the parasitic diode of power-rail ESD clamp circuit to the grounded VDD.

One ESD protection design with the additional substrate-triggered lateral n-p-n BJT device has been used to protect the mixed-voltage I/O circuits in a fully salicided, 0.35-μm, thin-epi CMOS process [81]. The ESD protection design with substrate-triggered circuit and the lateral n-p-n BJT device for the mixed-voltage I/O circuits is re-drawn in Fig. 7.37(a). The design concept of this substrate-triggered circuit is similar to that in the aforementioned designs. The substrate-triggered circuit should meet the design constraints for providing effective ESD protection to the mixed-voltage I/O circuits, but without suffering the gate-oxide reliability issue. In this design, the substrate-triggered circuit is mainly composed of the diode string and a pMOS Mp1 to provide the substrate current for triggering on the lateral n-p-n BJT during ESD stress. A positive feedback network is formed with Mp2, Mn1, and R1, which maintains Mp1 in a highly conductive state to provide the substrate current during ESD stress. Moreover, to improve the turn-on efficiency of lateral n-p-n BJT device in a thin-epi CMOS process with much smaller substrate resistance (Rsub), the device structure of lateral n-p-n BJT is specifically designed in Fig. 7.37(b). The lateral n-p-n BJT device consists of an n+ diffusion (emitter), an n-well (collector), and a p+ diffusion as its base. A dummy gate is formed between the p+ base and n+ emitter regions. The collector n-well encloses a portion of the p+ base region. In this design, the HBM ESD level of the mixed-voltage I/O circuits has been verified greater than 2kV in a fully-



(a) (b)

Figure 7.38: (a) ESD protection circuit with the SNTSCR device to protect the mixed-voltage I/O circuits. (b) Realizations of the SNTSCR device and the ESD detection circuit with the gate-coupling technique to trigger on the SNTSCR device.

salicided thin-epi CMOS process.

Another ESD protection design, by using the additional stacked-nMOS triggered silicon controlled rectifier (SNTSCR), has been reported to protect the mixed-voltage I/O circuits [82]. The ESD protection design with the additional SNTSCR device for protecting the mixed-voltage I/O circuits is shown in Fig. 7.38(a). The device structure of SNTSCR and the corresponding ESD detection circuit are shown in Fig. 7.38(b). The ESD detection circuit, designed by using the gate-coupled technique with consideration of the gate-oxide reliability issue, is used to provide suitable gate bias to trigger on the SNTSCR device under ESD stress condition. On the contrary, this ESD detection circuit must keep the SNTSCR off when the IC is under normal circuit operating condition. During normal circuit operating condition, the Mn3 in Fig. 7.38(b) acts as a resistor to bias the gate voltage (Vg1) of Mn1 at VDD. But, the gate of Mn2 is grounded through the resistor R2 and Mn4. So, all the devices in the ESD protection circuit can meet the electrical-field constraint of gate-oxide reliability under normal circuit operating condition. Under PS-mode ESD stress condition, the Mp1 is turned on but Mn3 is off since the initial voltage level on the floating VDD line is $\sim$0V. The capacitors C1 and C2 are designed to couple ESD transient voltage from the I/O pad to the gates of Mn1 and Mn2, respectively. The coupled voltage should be designed greater than the threshold voltage of nMOS to turn on Mn1 and Mn2 for triggering on the SNTSCR device, before the devices in the mixed-voltage I/O circuit are damaged by ESD stress. With the gate-coupled circuit technique, the trigger voltage of SNTSCR can be significantly reduced, so the SNTSCR

can be quickly triggered on to discharge ESD current. By changing the connection of the ESD protection circuit from the I/O pad to the floating n-well of the pull-up pMOS in the mixed-voltage I/O circuit, the SNTSCR device can have a high enough noise margin to the overshooting glitch on the I/O pad, during the normal circuit operating condition. From the experimental results in a 0.35-μm CMOS process, the HBM ESD level of the mixed-voltage I/O circuits with this ESD protection design has been greatly improved up to 8kV, as compared with that ($\sim$2kV) of the original mixed-voltage I/O circuits with only stacked nMOS device.

7.4.3.3 Extra ESD Device between I/O pad and VDD

To improve ESD level of the mixed-voltage I/O circuits, the extra ESD device was added between I/O pad and VDD power line [83]-[85]. The ESD current at the I/O pad under PS-mode ESD stress is designed to be discharged through this additional ESD device to VDD power line, and then through the power-rail ESD clamp circuit to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be directly discharged through this additional ESD device to the grounded VDD.

Because the diode in forward-biased condition can sustain much higher ESD current, the diode string has been used for protecting the mixed-voltage I/O circuits [84], [84], or used to realize the power-rail ESD clamp circuit [86]. The ESD protection design with the diode string connected between the I/O pad and VDD power line for the mixed-voltage I/O circuits is shown in Fig. 7.39. The number of diodes in the diode string is determined by the voltage difference between the maximum input voltage at I/O pad and the VDD supply voltage. To reduce the turn-on resistance from I/O pad to VDD during ESD stress, the area of such diodes has to be scaled up by the number of the diodes in stacked configuration. The major concern of using the diode string for ESD protection in the mixed-voltage I/O circuits is the leakage current. While the mixed-voltage I/O circuit is operating at a high-temperature environment with a high-voltage input signal, the forward-biased leakage current from the I/O pad to VDD through the stacked diodes could trigger on the parasitic vertical p-n-p BJT devices in the diode string. The Darlington bipolar amplification of these parasitic p-n-p BJT devices in the diode string will induce a large leakage current into the substrate. In Fig. 7.39, an additional snubber diode (SD) was used to reduce the leakage current due to the Darlington bipolar amplification in the diode string [83], [84].

Another ESD protection design, by using the gated p-n-p BJT as the additional ESD device connected between I/O pad and VDD, has been

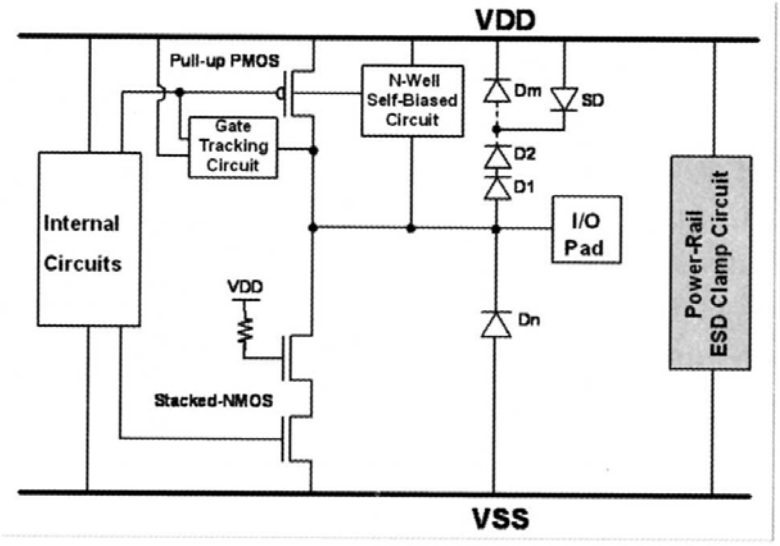


Figure 7.39: ESD protection design with the diode string connected between the I/O pad and VDD power line to protect the mixed-voltage I/O circuits. An additional snubber diode (SD) is used to reduce the leakage current of the diode string due to the Darlington amplification.

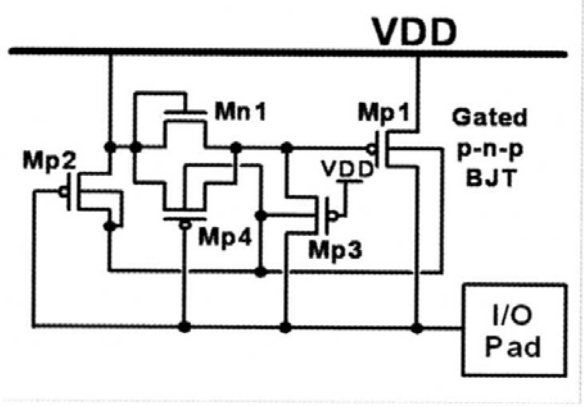


Figure 7.40: ESD protection design with gated p-n-p BJT as the ESD clamp device connected between I/O pad and VDD to protect the mixed-voltage I/O circuits.

designed to protect the mixed-voltage I/O circuits [85], as that shown in Fig. 7.40. In this ESD protection design, the pMOS Mp1 acting as ESD clamp device should be kept off to avoid the leakage current path during normal circuit operating condition. Under PD-mode ESD stress condition, the parasitic lateral p-n-p BJT in the device structure of Mp1 is turned on to discharge ESD current. In the 3.6V/5V mixed-voltage IC application, when the input voltage at I/O pad is 0V, the n-well voltage and gate voltage of Mp1 is clamped at VDD (3.6V) through the turn-on of Mp2 and Mp4. When the input voltage at I/O pad is 5V, the n-well voltage of Mp1

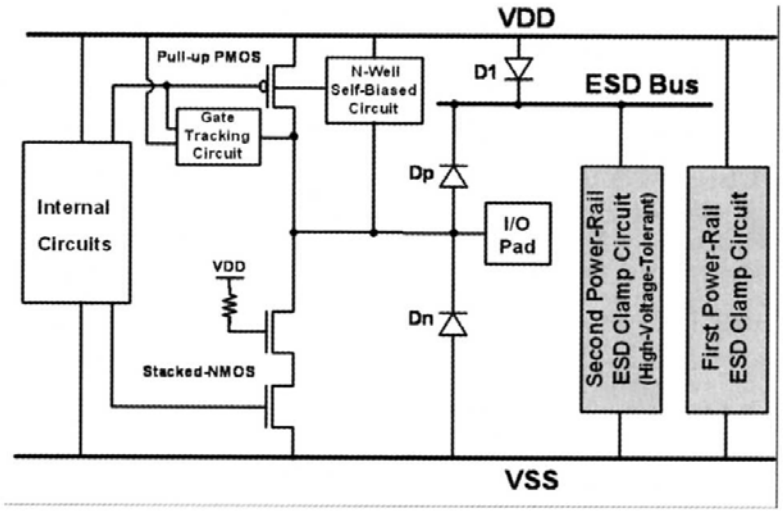


Figure 7.41: The ESD protection network with the additional ESD bus line for the mixed-voltage I/O circuits. One power-rail ESD clamp circuit is connected between VDD power line and VSS power line. A second power-rail ESD clamp circuit is connected between ESD bus line and VSS power line.

is maintained at 5-Vd (where Vd is the cut-in voltage of the parasitic drain-to-well diode), and the gate voltage of Mp1 is clamped at 5V through the turn-on of Mp3. Therefore, this design can meet the gate-oxide reliability constraints without leakage current path from I/O pad to VDD during normal circuit operating condition. Under ESD stress condition, the parasitic lateral p-n-p BJT in Mp1 is turned on to discharge ESD current by avalanche breakdown. Such a gated p-n-p BJT should be designed to effectively clamp the overstress ESD pulse without causing ESD damage in the mixed-voltage I/O circuits.

7.4.3.4 ESD Protection Design with ESD Bus

The whole-chip ESD protection scheme by using the additional ESD bus for the IC with power-down-mode application has been reported in [87]. Such design concept with ESD bus can be used to form the ESD protection network for the mixed-voltage I/O circuits, as shown in Fig. 7.41. The additional ESD bus line is realized by a wide metal line in CMOS IC [87], [88]. To save layout area, the ESD bus can be realized by the different metal layer, which overlaps the VDD power line. The ESD bus is not directly connected to an external power pin, but biased to VDD through the diode D1 in Fig. 7.41. The diode D1 connected between the VDD power line and ESD bus is also used to block the leakage current path from the I/O pad to VDD during normal circuit operating condition with a high-voltage input signal. The diode Dp is connected between I/O pad and ESD

bus, whereas the diode Dn is connected between VSS power line and I/O pad. One (the first) power-rail ESD clamp circuit is connected between VDD power line and VSS power line. Another (the second) power-rail ESD clamp circuit is connected between the ESD bus and VSS power line. The second power-rail ESD clamp circuit connected between ESD bus and VSS power line should be designed with high-voltage-tolerant constraints without suffering the gate-oxide reliability issue. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through the diode Dp to the ESD bus, and then through the second power-rail ESD clamp circuit to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be discharged through the diode Dp to the ESD bus, the second power-rail ESD clamp circuit to VSS power line, and then through the parasitic diode of the first power-rail ESD clamp circuit to the grounded VDD. With the turn-on-efficient power-rail ESD clamp circuits, high ESD level for the mixed-voltage I/O circuits can be achieved by this ESD protection scheme with ESD bus.

7.4.4 High-Voltage-Tolerant Power-Rail ESD Clamp Circuit

In aforementioned description, the turn-on-efficient power-rail ESD clamp circuit is much helpful to improve ESD robustness of the mixed-voltage I/O circuits under the four modes of pin combination in ESD test. For some mixed-voltage circuit applications, the power supply voltage may exceed the ordinary VDD of the process to drive a high-voltage output signal [89]. Therefore, it is required to design the high-voltage-tolerant power-rail ESD clamp circuit with low-voltage devices but without suffering the gate-oxide reliability issue. In the high-voltage-tolerant power-rail ESD clamp circuit, the standby leakage current between the power rails is an important concern, especially when the IC is operating at high-temperature environment.

The diode string in stacked configuration has been used as the power-rail ESD clamp circuit [86]. However, the Darlington bipolar amplification of the parasitic p-n-p BJT devices in the diode string induces a huge leakage current between the power rails. To reduce the leakage current of the diode string between the power rails, some modified designs, such as the Cladded diode string, Boosted diode string, and Cantilevered diode string, were reported in [86]. An improved design by adding an nMOS-controlled SCR device into the diode string to significantly reduce the leakage current between the power rails was reported in [90]. Besides, with the extra triple well in the process technology, the leakage current of the diode string can

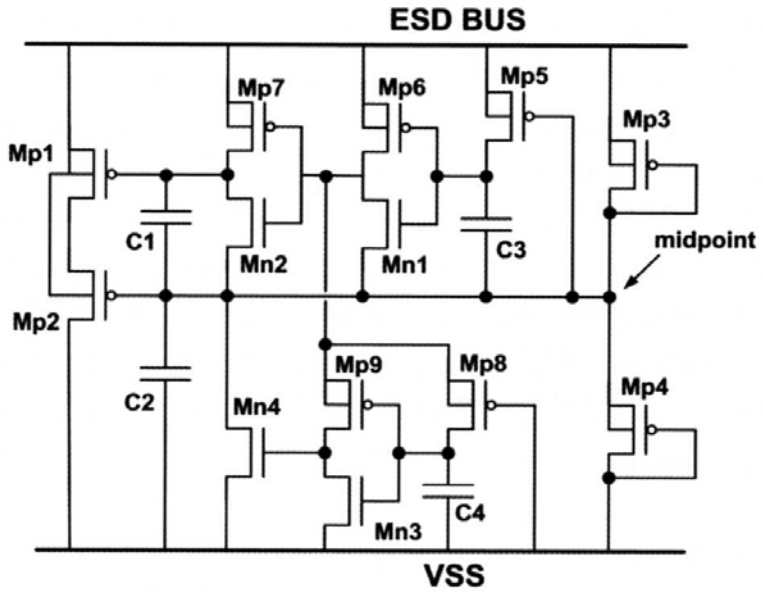


Figure 7.42: High-voltage-tolerant power-rail ESD clamp circuit realized with stacked-pMOS structure for the power line (VDD_h) of twice the ordinary VDD.

be further reduced [91].

The stacked-MOS configuration has been also used in the high-voltage-tolerant power-rail ESD clamp circuit [92]-[94]. Besides the gate-oxide reliability issue, how to improve the turn-on efficiency of the stacked-MOS structure during ESD stress and how to have a low standby leakage current between the power rails during normal circuit operating condition will be the design challenges.

One high-voltage-tolerant power-rail ESD clamp circuit realized with the stacked-pMOS structure has been reported in [92], [93] for 2xVDD tolerance, as shown in Fig. 7.42. In this power-rail ESD clamp circuit, the stacked-pMOS structure (Mp1 and Mp2) with large device width is designed to discharge ESD current between the ESD bus and VSS under ESD stress. The Mp3 and Mp4 are the long-channel devices which divide the high voltage at ESD bus by two for the midpoint with consideration of minimal leakage current. The gates of Mp1 and Mp2 are individually controlled by the RC-based ESD detection circuits. During normal circuit operating condition, the gate of top pMOS Mp1 is biased by the high voltage ESD bus, and the gate of bottom pMOS Mp2 is biased at half of the high voltage at ESD bus. Therefore, the Mp1 and Mp2 are kept off without the gate-oxide reliability issue. Under ESD stress condition, both gates of Mp1 and Mp2 are initially biased at $\sim$0V by the ESD detection circuits, therefore the ESD current is discharged through the turned-on stacked-pMOS structure. The design concept of stacked-pMOS configura-

tion can be further applied to implement the power-rail ESD clamp circuit for 3xVDD tolerance [92]. The standby leakage current through the voltage divider in the ESD detection circuit between the power-rails should be further reduced for low-power applications.

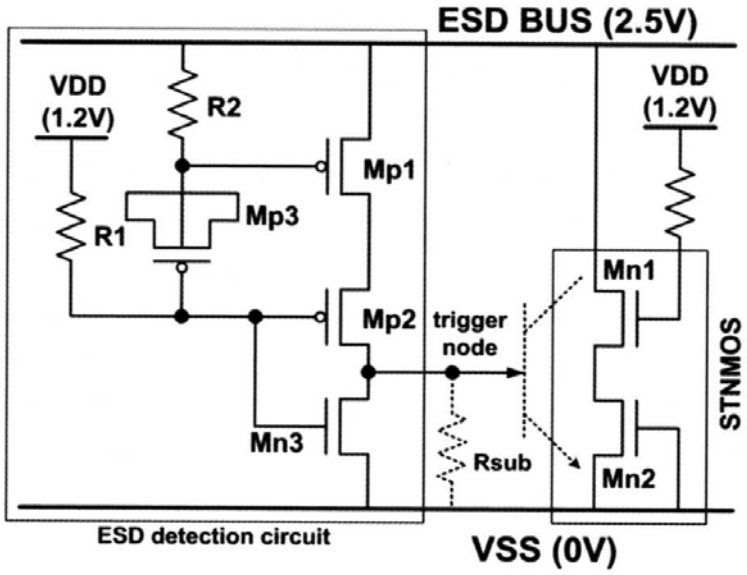


Figure 7.43: The high-voltage-tolerant power-rail ESD clamp circuit designed with only 1.2-V devices for operating with ESD bus of 2.5V.

Fig. 7.43 shows another high-voltage-tolerant power-rail ESD clamp circuit realized with only 1.2-V devices for 2.5-V (2xVDD tolerance) I/O applications [94], which contain the ESD clamp device and an ESD detection circuit. The ESD clamp device (Mn1 and Mn2) is realized by the stacked-NMOS (STNMOS) with the substrate-triggered technique. The STNMOS is kept off without gate-oxide reliability during normal operation conditions. The ESD detection circuit is kept inactive during normal operation conditions, but it becomes active to provide substrate-triggered current to quickly trigger STNMOS on under ESD stress conditions. Here, the time constant of R2 and C (realized by Mp3) should be designed to distinguish the power-on transition from the ESD transition. In normal operation conditions with VDD power supply of 1.2V, the ESD bus line could be charged up to maximum 2.5V by the 2.5-V input signal at I/O pad. With a maximum voltage level of 2.5V on the ESD bus, Mp1 and Mp2 are kept off but Mn3 is turned on to bias the substrate of STNMOS at VSS, such that STNMOS is guaranteed to be kept off. The voltages across the gate-drain, gate-source, and gate-bulk terminals of every device in Fig. 7.43 do not exceed the process limitation ($\sim$1.32V in a given 1.2-V CMOS process). When ESD transient voltage is conducted to ESD bus from I/O pad with VSS relatively grounded, but VDD floating with an

initial voltage level of 0V, Mp1 and Mp2 (whose initial gate voltages are at a low voltage level of ~0V) can be quickly turned on by ESD energy to generate the substrate-triggered current to trigger the STNMOS into its snapback region to discharge ESD current from ESD bus to VSS.

Substrate-triggered stacked-nMOS design can be further applied to implement the high-voltage-tolerant power-rail ESD clamp circuit [95] for 3xVDD tolerance, as shown in Fig. 7.44. In this design, the power-rail

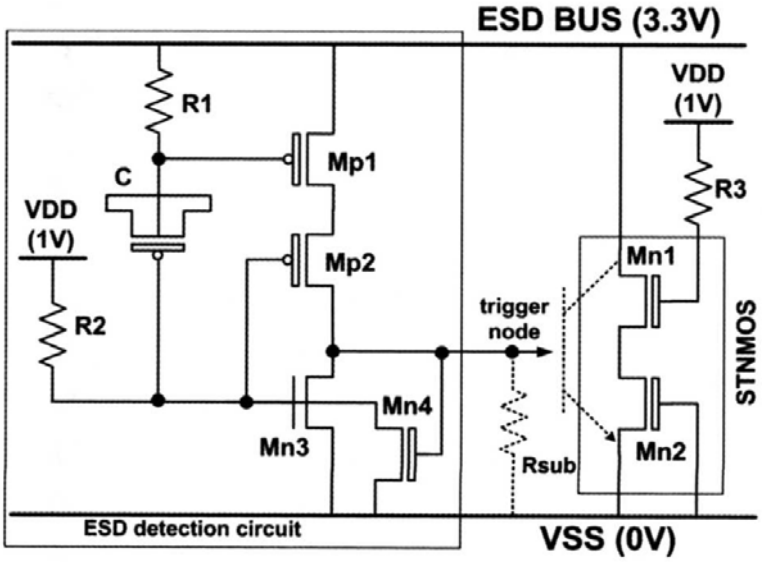


Figure 7.44: High-voltage-tolerant power-rail ESD clamp circuit realized with the substrate-triggered stacked-nMOS device. The power-rail ESD clamp circuit is realized by only 1-V and 2.5-V devices for the 3.3-V ESD bus without suffering the gate-oxide reliability.

ESD clamp circuit is realized by using only 1-V and 2.5-V devices for the ESD Bus of 3.3V. The internal power supply voltage is only 1V (VDD). The stacked-nMOS structure is formed by two 2.5-V nMOS transistors (Mn1 and Mn2). During normal circuit operating condition, the gate of top nMOS Mn1 is biased at VDD, and the gate of bottom nMOS Mn2 is biased at VSS. Therefore, the stacked-nMOS structure has no gate-oxide reliability problem under the 3.3-V bias of ESD Bus. The ESD detection circuit is composed of the two 2.5-V pMOS devices (Mp1 and Mp2), to provide the substrate current for triggering on the parasitic n-p-n BJT in the stacked-nMOS structure during ESD stress. The gates of Mp1 and Mp2 are individually controlled by the RC-based detection circuit. During normal circuit operating condition, the ESD detection circuit can meet the gate-oxide reliability constraints and the local substrate of the stacked nMOS is biased at VSS by the turn-on of Mn3. Under ESD stress condition, both the gates of Mp1 and Mp2 have the initial voltage level of ~

0V, while the VSS pin is grounded but the VDD pin floating. The ESD detection circuit will provide the trigger current flowing through the Mp1 and Mp2 into the p-substrate. The Mn4 is added in the ESD detection circuit to keep the Mn3 off and Mp2 in a conductive state under ESD stress condition. Once the parasitic n-p-n BJT in the stacked-nMOS structure is triggered on, the ESD current is discharged from the ESD Bus line to the grounded VSS. By this design, the turn-on-efficient high-voltage-tolerant power-rail ESD clamp circuit can be realized with an extremely low leakage current. Such a high-voltage-tolerant power-rail ESD clamp circuit can be used as the second power-rail ESD clamp circuit of Fig. 7.41 cooperating with the ESD bus for the mixed-voltage I/O buffer to receive 3xVDD input signals [96].

With the ESD protecton scheme of ESD Bus in Fig. 7.41, this ESD Bus (realized by wider metal lines in CMOS IC) and the high-voltage-tolerant power-rail ESD clamp circuit (connected between the ESD Bus and VSS) can be shared by other mixed-voltage I/O cells to save chip layout area. By the way, with this proposed ESD protection scheme of ESD Bus, the pin-to-pin ESD stresses across the mixed-voltage I/O cells can be effectively protected. The pin-to-pin ESD current discharging path along the I/O cells, which are designed with ESD Bus and high-voltage-tolerant power-rail ESD clamp circuit, is shown in Fig. 7.45. The pin-to-pin ESD stress current can be conducted through the diodes in forward-biased condition with the turned-on high-voltage-tolerant power-rail ESD clamp circuit to achieve a high ESD level for such mixed-voltage I/O interface circuits.

7.5 Summary

With the continue scaling on CMOS technologies into nanoscale dimension, more circuits and functions have been integrated into a chip, such as the system on a chip (SoC). With the scaled down CMOS process, the gate oxide becomes much thinner, which is more easily ruptured by the ESD overstress. The SoC integrated more circuits and functions into a chip often has a larger die size, which provides a larger body capacitance for storing the CDM charges in the body of IC. Besides, the SoC often have a lot of pin count of several hundreds. The layout area for each I/O cell in the high-pin-count SoC is critically limited. The layout area for drawing the ESD protection devices is also critically limited in such a high-pin-count SoC. In the SoC, it often has multiple separated power pins, which often cause some un-expected ESD failure located at the interface circuits between the circuit blocks. Therefore, the ESD issue will become much

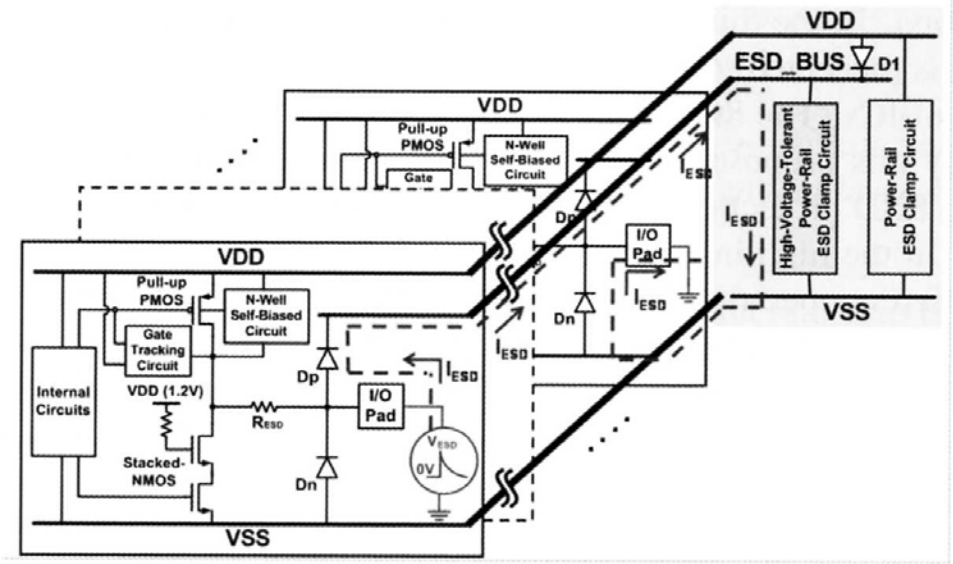


Figure 7.45: The pin-to-pin ESD current discharging path among the mixed-voltage I/O cells, which are protected by ESD Bus and the high-voltage-tolerant power-rail ESD clamp circuit. The ESD Bus (realized by wider metal lines in CMOS IC) and the high-voltage-tolerant power-rail ESD clamp circuit (connected between the ESD Bus and VSS) can be shared by all mixed-voltage I/O cells to save chip layout area.

worst than that we expected for the SoC fabricated in the nanoscale CMOS processes. Especially, the CDM ESD events will cause the main ESD failure in the SoC products.

The electronics products are very weak to sustain ESD stresses during the assembly, testing, package, and the field applications. ESD protection for nanoelectronics is not the process issue but more strong dependence of the design issue, which has been an important topic that the circuit designers must watch. In this tutorial, with the contents including (1) Introduction to Electrostatic Discharge, (2) Design Techniques of ESD Protection Circuit, (3) Whole-Chip ESD Protection Design, and (4) ESD Protection for Mixed-Voltage I/O Interface, the clear ESD protection design concepts and detailed circuit implementations have been presented, which are very helpful to the IC industry and academic researches.

In the first part, a brief introduction on ESD issue and standards to IC products is presented with some typical failure analysis pictures to demonstrate the impact of ESD on the reliability of IC products. In the second part, the design techniques of on-chip ESD protection circuits are presented with the consideration of turn-on behaviors on MOSFET. The state-of-the-art ESD protection techniques, gate-driven design and substrate-triggered design, are shown with design concepts and real circuit imple-

mentations. In the third part, the concept of "*whole-chip ESD protection design*" is presented to achieve the ESD protection for the core (internal) circuits of ICs. The SOC with separated power domains can be fully protected by this proposed whole-chip ESD protection design. In the forth part, the ESD protection design of the mixed-voltage I/O interface is presented. In the high-integration SOC applications, the circuit blocks may have different operating voltage levels. Therefore, the high-integration IC products often meet the mixed-voltage I/O interfaces. For such mixed-voltage I/O interfaces, the on-chip ESD protection circuits need to meet the limitations of mixed-voltage I/O interfaces, which cause more difficulty to achieve good ESD protection design for mixed-voltage I/O interfaces. In this forth part, a comprehensive overview on the ESD protection designs for the mixed-voltage I/O circuits without suffering the gate-oxide reliability issue. To improve ESD level of the mixed-voltage I/O circuits, the ESD protection design without increasing the process complexity is strongly requested by the mixed-voltage I/O circuits in consumer IC products. Such ESD protection design in the mixed-voltage I/O circuits still meets the gate-oxide reliability constraints, and needs to prevent the undesired leakage current paths during normal circuit operating condition. To design the efficient ESD protection circuit for the mixed-voltage I/O circuits with low parasitic capacitance for high-speed I/O applications and low standby leakage current for low-power applications will continually be an important challenge to SOC implementation in the nanoscale CMOS technology.

Finally, from long-term experience in ESD protection design, the IC chips should be designed with well-arranged ESD current discharging paths. To conduct ESD current under the desired discharging paths, but don't let ESD find its own discharging path in your IC. ESD protection design is more important in the nanoscale CMOS technology. High ESD robustness can not be achieved with only process solutions. The circuit design solutions should be added into the chips with suitable layout arrangement to achieve the purpose of whole-chip ESD protection for IC products.

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