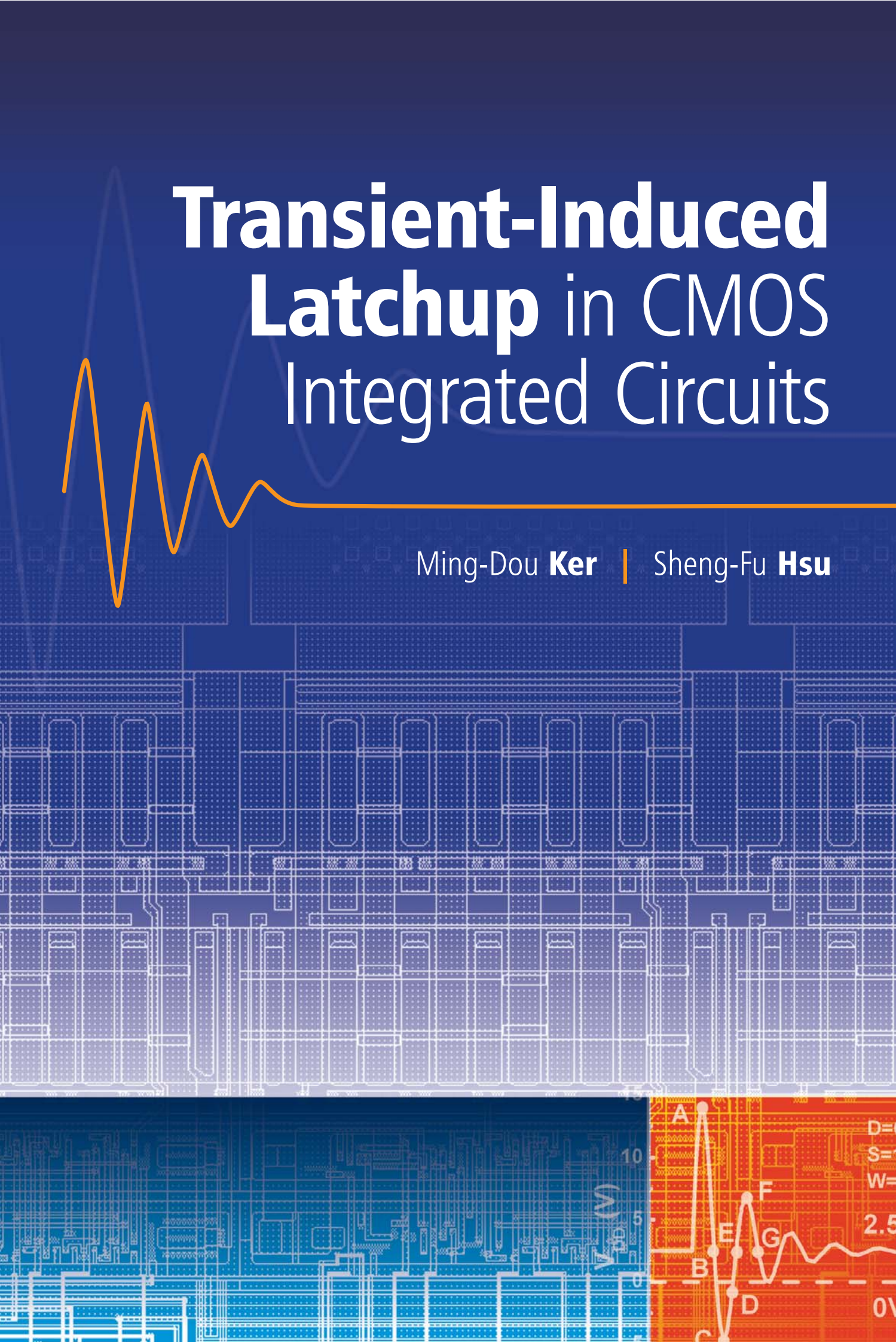
Transient-Induced Latchup in CMOS Integrated Circuits

Ming-Dou **Ker** | Sheng-Fu **Hsu**



Transient-Induced Latchup in CMOS Integrated Circuits

The book all semiconductor device engineers must read to gain a practical feel for latchup-induced failure to produce lower-cost and higher-density chips.

Ming-Dou Ker, *National Chiao-Tung University, Taiwan*
Sheng-Fu Hsu, *National Chiao-Tung University, Taiwan*

Transient-Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout. Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup, explaining the critical issues that have resurfaced for CMOS technologies. Once readers can gain an understanding of the standard practices for TLU, Ker and Hsu discuss the physical mechanism of TLU under a system-level ESD test, while introducing an efficient component-level TLU measurement setup. The authors then present experimental methodologies to extract safe and area-efficient compact layout rules for latchup prevention, including layout rules for I/O cells, internal circuits, and between I/O and internal circuits. The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0.18-micrometer 1.8V/3.3V silicided CMOS process.

- Presents real cases and solutions that occur in commercial CMOS IC chips
- Equips engineers with the skills to conserve chip layout area and decrease time-to-market
- Written by experts with real-world experience in circuit design and failure analysis
- Distilled from numerous courses taught by the authors in IC design houses worldwide
- The only book to introduce TLU under system-level ESD and EFT tests

This book is essential for practicing engineers involved in IC design, IC design management, system and application design, reliability, and failure analysis. Undergraduate and post-graduate students, specializing in CMOS circuit design and layout, will find this book to be valuable introduction to real-world industry problems and a key reference during the course of their careers.

Contents