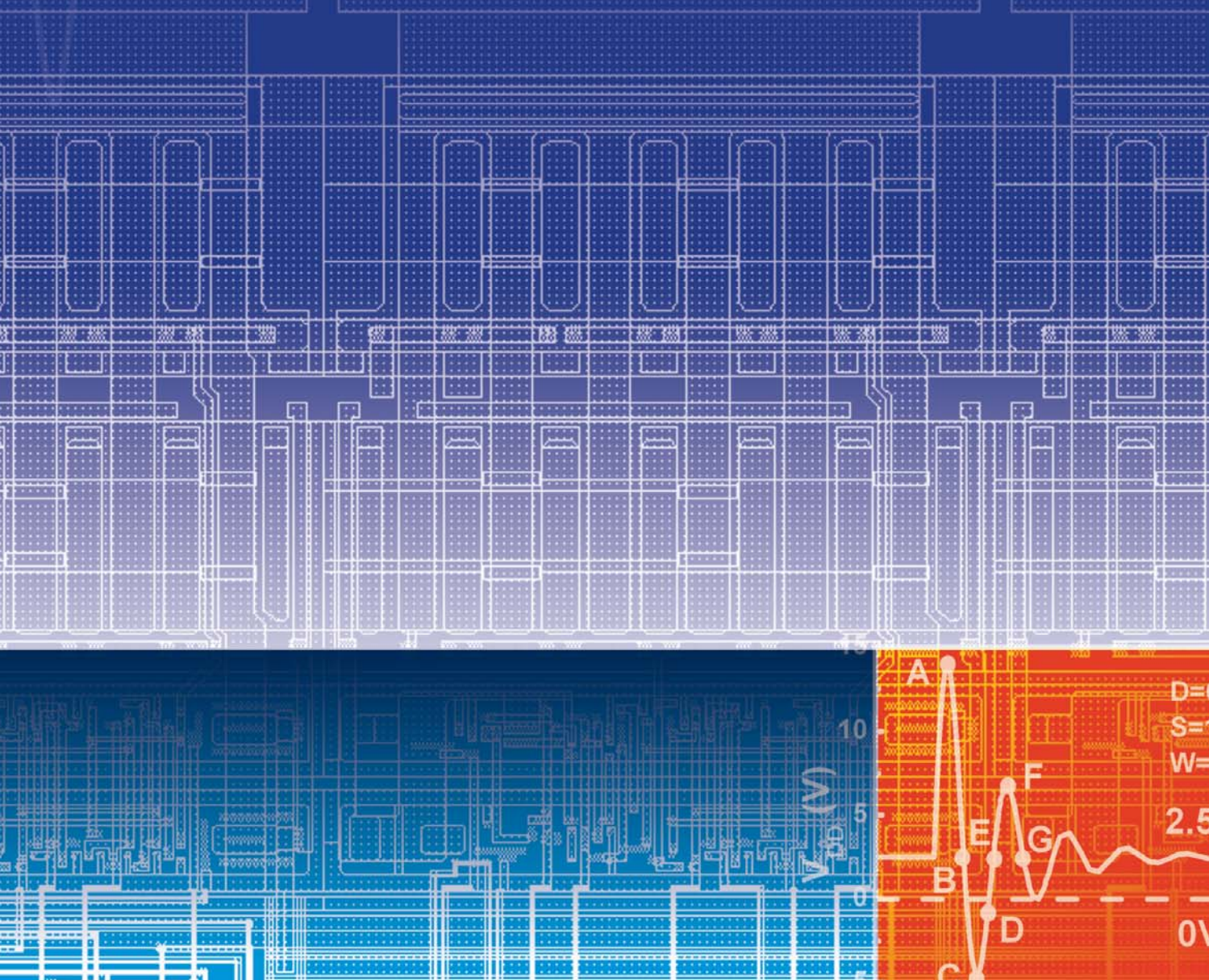


Transient-Induced Latchup in CMOS Integrated Circuits

Ming-Dou **Ker** | Sheng-Fu **Hsu**



Transient-Induced Latchup in CMOS Integrated Circuits

The book all semiconductor device engineers must read to gain a practical feel for latchup-induced failure to produce lower-cost and higher-density chips.

Ming-Dou Ker, *National Chiao-Tung University, Taiwan*
Sheng-Fu Hsu, *National Chiao-Tung University, Taiwan*

Transient-Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout. Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup, explaining the critical issues that have resurfaced for CMOS technologies. Once readers can gain an understanding of the standard practices for TLU, Ker and Hsu discuss the physical mechanism of TLU under a system-level ESD test, while introducing an efficient component-level TLU measurement setup. The authors then present experimental methodologies to extract safe and area-efficient compact layout rules for latchup prevention, including layout rules for I/O cells, internal circuits, and between I/O and internal circuits. The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0.18-micrometer 1.8V/3.3V silicided CMOS process.

- Presents real cases and solutions that occur in commercial CMOS IC chips
- Equips engineers with the skills to conserve chip layout area and decrease time-to-market
- Written by experts with real-world experience in circuit design and failure analysis
- Distilled from numerous courses taught by the authors in IC design houses worldwide
- The only book to introduce TLU under system-level ESD and EFT tests

This book is essential for practicing engineers involved in IC design, IC design management, system and application design, reliability, and failure analysis. Undergraduate and post-graduate students, specializing in CMOS circuit design and layout, will find this book to be valuable introduction to real-world industry problems and a key reference during the course of their careers.

Contents

Preface	xi
1 Introduction	1
1.1 Latchup Overview	1
1.2 Background of TLU	7
1.3 Categories of TLU-Triggering Modes	7
1.3.1 Power-On Transition	7
1.3.2 Transmission Line Reflections	8
1.3.3 Supply Voltage Overshoots	11
1.3.4 Cable Discharge Event	12
1.3.5 System-Level ESD Event	13
1.4 TLU Standard Practice	16
References	19
2 Physical Mechanism of TLU under the System-Level ESD Test	23
2.1 Background	23
2.2 TLU in the System-Level ESD Test	24
2.3 Test Structure	26
2.4 Measurement Setup	28
2.5 Device Simulation	30
2.5.1 Latchup DC I–V Characteristics	32
2.5.2 Negative V_{Charge}	32
2.5.3 Positive V_{Charge}	35
2.5.4 A More Realistic Case	37
2.6 TLU Measurement	38
2.6.1 Latchup DC I–V Characteristics	38
2.6.2 Negative V_{Charge}	39
2.6.3 Positive V_{Charge}	39
2.7 Discussion	41
2.7.1 Dominant Parameter to Induce TLU	41
2.7.2 Transient Responses on the Minority Carriers Stored within the SCR	43

2.8 Conclusion	44
References	44
3 Component-Level Measurement for TLU under System-Level ESD Considerations	47
3.1 Background	47
3.2 Component-Level TLU Measurement Setup	48
3.3 Influence of the Current-Blocking Diode and Current-Limiting Resistance on the Bipolar Trigger Waveforms	49
3.3.1 Positive V_{Charge}	51
3.3.2 Negative V_{Charge}	51
3.4 Influence of the Current-Blocking Diode and Current-Limiting Resistance on the TLU Level	54
3.4.1 Latchup DC I–V Characteristics	54
3.4.2 Positive TLU Level	55
3.4.3 Negative TLU Level	57
3.5 Verifications of Device Simulation	59
3.5.1 Dependences of the Current-Blocking Diode on TLU Level	59
3.5.2 Dependences of Current-Limiting Resistance on TLU Level	62
3.6 Suggested Component-Level TLU Measurement Setup	62
3.7 TLU Verification on Real Circuits	63
3.8 Evaluation on Board-Level Noise Filters to Suppress TLU	66
3.8.1 TLU Transient Waveforms of the Ring Oscillator	69
3.8.2 TLU Level of the Ring Oscillator with Noise Filters	70
3.9 Conclusion	72
References	73
4 TLU Dependency on Power-Pin Damping Frequency and Damping Factor in CMOS Integrated Circuits	75
4.1 Examples of Different D_{Freq} and D_{Factor} in the System-Level ESD Test	76
4.2 TLU Dependency on D_{Freq} and D_{Factor}	80
4.2.1 Relations between D_{Factor} and Minimum Positive (Negative) V_P to Initiate TLU	80
4.2.2 Relations between D_{Freq} and Minimum Positive (Negative) V_P to Initiate TLU	82
4.2.3 Relations between D_{Factor} and Minimum (Maximum) D_{Freq} to Initiate TLU	84
4.3 Experimental Verification on TLU	86
4.4 Suggested Guidelines for TLU Prevention	89
4.5 Conclusion	92
References	93

5	TLU in CMOS ICs in the Electrical Fast Transient Test	95
5.1	Electrical Fast Transient Test	95
5.2	Test Structure	98
5.3	Experimental Measurements	102
5.3.1	Negative EFT Voltage	103
5.3.2	Positive EFT Voltage	104
5.3.3	Physical Mechanism of TLU in the EFT Test	105
5.4	Evaluation on Board-Level Noise Filters to Suppress TLU in the EFT Test	106
5.4.1	Capacitor Filter, LC-Like Filter, and π -Section Filter	106
5.4.2	Ferrite Bead, TVS, and Hybrid Type Filters	109
5.4.3	Discussion	111
5.5	Conclusion	112
	References	112
6	Methodology on Extracting Compact Layout Rules for Latchup Prevention	113
6.1	Introduction	113
6.2	Latchup Test	114
6.2.1	Latchup Testing Classification	114
6.2.2	Trigger Current Test	115
6.2.3	V_{supply} Over-Voltage Test	117
6.3	Extraction of Layout Rules for I/O Cells	121
6.3.1	Latchup in I/O Cells	121
6.3.2	Design of Test Structure for I/O Cells	124
6.3.3	Latchup Immunity Dependency of I/O Cells	125
6.4	Extraction of Layout Rules for Internal Circuits	129
6.4.1	Latchup in Internal Circuits	129
6.4.2	Design of Test Structure for Internal Circuits	130
6.4.3	Latchup Immunity Dependency of the Internal Circuits	131
6.5	Extraction of Layout Rules between I/O Cells and Internal Circuits	136
6.5.1	Layout Considerations between I/O Cells and Internal Circuits	136
6.5.2	Design of Test Structure between I/O Cells and Internal Circuits	139
6.5.3	Threshold Latchup Trigger Current Dependency	141
6.6	Conclusion	148
	References	149
7	Special Layout Issues for Latchup Prevention	151
7.1	Latchup between Two Different Power Domains	151
7.1.1	Practical Examples	152
7.1.2	Suggested Solutions	156

7.2	Latchup in Internal Circuits Adjacent to Power-Rail ESD Clamp Circuits	156
7.2.1	Practical Examples	157
7.2.2	Suggested Solutions	159
7.3	Unexpected Trigger Point to Initiate Latchup in Internal Circuits	159
7.3.1	Practical Examples	161
7.3.2	Suggested Solutions	165
7.4	Other Unexpected Latchup Paths in CMOS ICs	165
7.5	Conclusion	167
	References	168
8	TLU Prevention in Power-Rail ESD Clamp Circuits	169
8.1	In LV CMOS ICs	169
8.1.1	Power-Rail ESD Clamp Circuits	171
8.1.2	TLU-Like Issues in LV Power-Rail ESD Clamp Circuits	174
8.1.3	Design of TLU-Free Power-Rail ESD Clamp Circuits	183
8.2	In HV CMOS ICs	189
8.2.1	High-Voltage ESD Protection Devices	190
8.2.2	Design of TLU-Free Power-Rail ESD Clamp Circuits	197
8.3	Conclusion	204
	References	205
9	Summary	207
9.1	TLU in CMOS ICs	207
9.2	Extraction of Compact and Safe Layout Rules for Latchup Prevention	209
	Appendix A: Practical Application—Extractions of Latchup Design Rules in a 0.18-μm 1.8 V/3.3 V Silicided CMOS Process	211
A.1	For I/O Cells	211
A.1.1	Nomenclature	211
A.1.2	I/O Cells with Double Guard Rings	212
A.1.3	I/O Cells with a Single Guard Ring	215
A.1.4	Suggested Layout Rules for I/O Cells	221
A.2	For Internal Circuits	223
A.2.1	Nomenclature	223
A.2.2	Design of Test Structures	223
A.2.3	Latchup Immunity Dependency of Internal Circuits	224
A.2.4	Suggested Layout Rules for Internal Circuits	226
A.3	For between I/O and Internal Circuits	226
A.3.1	Nomenclature	226
A.3.2	I/O and Internal Circuits (SCR)	227

A.3.3 I/O and the Internal Circuits (Ring Oscillator)	233
A.3.4 Suggested Layout Rules for between I/O and the Internal Circuits	235
A.4 For Circuits across Two Different Power Domains	237
A.4.1 Nomenclature	237
A.4.2 Design of Test Structures	237
A.4.3 Latchup Immunity Dependency between Two Different Power Domains	241
A.4.4 Suggested Layout Rules between Two Different Power Domains	242
A.5 Suggested Layout Guidelines	244
A.5.1 Latchup Design Guidelines for I/O Circuits	244
A.5.2 Latchup Design Guidelines for between I/O and the Internal Circuits	245
A.5.3 Latchup Design Guidelines for Internal Circuits	246
A.5.4 Latchup Design Guidelines for Circuits across Two Different Power Domains	246
Index	247