Closed-Loop Neuromodulation System-on-Chip (SoC) for Detection and Treatment of Epilepsy

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1. Abstract

This chapter presents a 16-channel closed-loop neuro-modulation system-on-chip (SoC) for detection and treatment on human epilepsy. In this SoC, a 16-channel neural-signal acquisition unit (NSAU), a bio-signal processor (BSP), a 16-channel high-voltage-tolerant stimulator (HVTS), as well as wireless power and bidirectional data telemetry are included. In the NSAU, the input protection circuit is used to prevent MOSFET devices from electrical overstress during the high-voltage stimulations. Hence, NSAUs can share the same electrodes with stimulators. The auto-reset chopper-stabilized capacitive-coupled instrumentation amplifiers (AR-CSCCIAs) are designed with the chopper-stabilized technique with offset reduction loop. The entropy-and-spectrum seizure detection algorithm is implemented in the BSP, which can perform 0.76-s seizure detection latency and 97.8% detection accuracy in the experimental results. When the seizure onset is detected by the BSP, the HVTS with adaptive supply control can deliver biphasic current stimulation of 0.5 ~ 3 mA to suppress the seizure onset. The developed SoC is powered wirelessly, and the bidirectional data telemetry is realized through the same pair of coils in 13.56 MHz. The downlink data rate is 211 Kb/s with the binary phase-shift keying (BPSK) modulation and a BPSK demodulator. The uplink data rate is 106 Kb/s with the load-shift keying (LSK) modulation. The developed SoC has been fabricated in a 0.18-μm low-voltage CMOS

process with 1.8V/3.3V devices. Electrical tests have been performed to characterize the SoC performance. In vivo animal experiments using mini-pigs have been performed to successfully verify the closed-loop neuromodulation functions on epileptic seizure suppression. In human clinical trials, the developed SoC has been performed to successfully suppress human epileptic seizures by closed-loop stimulation.

2. Keywords

Neuromodulation, system-on-chip (SoC), epilepsy, closed-loop seizure control, low-noise neural-signal amplifier, biphasic stimulation, wireless bidirectional data telemetry, wireless power transmission.

3. Introduction

Epilepsy, the common neurological disorder, afflicts about 1% of world's population [1]. It is characterized by recurrent seizures that occur after an episode of abnormal electrical activities in the brain. Epileptic seizures may cause a brief lapse of attention, unnatural posturing, or severe and prolonged convulsions. The unexpected seizures impact the quality of life on patients and their families.

Traditionally, the common treatment for epilepsy is medication. However, still around 30% of epileptic patients are drug resistant or have intolerable adverse effects. For these patients, the resection surgery of seizure onset region in the brain might be beneficial. But, the risks of neurologic deficits after the surgery, such as memory impairment, visual field loss, or movement malfunctions are always of serious concern.

Electrical neuromodulation on the central nervous system for drug-resistant epileptic patients has been attempted and the preliminary results have shown that it could be a promising solution, e.g. [2]-[3]. There are two types of neuromodulation systems, namely, open-loop and closed-loop. In the open-loop neuromodulation system, continuous electrical

stimulation is delivered to the brain, leading to a higher power dissipation which decreases the battery lifetime of the implanted devices.

On the other hand, the closed-loop or responsive neuromodulation system for epilepsy delivered electrical impulses to the selected brain region in response to the detected epileptic or pre-epileptic activities [4]-[8]. The closed-loop neuromodulation system is a more promising treatment for epilepsy because it can immediately and accurately detect epileptic activities and suppress seizures on the right brain region to achieve a higher treatment efficacy, less power dissipation, and longer battery lifetime.

From the clinical data [9], electrical current stimulation of up to 3 mA on cortical surface at seizure onset site was required to control human epileptic seizures. Recently, implantable medical devices (IMDs) with closed-loop electrical stimulation and wireless power/data telemetry for seizure control have been reported [4], [7], [8], [10] as a potential and efficient clinical treatment. In [4], the closed-loop neural prosthetic system with seizure detection achieved detection latency of 0.8s. However, since the system is designed for rats, the stimulation current is only 30uA. In [7], the stimulation current is up to 1mA. In [8], the stimulation current is up to 1.35mA, both are not enough for human. Moreover, there are two frequency bands used in the implanted system for power and data transmission. The large antenna area could be an issue for the implanted system. In [10], the wireless power and data telemetry is not integrated into the SoC, where the stimulation current is only up to 1 mA, still not enough for human.

Wireless power and bidirectional data telemetry is required in IMDs. So far, many structures have been reported [11]-[14]. Among them, wireless power and only uplink data telemetry was realized in one pair of coils [11] or two pairs of coils [12]. In [13], only data telemetry is implemented on chip with one pair of coils, but power telemetry has not been integrated on the same chip. In [14], only downlink telemetry is integrated with power telemetry in one pair of coils. However, the data rate is only a few kilo bit per second (bps).

In practical applications, one pair of coils is preferred to fit the size limitation of implanted medical device. Bi-directional data telemetry with high data rate is required to transmit bio-signals out and get data in to parameterize the implants through external control units.

A 16-channel closed-loop seizure control CMOS system-on-chip (SoC) for human epileptic seizure control is presented in this chapter. In this system, each channel (electrode) can sense ECoG and stimulate tissue independently. According to the clinician's experience, 16 channels (electrodes) can cover the possible seizure onset zone. Up to 3mA biphasic stimulation current are designed to be delivered to the tissue. An input protection circuit in the front-end preamplifier sharing the same electrode with the stimulator is designed to protect transistors from overstressing by high stimulation voltage [15]. In [15], only the neural-signal acquisition unit is described. However, this work presents the whole system including SoC with the wireless power and bi-directional data telemetry. The wireless power and bidirectional data telemetry circuits are designed to achieve high transmitted power with high power conversion efficiency (PCE) for the implantable SoC, as well as to obtain high uplink and downlink data rates through the same pair of high-Q coils in ISM band (13.56MHz). In the wireless power transfer, a new 2X/3X active rectifier with 2V and 3V output voltages and delay compensation is developed to enhance the power conversion efficiency. In the wireless data telemetry, a new binary phase-shift keying (BPSK) demodulator is designed to demodulate downlink BPSK data, and a load-shift keying (LSK) modulator is designed to transmit Electrocorticography (ECoG) data to the external device through the high-Q coils. The closed-loop seizure control SoC achieves a high seizure detection accuracy of 97.8% within 0.76s of detection latency, as verified on the animal in-vivo experiments of mini pigs and human clinical trials.

4. System-on-Chip (SoC) for Closed-Loop Neuromodulation

4.1 System Architecture

Fig. 1 shows the architecture of the overall microsystem including the closed-loop seizure control SoC in the IPG (Implantable Pulse Generator) case, a pair of high-Q coils, and the chip of external control system. In the SoC, a neural-signal acquisition unit (NSAU), a bio-signal processor (BSP), a high-voltage-tolerant stimulator (HVTS), and a wireless power and data telemetry unit are integrated. The signal processing flow is described as follows. The ECoG signals are sensed through the electrodes on cortical surface and sent to the NSAU in the SoC. The sensed ECoG signals are amplified and processed by the auto-reset chopper-stabilized capacitive-coupled instrumentation amplifiers (AR-CSCCIA), the programmable transconductance gain amplifiers (PTGA), the multiplexer (MUX), and the transimpedance amplifier (TIA) [5]. Then the signals are digitized by the delta-modulated SAR ADC and further processed by the BSP to extract both entropy and power spectral density in specific frequency bands for seizure detection. Once the seizure is detected, the BSP sends a stimulation control signal to activate the HVTS in order to generate biphasic stimulation currents to suppress abnormal brain activities. Moreover, the BSP also resets the memory. Thus each seizure detection result is independent, which can avoid instability of the closed-loop system. To achieve a constant stimulation current over a wide impedance range of electrodes-tissue interface, the adaptive regulated charge pump, the current digital-to-analog converter (DAC), and high-voltage-tolerant stimulus drivers are used [16]-[18]. The adaptive regulated charge pump generates a high voltage up to 12V without gate reliability issues in low voltage CMOS process. The output voltage is regulated by pulse-frequency-modulation (PFM) feedback. The maximum output stimulation current is 3mA. The control clock of each charge pump stage has a phase shift from each other, which can reduce the maximum peak current from 3V supply voltage provided by the 2X/3X active

rectifier. The adaptive supply voltage control technique is used in the adaptive charge pump, which can reduce the conduction loss on high-voltage-tolerant stimulus driver.

The external control system consists of a bidirectional data transceiver and a class-E power amplifier (PA). The detection and stimulation parameters in the BPSK form and the power of SoC are transmitted from external control system to the SoC wirelessly. The BPSK data is demodulated by the BPSK demodulator whereas the power is regulated by the 2X/3X active rectifier and the low-dropout regulators (LDOs). The seizure detection result and the recorded ECoG in the LSK form are transmitted back from the LSK modulator of SoC to the external control system through the same coil.

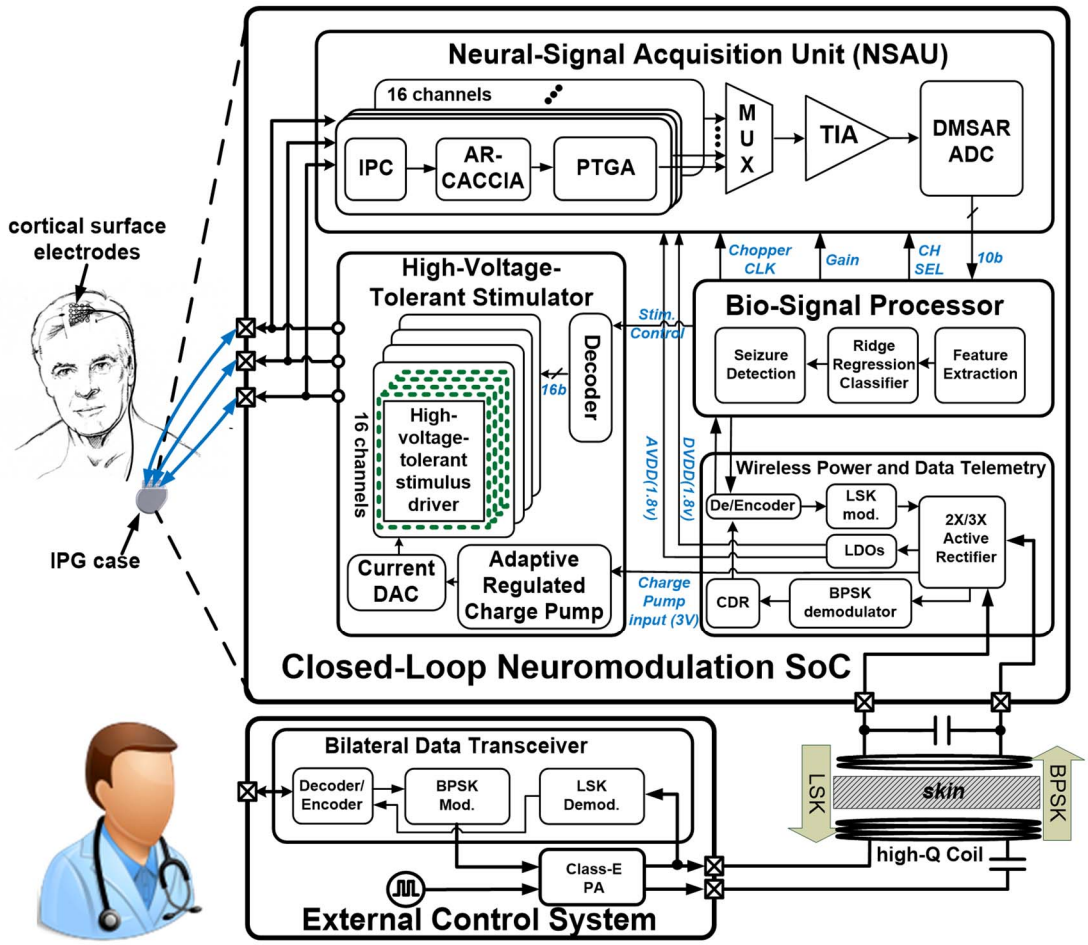


Fig. 1 Block diagram of the proposed closed-loop seizure control SoC and external control system.

4.2 Circuit Design

The circuit implementation can be divided into four different parts: NSAU (neural-signal acquisition unit), BSP (bio-signal processor), 16-channel HVTS (high-voltage-tolerant stimulator), and wireless power/data telemetry unit.

4.2.1 Neural-Signal Acquisition Unit (NSAU)

As shown in Fig. 2, the 16-channel NSAU consists of 16 input protection circuits, AR-CSCCIAs, PTGAs, a MUX, a TIA, a 10-bit delta-modulated SAR ADC, a ripple reduction loop (RRL) global control, and a clock controller [15]. The ECoG signals sensed from the electrodes through the input protection circuit are amplified by the AR-CSCCIA with 45-dB gain and the PTGA with a programmable gain of 5/15/25 dB for patient-specific ECoG signal acquisition. The PTGA also converts differential voltage ECoG signals into single-ended current signals for the MUX so that the fast channel selection on current signals can be achieved in the MUX. The TIA is used to convert input current signals into voltage signals and drive the capacitor array of delta-modulated SAR ADC. Since the channel multiplexing frequency is 32 kHz, the TIA output should be settled down before SAR ADC sampling, which means that the maximum settling time is 7.8125 μs. Considering the linearity and dynamic range, the current-based topology is better than the voltage topology. The PTGA is designed by using the source degeneration circuit. Since the signal paths among PTGA, MUX, and TIA are of current signals with low impedance, high slew rate, high dynamic range, high channel selection rate, and short transient time of PTGA can be achieved. In the proposed closed-loop seizure control system, the NSAU, which senses the ECoG signal, has to share the same electrode with the HVTS, which delivers the constant current stimulation to suppress the seizure onset. During the stimulation, the gate-oxide overstressing caused by the high voltage generated by the HVTS on the MOS devices in the

NSAU should be avoided. To prevent this overstressing, an input protection circuit is designed by using high-voltage-tolerant switches and self-adaption bias circuits [15].

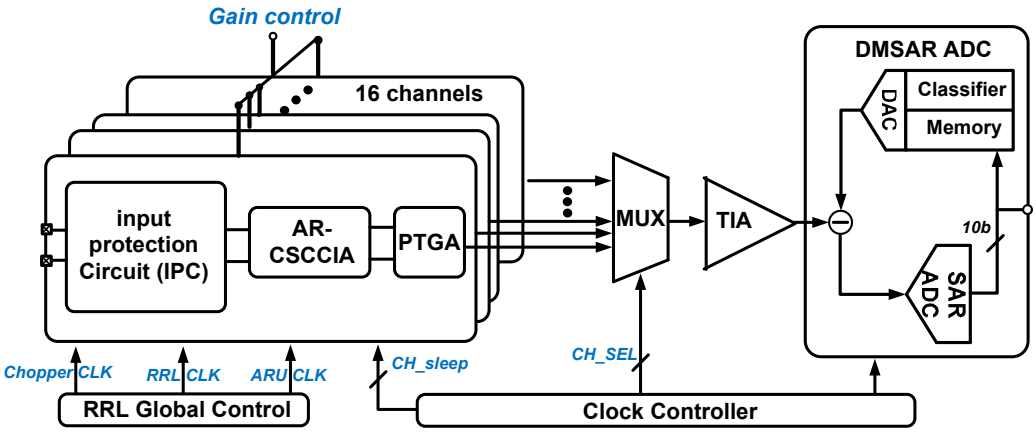


Fig. 2 Structure of the NSAU [15].

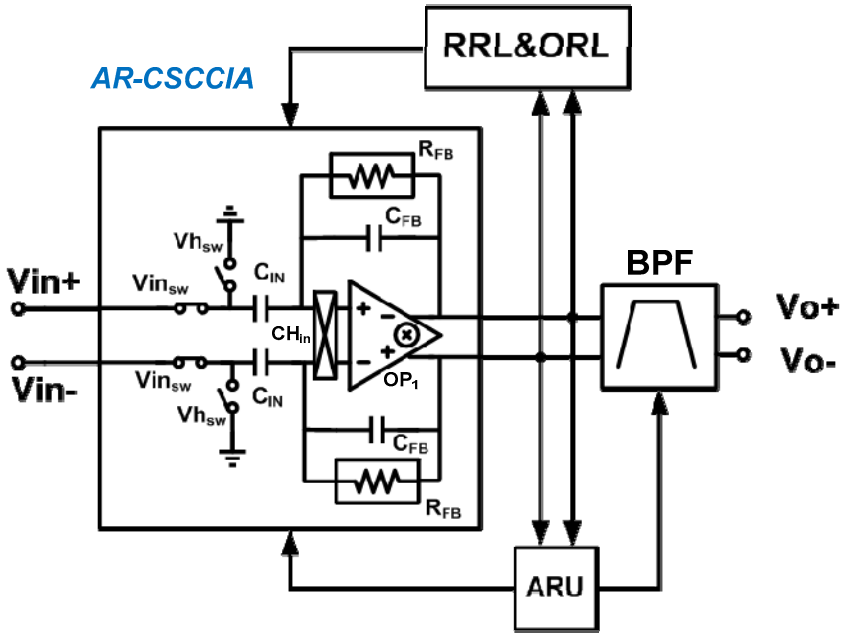
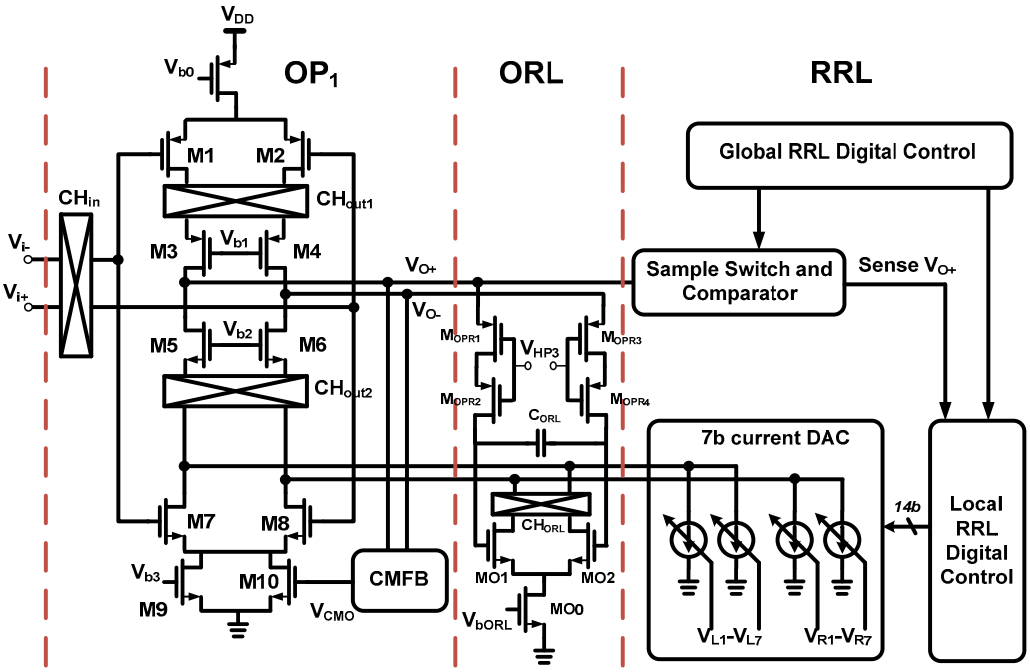


Fig. 3 Architecture of the AR-CSCCIA.

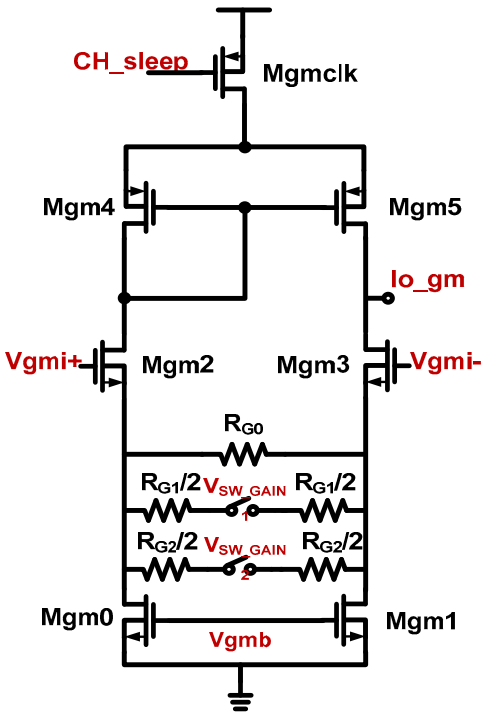
Fig. 3 shows the architecture of the AR-CSCCIA, which is composed of an operational amplifier (OP1), an RRL, an offset reduction loop (ORL), an auto-reset unit (ARU), and a bandpass filter (BPF). To filter out the flicker noise while amplifying the ECoG signal, the chopper modulation technique is used. The input modulator CHin is placed after the input

capacitors *C*IN to achieve high input impedance and good electrode dc offset rejection capability. Since the signal is demodulated back to the baseband before reaching the output, the output dominate pole and the bandwidth (BW) of OP1 can be designed as small as that of the amplifier without chopper modulation. Fig. 4(a) shows the schematic of AR-CSCCIA. The inverter-based cascode OP amplifier OP1 uses both PMOS and NMOS transistors as input pairs to form the inverter-based cascode structure and achieve a better noise-efficiency factor (NEF). The RRL and the ORL are designed to reduce the chopper-induced artifacts of chopper ripple and input-referred offset, respectively [15]. Without the ORL, the offset of AR-CSCCIS caused by the mismatches of input chopper switches and parasitic capacitors at the virtual ground nodes of OP1 would be amplified by chopper modulation. Then, the output offset voltage might cause the undesired gain degradation and dc operating point shift of the PTGA. Because of the stimulation artifacts and interfaces, the AR-CSCCIA may be saturated and recovered slowly. To improve this situation, an ARU is added in the AR-CSCCIA by comparing the output voltage of the AR-CSCCIA with the preset voltages. Once the output voltage exceeds the preset margin, the gate voltage of the pseudo-resistors *R*FB in Fig. 3 is shorted to ground to provide a fast reset path. With the ARU, the stimulation artifact is settled down in 9 ms. A source degeneration architecture is used in the design of PTGA as given in [15]. The circuit is shown in Fig. 4(b). When the channel is deselected, the power control gate is turned off (CH_sleep = 1.8 V) to save the power dissipation of the deselected PTGA. When the channel is selected and the power control gate is turned on, the transit time is designed to obtain the output with low distortion. Since the interface between the PTGA and the TIA is at low impedance, it can achieve a high slew rate, low transit time, and small output swing. The small output swing benefit to the linearity of the amplifier [5]. Note that the mismatch issue of PTGA and TIA is less significant because the preceding AR-CSCCIA has the high enough gain of 45 dB. The NSAU provides a three-step gain (50,

60, and 70 dB) for patient-specific signal scaling. The high-pass corner is at 0.59 Hz and the low-pass corner is at 117 Hz. The NEF of AR-CSCCIA is 3.78.



(a)



(b)

Fig. 4. (a) Schematic of the AR-CSCCIA (b)Schematic of PTGA [15].

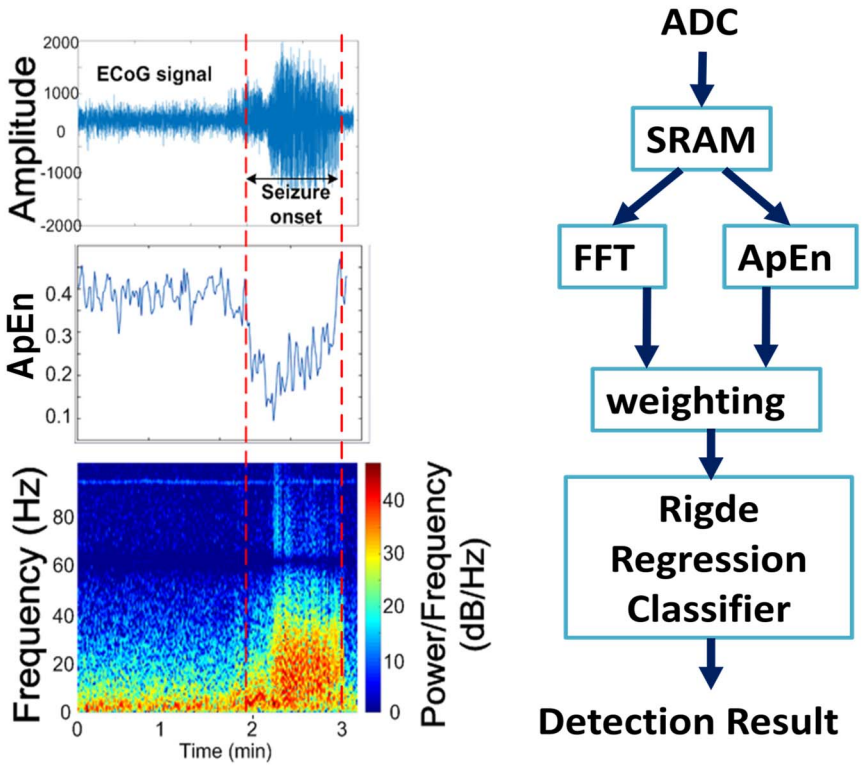
4.2.2 Bio-Signal Processor (BSP)

Complex analysis such as the approximate entropy (ApEn) has proven to work well on distinguishing from Electroencephalography (EEG) signals during wakefulness and seizures. The ApEn is a measurement that quantifies both regularity and predictability over time-series data. The time-series signals containing many repetitive patterns have a relatively smaller ApEn. Conversely, the less predictable process has a higher ApEn. Because of the fact that the periodic signal components of seizures reduce the complexity levels and the ApEn significantly, the ApEn is utilized to analyze the complexity of ECoG signals. Fig. 5(a) shows the ApEn value versus the time. It can be seen from Fig. 5(a) that during the seizure onset of human, the ApEn value is nearly zero.

However, only the feature of ApEn value for the seizure detection cannot achieve enough accuracy because artifacts and slow-wave sleep waveforms may have lower ApEn values. The ECoG spectral analysis based on short-term Fourier-transform shows that the seizure has a large spectral power in 7-9 Hz and

14-18 Hz bands as observed in the epilepsy experiments of rats. However, the human epilepsy is much more complex than the rat epilepsy. The power spectral density in frequency bands from 4-64 Hz shows significant changes during the human epileptic seizure onset. Thus, the average powers spectral densities over the 4 Hz intervals are calculated in the 4-64 Hz band as the 15 features. As shown in Fig. 5(a), the band power distribution of 4-64 Hz is obvious during the seizure onset of human. Thus, the 15 features of average band power spectral density can be extracted. The decimation-in-frequency (DIF) fast Fourier transform (FFT) is used for the hardware implementation to calculate the power of specific frequency bands. In the calculation of the overall feature of power spectral density, the multiple outputs of FFT in the specific frequency bands are multiplied by weighting factors and summed up together.

The seizure detection algorithm is shown in Fig. 5(b) where the extracted features of ApEn and power spectral density from FFT are fed into the ridge regression classifier (RRC). The RRC method finds a best fitting linear model that minimizes the mean square error between the system output and the desired output. Since the output of linear model is the weighted sum of input features, it is suitable for hardware implementation with reduced computational cost.



(a) (b)

Fig. 5 (a) ApEn and spectrum features in seizure onset waveforms of human. (b) Seizure detection algorithm.

Fig. 6 shows the hardware implementation diagram of BSP where the 128-point DIF FFT and Mean Band Power are used to calculate the power spectral density. The Entropy calculation is used to calculate the ApEn. The power spectral density and ApEn are then processed by the RRC. The RRC determines the seizure onset channel within 0.36ms calculation time.

The training of the regression classifier was performed in an off-line computer by using the recorded ECoG data of 5 patients to extract the 16 weights and the threshold of the regression classifier. Then different recorded ECoG data of the 5 patients were used in the testing stage. The accuracy, sensitivity, and specificity were obtained through the average of the results from the 5 patients. The accuracy, sensitivity, and specificity are 97.8%, 96.0%, and 100%, respectively.

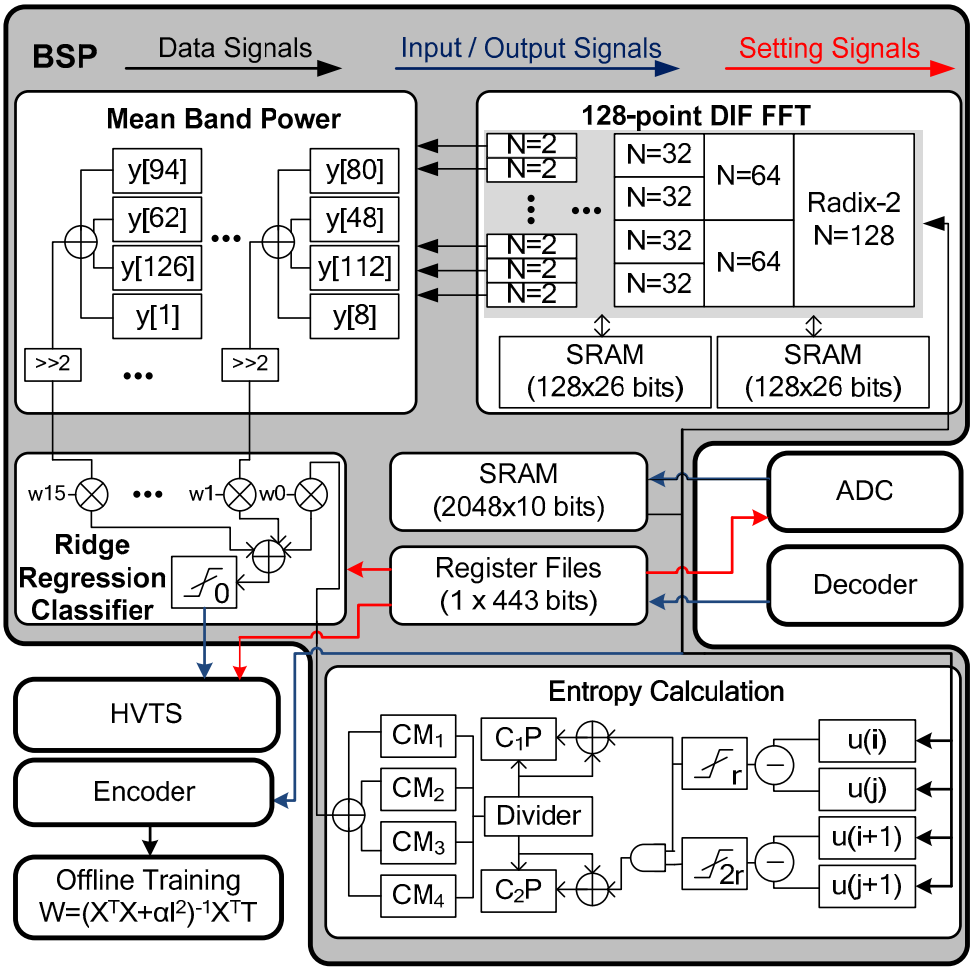


Fig. 6 Hardware implementation of the bio-signal processor.

4.2.3 High-Voltage-Tolerant Stimulator (HVTS)

Fig. 7 shows the architecture of 16-channel HVTS [16]-[18], which consists of a 3-stage adaptive regulated charge pump, a current DAC with the triode indicator, a decoder, and the 16-channel high-voltage-tolerant stimulus drivers. The biphasic stimulation current

pulses are adjustable from 0.5mA to 3mA. The structures of adaptive regulated charge pump and high-voltage-tolerant stimulus driver are shown in Fig. 8. In the adaptive regulated charge pump, the output voltage is proportional to the output clock frequency of 4-phase clock generator. It uses the PFM feedback to generate the regulated output voltage of 4xVDD. The PFM feedback consists of 4-phase clock generator, voltage-controlled oscillator (VCO), and error amplifier. By applying phase-shift clock control scheme, the control clock of each charge pump stage has a phase shift different from each other. This can decrease the peak current from supply and enhance the transient response of the wireless power telemetry.

To integrate with other circuits in the SoC and decrease the mask cost, the HVTS is implemented in 180nm low-voltage process. The problems of gate-oxide overstressing, hot-carrier effect, and other reliability issues should be considered. The high-voltage-tolerant stimulus driver is designed to solve both reliability and safety issues.

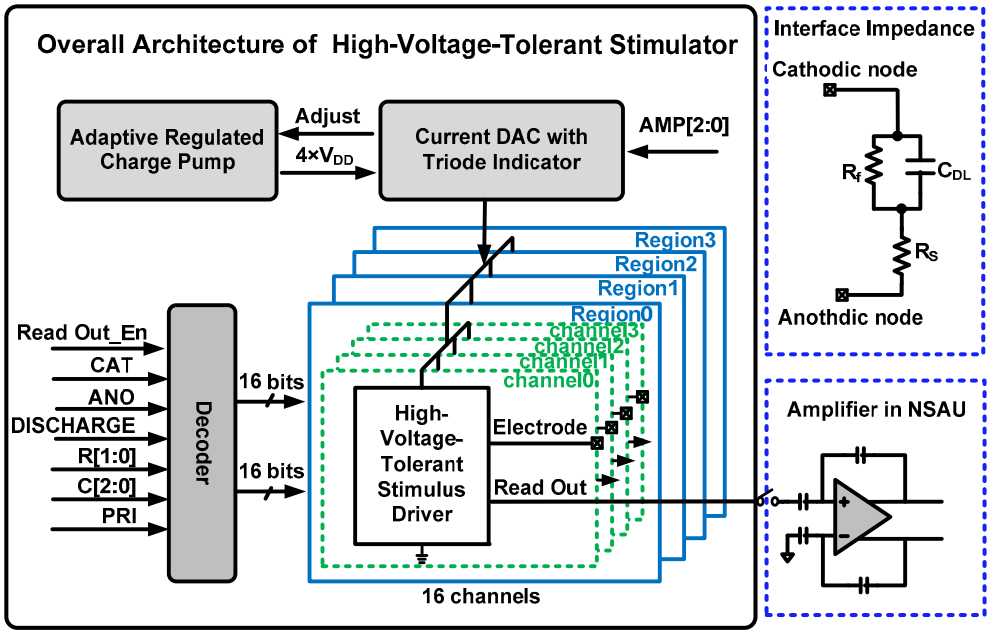


Fig. 7 Architecture of the high-voltage-tolerant stimulator (HVTS) [17]-[18].

As shown in Fig. 8, the transistors MB1 to MB6 act as a self-adaption bias circuit to keep the voltages across each MOS device in the stacked structures within 3.3 V under

4xVDD (12V) power supply. The output of the regulated charge pump is driven by the "adjust" signal. A triode indicator is used to control the regulated charge pump that provides an adaptive power supply at the 4xVDD node to ensure MC3 and MC4 operated in saturation region during constant current stimulation. Since the voltage on the double-layer capacitor of the electrode is increased gradually during constant current stimulation, the voltage drop across the transistors MC3 and MC4 becomes less than 0.8V. Once the cascode transistors (MC3 and MC4) are out of the saturation region, the triode indicator generates an "adjust" signal to the regulated charge pump which increases the supply voltage at 0.5V steps promptly to keep both MC3 and MC4 in saturation and maintain a constant stimulation current.

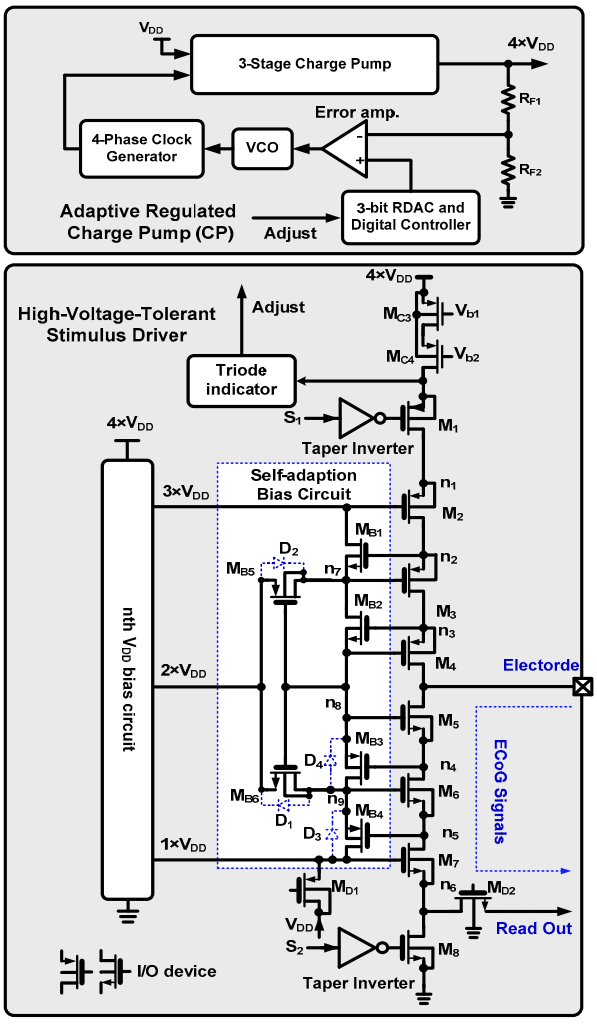


Fig. 8 Structures of adaptive regulated charge pump and high-voltage-tolerant stimulus driver [17]-[18].

4.2.4 Wireless Power and Bi-directional Data Telemetry

It is important for the implanted SOC to have a maximum power efficiency to reduce the power dissipation and keep the device temperature variation below 2°C [19]. Due to the maximum 3mA stimulation current, about 90% of power dissipates on the HVTS during the stimulation period. In order to get the highest power efficiency, minimizing the number of charge pump stages of the HVTS can increase the power efficiency because the higher number of charge pump stages leads to the lower efficiency. Therefore, a new architecture of active rectifier that can provide both 2V and 3V output voltages are adopted. By using the 3V as the input, the number of charge pump stages can be effectively reduced and its power efficiency can be increased.

Fig. 9 shows the architecture of wireless power and bidirectional data telemetry which consists of a 2X/3X active rectifier, 2 LDOs, a BPSK demodulator, a LSK modulator, and a De/Encoder. The received AC signal in the secondary coil is regulated by the 2X/3X active rectifier with delay compensation. The regulated 2V is connected to ALDO and DLDO for analog and digital power supply, respectively. The regulated 3V provides the input voltage of HVTS.

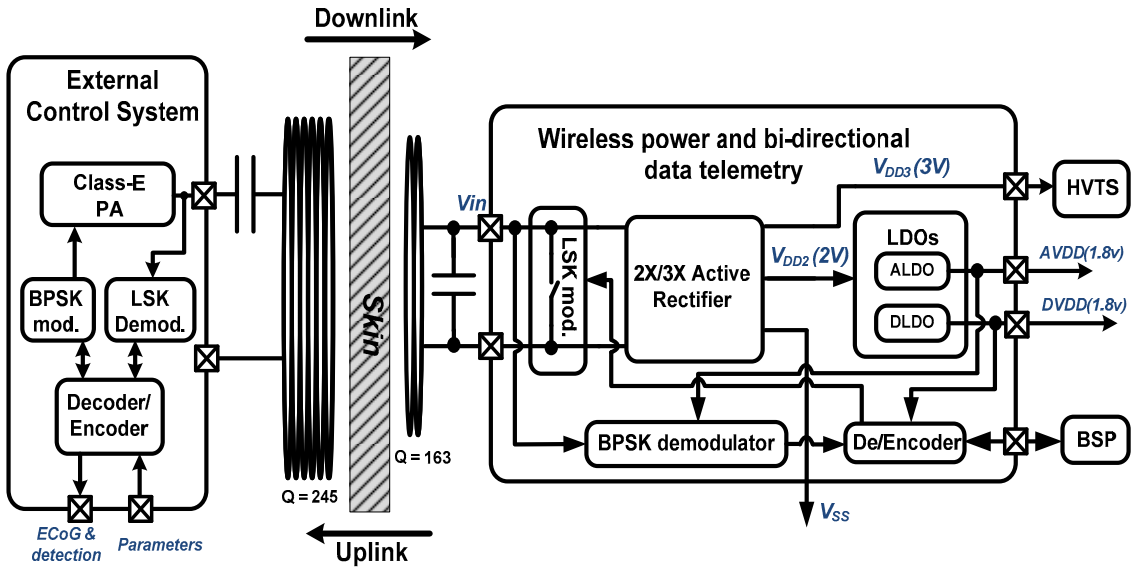


Fig. 9 The architecture of wireless power and bidirectional data telemetry

The circuit structure of the 2X/3X active rectifier is shown in Fig. 10, which consists of a start-up circuit, a NMOS active diode, two PMOS active diodes, two delay-compensated comparators (DCMPH and DCMPL) with delay compensation control, a level shifter, and off chip filtering capacitors.

In Fig. 10, the voltage level of the output voltage V_{g02p} of DCMPH is from 0V to V_{DD2} (2V). Since the I/O device can handle 3.3V in 0.18μm CMOS technology, a simple level shifter can be designed by using I/O devices to convert the voltage level from V_{DD2} to V_{DD3} (3V) without device over-stress issue. It converts the voltage level and enhances the driving ability to drive the large input capacitance of power transistor M_{P2}.

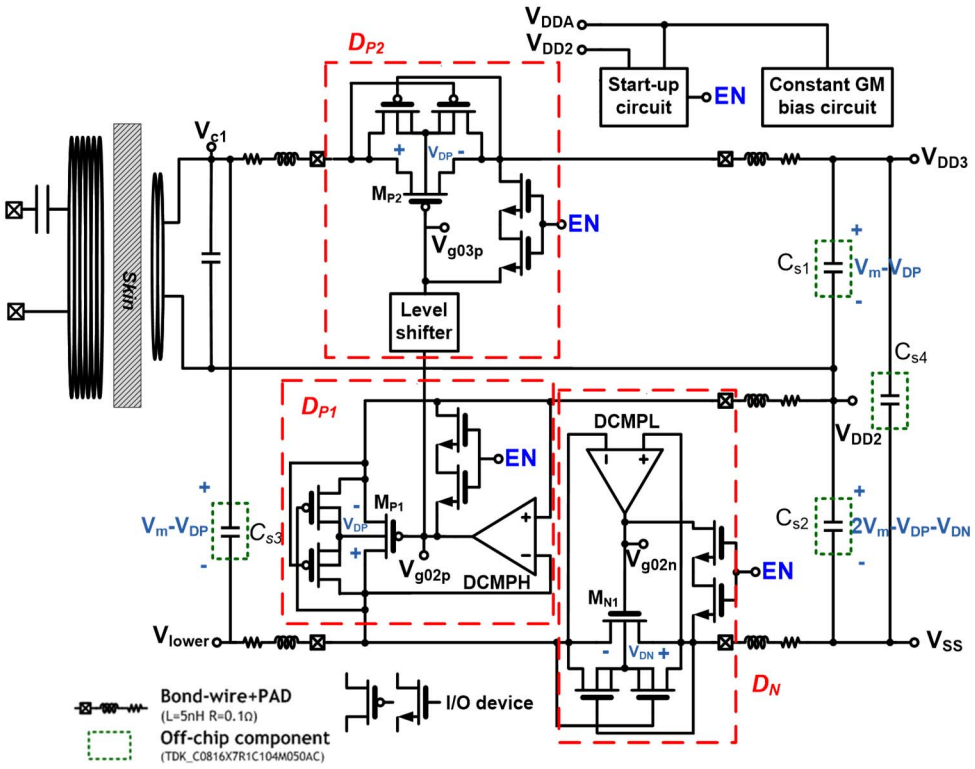


Fig. 10 The circuit structure of 2X/3X active rectifier.

To minimize the device size for implantation, only one pair of coils for both wireless power and bi-directional data telemetry is adopted in the proposed implanted SoC. The high-Q coils are used to achieve a high wireless PCE since the energy can be stored at the specific

frequency of 13.56MHz. The inductances and Q values of TX and RX coils are significantly increased by the permeability of the ferrite core. Thus the efficiency can also be increased. The resonant inductive link with ferrite core achieves 76.3% power transfer efficiency as reported in [20].

Since the pair of coils has high Q values of 245 in primary and 163 in secondary, the data channel capacity is decreased. Therefore the uplink and downlink data rates are designed to 106Kbps and 211Kbps, respectively. When a downlink BPSK data transition occurs, the secondary coil requires a few cycles to invert its phase. Under this situation, the edge of BPSK signal is not significant and the conventional edge-detection BPSK demodulators cannot be applied. Thus the PLL-based edge-detection BPSK demodulator is proposed as shown in Fig. 11(a) where a PLL is used to lock the carrier frequency. The source-switching topology is used in the charge pump to guarantee a lower charge sharing when the switch is turned on. The loop-bandwidth of PLL is designed at 900KHz to optimize phase noise performance. In Fig. 11(a), the phase-frequency detector can sense the phase change and generate phase difference signals when the data change. A trigger detector is designed to detect the output of phase-frequency detector and generate a trigger signal when the phase difference signals exceed a preset threshold. The data recovery is composed of a D Flip-Flop which inverts the current data when a trigger signal is generated. The output of data recovery is sent to the decoder. The clock recovery is composed of a divided-by-64 frequency divider. The input of the clock recovery is the carrier signal (13.56MHz) and its output generates a clock frequency of 211KHz. Due to the change of carrier frequency during the data transition, the clock recovery requires a reset signal, which is the trigger signal from the trigger detector, to prevent non-synchronization of data and clock.

Fig. 11(b) shows the schematic of voltage-controlled oscillator in the proposed PLL-based edge-detection BPSK demodulator. M_{VCO6}-M_{VCO11} are the inverter chain for oscillating. To eliminate the process-variation induced frequency shift which cause the

trigger detector failed to detect the data edges, a current control unit composed of M_{VCO1}-M_{VCO3} is designed to convert the input control voltage V_{ctrl} to the current I_{VCO} supplied to the VCO to control its output frequency. When the control voltage V_{ctrl} is fed from the loop filter, V_x in Fig. 11(b) can be written as

$$V_X = V_{ctrl} - V_{th} - \sqrt{\frac{2I_{bias}}{\beta_{MVCO2}}} \quad (1)$$

where I_{bias} is the constant bias current of the VCO, $\beta_{MVCO2} = \mu Cox(W/L)$, and μ , Cox , W, L, and Vth are the mobility, gate capacitance density, width, length, and threshold voltage of the MOS device M_{VCO2}, respectively. Since the bias current I_{bias} is a constant value, V_x is linearly proportional to V_{ctrl}. Thus the current I_{VCO} fed to the inverter chain can be expressed as

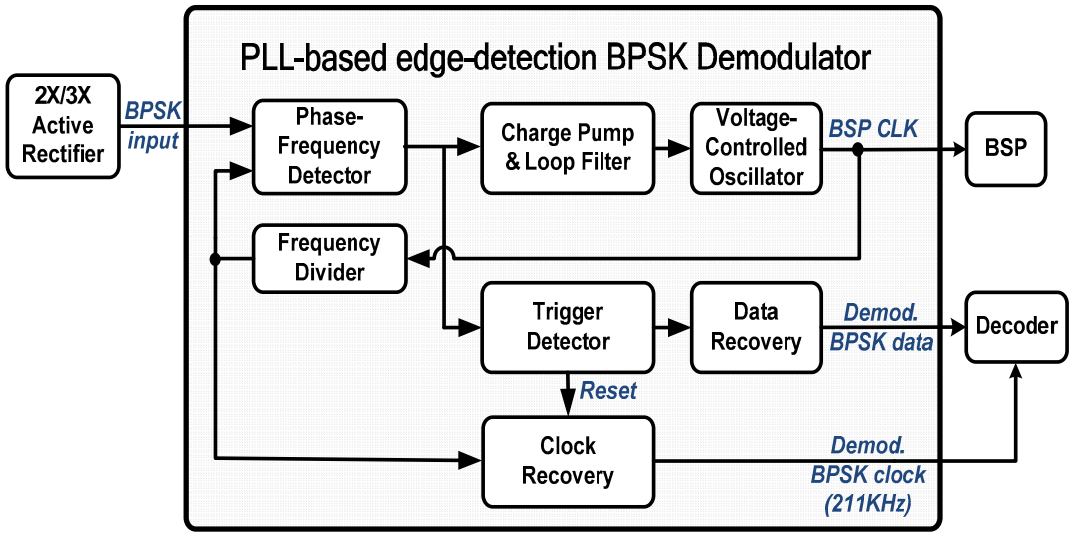
$$I_{VCO} = \frac{1}{2}\beta_{MVCO1}(V_{DD} - V_{ctrl} + \sqrt{(\frac{2I_{bias}}{\beta_{MVCO2}})})^2 \quad (2)$$

It can be seen from (2) that the current is not sensitive to V_{th} which can reduces the process variations. The tranconductance G_m and the VCO gain K_{VCO} of the VCO can be expressed as

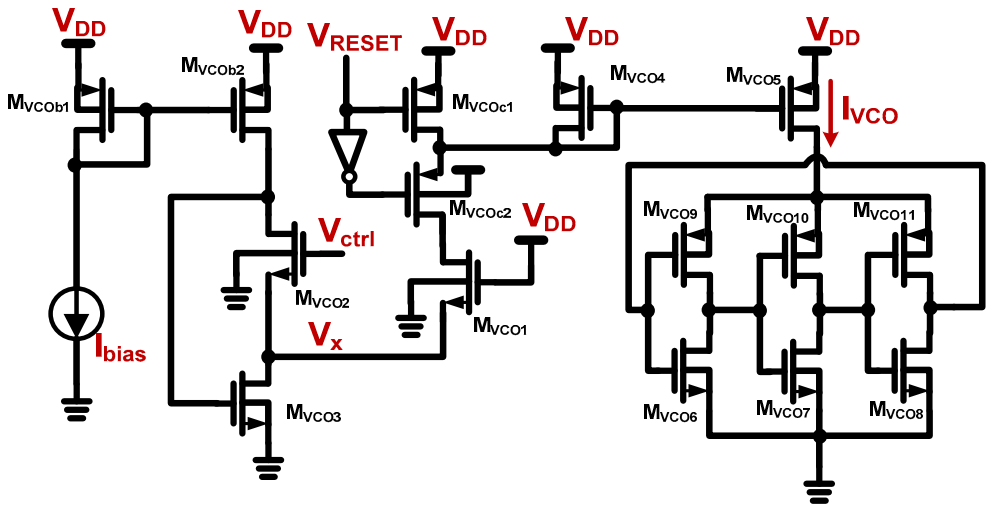
$$G_m = \beta_{MVCO1}(V_{DD} - V_{ctrl} + \sqrt{\frac{2I_{bias}}{\beta_{MVCO2}}}) \quad (3)$$

$$K_{VCO} = \frac{G_m}{2NC_{out}V_{sw}} \quad (4)$$

where the N is stage number of the inverter chain, Cout is the output capacitance of each stage in the inverter chain, and V_{sw} is the output signal swing of VCO. It can be seen from (3) and (4) that G_m and K_{VCO} are not affected by the variations of V_{th}.



(a)

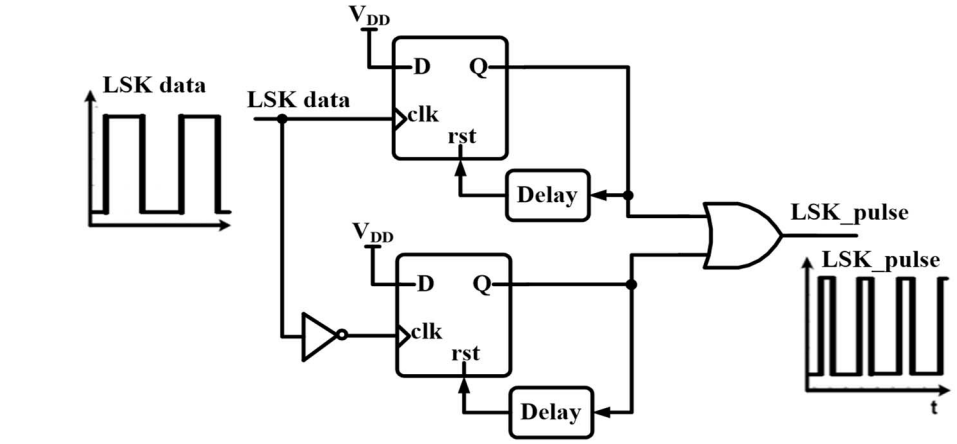


(b)

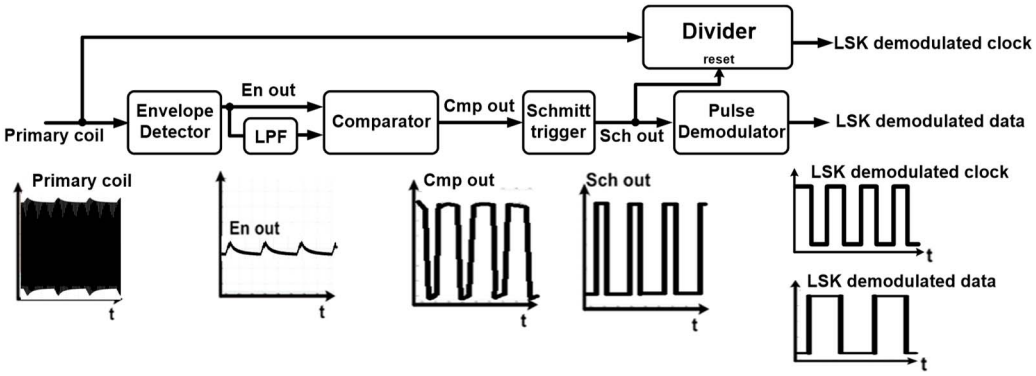
Fig. 11 (a) Block diagram of PLL-based edge-detection BPSK demodulator. (b) Schematic of the voltage-controlled oscillator in the proposed PLL-Based edge-detection BPSK Demodulator.

The LSK modulation is adopted to transmit the recorded ECoG signals and the seizure detection results as the uplink data to the external control system for monitoring purposes. The data is transmitted by changing the loading of secondary coil, which causes the amplitude change on the primary coil. Since the loading change of secondary coil by the LSK modulator decreases the wireless power transfer efficiency, the pulse modulation is

used in this design to maintain high wireless power conversion efficiency when the LSK data is transmitted.



(a)



(b)

Fig. 12 Block diagram of the (a) LSK modulator and (b) LSK demodulator.

Fig. 12(a) shows the block diagram of LSK modulator which consists of two D-Flip Flops and an OR gate. The LSK modulator sends a short pulse only when the LSK data changes. Fig. 12(b) shows the block diagram of LSK demodulator which consists of an envelope detector, a low pass filter (LPF), a comparator, a Schmitt trigger, and a pulse demodulator. The envelope of the signal on the primary coil is detected by the envelope detector. The comparator compares the output of envelope detector with its DC level extracted by the LPF to amplify the output of envelope detector. Then the pulse demodulator is used to demodulate the uplink data for the external control system. To synchronize the transmitted uplink data in receiver end at bit level, the divided-by-128 divider is used to

divide the primary coil signal at 13.56MHz and generate a clock at 106KHz for LSK demodulation. To eliminate the frequency drift due to the amplitude changes of primary coil signal caused by LSK data transmission, the reset signal of divider is connected to the output of Schmitt trigger to maintain LSK data synchronization.

4.3 Experimental Results

The closed-loop seizure control SoC and the chip of external control system were fabricated in 0.18-um CMOS technology with 1.8V/3.3V CMOS devices. The chip areas of the implanted SoC and the external chip are 20mm^2 and 3.38mm^2 (including the ESD pads), respectively, as shown in Fig. 13. Each circuit was tested separately, and the function of the whole system was verified in both electrical and animal tests.

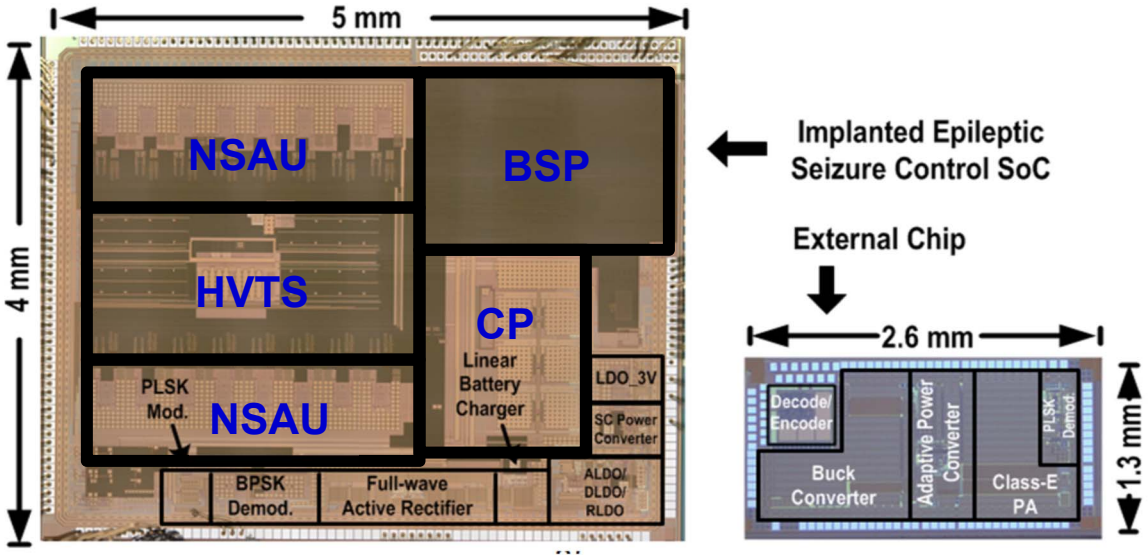


Fig. 13 Chip micrographs of the proposed closed-loop seizure control SoC and the external control system.

4.4.1 Electrical Test

The measured input-referred noise $V_{n,rms}$ of the fabricated AR-CSCCIA is shown in Fig. 14. The inputs of AR-CSCCIA are grounded while the output is analyzed by a dynamic

signal analyzer. The measured output noise is divided by the gain of AR-CSCCIA (45dB) to obtain the input-referred noise. With the chopper modulation, the input-referred noise of AR-CSCCIA is only 2.09 uVrms integrated in the bandwidth (BW) of 0.5Hz-117Hz when the SoC is wirelessly powered. The noise-efficiency factor NEF of the NSAU is 3.78. The measured spurious-free dynamic range (SFDR) of the fabricated NSAU is 50dB as shown in Fig. 15. The measured SNDR is 48.7dB and the effective number of bits (ENOB) of the SoC is 7.8 bit.

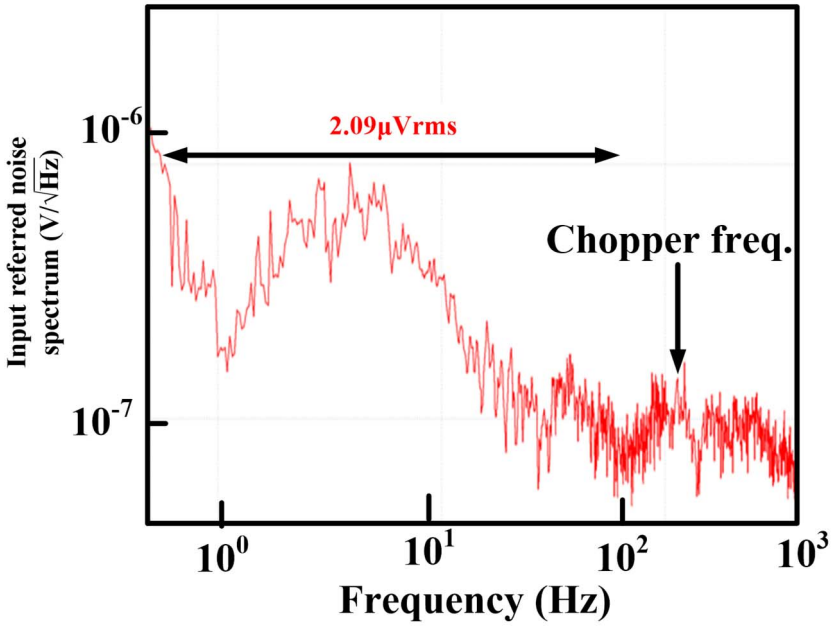


Fig. 14 The measured input-referred noise of the fabricated AR-CSCCIA.

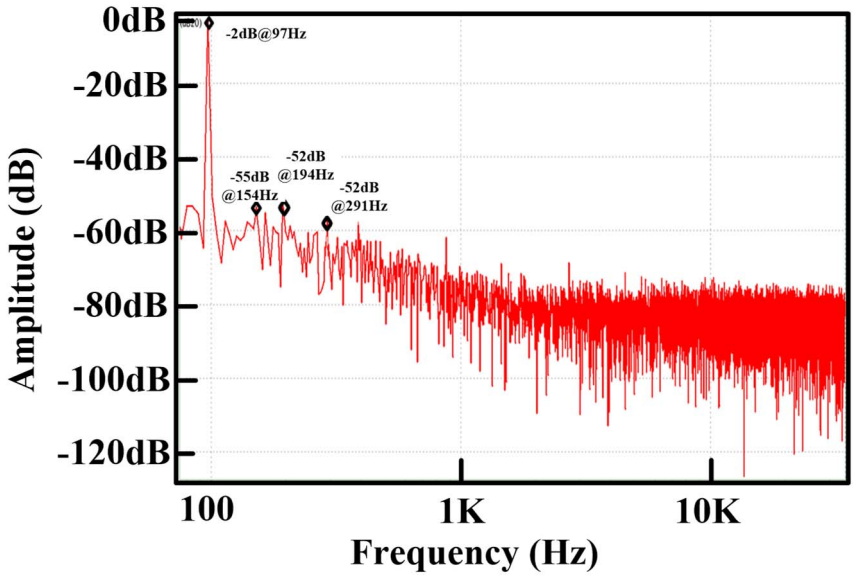


Fig. 15 The measured spectrum analysis of the fabricated NSAU.

Fig. 16 shows the measured biphasic stimulus current at 3mA and the corresponding measured adaptive power supply voltage with the measured "Adjust" signal of the fabricated HVTS as shown in Fig. 7 and 8. It can be seen from Fig. 16 that the adaptive power supply can be pumped and stepped up from 8V to 11.5V following the "Adjust" signal generated by the triode indicator. Since the voltage on the double-layer capacitor of the electrode is increased gradually during constant current stimulation, using the adaptive power supply can decrease the conduction loss of the high-voltage-tolerant stimulus driver and increase the power efficiency of HVTS to 54% from the original 37% with a fixed 4xVDD of 12V, both under the stimulus current of 3mA. The overshoot current is about 0.2 mA, which is within the safe stimulation range.

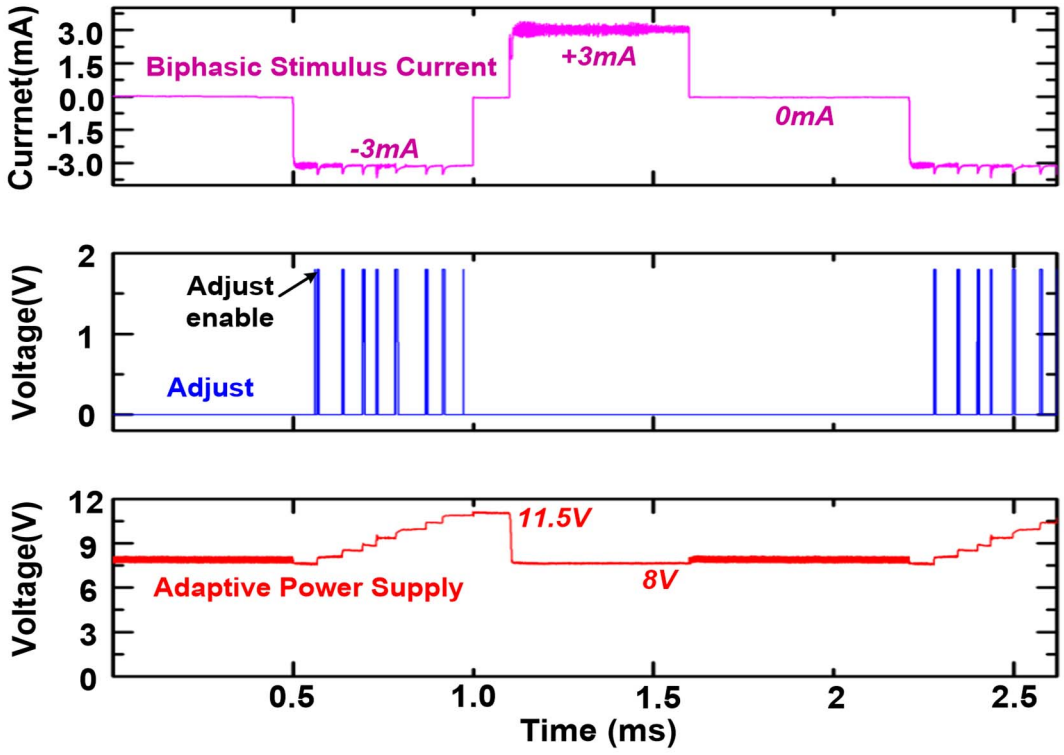


Fig. 16 Measurement results of the fabricated HVTS with adaptive supply voltage control.

Fig. 17 shows the measured secondary coil input waveforms, rectifier output voltages VDD3 and VDD2, and the output voltage AVDD of the fabricated 2X/3X active rectifier

and ALDO as shown in Fig. 9 and 10. It can be seen from Fig. 17 that 3V (VDD3) and 2V (VDD2) can be generated by the active rectifier whereas 1.8V (AVDD) can be generated by the ALDO to provide a stable supply voltage for the analog circuits of SoC. The measured power conversion efficiency of 2X/3X active rectifier is 80.8% and the measured ripples of VDD3, VDD2, and AVDD are 50.4mVpp, 40.2mVpp, and 39.2mVpp, respectively.

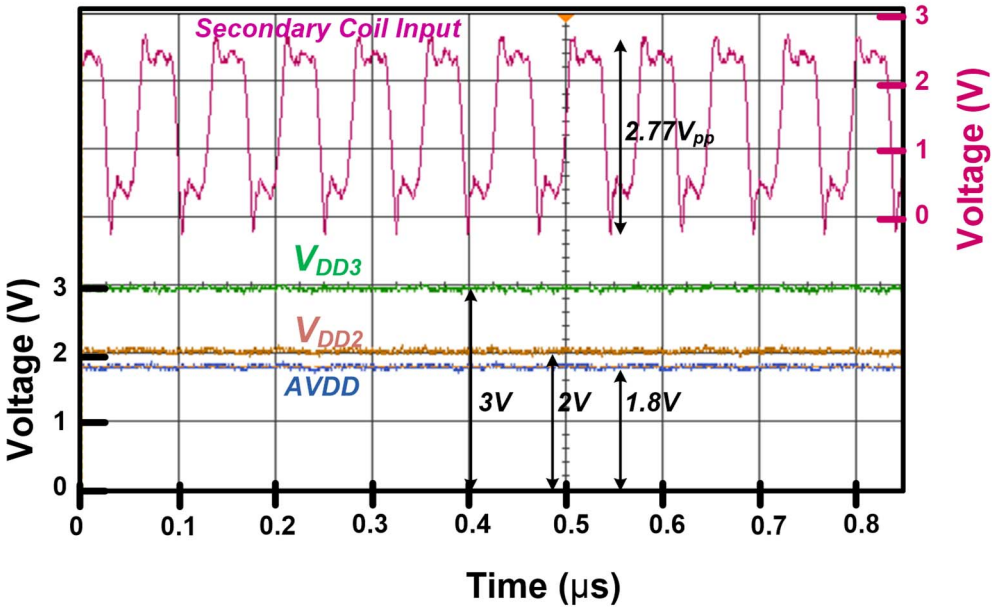


Fig. 17 Measurement results of the fabricated 2X/3X active rectifier and LDOs.

For the data transmission, the downlink data in BPSK form as demodulated by the proposed PLL-based edge-detection BPSK demodulator are shown in Fig. 18 where the generated 3V by the 2X/3X active rectifier is also shown. This verifies the capability of simultaneous downlink data and power transmission. The measured power conversion efficiency of 2X/3X active rectifier during BPSK data transmission is 76.7% at 1cm distance. When the input amplitude of the 2X/3X active rectifier is 2V, the measured bit error rate of the fabricated PLL-based edge-detection BPSK demodulator is 10^{-5} as shown in Fig. 19.

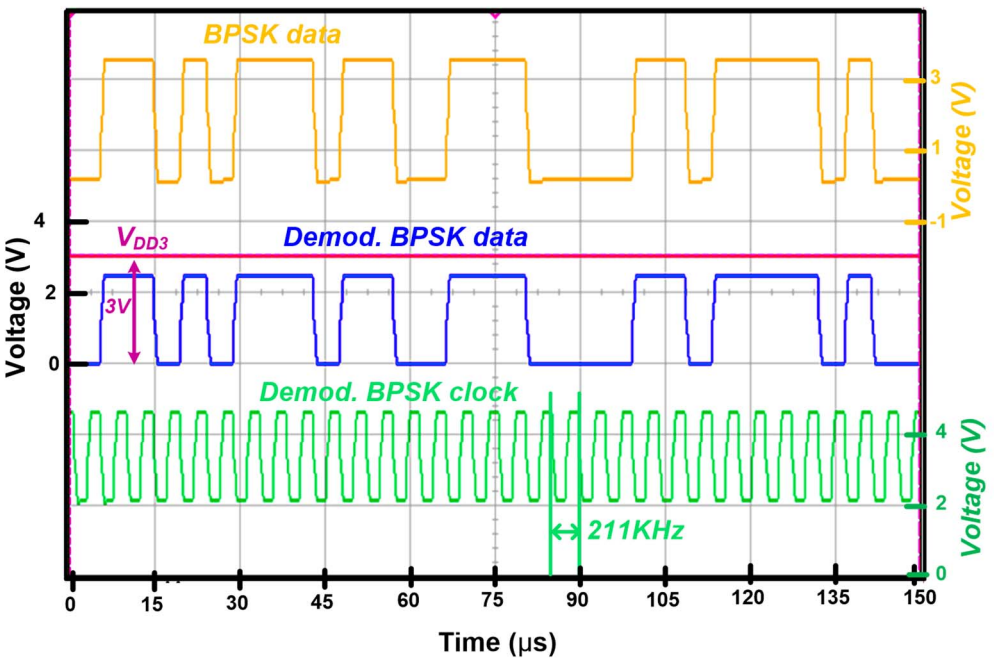


Fig. 18 Measurement results of the fabricated PLL-based edge-detection BPSK demodulator.

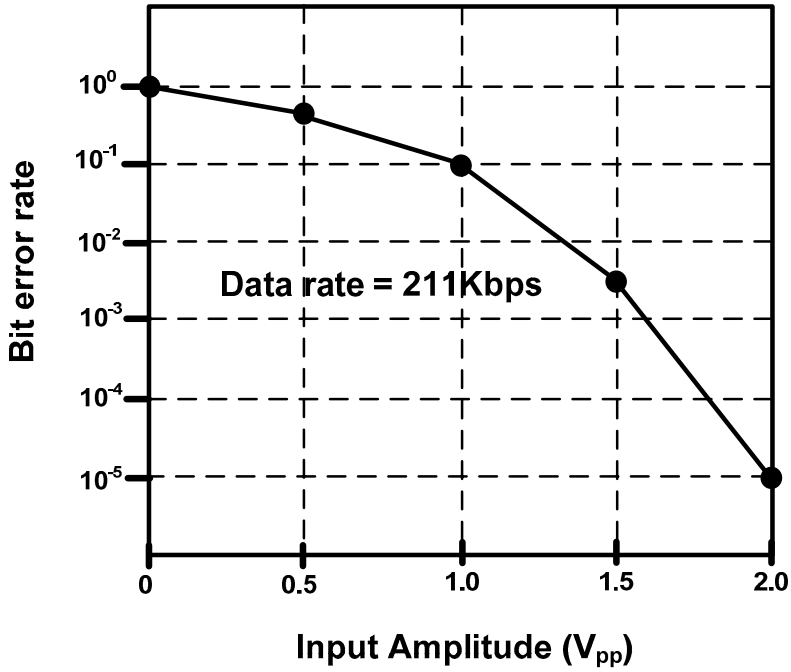


Fig. 19 The measured bit error rate of the fabricated PLL-based edge-detection BPSK demodulator.

The measured uplink data in LSK form as demodulated by the proposed LSK demodulator are shown in Fig. 20. The uplink data rate is 106Kbps and the measured bit

error rate is 10^{-4}. Since the neural signal in the uplink data is below 100Hz, the bit error rate of 10^{-4} under 106Kbps is acceptable according to [55]. When the LSK data change, the amplitude on the primary coil increases and the proposed LSK demodulator can demodulate the LSK data. The power conversion efficiency during LSK data transmission is 63.8%. The energy-per-bit of BPSK demodulator and LSK modulator are 1.027nJ/b and 0.14nJ/b with 211Kbps and 106Kbps, respectively.

The total power consumption of the proposed SoC is 3.12 mW in standby mode and 54mW in stimulation mode. The pie charts of power dissipation in these two modes are shown in Fig. 21.

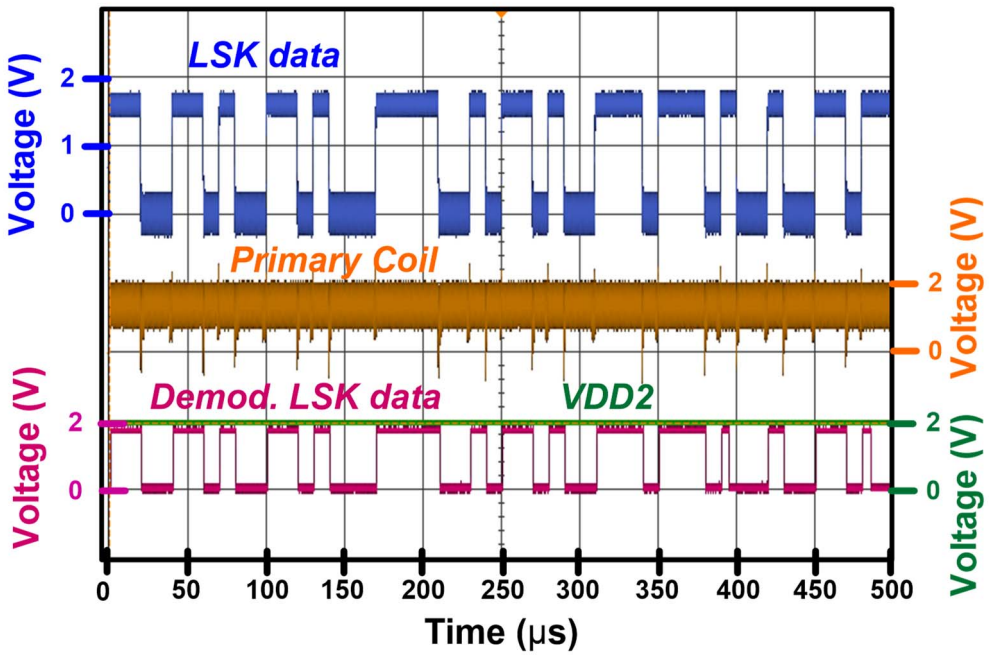
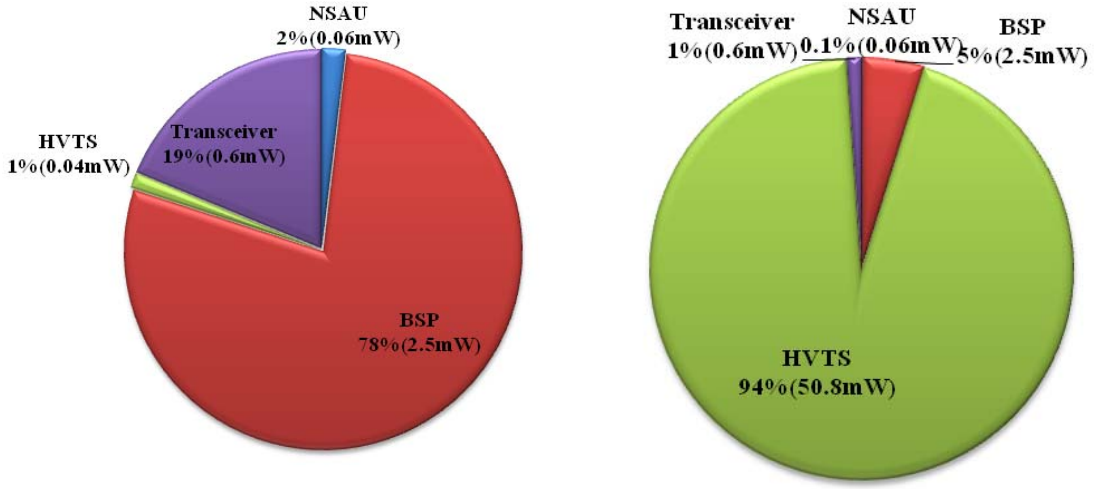


Fig. 20 Measurement results of demodulated data from the fabricated LSK demodulator and the voltage waveforms on the primary coil.



(a) (b)

Fig. 21 The measured power dissipation pie-chart of the seizure control SoC. (a) The seizure control SoC operated in standby mode. (b) The seizure control SoC operated in stimulation mode

The performance summary of the developed SoC is given in Table 1 where comparisons with that of [5]-[8] are also listed.

In the neural recording system [5]-[8], the low-frequency flicker noise is dominant. When the amplifier bandwidth is increased, the low-frequency noise has lower contribution to the total input-referred noise. Since the signal bandwidth of [5] is designed from 0.1Hz to 7KHz which is larger than that in this work, the NEF of [5] is lower. It can be seen from the comparison that the developed SoC achieves highest detection accuracy, highest programmable stimulation currents, and highest overall power conversion efficiency calculated from the input of primary coil to the output of 2X/3X active rectifier under the maximum loading currents of 3mA (2X) and 16mA (3X), while only one pair of coils is used for wireless power and bi-directional data telemetry.

Table 1 The performance summary of the developed closed-loop seizure control SoC

	JSSC'14 [5]	VLSI'16 [6]	JSSC'16 [7]	JSSC'17 [8]	This work
Process	0.18μm	0.18μm	0.13μm	0.13μm	0.18μm
# of channels	8	16	64	64	16
Input referred noise (μV_{rms}) (Bandwidth)	5.23 (0.1-7KHz)	5.9 (10-10KHz)	4.2 (1-5KHz)	1.13 (0.01-500Hz)	2.09 (0.59-117Hz)
NEF	1.77	2.94	6.9	2.86	3.78
Accuracy	92%	n.a	88-96%	88-96%	97.76%,
Sensitivity	n.a	100%	75%	75%	96%
Specificity	n.a	n.a	n.a	n.a	100%
Latency	0.8s	0.5s	n.a	n.a	0.76s
BSP Efficiency	77.91μJ/ (feature ext. + classification)	n.a	n.a	n.a	62.5μJ/ (feature ext. + classification)
Charge pump stage (PCE)	5 (38%)	No	No	No	3 (54%)
Stimulation current	30μA biphasic	<818uA biphasic	10-1000μA biphasic	10-1350μA biphasic	500-3000μA biphasic
Adaptive stimulation control	Yes	No	No	No	Yes
In-vivo object (stimulation current)	rat (30uA)	rat (560uA)	rat (150uA)	rat (150uA)	mini-pig (3mA)
Electrode model (Rs, Rf, Cdl)	(Rs=1-250KΩ, Rf=n.a, Cdl=4-200nF)	(Rs=1KΩ, Rf=n.a, Cdl=n.a)	(Rs=1KΩ, Rf=n.a, Cdl=n.a)	(Rs=1KΩ, Rf=n.a, Cdl=n.a)	(Rs=3KΩ, Rf=200KΩ, Cdl=400nF)
suitable object	rat	rat	rat	rat	human
Power dissipation	2.8mW (standby)	14.8uW (standby)	2.17mW (UWB) 5.8mW (FSK)	1.07mW (delay-based UWB) 5.44mW (VCO-based UWB)	3.12mW (standby) 54mW (stimulation)
Wireless transmission (carrier frequency)	Dual-band (13.56M, 400MHz)	No	Quad-band (1.5M, 916.4M, <1G, 3.1-10G)	Dual-band (1.5M, 3.1-10G)	Single-band (13.56MHz)
Downlink data rate (energy per bit)	4Mbps (0.07 nJ/b)	No	n.a	n.a	211Kbps (1.027 nJ/b)
Uplink data rate (energy per bit)	1Mbps (0.16 nJ/b)	No	1.2Mbps (3.08 nJ/b) 10Mbps (0.01 nJ/b) 10Mbps (2.22 pJ/b)	10Mbps (0.01 nJ/b) 46Mbps (0.08 pJ/b)	105Kbps (0.14 nJ/b)
Power transfer efficiency	~8.3% (Overall)	No	40% (overall)	n.a	48% (overall)

4.4.2 Animal Test

The function of the fabricated closed-loop seizure control SoC in 0.18μm CMOS technology was verified with the in-vivo animal tests of mini pigs. Fig. 22 shows the animal experimental setup where the mini pig was implanted with 16-channel planar electrodes on the cortical surface. The seizure onset of mini pigs was induced by injecting penicillin. The SoC was parameterized by a compact DAQ controller through an input pad. The recorded ECoG by the NSAU, the stimulation control signal by the BSP, and anodic and cathodic simulation current waveforms by the HVTS were connected to the oscilloscope through output pads. Fig. 23 shows the waveforms of recorded ECoG, stimulation control signal, and the generated stimulus currents. It can be seen that the seizure onset is detected and the stimulus current of 3mA is delivered to the electrode within 0.76s. After the stimulation, the seizures is suppressed and the measured ECoG is recovered to the normal state. The closed-loop function of the proposed closed-loop seizure control SoC is verified successfully.

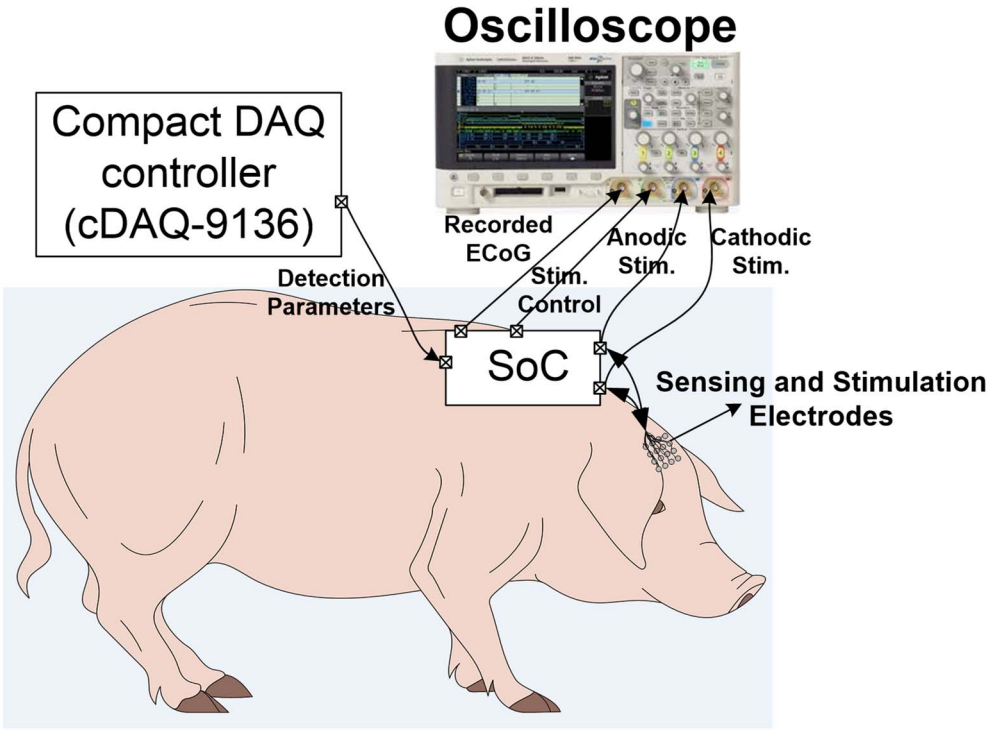


Fig. 22 Animal experimental setup.

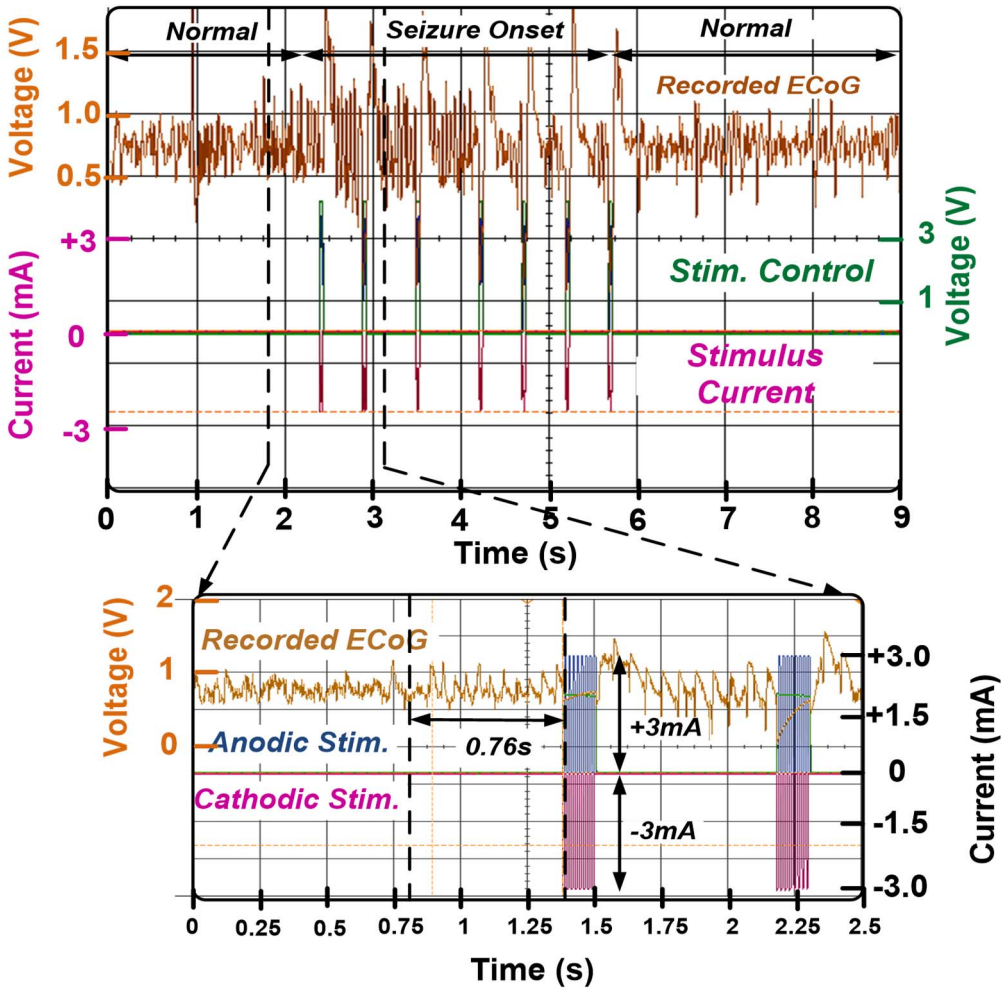


Fig. 23 Measurement results of animal experiment.

4.4.3 Human Clinical Trials

The fabricated SoC has been also verified by human clinical trial, the developed system has been certified by IEC 60601-1 and IEC 60601-1-2 for safety validation. Fig. 24 shows the screen of the developed system for medical applications, where the seizure events can be detected by the developed system, and the closed-loop stimulation is performed by the fabricated SoC. Fig. 25 shows the ECoG waveform recorded from epileptic patient without closed-loop stimulation, where the epileptic seizure duration is about 100s. Fig. 26 shows the ECoG waveform recorded from the same patient with closed-loop stimulation, where the seizure can be suppressed and the seizure duration is reduced to 20s. The clinical trials have been conducted on five patients under IRB regulation. With the closed-loop

stimulation, the average duration of seizure is reduced by 70%. The total number of seizures is 21 and the number of closed-loop stimulations is also 21, which means the seizure-event detection accuracy is 100%.

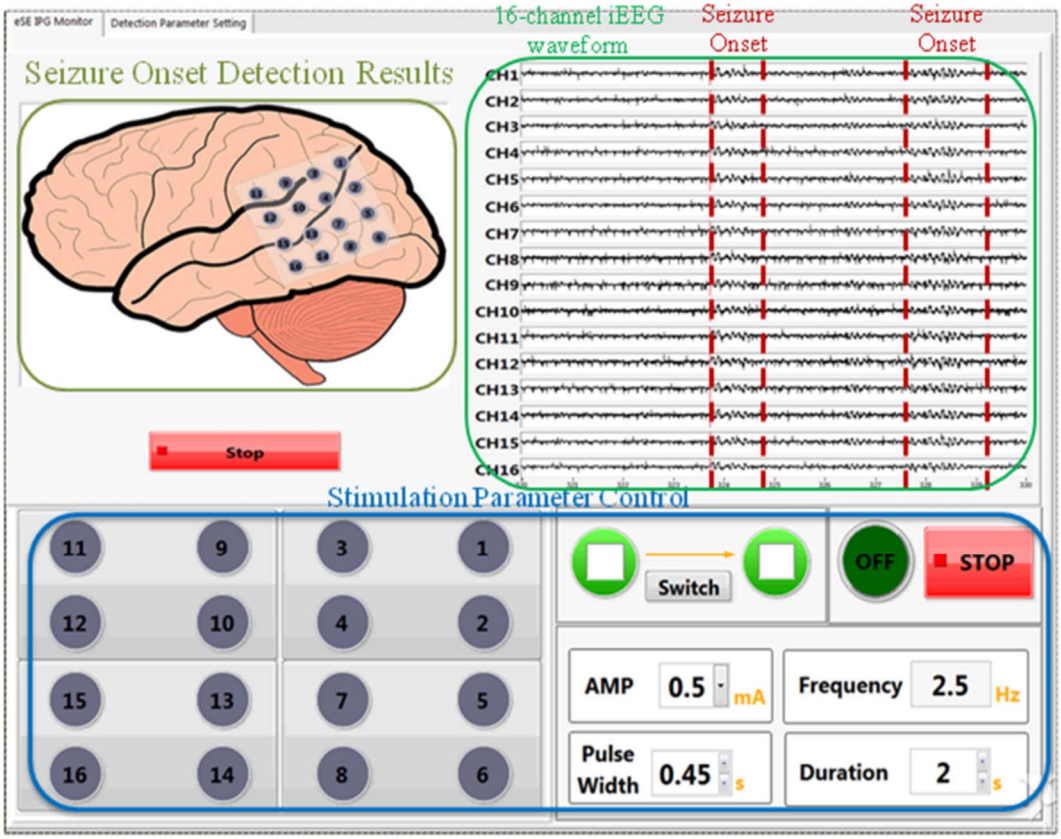


Fig. 24 Graphical user interface of the developed system.

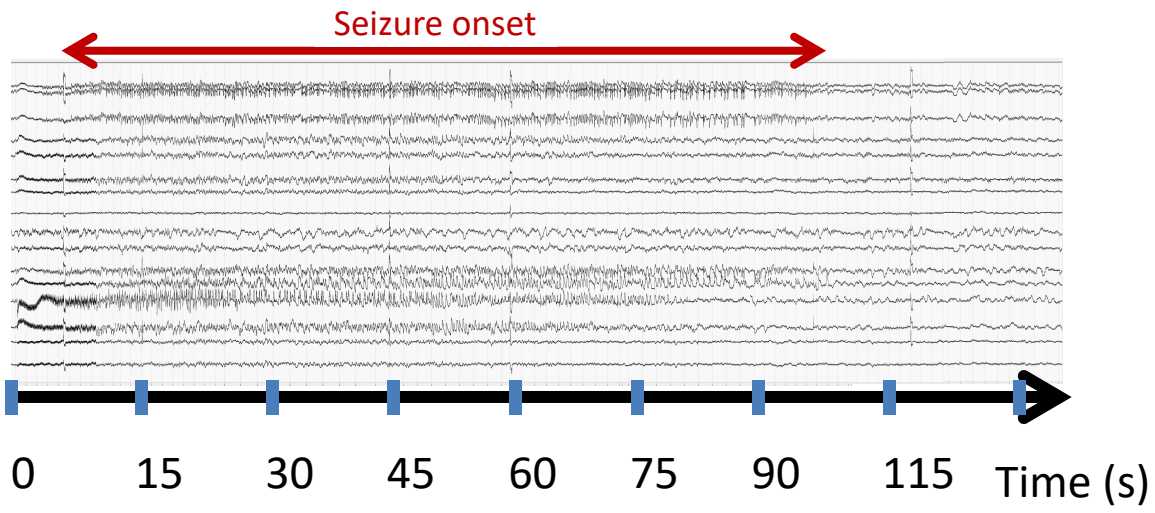


Fig. 25 ECoG waveform without closed-loop stimulation.

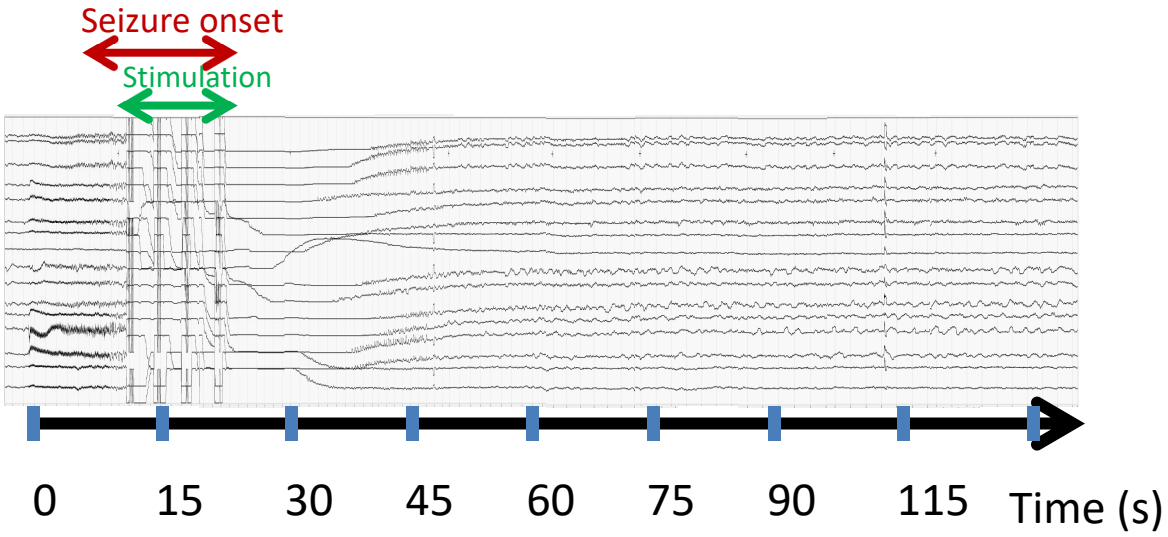


Fig. 26 ECoG waveform with closed-loop stimulation.

4.5 Summary

A 16-channel closed-loop neuromodulation SoC for human epileptic seizure control has been designed, fabricated, and verified. In the SoC, a 16-channel NSAU, a BSP, a 16-channel HVTS, and wireless power and bi-directional data telemetry are integrated together into a single silicon chip. Through in-vivo animal tests on mini pigs and the clinical trials on human, the closed-loop function of SoC has been successfully verified. The measured seizure detection latency is 0.76s with the accuracy of 97.8%. Up to 3mA biphasic current stimulation can be delivered through electrodes to suppress the epileptic seizures. The closed-loop neuromodulation SoC with seizure detection and biphasic current stimulation has been demonstrated to be a valuable solution to treat human epilepsy.

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