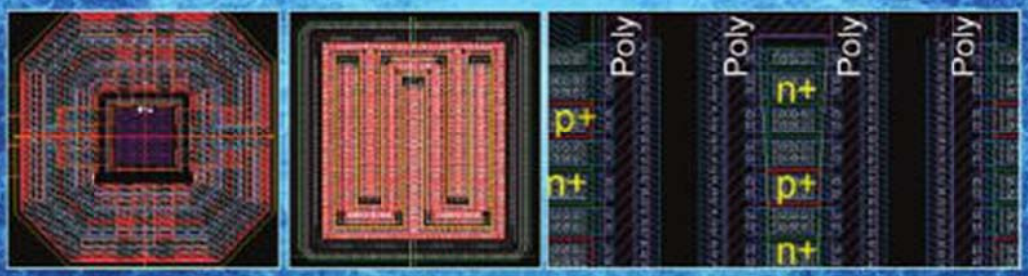
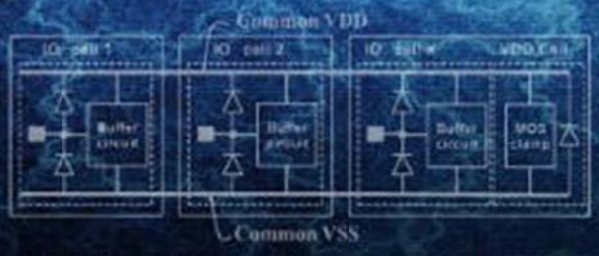
# Electrostatic Discharge Protection

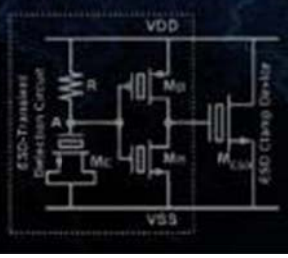
## Advances and Applications

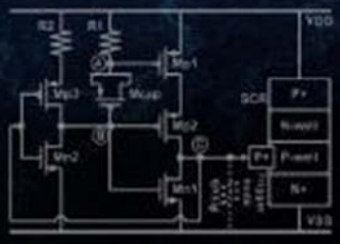
EDITED BY JUIN J. LIOU







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# 5 Design of Power-Rail ESD Clamp Circuits with Gate-Leakage Consideration in Nanoscale CMOS Technology

*Ming-Dou Ker and Chih-Ting Yeh*

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## 5.1 INTRODUCTION

Electrostatic discharge (ESD) phenomenon is a charge flow when two objects with different voltage potentials reach contact. Such ESD events can cause serious damage to the integrated circuit (IC) products, during assembly, testing, and manufacturing. To protect the IC products with the required ESD specifications, typically such as 2 kV in human body model (HBM) [1] and 200 V in machine model (MM) [2], the whole-chip ESD protection scheme formed with the power-rail ESD clamp circuit had been often used in the modern IC products [3]. As shown in Figure 5.1, the power-rail ESD clamp circuit is a vital element for ESD protection under different ESD stress modes. The ESD stress modes include $V_{dd}$-to-$V_{ss}$ (or $V_{ss}$-to-$V_{dd}$) ESD stress between the rails, as well as the positive-to-$V_{ss}$ (PS) mode, negative-to-$V_{ss}$ (NS) mode, positive-to-$V_{dd}$ (PD) mode, and negative-to-$V_{dd}$ (ND) mode, from input/output (I/O) to $V_{dd}$/$V_{ss}$. Therefore, the power-rail ESD clamp circuit must provide low-impedance discharging path under ESD events but keep in off-state with standby leakage current as low as possible under normal circuit operation conditions.

In advanced nanoscale CMOS technology, there are two commonly used processes provided from foundry for some specified purposes. They are low-power (LP) and general-purpose (GP) processes. LP process is used for LP product with a 1.2 V core design and 2.5 V or 3.3 V I/O option. Because LP process is developed for LP product, there is basically no serious gate leakage issue. Therefore, a large-sized MOSFET drawn in the layout style of big field-effect transistor (BigFET) is usually adopted as the ESD clamp device in the power-rail ESD clamp circuit.

GP process provides higher performance transistors for high-speed or high-frequency applications with 1 V core design and 2.5 V I/O option. In GP process, the thickness of gate-oxide layer is thinner than that in LP process (or with a lower threshold voltage, $V_{th}$) to gain higher driving current. However, the thinner gate oxide impacts

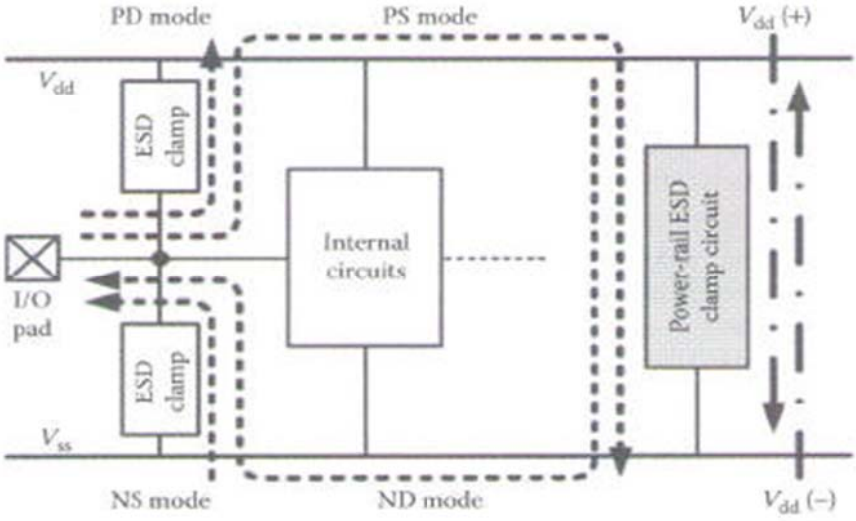
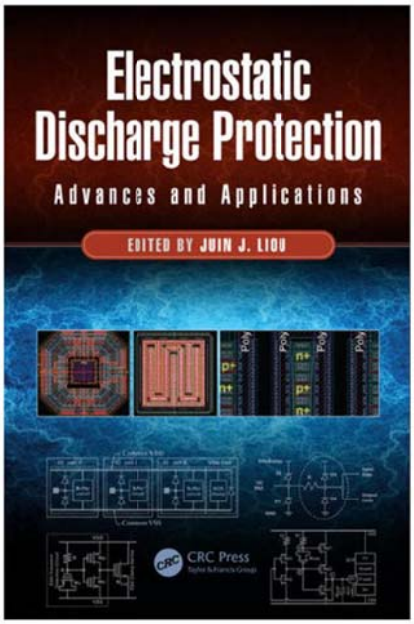



**FIGURE 5.1** Typical whole-chip ESD protection scheme with the power-rail ESD clamp circuit under different ESD stress conditions.

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# Electrostatic Discharge Protection: Advances and Applications

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