A NEW CHARGE PUMP CIRCUIT DEALING WITH GATE-OXIDE RELIABILITY ISSUE IN LOW-VOLTAGE PROCESSES

Ming-Dou Ker, Shih-Lun Chen, and Chia-Sheng Tsai
Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Taiwan

ABSTRACT

Charge Pump Circuits have been widely used in DRAM, EEPROM, flash memories, and in some low-voltage designs. In this paper, a new charge pump circuit is proposed. The charge transfer switches of the new proposed circuit can be turned on and turned off completely, so its pumping gain is much higher than the traditional designs. Besides, there is no gate-oxide reliability problem in the proposed charge pump circuit. The test chips have been implemented in a 3.3 V 0.35 μm CMOS process. The measured results show that the proposed charge pump circuit has better performance than that of prior arts. The proposed circuit can be used in low-voltage process because of its high pumping gain and no overstress across the gate oxide of the devices.

1. INTRODUCTION

Charge pump circuits can generate dc voltages which are higher than the power supply voltage or lower than the ground voltage. Charge pump circuits are usually applied to the nonvolatile memories, such as EEPROM and flash memories, to write or to erase the floating-gate devices [1]. Besides, charge pump circuits can also be used in some low-voltage designs to improve performance [2]. Most of charge pump circuits are based on the circuit proposed by Dickson [3].

Fig. 1 shows the traditional 4-stages Dickson charge pump circuit that uses diode-connected MOSFET to transfer the charges from this stage to next stage. As shown in Fig. 1, the charges are pushed from the power supply to the Cout stage-by-stage. Therefore, the output voltage of the charge pump circuit can be pumped high, expectedly. The voltage fluctuation of each pumping node can be expressed as

$$\Delta V = V_{clk} \cdot \frac{C_{pump}}{C_{pump} + C_{par}} - \frac{I_o}{f \cdot \left(C_{pump} + C_{par}\right)} \quad (1)$$

where *Vclk* is the amplitude of the clock signals, *Cpump* is the pumping capacitor, *Cpar* is the parasitic capacitance at each pumping node, *Io* is output current, and *f* is the clock frequency. If the *Cpar* and *Io* are small enough, they can be neglected. Because *Vclk* is usually the same as the nominal power supply voltage VDD, the voltage fluctuation of each pumping node can be simply expressed as

$$\Delta V \approx V_{clk} = \mathrm{VDD}. \quad (2)$$

However, the voltage difference between drain terminal and source terminal of the diode-connected MOSFET is the threshold voltage of the MOSFET. Thus, the output voltage of the 4-stages Dickson charge pump circuit is

$$V_{out} = \mathrm{VDD} + \sum_{i=1}^{4} (\mathrm{VDD} - V_{t(Mi)}) \quad (3)$$

where $Vt_{(Mi)}$ denotes the threshold voltage of the diode-connected MOSFET Mi. The threshold voltage $Vt_{(Mi)}$ becomes larger due to body effect as the voltage of each pumping node is pumped higher. Therefore, the pumping efficiency of the traditional Dickson charge pump circuit is low.

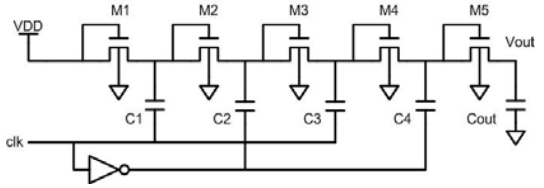


Fig. 1. The traditional Dickson charge pump circuit with 4-stages.

Several charge pump circuits based on Dickson charge pump circuit were proposed to enhance the pumping gain [4]-[8]. Using floating-well technique to eliminate the body effect was proposed in [5]. However, it may generate substrate current in the floating devices to cause the latch-up problem. Using auxiliary MOSFETs to control the body terminals may also generate the substrate current [6]. Four-phase charge pump circuits were proposed, but they must have complex clock generators [7]. Wu and Chang proposed the charge pump circuit that use charge transfer switches (CTS's) to transfer charges without the limitation of threshold voltage [8]. The CTS's can be turned on or turned off properly by the control circuits. Thus, the output voltage of this charge pump circuit is about 5×VDD. The pumping gain is enhanced by the CTS's. However, the output stage of Wu and Chang's charge pump circuit is also a diode-connected MOSFET that also has the body effect problem. In addition, the maximum voltage difference of

each stage is 2×VDD, so that this circuit has the serious voltage overstress across the gate oxide of MOSFET devices. Thus, not only to enhance the pumping gain but also to avoid overstress on the gate oxide must be considered in design of charge pump circuits in deep-submicron CMOS process. Especially, when the CMOS processes migrate to the nanoscale, the operating voltage across the gate oxide of the MOSFET devices is critically limited to avoid gate-oxide reliability issue [9]. In this paper, a new charge pump circuit that has high pumping gain and can operate without any gate-oxide overstress is presented.

2. NEW PROPOSED CHARGE PUMP CIRCUIT

Fig. 2 shows the scheme and the waveforms of the new proposed charge pump circuit with 4-stages. Clock signals φ1 and φ2 are out-of-phase and their amplitudes are as high as the power supply voltage VDD. As shown in Fig. 2, there are two charge transfer branches named branch A and branch B in the proposed charge pump circuit. The difference between branches A and B is that the clock signals are out-of-phase. If the clock signals of the first and third pumping stage in branch A are φ1, those in branch B are φ2. Similarly, if the clock signals of the second and forth pumping stage in branch A are φ2, those in branch B are φ1. Thus, branches A and B can be seen as two independent charge pump circuits and their output nodes are connected together. Because the clock signals of branch A and those of branch B are out-of-phase, the waveforms of nodes 1-4 and those of nodes 5-8 are also out-of-phase. Thus, branches A and B pump the output voltage high alternately. The detailed operation principle of the proposed charge pump circuit is described bellow.

2.1. For the first stage

As illustrated in Fig. 2(b), clock signal φ1 is LOW, and clock signal φ2 is HIGH at time interval T1. At this moment, the voltage difference between node 1 and node 5 (V_{15}) is –VDD for nominal operation. Thus, MOSFET switch Mna1 is turned on to push the charges from power supply to node 1, and switch Mnb1 is turned off to cut off the path from node 5 back to power supply. Similarly, V_{15} is VDD for ideal operation at time interval T2. Switch Mna1 is turned off to cut off the path from node 1 back to power supply, and switch Mnb1 is turned on to push the charges from power supply to node 5.

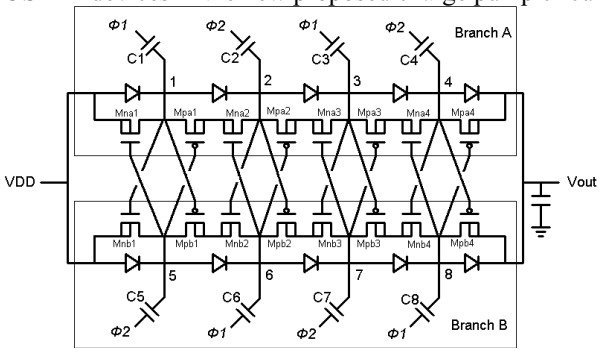
2.2. For the other pumping stages

Consider the second stage for example. Clock signal φ1 is LOW and clock signal φ2 is HIGH at time interval T1. At this time, V_{15} and V_{26} (voltage difference between node 2 and node 6) are –VDD and VDD for nominal operation, respectively. Therefore, MOSFET switches Mpa1 and Mna2 are turned on to push the charges from node1 to node 2, and MOSFET switches Mpb1 and Mnb2 are turned off to cut off the path from node 6 back to node 5. Similarly, V_{15} and V_{26} are VDD and –VDD at time interval T2, respectively. MOSFET switches Mpa1 and Mna2 are turned off in order to cut off the path from node 2 back to node 1, and switches Mpb1 and Mnb2 are turned on to push the charges from node 5 to node 6.

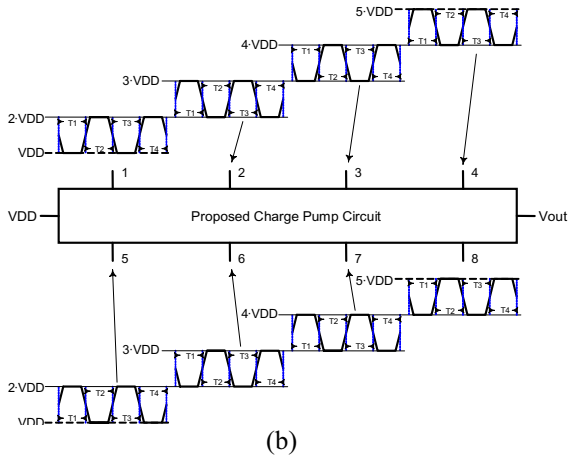
2.3. For the output stage

Clock signal φ1 is LOW and clock signal φ2 is HIGH at time interval T1. At this time, V_{48} (voltage difference between node 4 and node 8) is VDD for nominal operation. Therefore, MOSFET switch Mpa4 is turned on to push the charges from node 4 to the output node, and Mpb4 is turned off to cut off the path from the output node back to node 8. On the other hand, V_{48} is –VDD at time interval T2. Switch Mpa4 is turned off to cut off the path from the output node back to node 4, and switch Mpb4 is turned on to push the charges from node 8 to the output node.

As shown in Fig. 2, all gate-source voltage (Vgs) and gate-drain voltage (Vgd) of MOSFETs in the proposed charge pump circuit will not exceed in VDD. Although the gate-bulk voltage (Vgb) of MOSFET can exceed in VDD, it still has somewhat reliability concern. If the process provides the triple-well technology, the bulk terminal of MOSFET can be connected to source terminal to avoid this problem. Thus, there is no overstress on the gate oxide of MOSFET devices in the new proposed charge pump circuit.



(a)



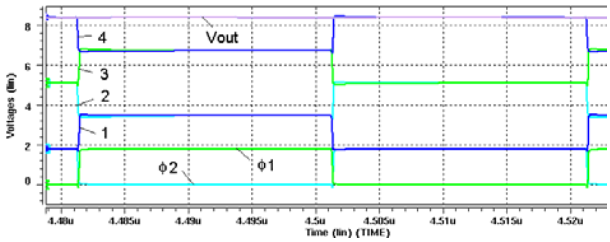
(b)

Fig. 2. (a) Scheme and (b) voltage waveforms of the new proposed charge pump circuit with 4-stages.

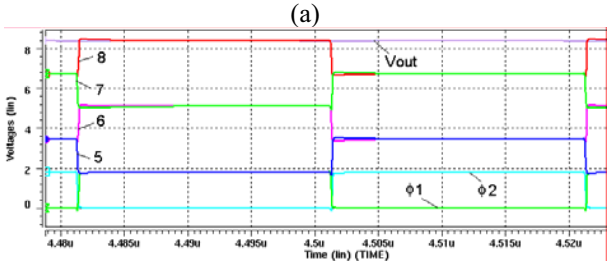
3. EXPERIMENTAL RESULTS

3.1. Simulation

A 1.8 V 0.18 μm SPICE model is used to simulate these charge pump circuits. Fig. 3 shows the simulated waveforms of the 4-stages proposed charge pump circuit with 5 μA output current. The expected waveforms shown in Fig. 2(b) are similar to the simulated waveforms shown in Fig. 3. Because of the parasitic capacitance and the output current, the simulated output voltage (Vout) of the proposed charge pump circuit is 8.39 V, not 9 V (1.8×5).



(a)



(b)

Fig. 3. Simulated waveforms of the new proposed charge pump circuit with 4-stages. (a) nodes 1-4 and (b) nodes 5-8. (VDD=1.8 V)

Fig. 4 compares the Dickson charge pump circuits, Wu and Chang's charge pump circuit, and the new proposed charge pump circuit. As all pumping capacitors are 1 pF, the proposed charge pump circuit has better performance with different output currents. Especially, at high output current, the proposed charge pump has much better performance than others. The proposed charge pump circuit has two branches to pump the charges so that the degradation of output voltage is small as the output current is large.

Actually, pumping capacitors take a great part in area of a charge pump circuit. For fair comparison, these charge pump circuits are compared again after equaling the total pumping capacitors. Thus, the pumping capacitors in Wu and Chang's charge pump circuit and Dickson charge pump circuit are replaced with 1 pF × 8/5 = 1.6 pF and 1 pF × 8/4 = 2 pF. As shown in Fig. 4, the output voltages of Wu and Chang's charge pump circuit and Dickson charge pump circuit with the higher pumping capacitors are less sensitive to the output current loading. Even in this case, the proposed charge pump circuit pumps the output voltage to the highest level. The output stage of the prior design is just a diode that has turn-on voltage Vt, but that of the proposed circuit is a MOSFET switch which can be fully turned on.

Branches A and B of the proposed charge pump circuit pump circuit pump the output node alternately, but Wu and Chang's charge pump circuit and Dickson charge pump circuit pump charges to output node per clock cycle. Fig. 5 shows the output waveforms of these charge pump circuits those provide 20 μA output current. As shown in Fig. 5, the output voltage ripple of the proposed charge pump circuit is smaller than those of Wu and Chang's charge pump circuit and Dickson charge pump circuit.

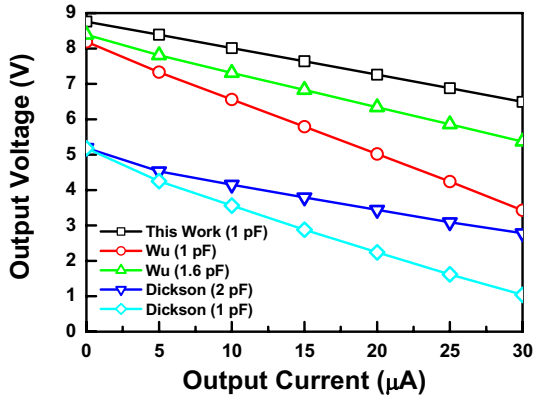


Fig. 4. Output voltage of the new proposed charge pump circuit with 4-stages under different output current. (VDD=1.8 V)

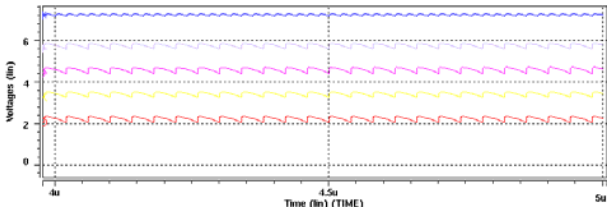


Fig. 5. Simulated output waveforms of the new proposed charge pump circuit with 4-stages. (VDD=1.8 V)

3.2. Silicon Verification

Two test chips have been implemented in a 3.3 V 0.35 μm CMOS process. The one photograph of these test chips are shown in Fig. 6. These two test chips include the 4-stages proposed charge pump circuit with 2 pF pumping capacitors, the 2-stages proposed charge pump circuit with 2 pF pumping capacitors, the 4-stages Wu and Chang's charge pump circuit with 2 pF pumping capacitors, the 4-stages Wu and Chang's charge pump circuit with 3.2 pF pumping capacitors, the 4-stages Dickson charge pump circuit with 2 pF pumping capacitors, the 4-stages Dickson charge pump circuit with 2 pF pumping capacitors, the 4-stages proposed charge pump circuit with 4 pF pumping capacitors, and the 3-stages proposed charge pump with 2 pF pumping capacitors. Fig. 7 shows the measured output voltages under different output currents. It shows that the proposed charge pump circuit has better performance than that of prior arts. As the output current is too large, all of these charge pump circuits can not pump voltage high. Fig. 8 compares the measured output voltage of the proposed

charge pump circuit that has 2-stages, 3-stages, and 4-stages, respectively. Similarly, as the output currents of the proposed circuits are larger than 30 μA, the proposed circuits (2-stages, 3-stage, and 4-stages) can not pump output voltage high, as shown in Fig. 8. To generate a higher output current, the pumping capacitor and the MOSFET device dimension should be enlarged.

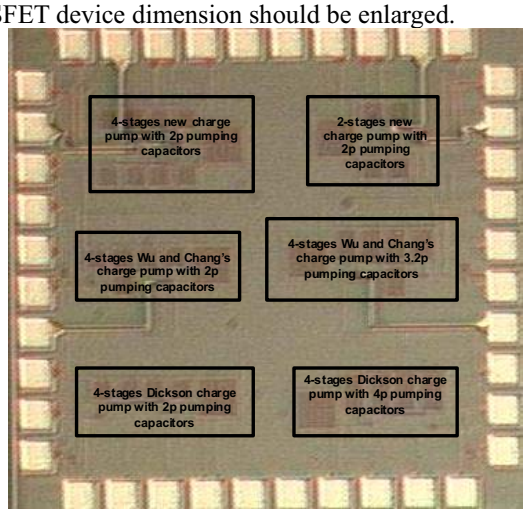


Fig. 6. Photograph of test chip 1.

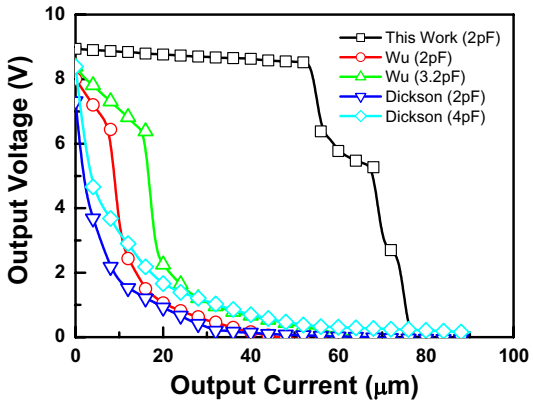


Fig. 7. Comparison on the measured output voltages of the different charge pump circuits with 4-stages under different output currents. (VDD=3.3 V)

4. CONCLUSION

A new charge pump circuit is proposed in this paper. Because the charge transfer switches of proposed circuit can be fully turned on and turned off and the output stage of proposed charge pump circuit don't have the threshold drop problem, its pumping gain is higher than that of the prior arts. The devices in the proposed charge pump circuit have no gate-oxide reliability problem. For comparison, two test chips have been implemented in a 3.3 V 0.35 μm CMOS process. The measured results show that the proposed charge pump circuit has better performance than that of prior arts. The proposed circuit can be used in low-voltage process due to its high pumping gain and no overstress across the gate oxide of MOSFET devices.

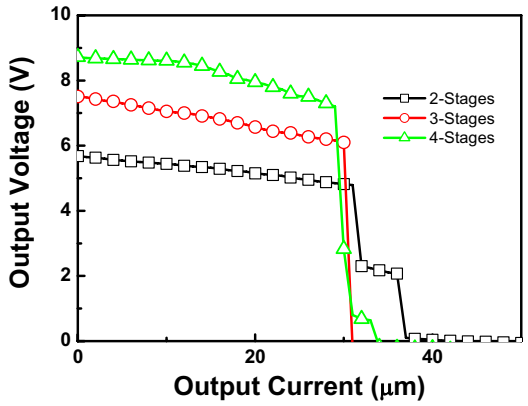


Fig. 8. Measured output voltages of the proposed charge pump circuit with different stages. (VDD=2.5 V)

5. REFERENCES

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