A NEW SCHMITT TRIGGER CIRCUIT IN A 0.13 μm 1/2.5 V CMOS PROCESS TO RECEIVE 3.3 V INPUT SIGNALS

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ABSTRACT

A new Schmitt trigger circuit, which consists of low-voltage devices, can receive the high-voltage signal without gate-oxide reliability problem, is proposed. The new proposed circuit, which can operate in a 3.3 V signal environment without suffering high-voltage gate-oxide stress, has been fabricated in a 0.13 μm 1/2.5 V CMOS process. The experimental results show that the measured transition threshold voltages of the new proposed Schmitt trigger circuit are about 1 V and 2.5 V, respectively. The proposed Schmitt trigger circuit is suitable for mixed-voltage I/O interfaces circuit to receive the input signals and reject the input noise.

1. INTRODUCTION

As the semiconductor process is scaled down, the thickness of gate-oxide becomes thinner in order to decrease the core power supply voltage (VDD) [1]. However, the board voltage (VCC) is still kept the same (3.3 V or 5 V), such as PCI-X interface. Therefore, the high-voltage stress across the thinner gate oxide becomes more serious in deep submicron (DSM) processes [2]. The I/O circuit must be designed carefully to avoid the high-voltage gate-oxide stress [3]-[5]. Schmitt trigger circuit has been widely used in the input buffers to increase noise immunity. Fig. 1 shows the conventional input buffer, which consists of a Schmitt trigger and a level converter. As shown in Fig. 1, the Schmitt trigger circuit receives the input signal from the I/O pad and rejects the input noise. Then, the level converter can convert the signal swing from VCC to VDD. The circuit and the transfer curve of the conventional Schmitt trigger circuit are shown in Fig. 2. Transistors P1, P2, P3, N1, N2, and N3 in Fig. 2(a) are the I/O (high-voltage (VDDQ)) devices. If VCC is equal to VDDQ, the gate-drain and gate-source voltages of transistors P1, P2, P3, N1, N2, and N3 in Fig. 2(a) will not exceed VDDQ. Therefore, the conventional Schmitt trigger circuit can operate without high-voltage gate-oxide stress. As shown in Fig. 2(b), the conventional Schmitt trigger circuit with different high-to-low and low-to-high transition threshold voltages has better noise immunity than the inverter. As input signal IN goes up to VCC from GND, the threshold voltage of the conventional Schmitt trigger circuit is V_H. In other words, output signal OUT is pulled low as signal IN exceeds V_H. Similarly, as input signal IN goes down to GND from VCC, the threshold voltage of the conventional Schmitt trigger circuit is V_L. In other words, output signal OUT is pulled up as signal IN is lower than V_L. Hence, the noise immunity of the conventional Schmitt trigger circuit is better than that of inverter.

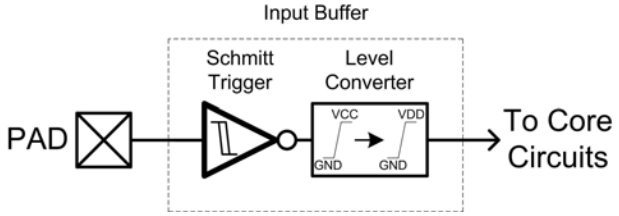

Fig. 1. The conventional input buffer.

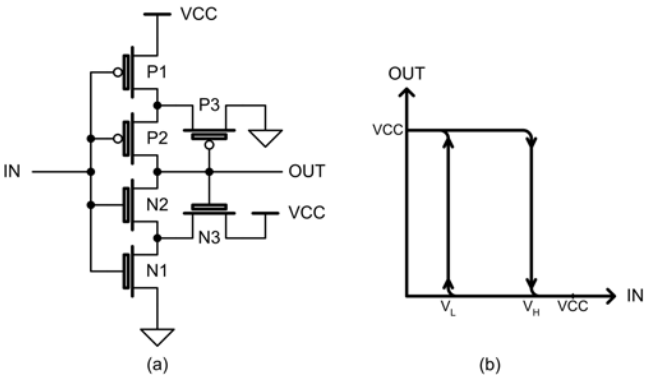

Fig. 2. (a) Circuit and (b) transfer curve of the conventional Schmitt trigger circuit.

Several modified Schmitt trigger circuits had been reported [6]-[9]. Fig. 3(a) shows the Schmitt trigger circuit reported in [6]. The extra bias voltage VB and the extra transistors P4 and N4 are used to control the two threshold voltages V_L and V_H. In reference [7], a multi-layers Schmitt trigger circuit was reported to increase the voltage difference between the two threshold voltages V_H and V_L.

The two layers Schmitt trigger circuit is shown in Fig. 3(b). However, as the power supply voltage is scaled down, the multi-layers Schmitt trigger circuit can not operate correctly. In reference [8], a low power Schmitt trigger circuit was proposed. An alternative circuit, which has the hysteresis characteristic like a conventional Schmitt trigger, was reported in [9].

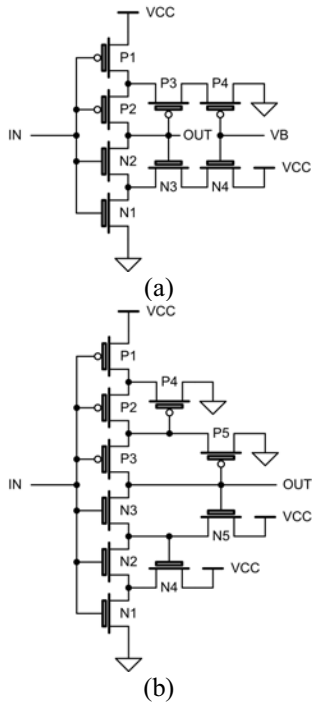

Fig. 3. (a) Schmitt trigger with controllable hysteresis and (b) two layers Schmitt trigger.

However, the aforementioned Schmitt trigger circuits have high-voltage gate-oxide stress problem if VCC is higher than VDDQ. For example, if VCC is 3.3 V and VDDQ is 2.5 V, the gate-source voltage and gate-drain voltage of transistors P1, P2, P3, N1, N2, and N3 in Fig. 2(a) will be larger than 2.5 V. Thus, all transistors in Fig. 2(a) have the high-voltage gate-oxide stress problem. Similarly, the other Schmitt triggers [6]-[9] also have the gate-oxide reliability problem. In this paper, a new Schmitt trigger circuit with low-voltage devices is proposed to receive the high-voltage input signal. The proposed circuit is implemented in a 0.13 μm 1/2.5 V CMOS process and operates in 3.3 V signal environment.

2. NEW PROPOSED SCHMITT TRIGGER

The new proposed Schmitt trigger circuit is shown in Fig. 4. All devices of the proposed Schmitt trigger circuit in Fig. 4 are the I/O (VDDQ) devices. In a 0.13 μm 1/2.5 V CMOS process, VDDQ is 2.5 V and VDD is 1 V. Therefore, the voltage across the gate oxide of the I/O device can not exceed 2.5 V. Because the drains of transistors P3 and N3 in Fig. 4 are connected to 1 V (VDD), the gate-drain voltages of transistors P3 and N3 will not exceeds 2.5 V. The maximum gate-drain voltages of transistors P3 and N3 are about 2.3 V (3.3−1=2.3). Because the gates of transistors P2 and N2 are connected to 1 V (VDD), the gate-drain voltages and gate-source voltages of transistors P2 and N2 will not exceeds 2.5 V. The maximum gate-drain voltages of transistors P2 and N2 are also about 2.3 V (3.3−1=2.3). If the gate voltage of transistor P1 (node A) is larger than 0.8 V (3.3−2.5=0.8) and the gate voltage of transistor N1 (node B) is smaller than 2.5 V, transistors P1 and N1 don't have the high-voltage gate-oxide stress problem. Thus, transistors P4, P5, P6, and P7 prevent the gate voltage of transistor P1 under 0.8 V, whereas transistors N4, N5, N6, and N7 prevent the gate voltage of transistor N1 over 2.5 V.

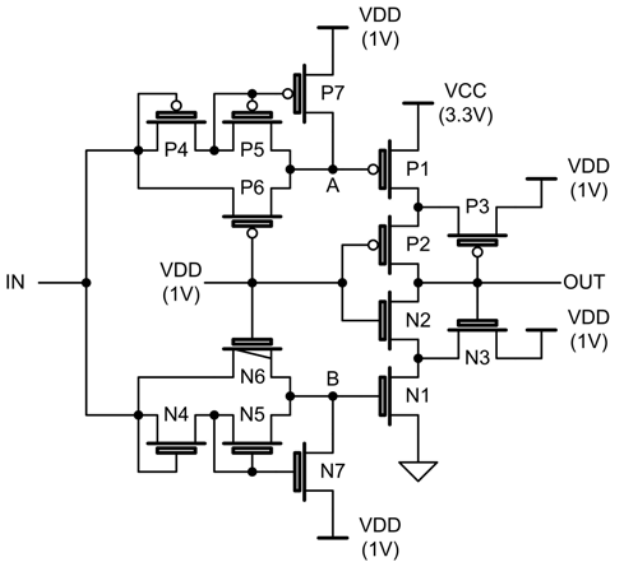

Fig. 4. The new proposed Schmitt trigger circuit.

When signal IN stays at 3.3 V (VCC), node A is also kept at 3.3 V because transistor P6 is turned on. When signal IN goes to 0 V, node A is kept at 2·|Vtp| because transistors P4 and P5 are in diode-connected structure. In the 0.13 μm 1/2.5 V CMOS process, |Vtp| is about 0.6 V. Therefore, the minimum gate voltage of transistor P1 (node A) is about 1.2 V. However, the diode-connected transistors P5 and P6 may make node A to 0 V as signal IN stays at 0 V for a long time, because of the subthreshold current of transistors P5 and P6. An extra transistor P7 is added to avoid node A over 1 V induced by the subthreshold current of transistors P5 and P6. As the node A is under 1 V, transistor P7 will be turned on to keep the voltage at 1 V.

When signal IN stays at 0 V, node B is also kept at 0 V because transistor N6 is turned on. When signal IN goes to 3.3 V, node B is kept at 3.3−2·|Vtn|, because transistors N4 and N5 are in diode-connected structre. In the 0.13 μm 1/2.5 V CMOS process, |Vtn| is about 0.5 V. Therefore, the maximum gate voltage of transistor N1 (node B) is about 2.3 V. However, the diode-connected transistors N5 and N6

may make node B to 3.3 V, when signal IN stays at 3.3 V for a long time, because of the subthreshold current of transistors N5 and N6. A weak transistor N7 is added to avoid node B over 2.5 V induced by the subthreshold current of transistors N5 and N6. As the node B goes to 3.3 V, transistors N7 provides a small current to keep the gate voltage of transistor N1 under 2.5 V.

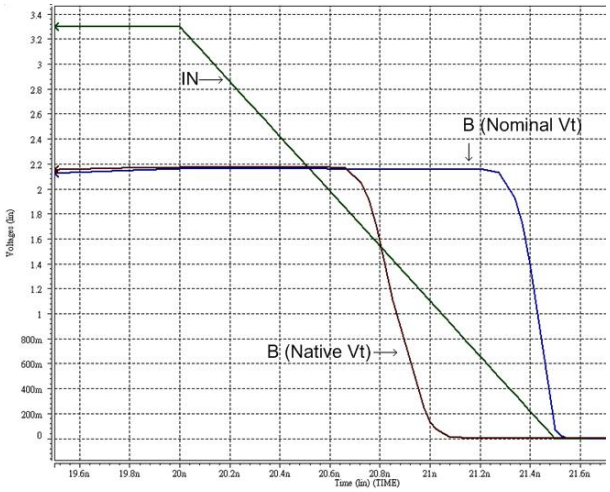

Fig. 5. Simulated waveforms at nodes IN and B.

In addition, transistor N6 is a 2.5 V native Vt transistor instead of a 2.5 V nominal Vt transistor. Because the gate-source voltage of transistor N6 is so small, node B follows signal IN to 0 V slowly. Thus, a native Vt transistor is more suitable than a nominal Vt transistor of transistor N6. Because the native Vt device is one of the standard devices in a 0.13 μm 1/2.5 V CMOS process, no extra process or mask is needed [10]. Fig. 5 compares the voltages at node B when transistor N6 is a native Vt transistor and a nominal Vt transistor in a 0.13 μm 1/2.5 V CMOS process. As shown in Fig. 5, node B is pulled down more quickly as transistor N6 is a native Vt transistor.

3. EXPERIMENTAL RESULTS

3.1. Simulation

A 0.13 μm 1/2.5 V CMOS SPICE model is used to simulate the new proposed Schmitt trigger circuit. Fig. 6 shows the simulated waveforms of the new proposed Schmitt trigger circuit. The input signal can be correctly translated to the output by the proposed Schmitt trigger circuit. Besides, signal A is higher than 0.8 V and signal B is lower than 2.5 V, as shown in Fig. 6. Therefore, transistors P1 and N1 of the new proposed Schmitt trigger circuit don't have high-voltage gate-oxide reliability problem, when the input signal swing is 3.3 V. In other words, the new proposed Schmitt trigger circuit can receive the high-voltage input signal, but it is realized by only using the low-voltage devices with thin gate oxide.

Fig. 7 shows the simulated transfer curve of the new proposed Schmitt trigger circuit. As shown in Fig. 7, the new proposed circuit has an obvious hysteresis characteristic. The simulated transition threshold voltages V_L and V_H of the new proposed Schmitt trigger circuit are about 1.1 V and 2.6 V, respectively.

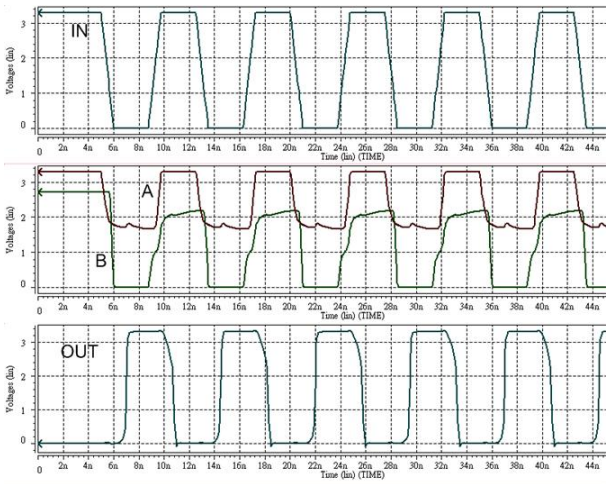

Fig. 6. Simulated waveforms of the new proposed Schmitt trigger circuit.

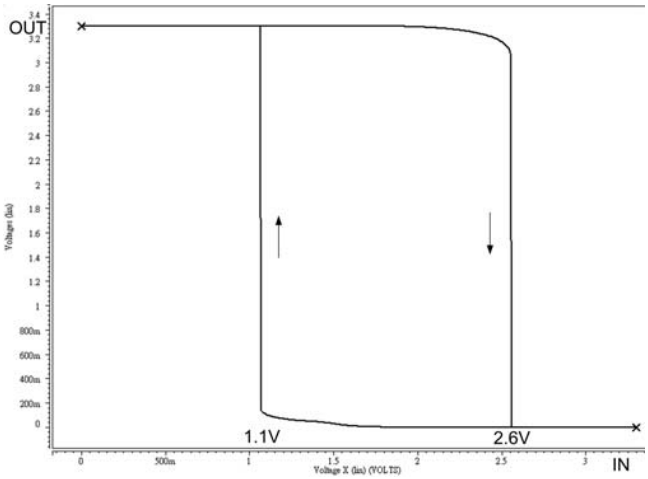

Fig. 7. Simulated transfer curve of the new proposed Schmitt trigger circuit.

3.2. Silicon Verification

The new proposed Schmitt trigger circuit has been implemented in a 0.13 μm 1/2.5 V CMOS process. Fig. 8 shows the layout of the new proposed Schmitt trigger circuit. Because the proposed circuit is applied to an input buffer, a guard ring surrounds the proposed Schmitt trigger circuit. The area of the proposed Schmitt trigger circuit including the guard ring is only 8.7×19 μm^2. The measured results are shown in Figs. 9 and 10. Fig. 9 shows the measured waveforms at the input node and output node of the new proposed Schmitt trigger circuit. As shown in Fig. 9, the new proposed Schmitt trigger can operate correctly in

the input buffer. In Fig. 10, the input signal is a slow triangular wave, and thus, the transition threshold voltages V_L and V_H of the new proposed Schmitt trigger circuit can be measured according to the input signal and output signal. As shown in Fig. 10, the two transition threshold voltages of the new proposed Schmitt trigger circuit are around 1 V and 2.5 V, respectively. The measured transition threshold voltages are similar to the simulated transition threshold voltages.

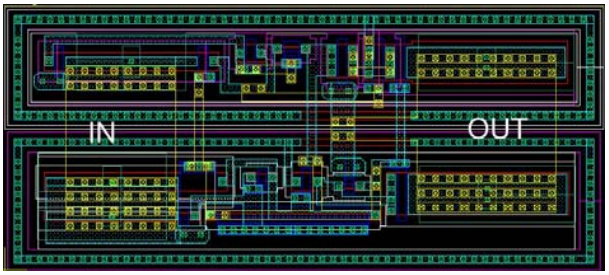

Fig. 8. Layout of the new proposed Schmitt trigger circuit.

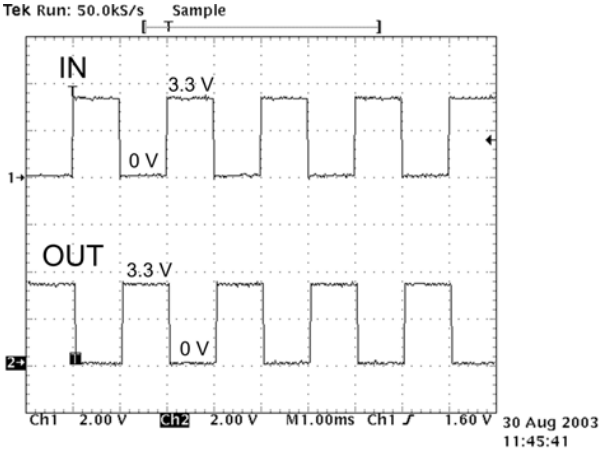

Fig. 9. Measured waveforms of the new proposed Schmitt trigger circuit.

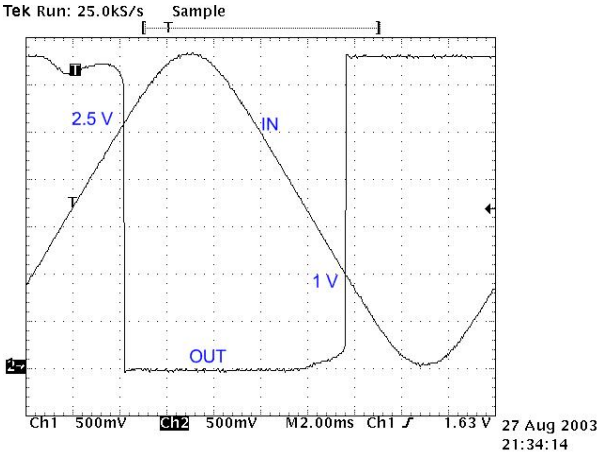

Fig. 10. Measured transition threshold voltages V_L and V_H of the new proposed Schmitt trigger circuit.

4. CONCLUSION

A new Schmitt trigger circuit, which has been realized with low-voltage devices in a 0.13 μm 1/2.5 V CMOS process, is proposed in this paper. The new proposed circuit, which consists of low-voltage devices, can operate correctly without suffering high-voltage gate-oxide stress as input signal swing is 3.3 V. The experimental results show that the two threshold voltages V_L and V_H of the new proposed Schmitt trigger are 1 V and 2.5 V, respectively. The new proposed Schmitt trigger circuit is suitable to reject noise for mixed-voltage interface applications.

5. REFERENCES

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