DESIGN ON MIXED-VOLTAGE-TOLERANT I/O INTERFACE WITH NOVEL TRACKING CIRCUITS IN A 0.13-μM CMOS TECHNOLOGY

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ABSTRACT

This paper presents a 1.2V/2.5V tolerant I/O buffer design with only thin gate-oxide devices. The novel floating N-well and gate-tracking circuits in mixed-voltage I/O buffer are proposed to overcome the problem of leakage current, which will occur in the conventional CMOS I/O buffer when using in the mixed-voltage I/O interfaces. The new proposed 1.2V/2.5V tolerant I/O buffer design has been successfully verified in a 0.13-μm salicided CMOS process, which can be also applied in other CMOS processes to serve different mixed-voltage I/O interfaces.

1. INTRODUCTION

When CMOS technology had been scaled down toward nanometer generation, the power supply voltage is also decreased to reduce power consumption [1]. For example, the VDD is decreased to 1.2V in the typical 0.13-μm CMOS process. However, some peripheral components or other ICs are still operated with the higher voltage levels such as 2.5V, 3.3V, or 5V for different system specifications [2]. In other words, the chip with output voltage of 2.5V may use to drive the chip with power supply voltage of 1.2V in a system, and vice versa. The conventional CMOS I/O buffer design is not suitable in the mixed-voltage system, because several issues may arise, such as gate-oxide reliability [3], hot carrier degradation [4], and undesirable leakage current paths [5]-[7].

Fig. 1 shows the leakage current path and gate-oxide overstress issues for the conventional CMOS I/O buffer using in a 1.2V/2.5V mixed-voltage application. The power supply voltage VDD is 1.2V, but the input signal at the I/O pad may rise up to 2.5V in the receiving (input) mode. In order to turn off the pull-down NMOS and the pull-up PMOS in the receiving (input) mode, the gates of pull-down NMOS and pull-up PMOS are biased at 0V and 1.2V by the pre-driver circuit, respectively. But, if the input voltage at the pad rises as high as 2.5V, the parasitic drain-to-well diode in the pull-up PMOS will be forward biased to cause a leakage current path from pad to VDD. Furthermore, because the |Vgd| of the pull-up PMOS equals to 1.3V, which is higher than |Vtp|, this PMOS conducts incorrectly to cause another leakage current path from pad to VDD through its channel. Besides, the overstress voltage across gate oxide is another serious danger to the mixed-voltage I/O interface circuits. As shown in Fig. 1, the pull-down NMOS and transistors in the input buffer suffer overstress voltage across their thin gate oxides. The thin gate oxide may become leaky due to tunneling effect or dielectric breakdown. If the electric field across the thin gate oxide is too large, it may even be permanently damaged.

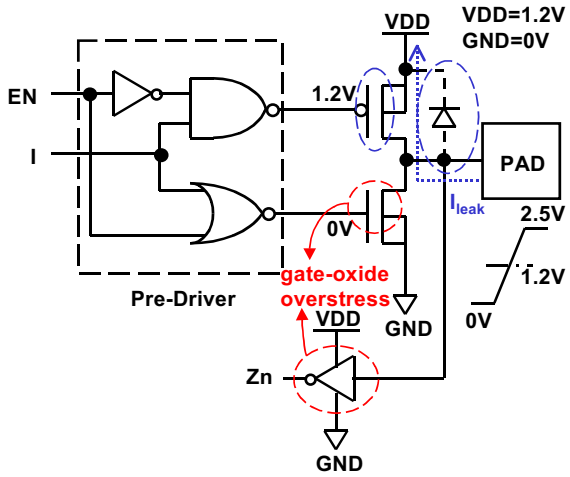


Fig. 1 The conventional CMOS I/O buffer in the 1.2V/2.5V mixed-voltage application.

In order to solve the aforementioned issues in the mixed-voltage applications, the thick gate-oxide devices [8] and additional N-well bias [9] had been used in some CMOS I/O buffers. However, the use of thick gate-oxide devices increases the cost of wafer fabrication with the dual-oxide option in CMOS processes. Moreover, it changes the threshold voltages of the pull-up/pull-down transistors and degrades the performance of the I/O buffer. On the other hand, there are also some drawbacks in using additional N-well bias in the mixed-voltage I/O buffer. First, the difficulty in layout routing is increased by the requirement of the additional pad and associated metal connection delivering the bias to the body terminal of PMOS transistors. Second, because the body terminal is coupled to an external voltage source higher than the voltage of the source terminal, which is coupled to internal voltage supply, the threshold voltage of the pull-up PMOS is increased due to the body effect. In addition to these drawbacks, the gate voltage of pull-up PMOS also needs to be well controlled for reducing leakage current.

In this paper, a mixed-voltage I/O buffer design with novel floating N-well and gate-tracking circuits is proposed to overcome the undesirable leakage current and gate-oxide overstress issues, without using thick gate-oxide devices and additional N-well bias. The new proposed 1.2V/2.5V tolerant I/O buffer has been successfully verified in the 0.13-μm salicided CMOS process with a small layout area and a high ESD (Electrostatic Discharge) level.

2. MIXED-VOLTAGE I/O INTERFACE CIRCUIT

2.1. Design Concept

The new proposed 1.2V/2.5V tolerant I/O buffer design with novel floating N-well and gate-tracking circuits is shown in Fig. 2, where the thick gate-oxide devices are not used. The floating N-well circuit is used to control the N-well voltage of pull-up PMOS for overcoming leakage current from pad to VDD through the parasitic drain-to-well junction diode. The gate-tracking circuit is used to control the gate voltage of pull-up PMOS for overcoming leakage current from pad to VDD through the pull-up PMOS with incorrect conduction. The pre-driver is used to control the I/O buffer into the receiving (input) mode or the transmitting (output) mode by the control port EN. The ESD protection circuit is used to enhance the ESD robustness of the mixed-voltage I/O buffer.

When EN is biased at logic 1 (1.2V), the I/O buffer is operated in the receiving (input) mode. Therefore, the signal coupled to I has no effect on pad voltage, and the voltage of Zn is driven by the external input signal coupled to the pad. If the I/O pad is driven by 2.5V signal, the floating N-well and gate-tracking circuits will charge the N-well and the gate of the pull-up PMOS to 2.5V to turn off the parasitic drain-to-well diode and the pull-up PMOS. Therefore, the leakage current flow from the pad to VDD through them can be completely prevented. If the I/O pad is driven by 0V or 1.2V signals, the floating N-well and gate-tracking circuits will charge the N-well and the gate of the pull-up PMOS to 1.2V for keeping this PMOS off without body effect.

When EN is biased at logic 0 (0V), the I/O buffer is operated in the transmitting (output) mode. Therefore, the voltage of pad is driven by the signal coupled to I. The floating N-well circuit has to keep the N-well voltage of pull-up PMOS at 1.2V for avoiding body effect in the transmitting mode, no matter the signal coupled to I is logic 0 (0V) or logic 1 (1.2V). The gate-tracking circuit must transfer the signal from I to the gate of pull-up PMOS through pre-driver exactly.

2.2. Circuit Implementation

The complete realization of the floating N-well and the gate-tracking circuits in 1.2V/2.5V tolerant I/O buffer is shown in Fig. 3. The ESD protection circuit that is not shown in Fig. 3 should be also added in the mixed-voltage I/O buffer [10]. The NMOS devices N_{o2} and N_{i1} are used as high voltage block for avoiding gate-oxide overstress on N_{o1} and INV1, respectively [9]-[13]. The PMOS device P_{i1} in the input stage is added to serve a pull-up element for pulling the final voltage level of logic 1 to 1.2V (VDD) at the input node of INV1. The explanation for the operations on floating N-well and gate-tracking circuits in different modes will be clearly describing in the following sub-sections.

2.3. Operating in the Receiving (input) Mode

When the I/O buffer is operated in the receiving mode, the upper and lower output ports of pre-driver in Fig. 3 will be 1.2V and 0V, respectively. The input signal coupled to pad for logic 0 is 0V, and for logic 1 is 2.5V. If the pad voltage is coupled to 2.5V, the PMOS devices P_{o7} and P_{o8} in the floating N-well circuit are turned on. Therefore, the PMOS P_{o6} is turned off by its gate voltage coupled to 2.5V through P_{o8}, and the N-well voltage is coupled to 2.5V through P_{o7}. On the other hand, P_{o2} and P_{o4} in the gate-tracking circuit are also turned on in this operating condition. Therefore, P_{o3} is turned off by its gate voltage coupled to 2.5V through P_{o4}, and the gate voltage of P_{o1} is coupled to 2.5V through P_{o2}. Because the N-well and the gate voltages of P_{o1} are both coupled to 2.5V, there is no leakage path from pad to VDD when pad voltage is coupled to 2.5V. If the pad voltage is coupled to 0V, the gate voltage of P_{o6} is coupled to 0V through N_{o8}. Therefore, P_{o6} is turned on and the N-well voltage is kept at 1.2V through P_{o6}. On the other hand, the gate voltage of P_{o3} is coupled to 0V through N_{o4}. Therefore, P_{o3} is turned on and the gate voltage of P_{o1} is coupled to 1.2V through P_{o3}. With such arrangement, this I/O buffer can be correctly operating in the receiving mode in the mixed-voltage interface.

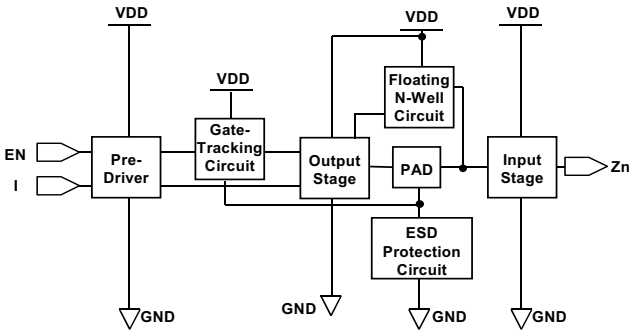


Fig. 2 The block diagram of the new proposed 1.2V/2.5V tolerant I/O buffer design with only thin gate-oxide devices.

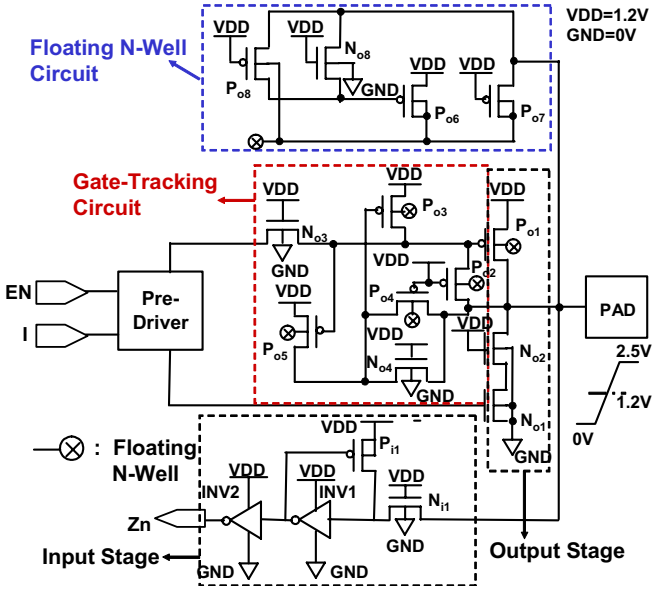


Fig. 3 The novel floating N-well and gate-tracking circuits in the 1.2V/2.5V tolerant I/O buffer design with only thin gate-oxide devices.

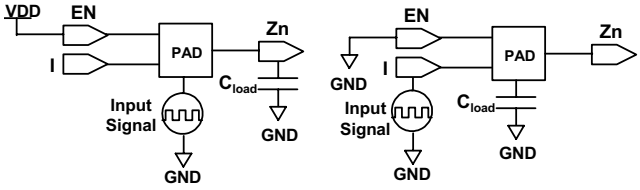
2.4. Operating in the Transmitting (output) Mode

When the I/O buffer is operated in the transmitting mode, the upper and lower output ports of pre-driver in Fig. 3 will be controlled by the signal coupled to I, and the pad voltage is controlled by I. The input signal coupled to I for logic 0 is 0V, and

for logic 1 is 1.2V. If the signal coupled to I is 0V, the two output ports of pre-driver are biased at 1.2V, and N_{o1} of the output stage is turned on to kept the pad voltage at 0V. Therefore, the N-well and the gate voltages of P_{o1} in the output stage are kept at 1.2V by the floating N-well circuit and the gate-tracking circuit. If the signal coupled to I is 1.2V, the two output ports of pre-driver are biased at 0V, and P_{o1} is turned on to keep the pad voltage at 1.2V. In order to keep the gate voltage of P_{o1} at 0V exactly, P_{o5} is added to quickly turn off P_{o3} in this operating condition, where to avoid charging effect on the gate of P_{o1}. On the other hand, the N-well voltage is kept at 1.2V because all the transistors in the floating N-well circuits are off without leakage path.

2.5. Simulation Results

In order to prove the function of the new proposed floating N-well and gate-tracking circuits, SPICE is used to simulate the 1.2V/2.5V tolerant I/O buffer in the 0.13-µm salicided CMOS process. The simulation methods on this I/O buffer in the receiving mode and transmitting mode are shown in Fig. 4(a) and 4(b), respectively. In the receiving mode, EN is coupled to VDD (1.2V) and the pad is coupled to input signal of 0V ~ 2.5V. A loading capacitance C_{load} of 30pF is added at Zn for simulation. In the transmitting mode, EN is coupled to GND (0V) and I is coupled to input signal of 0V ~ 1.2V. A loading capacitance C_{load} of 30pF is added at the pad for simulation. The simulation waveforms are shown in Fig. 5. In the receiving mode, the N-well and the gate voltages of P_{o1} are at 1.2V and 2.5V when pad voltage is at 0V and 2.5V, respectively. In the transmitting mode, the gate voltage of P_{o1} is changing from 1.2V to 0V when I voltage is changing from 0V to 1.2V, and the N-well voltage is kept at 1.2V. From the simulation results, the novel floating N-well and gate-tracking circuits are operating correctly for mixed-voltage I/O buffer to overcome leakage current issue.



(a) (b)

Fig. 4 The simulation methods on the proposed 1.2V/2.5V tolerant I/O buffer (a) in the receiving mode, and (b) in the transmitting mode, with a 30pF load.

3. EXPERIMENTAL RESULTS

Fig. 6 shows the layout top view of the 1.2V/2.5V tolerant I/O buffer with the novel floating N-well and gate-tracking circuits in a 0.13-µm salicided CMOS process. The ESD protection circuit [10] is added in this I/O buffer. The cell pitch and cell height (without bond pad) are only 65µm and 116.9µm, respectively. In order to verify the I/O function, the input signal of 0V ~ 2.5V is applied to one pad which is operated in the receiving (input) mode. This signal is transferred to another pad which is operated in transmitting (output) mode. Figs. 7(a) and 7(b) show the measured waveforms on the I/O buffer in receiving mode and transmitting mode under frequency of 1MHz and 100MHz, respectively. From the measured results, the I/O buffer can be operated in a wide frequency range.

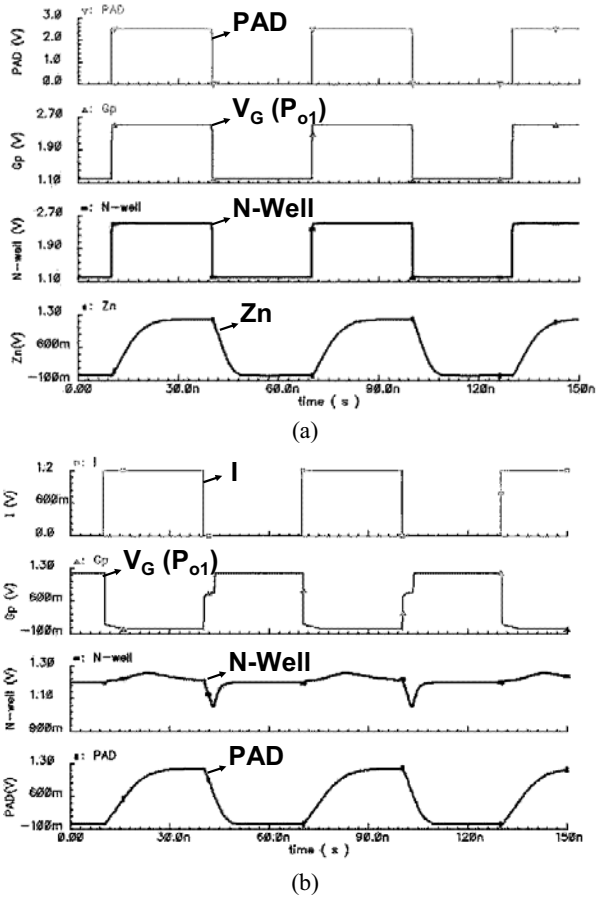


Fig. 5 The simulation waveforms on the proposed 1.2V/2.5V tolerant I/O buffer (a) in the receiving mode, and (b) in the transmitting mode, with a 30pF load.

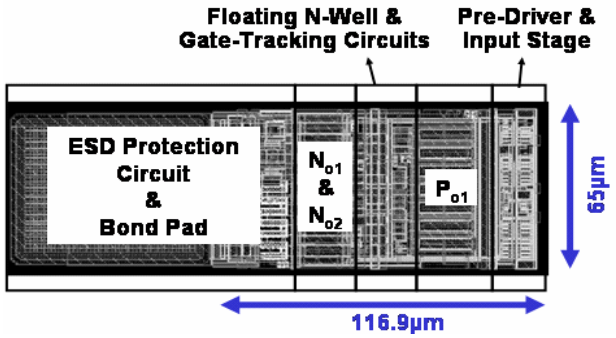
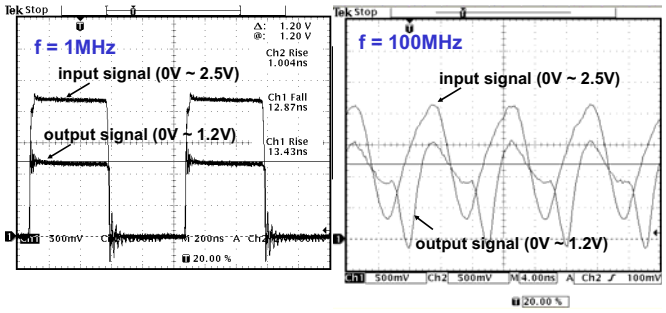


Fig. 6 The layout top view of the 1.2V/2.5V tolerant I/O cell with the novel floating N-well and gate-tracking circuits in the 0.13-µm salicided CMOS process. The cell pitch and cell height (without bond pad) are only 65µm and 116.9µm, respectively.

For I/O buffer design, ESD protection is a major concern in nano-scale CMOS technology. For whole-chip ESD protection, the power-rail ESD clamp circuit shown in Fig. 8 is used in both VDD and GND cells with the substrate-triggered field-oxide device (STFOD) [14]. The transmission-line-pulsing (TLP) [15] measured I-V curves of the fabricated 1.2V/2.5V tolerant I/O buffers with or without the power-rail ESD clamp circuit are shown in Fig. 9. The secondary breakdown currents (It2) of these two conditions are

both greater than 6A, which imply that the human-body-model (HBM) ESD level of the I/O cells can be greater than 9kV.



(a) (b)

Fig. 7 The measured waveforms on the proposed 1.2V/2.5V tolerant I/O buffer in the receiving mode and transmitting mode under (a) f = 1MHz, and (b) f = 100MHz.

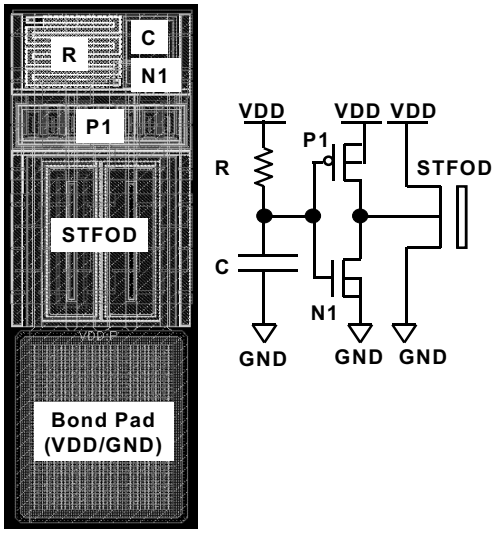


Fig. 8 The layout top view and circuit diagram of the power-rail ESD clamp circuit.

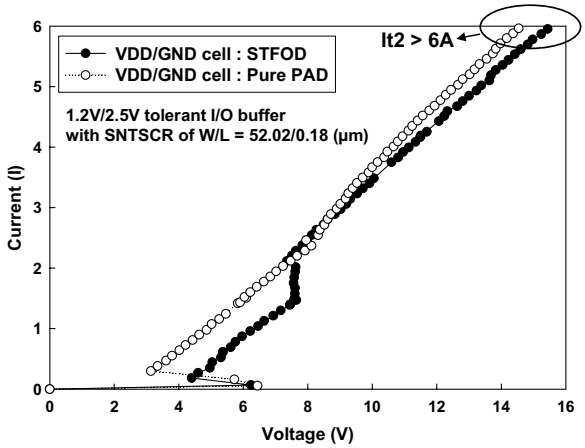


Fig. 9 The TLP-measured I-V curves of the new proposed 1.2V/2.5V tolerant I/O buffers with or without the power-rail ESD clamp circuit.

4. CONCLUSION

A 1.2V/2.5V tolerant I/O buffer with novel floating N-well and gate-tracking circuits has been proposed and successfully verified in a 0.13-μm salicided CMOS process with a small layout area and a high ESD level. The leakage and gate-oxide overstress issues have been overcome by this design, without using the thick gate-oxide devices. Based on the new proposed mixed-voltage I/O buffer design, one set of area-efficient I/O cell library has been practically built up in a 0.13-μm salicided CMOS process for SoC design and IP-reuse applications.

5. REFERENCES

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