ESD PROTECTION DESIGN FOR IC WITH POWER-DOWN-MODE OPERATION

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ABSTRACT

A new ESD protection design for IC with power-down operation is proposed. By adding a VDD ESD bus line and diodes into the new ESD protection scheme, the leakage current from I/O pin to VDD power line can be blocked to avoid malfunction under the power-down-mode operating condition. Under normal circuit operating condition, the proposed ESD protection schemes have no leakage path to interfere with the normal circuit functions. Power-rail ESD clamp circuits between the VDD/VSS power lines and VDD ESD bus line are used to achieve whole-chip ESD protection design. From the experimental results, the human-body-model (HBM) ESD level of the new proposed ESD protection schemes can be greater than 7.5kV in a 0.35-μm silicided CMOS process.

1. INTRODUCTION

To save power consumption, IC with power-down-mode operation becomes necessary, especially in SOC (System on a Chip) design for the portable and mobile products. When the power-down-mode operation of the IC is needed, modification on the design of I/O circuits and ESD protection circuits has been studied [1], [2]. An example of two chips connected in a system is shown in Fig. 1, where the output pad of the chip_1 is connected to the input pad of the chip_2. When the chip_2 goes into the power-down-mode operation, two situations are explained as follows. First, if VDD2 power line is grounded, a large leakage current may be induced from the input pad to the VDD2 power line through the parasitic diode of pMOS connected between the input pad and VDD2 power line, when the output voltage level of the chip_1 is high. Second, if the VDD2 power line is floating, the internal circuits of the chip_2 may be triggered to cause malfunction by charging the VDD2 power line through the parasitic diode of pMOS, when the output voltage level of the chip_1 is high. Therefore, the parasitic diode of pMOS connected between the input pad and VDD2 power line must be removed to avoid leakage current or malfunction, when the chip_2 goes into the power-down-mode operation.

ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) ESD zapping conditions. To avoid unexpected ESD damage in the internal circuits of CMOS ICs [3], the turn-on efficient power-rail ESD clamp circuit had been placed between the VDD and VSS power lines of ICs [4]. Due to the limitation of placing a diode from the I/O pad to VDD in the power-down-mode operation, ESD current at the I/O pad under the PS-mode ESD stress cannot be diverted from the pad to VDD power line, and cannot be discharged through the VDD-to-VSS ESD clamp circuit. Such PS-mode ESD current at the I/O pad is discharged only through the gate-grounded nMOS (GGNMOS) between the I/O pad and VSS power line by snapback breakdown. Because the junction breakdown voltage is close to the oxide breakdown voltage as the device is shrunk, the GGNMOS could not provide efficient ESD protection to the internal circuits in sub-quarter-micron CMOS technology. Especially, the non-uniform turn-on issue often causes the GGNMOS to have a low ESD level. Under the PD-mode ESD stress, there is no direct discharging path from the I/O pad to VDD due to the limitation to put the diode from I/O pad to VDD. Therefore, the absence of the diode between I/O pad and VDD power line for power-down-mode operation will seriously degrade ESD performance of the I/O pad under the PS-mode and PD-mode ESD stresses. To solve the ESD protection and leakage issue for IC with power-down-mode operation, some modified designs had been reported in [5]-[7].

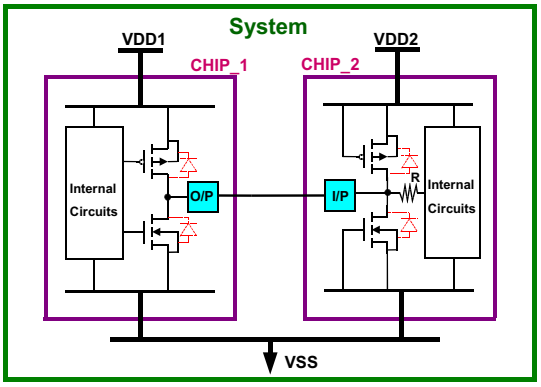


Fig. 1 An example to show the power-down-mode operation issue on a system with two chips, which are biased with separated VDD1 and VDD2 power supplies.

In this paper, two new ESD protection schemes for IC with power-down-mode operation are proposed. The new ESD protection schemes can overcome the leakage issue and have a very high ESD level for IC with power-down-mode operation, which have been successfully verified in a 0.35-μm silicided CMOS process.

2. NEW ESD PROTECTION SCHEMES FOR IC WITH POWER-DOWN-MODE OPERATION

2.1 ESD Protection Scheme I

The proposed ESD protection scheme I for the IC with power-down-mode operation is shown in Fig. 2 with the

additional ESD bus line (VDD_ESD), which is realized by wide metal line in CMOS IC. The VDD_ESD bus line is not directly connected to an external power supply pin. The diode D1 is connected between the VDD power line and VDD_ESD bus line to block the leakage current path from the input pad to VDD, when the power of VDD is off. The diode D2 is connected between the VDD power line and the source of output pMOS (Mp_out) to block the leakage current path from the output pad to VDD, when the power of VDD is off. The VDD_ESD bus line is not connected to the source of Mp_out in this scheme I, because the gate voltage of Mp_out will be dropped down and induces leakage current between I/O pads when the power of VDD is off. The diode D3 is connected between the output pad and VDD_ESD bus line for ESD protection purpose. One power-rail ESD clamp circuit is connected between VDD power line and VSS power line. A second power-rail ESD clamp circuit is connected between VDD_ESD bus line and VSS power line. The ESD current at the input (or output) pad under the PS-mode ESD stress can be discharged through the parasitic diode of Mp_in (or the diode D3) to the VDD_ESD bus, and then discharged through the ESD clamp circuit from the VDD_ESD bus to the grounded VSS power line. The ESD current at the input (or output) pad under the PD-mode ESD stress condition can be discharged through the parasitic diode of Mp_in (or the diode D3) to VDD_ESD bus line, the ESD clamp circuit to VSS power line, and then through the parasitic diode of ESD clamp circuit to the grounded VDD power line. The ESD current at the input (or output) pad under the NS-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to ground. The ESD current at the input (or output) pad under the ND-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to VSS power line, and then discharged through the VDD-to-VSS ESD clamp circuit to the grounded VDD power line.

2.2 ESD Protection Scheme II

The proposed ESD protection scheme II for IC with power-down-mode operation is shown in Fig. 3. The design concept is similar to that of the ESD protection scheme I. The diode D1 is connected between the VDD power line and VDD_ESD bus line to block the leakage current path from the input or output pad to VDD, when the power of VDD is off. The gate of Mp1 is connected to the VDD power line. Therefore, Mp1 is turned off under normal circuit operating condition. Under power-down-mode operating condition, the Mp1 is turned on to keep the Mp_out off. In addition, the power line of the pre-driver circuits which controlled the gate of Mp_out is connected to the VDD_ESD bus line to avoid the leakage current from the pre-driver circuits to VDD power line, when the power of VDD is off. The ESD current at the input (or output) pad under the PS-mode ESD stress can be discharged through the parasitic diode of Mp_in (or Mp_out) to the VDD_ESD bus, and then discharged through the ESD clamp circuit from the VDD_ESD bus to the grounded VSS power line. The ESD current at the input (or output) pad under the PD-mode ESD stress can be discharged through the parasitic diode of Mp_in (or Mp_out) to VDD_ESD bus line, the ESD clamp circuit to VSS power line, and then through the parasitic diode of ESD clamp circuit to VDD power line.

Therefore, with the new proposed ESD protection schemes, the leakage current or malfunction issues for the IC with power-down-mode condition can be avoided. The internal circuits of CMOS IC can be fully protected against ESD damage by the new proposed ESD protection schemes.

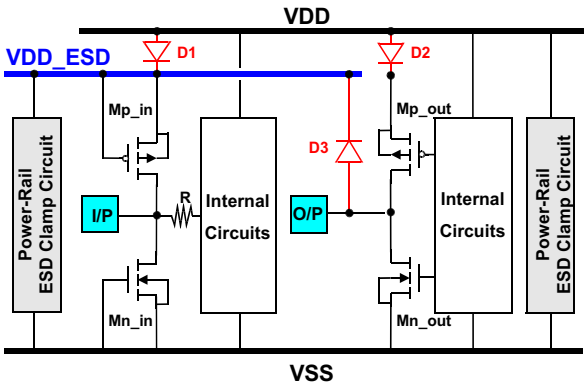


Fig. 2 The new proposed ESD protection scheme I for the IC with power-down-mode operation.

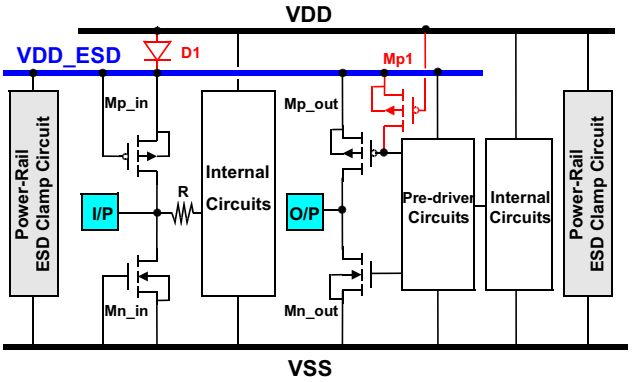


Fig. 3 The new proposed ESD protection scheme II for the IC with power-down-mode operation.

3. EXPERIMENTAL RESULTS

The testchips with the traditional ESD protection scheme, the proposed ESD protection scheme I, and the proposed ESD protection scheme II, fabricated in a 0.35-μm silicided CMOS process, are shown in Figs. 4(a) ~ 4(c), respectively. The input ESD protection devices are realized by the gate-connected-to-source pMOS (Mp_in) and gate-grounded nMOS (Mn_in) with both the device dimensions (W/L) of 490/0.5 (μm/μm). The output ESD protection devices are realized by the gate-connected-to-source pMOS (Mp_out), output buffer of pMOS (Mp_b), gate-grounded nMOS (Mn_out), and output buffer of nMOS (Mn_b) with the device dimensions (W/L) of 350/0.5, 140/0.5, 420/0.5, and 70/0.5 (μm/μm), respectively. Each gate bias of output buffers (Mp_b and Mn_b) is controlled by the input pad through two series inverters. In the proposed ESD protection scheme I, the junction perimeter of the diodes (D1, D2, and D3) is drawn as 50μm. In the proposed ESD protection scheme II, the junction perimeter of the diode (D1) is drawn as 50μm, and the device dimension (W/L) of the Mp5 is drawn as 20/0.5 (μm/μm). The power-rail ESD clamp circuit is realized by the substrate-triggered field-oxide device (STFOD) to have high enough ESD level in a limited layout area [8].

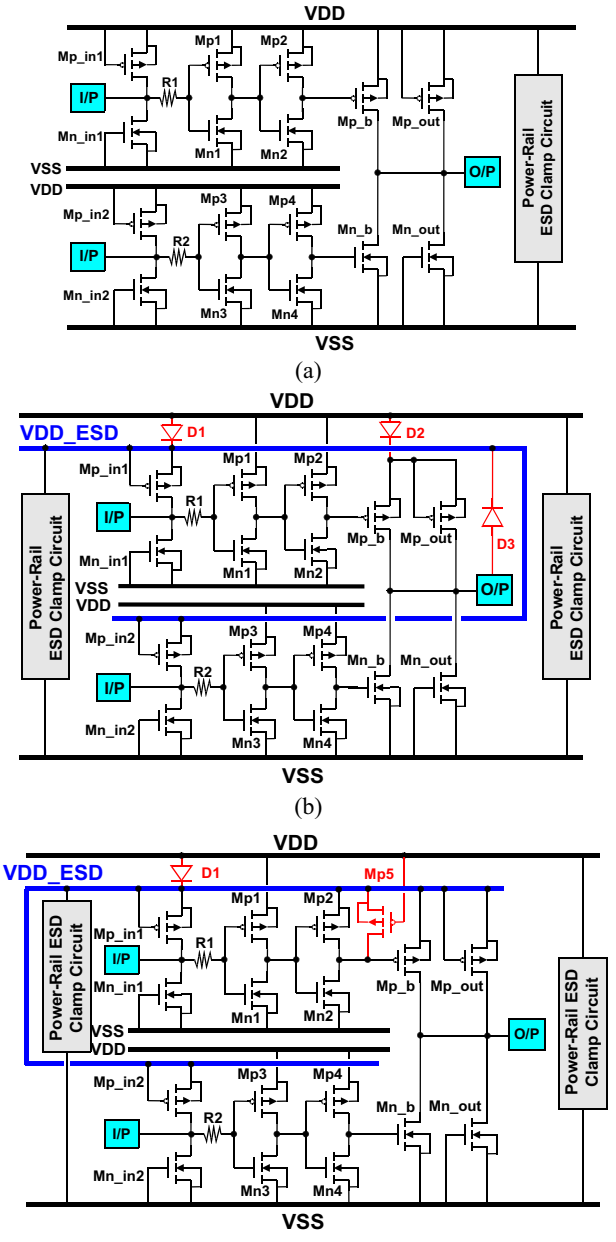


Fig. 4 The testchips with (a) the traditional ESD protection scheme, (b) the proposed ESD protection scheme I, and (c) the proposed ESD protection scheme II, fabricated in a 0.35-μm silicided CMOS process.

3.1. Leakage Current

The leakage current from the I/O pin to the VDD power line is a major concern when IC goes into power-down-mode operation with VDD of 0V. The leakage currents at the input pad and output pad among the different designs under power-down-mode operating condition are measured and compared in Figs. 5(a) and 5(b), respectively. The leakage current is measured by applying a voltage ramp from 0 to 3.3V to the input or output pad under the bias condition of 0-V VDD and 0-V VSS. In Fig. 5(a), the leakage currents of the proposed ESD protection schemes I and II with a 3.3-V input signal applying to the input pad are only ~ 130pA. On the contrary, the traditional ESD protection scheme has a very high leakage current of up to several mA when the input voltage is only increased to 0.7V. The leakage currents of output pad in Fig. 5(b) show the same result to that in Fig. 5(a). The experimental results have verified that the new proposed ESD protection schemes can avoid the leakage current from the I/O pin to VDD power line under the power-down-mode operating condition.

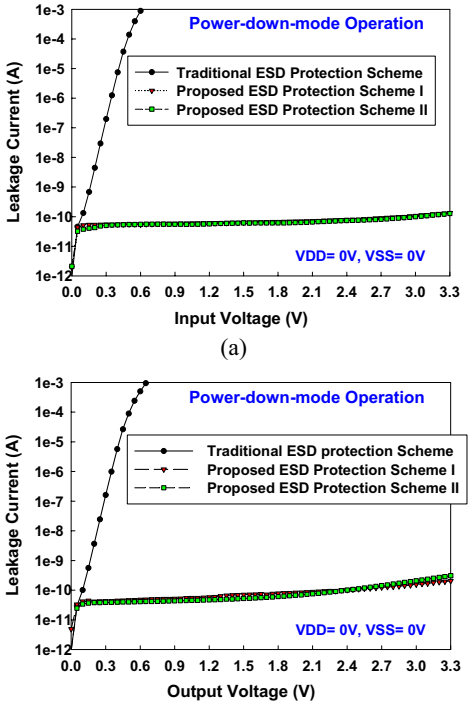


Fig. 5 Comparison of the leakage currents between the proposed ESD protection schemes and the traditional ESD protection scheme for (a) the input pad under power-down-mode operating condition, and (b) the output pad under power-down-mode operating condition.

3.2 Function Verification

The measurement setup to verify the function of I/O cells with the new proposed ESD protection schemes, or the traditional ESD protection scheme, under power-down-mode operating condition is shown in Fig. 6. A 0-to-3.3 V voltage pulse with a rise time of 20 ns is applied to the input pad under the power-down-mode condition of 0-V VSS but VDD is floating.

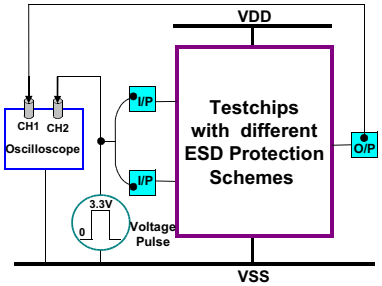
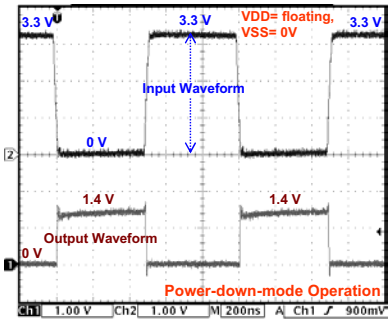
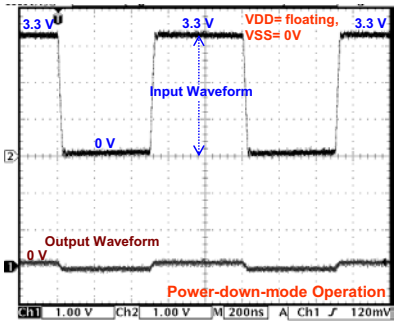


Fig. 6 The measurement setup to verify the ESD protection schemes for IC with power-down-mode operation.

The voltage waveforms on the input/output pads of the testchips with the traditional ESD protection scheme and the proposed ESD protection scheme I under power-down-mode operating condition are shown in Figs. 7(a) and 7(b), respectively. With the traditional ESD protection scheme, the voltage waveform on the output pad has a voltage level of ~1.4V, when the input voltage level is 0V, as that shown in Fig. 7(a). It implies that the internal circuits are triggered by the input voltage waveform under power-down-mode operating condition, although the circuits are expected to be off. With the wrong voltage waveform at the output pads, the system could be malfunction. However, with the proposed ESD protection scheme I, the voltage level on the output pad is always kept at ~ 0V, as shown in Fig. 7(b). It implies that the internal circuits can be really turned off by the proposed ESD protection scheme I under power-down-mode operating condition. In addition, the voltage waveforms on the input/output pads of testchip with the proposed ESD protection scheme II show the same results to that in Fig. 7(b) under power-down-mode operating condition.



(a)



(b)

Fig. 7 The measured voltage waveforms on the input/output pads of IC with (a) the traditional ESD protection scheme, and (b) the proposed ESD protection scheme I, under power-down-mode operating condition. (*Y* axis= 1V/Div., *X* axis= 200 ns/Div.)

3.3 ESD Robustness

The HBM ESD robustness of I/O pads with the proposed ESD protection schemes under the four pin-combination modes of ESD stresses on the I/O pad and VDD-to-VSS ESD stress is listed in Table I. The failure criterion is defined as the leakage current of the circuits after ESD zapping is greater than 1μA under the normal operating voltage of 3.3V. With the proposed ESD protection scheme I, the ESD levels of the input pad under the PS- and PD-mode ESD stresses are 7.5kV. With the proposed ESD protection scheme II, the ESD levels of the input pad under the PS- and PD-mode ESD stresses are 7.75kV. The ESD levels of the output pad with ESD protection scheme II under the PS- and PD-mode ESD stresses are 7.5kV and over 8kV, respectively. From the experimental results, the ESD levels of the I/O pad under the PS- and PD-mode ESD stresses can be efficiently improved by the proposed ESD protection schemes for IC with power-down-mode operation.

TABLE I
HBM ESD robustness of the proposed ESD protection schemes

HBM ESD ESD Stress / Protection Scheme	PS-Mode VSS(+)	NS-Mode VSS(-)	PD-Mode VDD(+)	ND-Mode VDD(-)	VDD-to-VSS(+)	VDD-to-VSS(-)
Scheme I (Input Pin)	7.5kV	>8kV	7.5kV	>8kV	>8kV	>8kV
Scheme I (Output Pin)	>8kV	>8kV	>8kV	>8kV		
Scheme II (Input Pin)	7.75kV	>8kV	7.75kV	>8kV	>8kV	>8kV
Scheme II (Output Pin)	7.5kV	>8kV	>8kV	>8kV		

4. CONCLUSION

The new ESD protection schemes for IC with power-down-mode operation have been successfully designed and verified in a 0.35-μm silicided CMOS process. Under the power-down-mode operating condition, the proposed ESD protection schemes can provide the I/O pad with a very low leakage current and avoid to trigger the circuits those should be "off". High ESD robustness has been practically achieved in the testchips with the proposed ESD protection schemes to sustain the HBM ESD stress of 7.5kV in a 0.35-μm silicided CMOS process.

5. REFERENCES

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