Layout Optimization on Low-Voltage-Triggered PNP Devices for ESD Protection in Mixed-Voltage I/O Interfaces

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Abstract -- Layout optimization on low-voltage-triggered PNP (LVTPNP) devices for ESD protection in mixed-voltage I/O interfaces is proposed in this paper. The experimental results in both 0.35-μm and 0.25-μm CMOS processes have proven that the ESD levels of the LVTPNP drawn in the multi-finger layout style are higher than that drawn in the original layout style. Moreover, the LVTPNP device in multi-finger layout style has been implemented in a 0.25-μm salicided CMOS process to protect successfully the input stage of an ADSL IC with power-rail ESD clamp circuit.

1. Introduction

With the mix of power supply voltages in a complex electronic system, as shown in Fig. 1, the I/O interface circuit and electrostatic discharge (ESD) protection circuit must be designed to avoid electrical overstress across the gate oxide, to avoid hot-carrier degradation on the output devices, and to prevent undesirable leakage current paths between the chips [1], [2].

One of the mixed-voltage circuit applications, such as ADSL which has input signals with voltage levels higher than VDD and lower than VSS, is shown in Fig. 2. A new ESD protection design with the low-voltage-triggered PNP (called as LVTPNP) has been developed to protect the I/O interface circuits in such applications [3], shown in Fig. 3 . The LVTPNP with a low breakdown voltage, by avalanche breakdown across the P+/N_well or N+/P_sub junctions provides effective discharging path to protect the internal circuits of such mixed-voltage I/O interfaces. There are three types of the LVTPNP device structures, shown in Fig. 4. Under normal circuit operation conditions, the LVTPNP device is kept off without causing current leakage between the chips. However, the ESD robustness of the original layout style of the LVTPNP with a larger emitter area, shown in Fig. 5, can't meet the ESD specification of 2-kV human-body-model (HBM) [4] ESD levels in a limited silicon area.

In this paper, layout optimization for low-voltage-triggered PNP (LVTPNP) devices has been proposed. The multi-finger layout style of the LVTPNP is used to improve ESD robustness over 2-kV HBM ESD levels in a smaller silicon area. Moreover, the input stage of ADSL with LVTPNP devices has been implemented in a 0.25-μm salicided CMOS process. ESD protection for ADSL with LVTPNP devices has been successfully designed to achieve a good ESD protection.

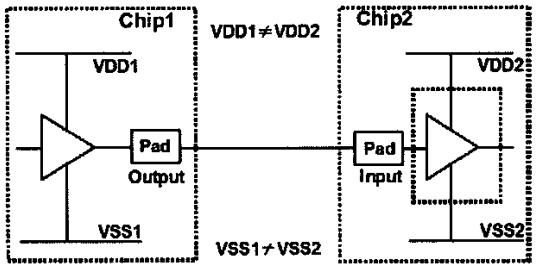

Fig. 1. The mixed-voltage I/O interfaces.

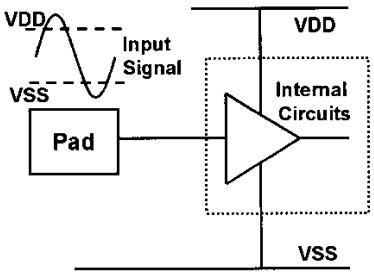

Fig. 2. The input signals with voltage levels higher than VDD and lower than VSS in some mixed-voltage I/O interfaces.

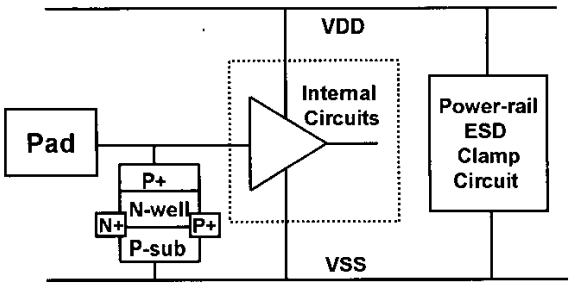

Fig. 3. A new ESD protection design with the LVTPNP device.

2. New Multi-Finger Layout Style for LVTPNP

In Fig. 4, based on the layout parameters (including the width, L_E, L_C, X_1, X_2, Y_1, Y_2, and Z) of LVTPNP devices, the ESD level mainly depends on the total current path from its emitter to its collector [3]. Hence, the LVTPNP with multi-finger layout style, shown in Fig. 6, is used to increase the effective current path for further ESD improvement in a limited silicon area. From the earlier experimental results [3], under the positive-to-VSS (PS) ESD-stress condition, ESD levels are independent to the

emitter length (L_E) and collector length (L_C). However, under the negative-to-VSS (NS) ESD-stress condition, ESD levels are independent to the L_C, but ESD levels are improved as L_E increases. Combined of these two ESD stress modes, the parameters of L_E and L_C are choice as minimum layout design rule in the multi-finger layout style to achieve higher ESD robustness per unit layout area.

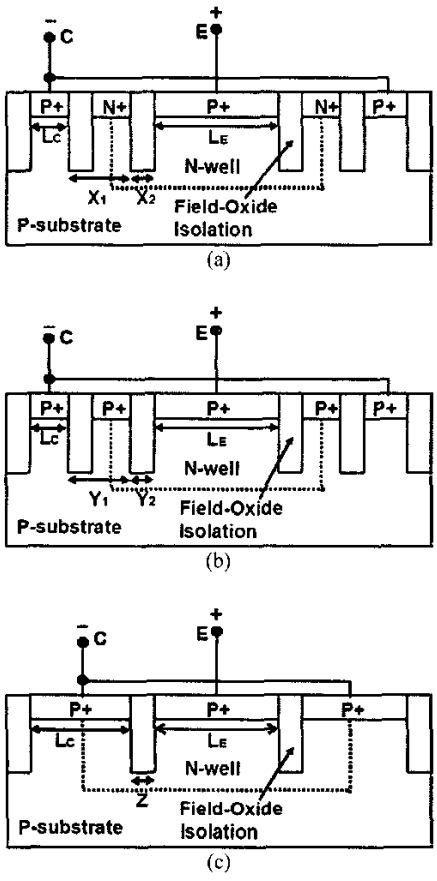

Fig. 4. The device structures of (a) the type1 LVTPNP, (b) the type2 LVTPNP, and (c) the type3 LVTPNP.

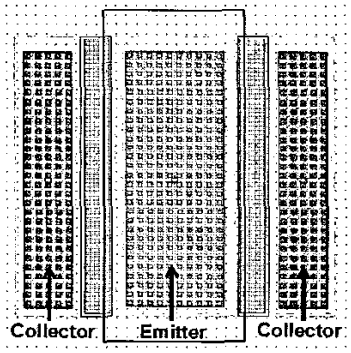

Fig. 5. The original layout style of the LVTPNP.

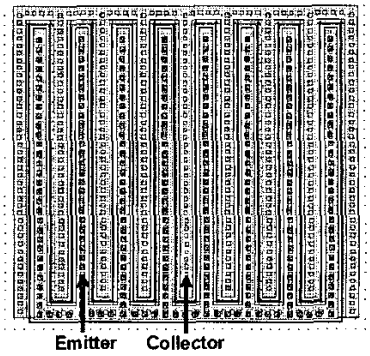

Fig. 6. The new proposed multi-finger layout style of the LVTPNP.

3. ESD Protection Design with LVTPNP for the Input Stage of ADSL

The LVTPNP devices can be used in the input ESD protection circuit for the ADSL interface, which has a high-voltage signal level of 5V and a low voltage signal level of -1V. The circuit application for such ADSL input stage is shown in Fig. 7, where the singled-ended operational amplifier is the input stage of ADSL. Under the 0.25-μm CMOS process with VDD of 2.5V, the voltage divider is used to scale down the ADSL input signals when the input signals (between 5V and -1V) transmitted into ADSL IC. The V_{i2} is biased at the reference voltage of 1.25V, which is half of VDD. The voltage divider is formed by R and R_f, which are designed to bias V_{i1} at the scaled-down voltage level and to make the singled-ended operational amplifier well operation. The dc bias of signal level at the output node of operational amplifier is 1.25V (VDD/2).

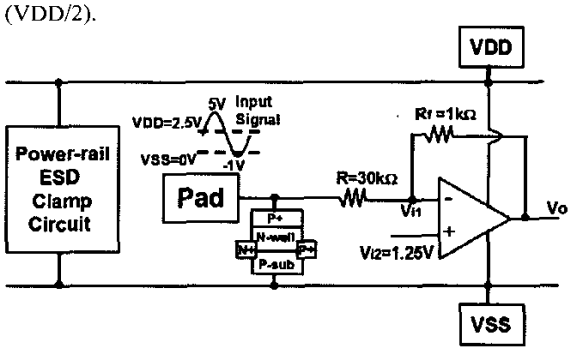

Fig. 7. The ADSL input stage with voltage divider formed by input R (30kΩ) and R_f (1kΩ) under 0.25-μm CMOS process.

The LVTPNP device is connected between input pad and VSS power line, which provides ESD protection in ADSL. Under normal operating condition, the LVTPNP is turned off as mentioned before, and has no influence to the ADSL input circuit. When ESD stress occurs to the input pin, the LVTPNP will break down with a lower trigger voltage to discharge ESD current. With the help of power-

rail ESD clamp circuit, the positive-to-VSS (PS), negative-to-VSS (NS), positive-to-VDD (PD), and negative-to-VDD (ND) ESD stresses [4] can be discharged through the LVTPNP to VSS or VDD. The ESD current paths in these four ESD-stress modes are shown in Figs. 8(a) ~ 8(d).

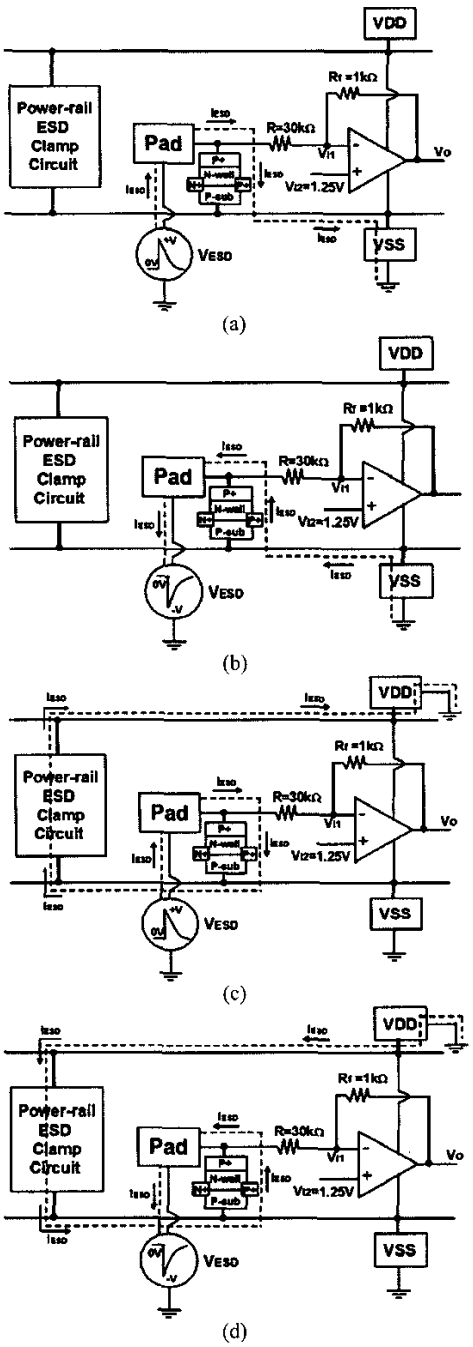

Fig. 8. The ESD current paths on ADSL input stage protected by LVTPNP under (a) PS-mode, (b) NS-mode, (c) PD-mode, and (d) ND-mode ESD-stress conditions.

4. Experimental Results

4.1. HBM ESD Levels of LVTPNP Devices with Different Layout Styles

The LVTPNP devices with original layout style and the new proposed multi-finger layout style have been fabricated in both 0.35-μm and 0.25-μm CMOS processes without any extra additional mask layer.

Under the positive-to-VSS (PS) ESD-stress condition, the HBM ESD levels of the LVTPNP devices with the original layout style and the new multi-finger layout style are compared in Table I. Under the negative-to-VSS (NS) ESD-stress condition, the HBM ESD levels of the LVTPNP devices with the original layout style and the new multi-finger layout style are compared in Table II. With suitable selection on the LVTPNP devices and the layout style, the overall ESD robustness of ADSL input stage can be designed to meet the ESD specification of 2-kV human-body-model (HBM) and 200-V machine-model (MM) ESD levels within a smaller silicon area. Especially, the LVTPNP in the type3 device structure with multi-finger layout style has an excellent ESD performance.

Because the doping concentration in a 0.25-μm salicided CMOS process is heavier than that in a 0.35-μm polycided CMOS process, the junctions have slightly lower breakdown voltages in a 0.25-μm CMOS process than that in a 0.35-μm CMOS process. HBM ESD levels of the LVTPNP devices in a 0.25-μm CMOS process are higher than those of the LVTPNP devices in a 0.35-μm CMOS process under both positive-to-VSS (PS) and negative-to-VSS (NS) ESD-stress conditions for the original layout style. Moreover, HBM ESD levels of the LVTPNP devices in a 0.25-μm CMOS process are higher than those of the LVTPNP devices in a 0.35-μm CMOS process under negative-to-VSS (NS) ESD-stress condition for the new multi-finger layout style.

However, HBM ESD levels of the LVTPNP devices in a 0.25-μm salicided CMOS process are lower than those of the LVTPNP devices in a 0.35-μm polycided CMOS process under positive-to-VSS (PS) ESD-stress condition for the new multi-finger layout style. The silicided diffusion in 0.25-μm salicided CMOS process causes degradation on ESD robustness of the LVTPNP device drawn in multi-finger layout style [5]. To further increase ESD level of the LVTPNP device, the optional silicide-blocking mask layer should be used to block the silicide formation around the perimeter of emitter region of the LVTPNP device in a 0.25-μm salicided CMOS process.

4.2. HBM ESD Levels of ADSL with the Type3 LVTPNP

Under PS-mode and PD-mode ESD-stress conditions, the ESD currents flow through LVTPNP from P+ diffusion to P-substrate (shown in Fig. 8(a) and 8(c)), so HBM ESD levels are determined by the LVTPNP in Table I in a 0.25-

μm salicided CMOS process. Under NS-mode and ND-mode ESD-stress conditions, the ESD currents flow through LVTPNP from P-substrate to P+ diffusion (shown in Fig. 8(b) and 8(d)), so HBM ESD levels are determined by the LVTPNP in Table II in a 0.25-μm salicided CMOS process.

Table I
HBM ESD Levels of the LVTPNP devices with different layout styles under positive-to-VSS (PS) ESD-stress condition.

Device Layout Style	Type1 Original Layout	Type2 Original Layout	Type3 Original Layout	Type1 Multi-Finger Layout	Type2 Multi-Finger Layout	Type3 Multi-Finger Layout
Layout Area (μm × μm)	36×32	36×32	36×30.8	33.6×36.5	33.6×36.5	33.6×36.5
HBM ESD Level (V) In a 0.35-μm CMOS Process	250	350	550	950	1050	3.6k
HBM ESD Level (V) In a 0.25-μm CMOS Process	350	350	750	850	900	1.4k
V_{ESD}/Area (V/μm²) In a 0.35-μm CMOS Process	0.22	0.3	0.5	0.77	0.86	2.94
V_{ESD}/Area (V/μm²) In a 0.25-μm CMOS Process	0.3	0.3	0.68	0.69	0.73	1.14

Table II
HBM ESD Levels of the LVTPNP devices with different layout styles under negative-to-VSS (NS) ESD-stress condition.

Device Layout Style	Type1 Original Layout	Type2 Original Layout	Type3 Original Layout	Type1 Multi-Finger Layout	Type2 Multi-Finger Layout	Type3 Multi-Finger Layout
Layout Area (μm × μm)	36×32	36×32	36×30.8	33.6×36.5	33.6×36.5	33.6×36.5
HBM ESD Level (V) In a 0.35-μm CMOS Process	1.2k	700	650	2.6k	2.4k	3.3k
HBM ESD Level (V) In a 0.25-μm CMOS Process	2.4k	2.2k	1.9k	2.7k	2.8k	3.8k
V_{ESD}/Area (V/μm²) In a 0.35-μm CMOS Process	1.04	0.61	0.59	2.12	1.96	2.69
V_{ESD}/Area (V/μm²) In a 0.25-μm CMOS Process	2.08	1.91	1.71	2.20	2.28	3.10

The input stage of ADSL with LVTPNP has been fabricated in a 0.25-μm salicided CMOS process. Among these types of LVTPNP devices, the type3 LVTPNP is used for input protection design in ADSL interface due to its highest HBM ESD levels. The HBM ESD levels of ADSL input stage under PS-mode, NS-mode, PD-mode, and ND-mode ESD-stress conditions are shown in Table III. As seen in Table III, with the type3 LVTPNP and power-rail ESD clamp circuit, the input stage of ADSL indeed can be protected from ESD stress.

In Table III, HBM ESD levels of input stage of ADSL with multi-finger layout style LVTPNP are higher than those of input stage of ADSL with original layout style LVTPNP. To further increase ESD level, the layout area of LVTPNP should be increased with the multi-finger layout style. Or, the silicide-blocking mask layer should be used to block the silicide formation around the perimeter of emitter region of the LVTPNP device.

Table III
HBM ESD Levels of ADSL input stage under PS-mode, NS-mode, PD-mode, and ND-mode ESD-stress conditions.

	PS-Mode	NS-Mode	PD-Mode	ND-Mode
ADSL Only	450V	350V	450V	400V
ADSL Including the Type3 LVTPNP with Original Layout Style	750V	1.9kV	750V	1.9kV
ADSL Including the Type3 LVTPNP with Multi-Finger Layout Style	1.4kV	3.8kV	1.3kV	3.8kV

5. Conclusion

The multi-finger layout style of the LVTPNP has been successfully designed to increase the effective current discharging path among the LVTPNP device for good ESD protection for the mixed-voltage I/O interfaces (such as ADSL) with inputs voltage levels higher than VDD and lower than VSS. Comparing these LVTPNP devices, due to the highest ESD robustness, the type3 LVTPNP with the multi-finger layout style will be the best choice as the ESD protection device for such mixed-voltage I/O interfaces. ESD protection design for ADSL with LVTPNP devices has been successfully designed to achieve a good ESD protection. The failure analysis on the ESD-tested samples will be shown in the presentation with EMMI pictures.

References

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