ESD Protection Design for High-Speed I/O Interface of Stub Series Terminated Logic (SSTL) in a 0.25-μm Salicided CMOS Process

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Abstract -- ESD protection design for high-speed I/O interface of stub series terminated logic (SSTL) is proposed. The SSTL I/O buffer with the proposed ESD protection design, which is designed to operate with a clock of 400MHz, has been fabricated and verified in a 0.25-μm salicided CMOS process. The human-body-model (HBM) and machine-model (MM) ESD levels of this SSTL I/O buffer can be greater than 8kV and 750V, respectively. Based on the excellent ESD performance, one set of area-efficient I/O cell library for SSTL in 1.8-V applications with this ESD protection design has been built up in a 0.25-μm salicided CMOS process.

1. Introduction

As the operating frequency of microprocessor up to giga-hertz (GHz), the DRAM with high-bandwidth I/O interface is necessary [1]. Double Data Rate Two (DDR2) SDRAM memory [2] with lower power, higher speed, and higher capacity than the conventional DDR memory has been developed. To support the desired fast I/O speed, DDR2 memory uses the new specified Stub Series Terminated Logic for 1.8-V application (SSTL_18) [3] as its I/O interface standard. The minimum frequency of clock operation for DDR2 is 200MHz, and may be up to 400MHz. However, with such a high operating frequency, the input loading of I/O pin in DDR2 has to be reduced. The conventional ESD (electrostatic discharge) protection designs on I/O pins with gate-grounded NMOS (GGNMOS) and gate-Vdd PMOS (GDPMOS) are not suitable, due to the large input parasitic capacitance. Therefore, an ESD protection circuit with small parasitic capacitance and high ESD robustness for SSTL_18 interface needs to be developed.

This paper presents the ESD protection design for SSTL_18 interface. The I/O buffer with the proposed ESD protection design can be operated with I/O speed of up to 400 MHz, which has been successfully verified in a 0.25-μm salicided CMOS process with a small layout area and very high ESD level.

2. Circuit Design and Layout Implementation

The proposed ESD protection circuits on input and output cells for SSTL_18 interface are shown in Figs. 1(a) and 1(b), respectively. Low-voltage-triggered silicon controlled rectifier (LVTSCR) with diode string [4]-[5] is used to discharge ESD current. The gate-coupled technique [6]-[7] is used to quickly trigger on the LVTSCR under ESD stress.

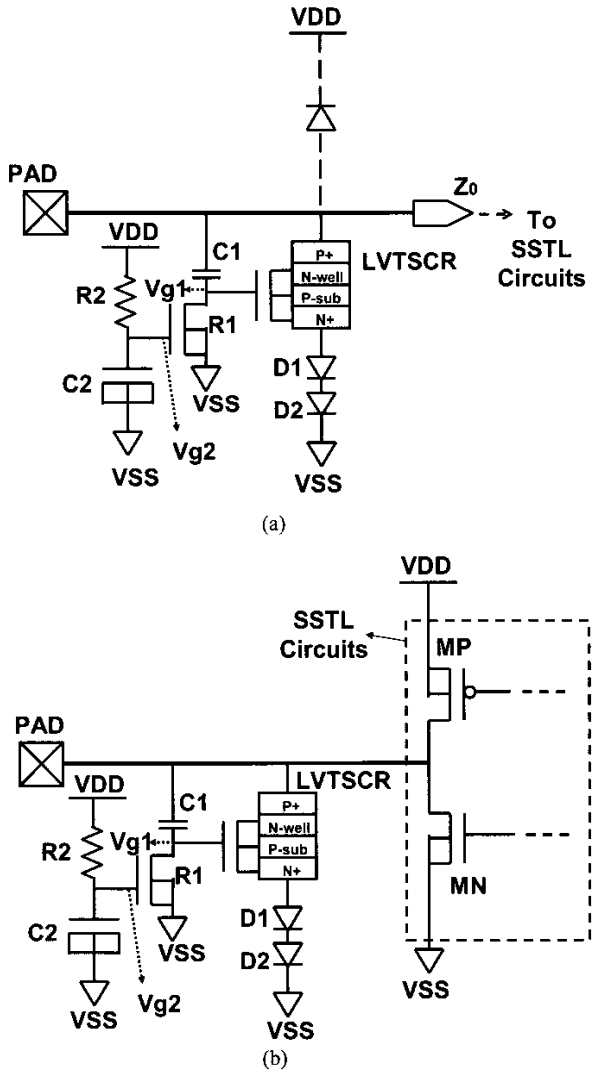
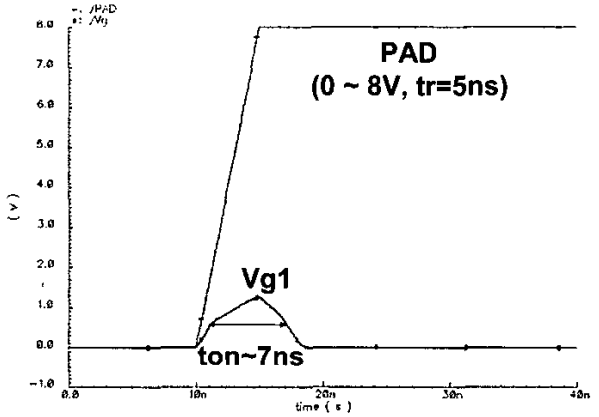
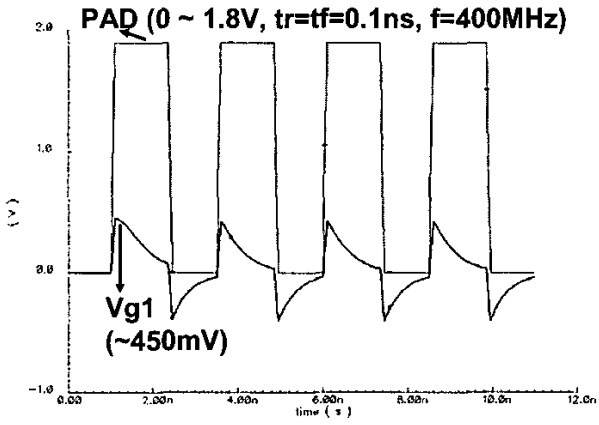


Fig. 1 The proposed ESD protection circuit for SSTL_18 interface on (a) input cell, and (b) output cell.

When a positive-to-VSS (PS-mode) ESD event is stressed at the input or output pad for SSTL_18, the gate voltage of LVTSCR (Vg1) is increased by the charge coupling through the capacitor C1. Because VDD is initially floating with a voltage level of 0V under PS-mode ESD stress, the coupled charge on the gate of LVTSCR will not be discharged through the resistor R1 which is realized by an NMOS. Therefore, LVTSCR can be turned on to conduct ESD current from pad to VSS through the LVTSCR and diode string. Fig. 2(a) shows the simulation result of the ESD protection circuit under PS-mode ESD stress, where a 0V-to-8V ESD-like pulse with a rise time of 5ns is applied to pad. The time duration (ton) of gate voltage (Vg1) on LVTSCR greater than the threshold voltage (Vth) is about 7ns. The LVTSCR can be turned on during this time duration (ton) to conduct ESD current under PS-mode ESD stress. This time duration (ton) can be adjusted by the R2 and C2 that connected to the gate of R1 NMOS. The capacitance C1 will also affect the time duration (ton). But, with consideration on the input loading of the pad, the capacitance of C1 is not suggested to be designed with a large value.



(a)



(b)

Fig. 2 Simulation results of the ESD protection circuit under (a) PS-mode ESD stress condition, and (b) normal circuit operating condition.

Under the normal circuit operating condition for SSTL_18, the gate voltage of R1 NMOS (Vg2) is biased at VDD through the resistor R2, and hence R1 NMOS is turned on to bias the Vg1 at 0V for keeping LVTSCR off. When the high-speed signal transition is applied to the pad, the charge coupled to Vg1 through C1 will be discharged through the turned-on R1 NMOS. Therefore, LVTSCR is kept off under normal circuit operating condition without latch-up or leakage issues. Fig. 2(b) shows the simulation result of the ESD protection circuit under normal circuit operating condition, where a 400-MHz signal with the rise and fall time of 0.1ns is applied to pad. The peak voltage of Vg1 under such high-speed I/O interface is only ~450mV, where is smaller than the threshold voltage of NMOS in a 0.25-μm salicided CMOS process.

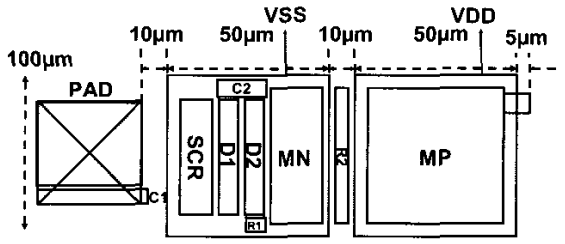
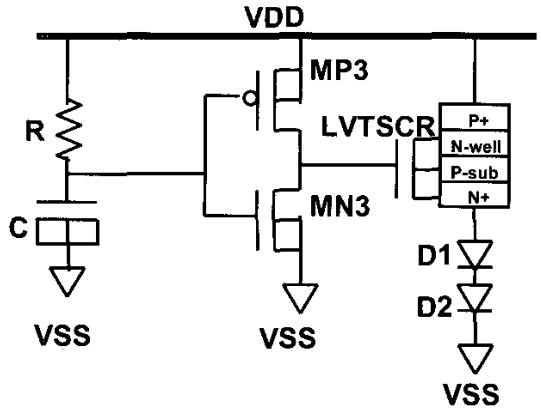
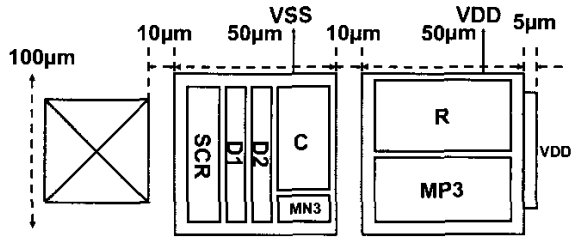


Fig. 3 The layout arrangement of SSTL_18 I/O interface with the proposed ESD protection circuit.



(a)



(b)

Fig. 4 The (a) circuit diagram, and (b) layout arrangement, of power-rail ESD clamp circuit.

The layout arrangement of the I/O cell for SSTL_18 interface with ESD protection design in a 0.25-μm salicided CMOS process is shown in Fig. 3. The channel width and channel length of embedded NMOS in the LVTSCR are 80μm and 0.24μm, respectively. The total layout area (excluding bonding pad) is only 125μm×100μm, which includes the ESD devices and the output stage of SSTL_18 interface. For whole-chip ESD protection consideration, the effective power-rail ESD clamp circuit, as shown in Fig. 4(a), is used in both VDD and VSS cells, which is also realized by the LVTSCR with gate-driven technique and diode string [5]. The R, C, MP3, and MN3 devices are used as the ESD detection circuit to quickly trigger on the LVTSCR under ESD stress. Under normal power-on operating condition, the ESD detection circuit can keep the LVTSCR off without latch-up issue. The layout arrangement of VDD cell is shown in Fig. 4(b). Fig. 5 shows the partial layout top-view of the test chip, which has been fabricated to verify ESD performance of the SSTL_18 I/O interface. A dummy NMOS with its gate connected to the input node Z0 of the input cell is used to verify the effectiveness of the new proposed ESD protection design.

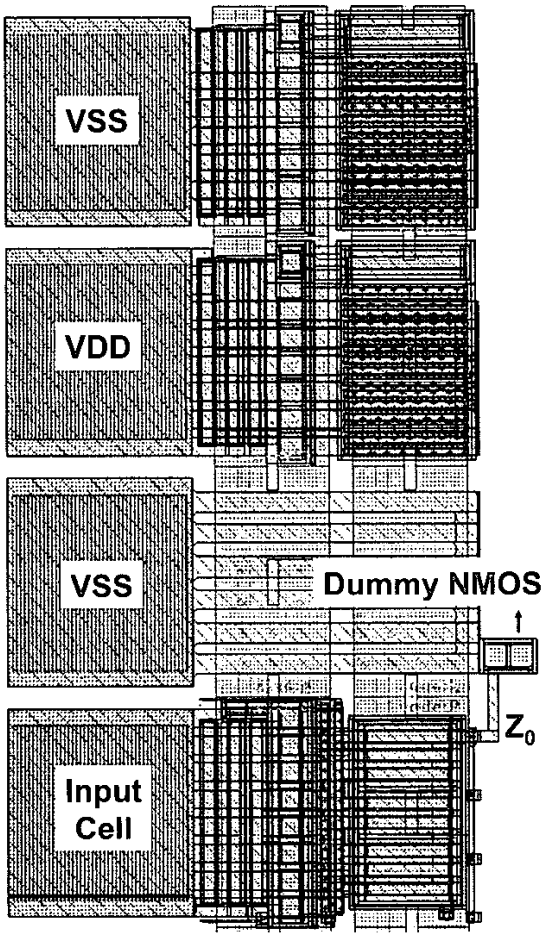


Fig. 5 The layout top-view of the test chip with dummy NMOS.

3. Experimental Results

The I/O buffer with the proposed ESD protection design has been fabricated in a 0.25-μm salicided CMOS process. A voltage pulse generated from a pulse generator (*HP8110A*) with a pulse height of 6V and a rise time of 5ns is used to simulate the rising edge of ESD pulse. Such a voltage pulse is applied to the pad of input cell with VSS pin relatively grounded to verify the turn-on behavior of the ESD protection circuit under PS-mode ESD stress condition. The measured results under PS-mode ESD stress condition are shown in Fig. 6(a), where the voltage level on the pad is clamped to ~3V which is greater than VDD (1.8V) without suffering latch-up issue. Besides, a 0-to-1.8V voltage pulse with the rise and fall time of 1.8ns is used to simulate the normal signal transition. Such a voltage pulse is applied to the pad of input cell to verify the operation of ESD protection circuit under normal circuit operating condition, and the result is shown in Fig. 6(b), where the LVTSCR is kept off without interference to the input signal.

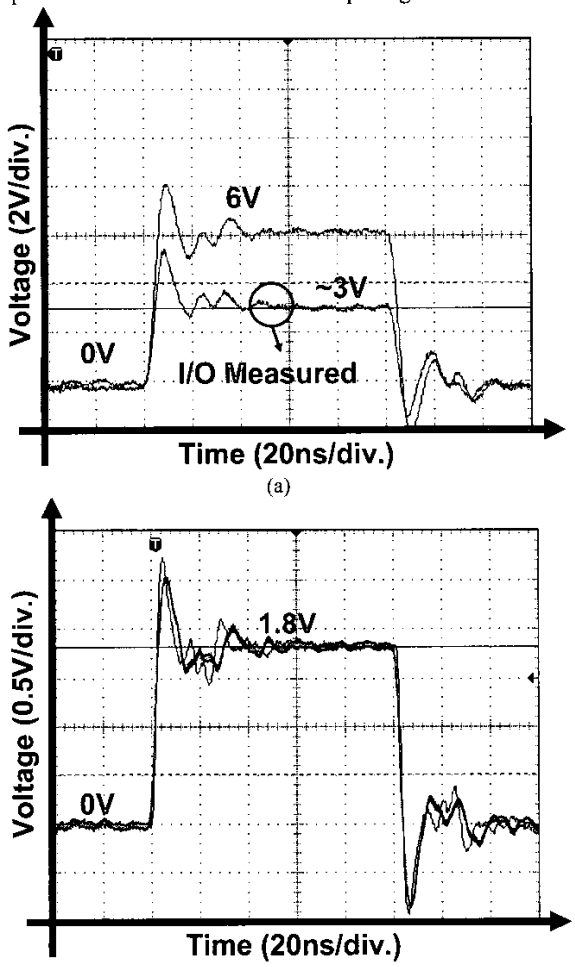


Fig. 6 Turned-on verification of the ESD protection circuit under (a) PS-mode ESD stress condition, and (b) normal circuit operating condition.

Table I The HBM ESD levels of the input and output cells with power-rail ESD clamp circuit in the VDD and VSS cells.

HBM ESD Level	PS-mode	NS-mode	PD-mode	ND-mode
Input Cell	> 8.0kV	> 8.0kV	> 8.0kV	> 8.0kV
Output Cell	> 8.0kV	> 8.0kV	> 8.0kV	> 8.0kV

Table II The MM ESD levels of the input and output cells with power-rail ESD clamp circuit in the VDD and VSS cells.

MM ESD Level	PS-mode	NS-mode	PD-mode	ND-mode
Input Cell	1000V	950V	1200V	800V
Output Cell	1250V	1000V	1600V	900V

Table III The HBM and MM ESD levels of the VDD cell.

ESD Level	VDD-to-VSS (+)	VDD-to-VSS (-)
HBM	> 8.0kV	> 8.0kV
MM	750V	950V

Table IV The HBM ESD levels of the input and output cells without power-rail ESD clamp circuit in the VDD and VSS cells.

HBM ESD Level	PS-mode	ND-mode
Input Cell	4.0kV	> 8.0kV
Output Cell	4.0kV	> 8.0kV

Table V The MM ESD levels of the input and output cells without power-rail ESD clamp circuit in the VDD and VSS cells.

MM ESD Level	PS-mode	ND-mode
Input Cell	950V	500V
Output Cell	950V	800V

The HBM [8] and MM [9] ESD levels of the input and output cells with the proposed ESD protection design for SSTL_18 interface have been verified by *KeyTek* ESD tester. The measured results of HBM and MM ESD levels are shown in Tables I and II, respectively. The power-rail ESD clamp circuit is used in the VDD and VSS cells. The failure criterion is defined as the voltage changes at ±1μA greater than ±30% after ESD stress. The HBM and MM ESD levels of power-rail ESD clamp circuit are shown in Table III. From the experimental results, the HBM ESD levels of all cells are greater than 8kV, and the minimum MM ESD level is 750V.

Tables IV and V show the HBM and MM ESD levels of the input/output cells without power-rail ESD clamp circuit in the VDD and VSS cells, respectively. The minimum HBM ESD level of the input/output cells is 4kV, and the minimum MM ESD level is 500V. Compared the measured results to Tables I and II, the power-rail ESD clamp circuit design used in VDD and VSS cells will enhance the ESD immunity of the input/output cells and achieve the whole-chip ESD protection.

4. Conclusion

ESD protection design for SSTL I/O interface in DDR2 SDRAM memory has been successfully verified in a 0.25-μm salicided CMOS process. The HBM ESD levels of all cells are greater than 8kV, and the minimum MM ESD level is 750V. The proposed ESD protection design for SSTL_18 interface has the advantage of small layout area, high ESD robustness, small parasitic capacitance, and no latch-up issue. Based on the proposed ESD protection design, one set of area-efficient SSTL_18 I/O cell library has been built up in a 0.25-μm salicided CMOS process for IP-reuse applications.

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