

Improve Latch-up Immunity by Circuit Solution

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Abstract- A concept of active guard ring and its corresponding circuit solution to enhance the latch-up immunity of integrated circuits (IC) are proposed and verified in a 0.6- μm 5-V CMOS process. By detecting the over-shooting/under-shooting trigger current during latchup current test (I-test), some compensation current generated from on-chip ESD PMOS or NMOS devices through special circuit design can effectively reduce the latchup trigger current that injecting into the core circuit blocks. Therefore, the latchup immunity of I-test with positive or negative trigger current applied at the I/O pins can be significantly improved.

I. INTRODUCTION

To avoid the possible short-circuit threat brought by the inherent parasitic PNP paths existing in CMOS chips, the IC products need to be implemented without suffering the related latchup failure and passed the qualification tests defined in the JEDEC standards. According to the newest standard [1], the highest latch-up level with I-test has been updated to be greater than 200mA from the earlier original spec. of only 100mA. Therefore, many companies promote their IC products against latchup with over 200-mA I-test as the target specification.

To increase the latch-up immunity of CMOS chips, several methods such as the guard rings [2]-[4] or trench structure [5], [6] have been developed and implemented in the IC products. Although the latch-up immunity can be increased by adopting those prior arts, to depress the fabrication cost against latchup failure are still requested by the IC industry. Some circuit solutions were ever reported to increase latchup immunity of CMOS ICs [7], [8]. Fig. 1 shows the prior art with the latch-up current self-stop circuit. The circuit contains a PMOS switch MP1, a diode-connected NMOS MN1 as well as its current mirror pair MN2, and the circuit (INV1 and R1) to bias the gate of the MP1. Once the current flow to the ground becomes abnormally large due to the happening of latchup, it is detected by the MN1/MN2, and the MOS switch MP1 is turned off to disturb the current path from the power line to the internal SCR structure. Thus, the latch-up state can be released after the trigger is over. Fig. 2 shows the patented latch-up recovery circuit. Similar with the concept in Fig. 1, the prior art in Fig. 2 detects the latch-up occurrence and shuts down the path to both power and ground. By disturbing the path and also the latch-up status, the prior art also shows the enhancement of the latchup immunity. However, the MOS switches are requested at the prior arts, which may take some area to implement the switch with acceptable transient/steady state voltage drops and the power loss. Besides, if other internal powers are required, especially the high voltage supply, additional design may be also required to reduce the effect of external latch-up triggers toward the inherent sensitive PNP paths which are connected to different internal powers.

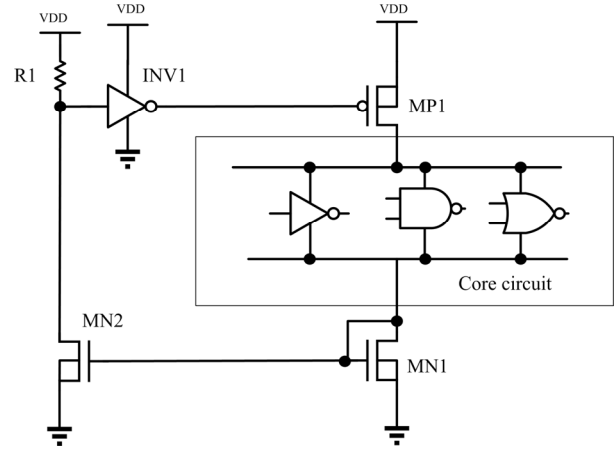


Fig. 1. Prior art with latch-up current self-stop circuit [7]

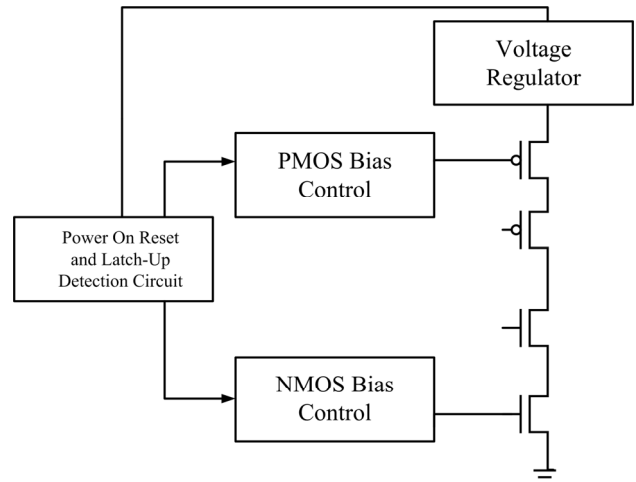


Fig. 2. Prior art with latch-up recovery circuit [8]

In this work, a novel circuit solution called as “active guard ring” is proposed to provide an useful solution to significantly enhance the latch-up immunity of CMOS IC products.

II. ACTIVE GUARD RING

A. Concept and Circuit Implementation

Fig. 3 shows the “active guard ring” concept proposed in this work against the injecting current that triggers latchup at the internal circuits when latchup I-test is applied at the I/O pad [9]. Besides of the traditional prevention method with guard ring to surround the I/O buffer (or ESD protection transistors) at the I/O pad, the proposed active guard ring with the adopted circuits actively provides extra sink or compensation currents (I_{sink} and I_{comp}) corresponding to the positive or negative latchup I-test, respectively.

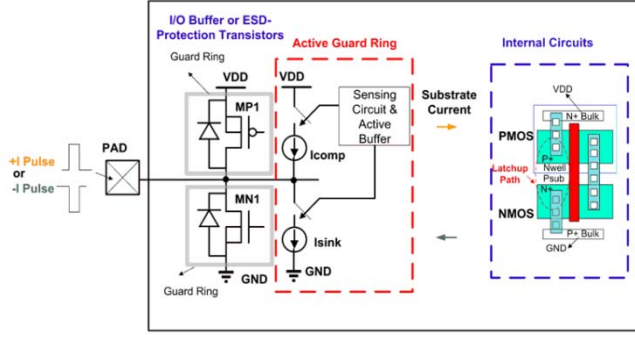


Fig. 3. Concept of “active guard ring” designed to depress the injecting current to the internal circuits during latch-up I-tests.

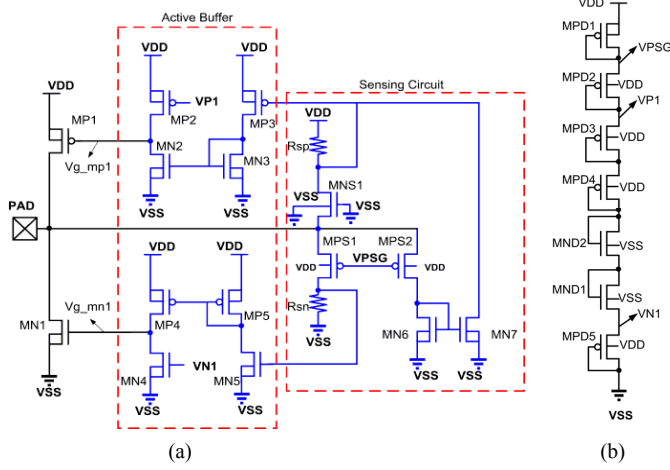


Fig. 4. (a) Circuit implementation for the concept of active guard ring, and (b) the diode-connected MOS string that generates the bias voltages for VP1, VN1, and VPSG used in the active guard ring.

The structure for active guard ring is composed of a sensing circuit block and an active buffer. The sensing circuit block is used to monitor whether the positive or negative latchup trigger current is applied. The active buffer will then control the gate voltages of the large-dimension ESD devices to keep them off at normal circuit operating condition, but to generate the corresponding sink or compensation current during latchup triggering events. The circuit implementation to realize the concept of active guard ring is shown in Fig. 4 (a). The MP1 and MN1 are the ESD devices. The sensing circuit block contains MPS1, MNS1, RSN, and RSP to detect the trigger current pulse. In addition, The MPS2, MN6, and MN7 are also used in the sensing circuit block to transmit the detection information to the active buffer. Devices MP2, MP3, MN2, and MN3 in the active buffer shown in Fig. 4(a) receive the information and turn into the force for gate control of MP1. Besides, the MP4, MP5, MN4, and MN5 are adopted to drive the gate terminal of MN1. The circuit which contains the MPD1~MPD5 and MND1~MND2 to generate related bias voltages (VP1, VN1, and VPSG) is shown in Fig. 4 (b). Since the VPSG is slightly smaller than VDD, if the PAD voltage is over VDD and large enough when the positive latchup trigger pulse is applied, related channel currents will occur at MPS1 and MPS2. The transistor MN5 and MP3 are thus turn on and transmit the current to MN3 and MP5. Through

the current mirror pair (MN3 and MN2), the gate terminal of MP1 will be pulled low to generate corresponding source-to-drain current (I_{sd_mp1}) if the mirrored current is larger enough compared with the current at MP2. Besides, the MN5 is also turned on with sufficient channel current at MPS1. The channel current in MN5 will induce the force to pull high the gate terminal of MN1 by the current mirror pair MP5 and MP4. The drain-to-source current (I_{ds_mn1}) is thus generated if the gate voltage of MN1 is large enough. With the corresponding compensation current (I_{sd_mp1} or I_{ds_mn1}), the induced substrate current toward the internal circuits will be decreased corresponding to the same external triggers, therefore the latchup immunity will be improved.

In the negative I-test, the PAD voltage is decreased to the value lower than Vss and turn on the MNS1 if sufficient trigger is applied. With the induced voltage difference across the resistor Rsp, transistor MP3 is turned on to generate the corresponding currents in transistor MP3, MN3, and MN2. The transistor MP1 will also be turned on if its source-to-gate voltage is sufficiently high. It can be achieved if the current flow in MN2 is much larger than the current flow from MP2. Related source-to-drain current of MP1 (I_{sd_mp1}) is then generated to compensate the trigger current at the pad. Thus, the perturbation to the internal circuits is reduced and the robustness against latchup for negative I-test is also increased.

B. Simulation

The simulations for the proposed “active guard ring” are done by doing a dc sweep at the PAD voltage from -1 V to 6 V under room temperature with 5-V supply voltage (VDD). The simulated waveforms for V_{g_mp1} , V_{g_mn1} , I_{sd_mp1} , and I_{ds_mn1} are shown in Fig. 5. The sink currents are generated as I_{sd_mp1} of -65 mA and I_{ds_mn1} of 200 mA under the pad voltage of 5.73 V, respectively. When the PAD voltage pulls low to beneath -0.63 V, I_{sd_mp1} of 194mA is induced as shown in Fig. 5. Those compensation current (I_{ds_mn1} and I_{sd_mp1}) can reduce the overshooting/undershooting PAD voltage against the applied positive/negative latchup test currents.

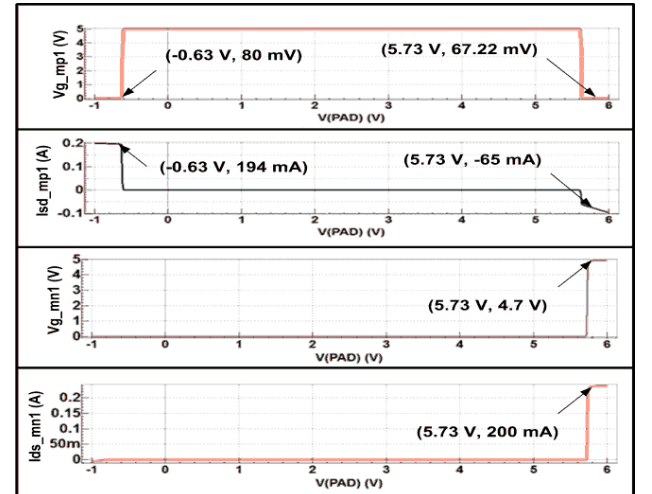


Fig. 5. Simulated waveforms of certain voltages and currents in this work with 5-V VDD supply voltage, under room temperature and dc sweep at the PAD voltage from -1 V to 6 V.

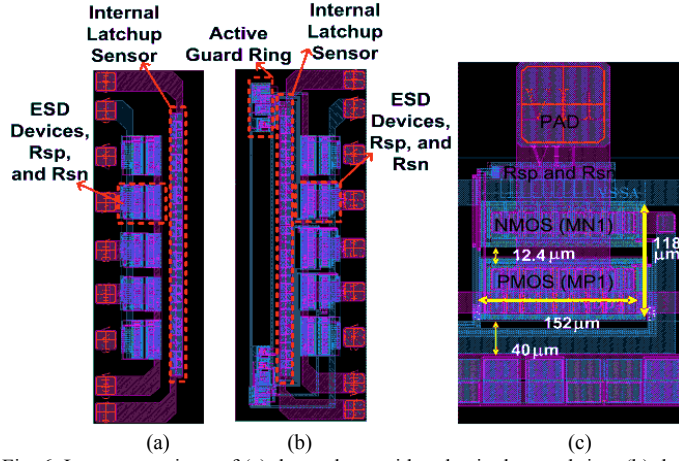


Fig. 6. Layout top views of (a) the testkeys with only single guard ring, (b) the testkeys with proposed active guard ring, and (c) the enlarged graph for the ESD devices and related resistors (Rsp and Rsn) of the testkey.

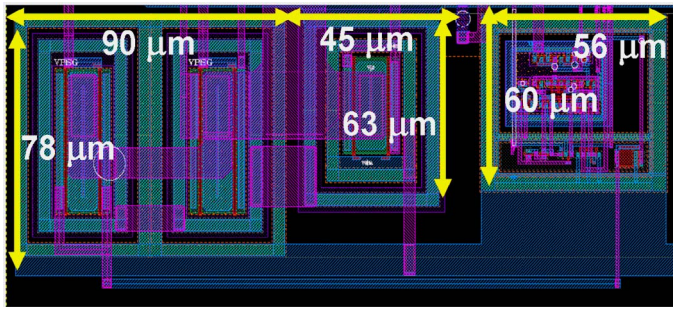


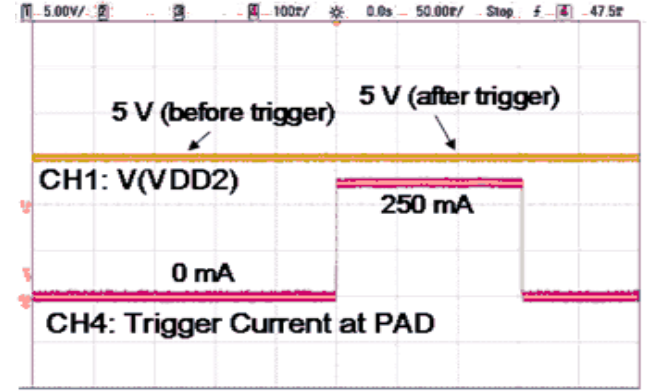
Fig. 7. Enlarged layout graph for the circuit solution of active guard ring.

III. EXPERIMENTAL RESULTS

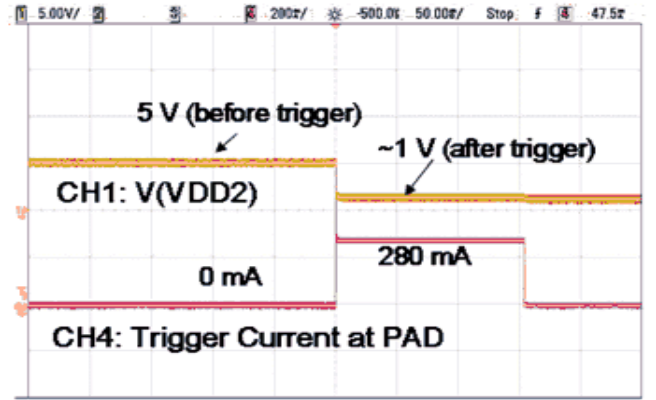
The test structure to verify latchup immunity of the traditional and the new proposed designs in a 0.6-μm 5-V CMOS process is referred to [2] with the internal latch-up sensor and the corresponding testkeys. The layout top views of the test chip and the enlarged graph for the ESD devices and the circuit to realize the active guard ring are shown in Fig. 6(a) to (c) and Fig. 7. The area for the ESD devices in Fig. 6 are $152\mu\text{m} \times 118\mu\text{m}$ and same for both of the proposed design and the traditional design with single guard ring. The distances from the bulk terminals of MP1 to the internal PNP cell and the bulk terminal of MN1 are $40\mu\text{m}$ and $12.4\mu\text{m}$, respectively. The enlarged layout graphs for the circuit solution of active guard ring is shown in Fig. 7. The total dimension is only 0.0132 mm^2 ($= 90\mu\text{m} \times 78\mu\text{m} + 45\mu\text{m} \times 63\mu\text{m} + 56\mu\text{m} \times 60\mu\text{m}$).

By connecting the power pin (VDD2) of the latch-up sensor with a 100-ohm resistor to 5-V DC supply, the latch-up event can be observed by acquiring the voltage drop happening when the external trigger currents are applied. The measured waveforms under the positive I-test to the test chip with 250-mA and 280-mA trigger currents are shown in Fig. 8(a) and (b), respectively. Besides, the measured waveforms of the proposed design are shown in Fig. 9(a) and (b) under -400-mA and -470-mA trigger current, respectively. Since the VDD2 is kept at 5 V in Fig. 8(a) and Fig. 9(a), no latchup occurring at the PNP sensor cells when the 250mA or -400mA trigger current

is applied to the input pad. As seen in Fig. 8(b) or Fig. 9(b), the VDD2 is dropped to $\sim 1\text{ V}$ to show latchup occurrence after the 280-mA or -470-mA trigger current is applied to the input pad. The latch-up test results on the testkeys with the traditional and the new proposed designs are listed in Table I. From the experiment results, the proposed work of active guard ring can significantly increase the latchup I-test levels.



(a)

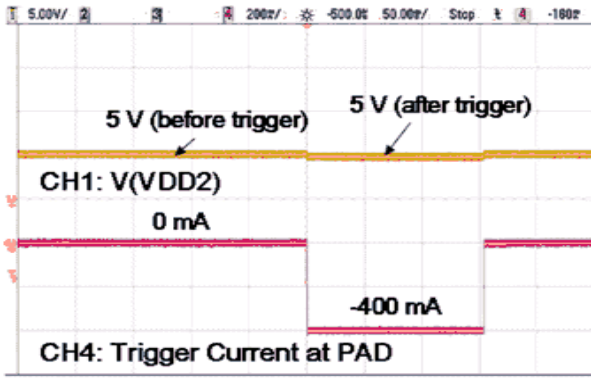


(b)

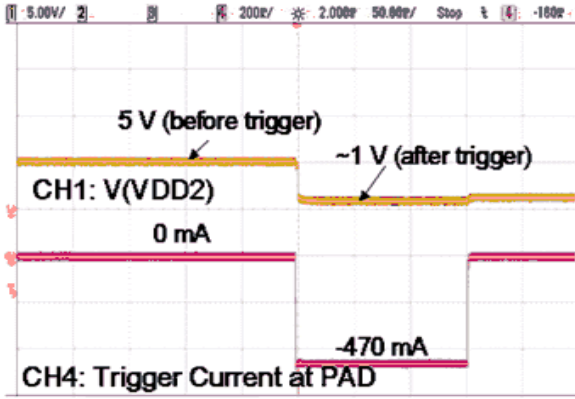
Fig. 8. Measured waveforms of the proposed work with active guard ring under (a) 250-mA, and (b) 280-mA, trigger current applied at the input PAD for positive I-test.

IV. APPLICATION TO OUTPUT BUFFER

In this work, the proposed active guard ring is realized with ESD devices of large-dimension MP1 and MN1. Theoretically, the I/O devices of output buffer can be also adopted to implement the MN1 and MP1 with some modification at the gate control of the logic block. Such application concept is depicted in Fig. 10 with a simplified example. The “and” logic can be used to connect between the V_{g_mp1} of the active buffer and the original gate control circuit for the PMOS transistor of the output driver. Besides, the “or” logic can be added between the V_{g_mn1} of the active buffer and the original gate control circuit for the NMOS transistor of the output driver. The schematic of active buffer can refer to Fig. 4(a). With modification as indicated in Fig. 10, the active guard ring structure can be also applied to the output transistors in the output buffer to improve latchup immunity.



(a)



(b)

Fig. 9. Measured waveforms of the proposed work with active guard ring under (a) -400-mA and (b) -470-mA trigger current applied at the input PAD for negative I-test.

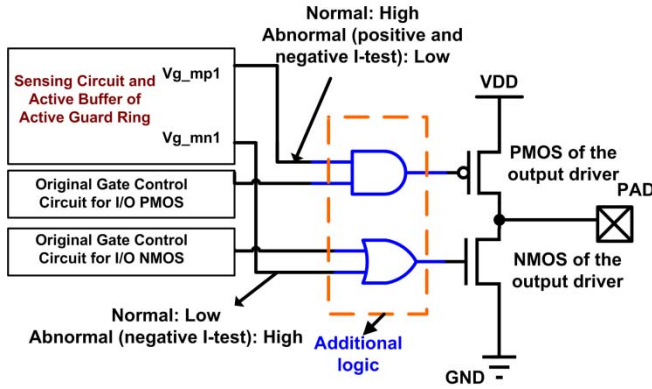


Fig. 10. Circuit block to control the gates of PMOS and NMOS in the output buffer co-designed with the circuit of “active guard ring”.

Table I
RESULTS FOR LATCHUP I-TEST

Latchup I-test	Test Cell with the Traditional Guard Ring		Test Cell with the Proposed Active Guard Ring	
	Pass	Fail	Pass	Fail
Positive I-test	5 mA	10 mA	260 mA	270 mA
Negative I-test	-190 mA	-200 mA	-430 mA	-440 mA

V. CONCLUSION

The proposed design of “active guard ring” has been fabricated and successfully verified in a 0.6- μm 5-V CMOS process. By adopting additional circuit and active buffer to turn on the ESD protection transistors, the large-dimension ESD (or I/O) devices can effectively turned on to generate extra compensation current to the negative or positive current triggers during the latch-up I-test. The new proposed solution shows much higher latch-up resistance, compared with the traditional prevention method with single guard ring. Since the proposed design of “active guard ring” is based on the MOS transistors instead of the parasitic devices, the circuit simulation can be used for the sizing determination and performance estimation. From the experimental results, the test chip with the proposed design can achieve 260-mA and -430-mA immunity against positive and negative latchup I-test, respectively.

ACKNOWLEDGMENT

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