A NEW ON–CHIP ESD PROTECTION CIRCUIT WITH DUAL PARASITIC SCR STRUCTURES FOR CMOS VLSI

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ABSTRACT:

A new CMOS on–chip ESD protection circuit which consists of dual parasitic SCR structures is proposed. Experimental results show that it can successfully perform negative and positive ESD protection with failure thresholds greater than ±1KV and ±10KV in machine–mode(MM) and human–body–mode (HBM) testing, respectively. Moreover, low triggering voltages in both SCRs can be readily achieved without involving device or junction breakdown.

I.INTRODUCTION

Due to its high current sinking/sourcing capability, the SCR device becomes one of the effective elements in electrostatic discharge(ESD) protection. Recently, the parasitic lateral SCR has been used in CMOS on–chip ESD protection circuits for single–polarity ESD input[1]–[3] rather than double–polarity inputs. The triggering voltage is as high as 50V[1]–[2] or may be lowered by incorporating a low–breakdown–voltage short–channel NMOSFET[3]. Based upon the understanding of CMOS transient latchup[4]–[5], a new double–polarity ESD protection circuit using dual SCR structures with low triggering voltages is proposed. It has been designed, fabricated, and tested. The experimental results show that it can perform very effective ESD protection with a small layout area.

II. PROTECTION CIRCUIT

A. circuit configuration:

The new protection circuit against ESD is shown in Fig.1(a) and its cross–sectional view is given in Fig.1(b) . The circuit consists of a parasitic lateral pnp transistor Q1(Q3) and a parasitic vertical npn transistor Q2(Q4) to form the upper(lower) lateral SCR structure against negative(positive) ESD pulses. Besides, a parasitic field–oxide NMOS(PMOS) Mn(Mp) with a threshold voltage greater than 40V is used to further enhance the turn–on speed of the lateral SCR during negative(positive) ESD transitions. The two–terminal protection circuit can be arranged around each I/O pad. Its fabrication process is fully compatible with that of the conventional CMOS.

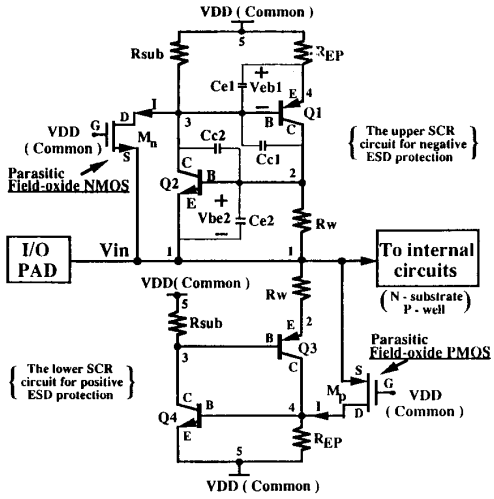

Fig.1(a) : The protection circuit for positive and negative ESD pulses.

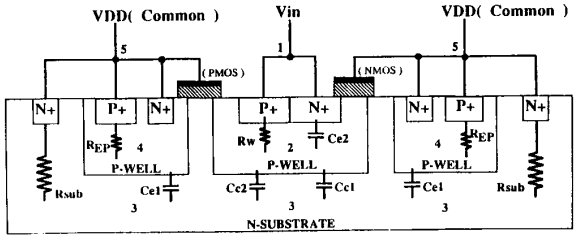

Fig.1(b) : The cross–sectional view of the ESD protection circuit.

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B. circuit operations and design concepts:

When a negative ESD pulse greater than certain threshold voltage occurs at the I/O pad, the upper SCR structure in Fig.1(a) is quickly triggered on by the transient currents generated by the junction capacitances Cc1 and Cc2 in Q1 and Q2, respectively. Thus a low–impedance path through the p–n–p–n structure is formed between VDD and Vin nodes. The triggering voltage can be adjusted through the design of the ratio between Ce1(Ce2) and Cc1+Cc2. The larger the value of Cc1+Cc2, the greater the voltage drops on Ce1 and Ce2 to forward bias the transistors Q1 and Q2 during the occurrence of negative ESD pulses. This leads to a lower triggering voltage. After the negative ESD pulse, Q1 and Q2 have to turn off. This can be achieved by designing a smaller P–well resistance Rw and a N–substrate resistance Rsub. Theoretical models have been developed to design the above mentioned capacitances and resistances[6].

When a positive ESD pulse occurs at the I/O pad, Vin becomes greater than VDD(common)+0.6V and the transistor Q3 quickly turns on because its base is the N–substrate biased at VDD(common). Then the collector current of Q3 flowing into the P–well causes a voltage drop on R_{EP} and the emitter junction of the transistor Q4 becomes forward biased. So the lower SCR is triggered to its ON state and the positive ESD energy is quickly discharged through its low–impedance path. After the positive ESD pulse, both Q3 and Q4 turn off. The speed of turning on the lower SCR can be enhanced through the increasing the beta–gain product of transistors Q3 and Q4 and the resistance R_{EP}.

C. circuit simulation

Fig.2 shows the SPICE simulation results of the suitably designed upper SCR circuit for negative ESD protection. It is shown that a negative 5–volt pulse is enough to turn on the SCR. Thus, the low triggering voltage can be achieved through appropriate circuit design without involving device or junction breakdown. After the negative pulse, the SCR turns off quickly because the base–emitter voltages of Q1 and Q2 quickly drop to zero. Figs.3(a) and 3(b) show the SPICE simulation results of both SCR circuits under positive and negative human–body–mode ESD pulses with the ESD voltage of +1000 and –1000 volts, respectively. The curves show that the ESD energy can be quickly bypassed through the SCR circuits around I/O pads and the internal circuits of the chip can be protected.

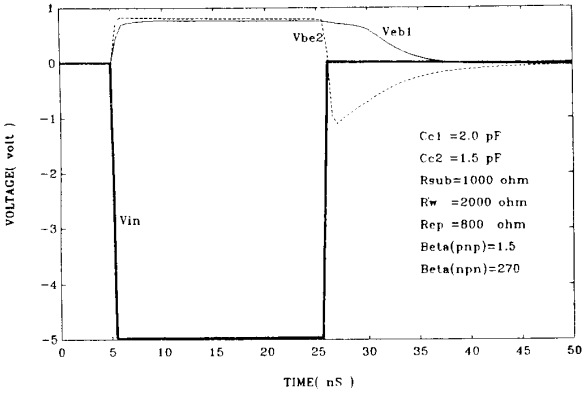


Fig.2 : SPICE simulation results of the upper SCR circuit in Fig.1(a) under a 5V negative transition.

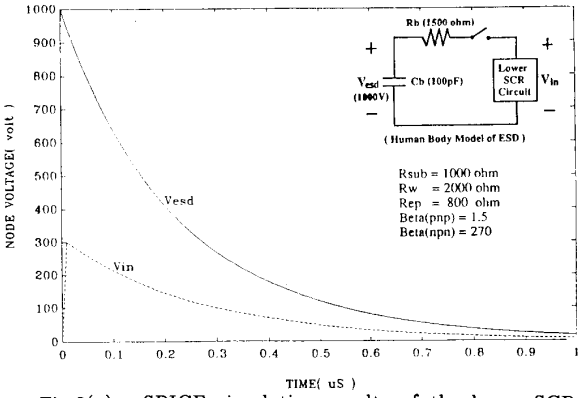


Fig.3(a) : SPICE simulation results of the lower SCR circuit under a positive HBM ESD pulse(+1000V).

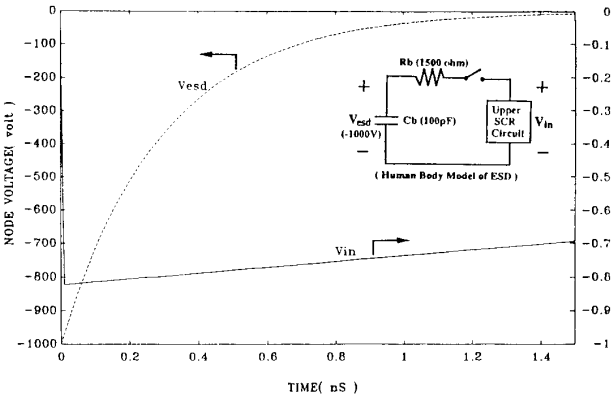


Fig.3(b) : SPICE simulation results of the upper SCR circuit under a negative HBM ESD pulse(–1000V).

III. EXPERIMENTAL RESULTS

One set of such new dual SCR ESD protection circuits with different layout dimensions has been implemented by using the 1.0μm p–well bulk CMOS process. The chip photomicrograph of one of the fabricated circuits is shown in Fig.4. The testing results of ESD failure threshold under different layout dimensions are listed in Table I. The results definitely show that failure thresholds can be greater than $\pm$1KV and $\pm$10KV in machine–mode and human–body–mode testing, respectively, for the new ESD protection circuit with a layout area as small as 8800μm^2. This successfully verifies the ESD protection capability of the proposed circuit.

The measured dc I–V characteristic of the upper SCR in the fabricated protection circuit is shown in Fig.5, where the dc triggering voltage is about 28.1V and the holding voltage is about 1.5V with 6Ω turn–on resistance. The test structure to measure the ac pulse–type triggering voltage of the upper SCR is illustrated in Fig.6. The VDD node is connected in series with the resistor R=1KΩ which is biased at 5V, and the output of the pulse generator is connected to the I/O pad. The applied pulse–type voltage generated from the pulse generator has a fixed maximum voltage of +5V and a tunable negative voltage level. When a $\pm$5V square–pulse voltage is applied, the upper SCR in the DUT block is still off so that the voltage waveform at the oscilloscope channel CH2 remain unchanged at +5V as shown in Fig.7(a). This guarantees that the upper SCR is never triggered to turn on by the normal chip input signals as the lower SCR is. When the negative level of the applied square–pulse voltage decreases to –16V, the upper SCR of the fabricated protection circuit is triggered on and the voltage at the common node(CH2) decreases from +5V to –14.5V as shown in Fig.7(b). As expected, this ac pulse–type triggering voltage is lower than its dc triggering voltage.

The measured dc and ac pulse–type triggering voltage of the fabricated upper SCR in various ESD protection circuits with different layout dimensions are listed in Table II. These measured results confirm that the low triggering voltage in the upper SCR of the proposed protection circuit can be readily achieved through suitable layout design. Moreover. this low triggering voltage does not affect the normal circuit operations.

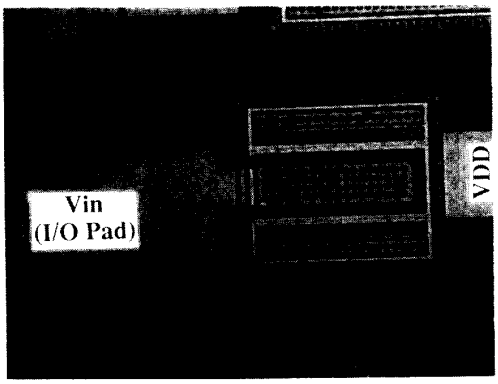


Fig.4 : The chip photomicrograph of the ESD protection circuit.

TABLE I

ESD failure threshold Voltage		Layout area of the fabricated ESD circuits (width x length , unit : um x um)				
		88x25	88x50	88x100	100x100	164x100
	Machine mode (MM) + -	150V	500V	>1000V	>1000V	>1000V
	Human body mode (HBM) + -	1800V	5500V	>10KV	>10KV	>10KV

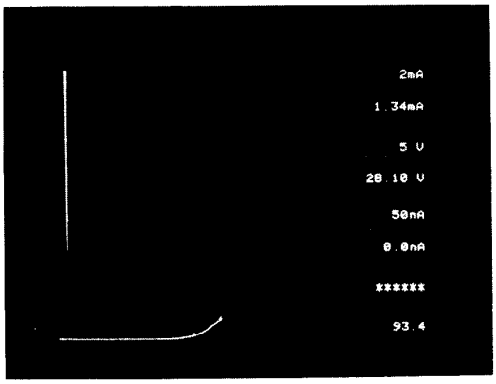


Fig.5 : The dc I–V characteristic of the upper SCR in the fabricated ESD protection circuit with 88×100 μm^2 layout area.

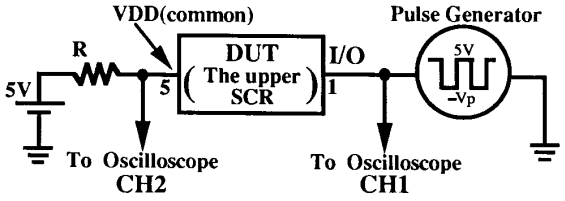
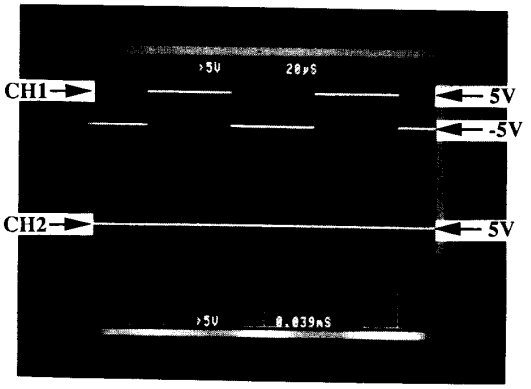
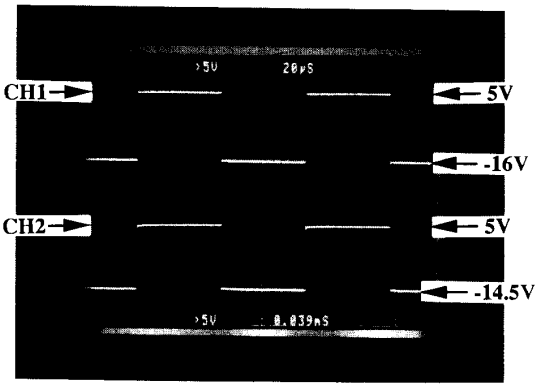


Fig.6 : Illustration of the method to measure the ac pulse–type triggering voltage of the fabricated ESD protection circuits.



7(a)



7(b)

Fig.7(a) & 7(b) : The voltage waveforms of measuring the ac pulse–type triggering voltage. CH1 is the applied square–pulse voltage. CH2 is the voltage at the VDD(common) node of the ESD protection circuit.

IV. CONCLUSION

A new on–chip CMOS ESD protection circuit with dual SCR structures has been successfully designed and fabricated. The testing results show that it can effectively perform the ESD protection with a small layout area. Moreover, the low triggering voltage of the protection circuit can also be achieved through the proper circuit design.

TABLE II

		Layout area of the fabricated ESD circuits (width x length , unit : um x um)				
		88x25	88x50	88x100	100x100	164x100
Triggering (turn-on) Voltage	DC condition	30.3V	27.6V	28.1V	44.7V	44.1V
	AC pulse-type condition	22.0V	20.3V	21.0V	31.7V	31.2V

REFERENCE

[1] R.N. Rountree, C. Duvvury, T. Maki, and H. Stiegler, " A Process–Tolerant Input Protection Circuit for Advanced CMOS Processes," in 1988 EOS/ESD Symp. Proc., vol. EOS–10, pp.201–205, 1988.

[2] R.N. Rountree, " ESD Protection for Submicron CMOS Circuits : Issues and Solutions," in IEDM Tech. Dig., pp.580–583, 1988.

[3] A. Chatterjee and T. Polgreen, " A Low–Voltage Triggering SCR for On–Chip ESD Protection at Output and Input Pads," in Proc. 1990 Symposium on VLSI Technology, pp.75–76, 1990.

[4] Chung–Yu Wu, Y.–H. Yang, et. al. " A New Approach to Model CMOS Latchup," IEEE Trans. Elec. Dev. Vol. ED–32, pp.1642–1653, Sept. 1985.

[5] Y.–H. Yang, Chung–Yu Wu, " A New Criterion for Transient Latchup Analysis in Bulk CMOS," IEEE Trans. Elec. Dev., Vol. ED–36, pp.1336–1347, July 1989.

[6] Chung–Yu Wu, Ming–Dou Ker, et. al. " A New Analytical Criterion for CMOS Transient Latchup," in Proc. 1990 International Electron Devices and Materials Symposium, Taiwan, R.O.C.,pp.18–21, 1990.