AN ON–CHIP ESD PROTECTION CIRCUIT WITH COMPLEMENTARY SCR STRUCTURES FOR SUBMICRON CMOS ICs

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Abstract —— A new on–chip ESD protection circuit with complementary SCR structures is proposed. This circuit can provide ESD protection above ±6500V and ±400V in human–body–mode and machine–mode ESD stresses, respectively, with the total layout area of 108μm × 242μm including the latchup guard–ring of 10–μm width and a 90μm × 90μm metal pad for wire bonding.

I. INTRODUCTION

Electrostatic discharge (ESD) is one of the major reliability problems in CMOS ICs, especially in the submicron CMOS technology. The LDD process and silicided diffusion in the advanced submicron CMOS technologies much degrade the ESD robustness of CMOS ICs [1]. Recently, the lateral SCR device has been used in the submicron CMOS ICs to improve ESD immunity [2]–[3]. But, the ESD voltage may have positive or negative polarities to both VDD and VSS nodes at each pad of a CMOS IC. Thus, an efficient ESD protection circuit should have effective discharging paths to bypass the four different ESD stresses [4].

In this paper, an on–chip ESD protection circuit with four different ESD discharging paths is proposed [5], which consists of two lateral SCR devices and two junction diodes in the complementary style. The complementary SCR structures can be designed with low ESD–trigger voltage to perform effective ESD protection. Thus, this ESD protection circuit can perform high–failure–threshold ESD protection in a small layout area for high–density applications in submicron CMOS VLSI/ULSI.

II. COMPLEMENTARY–SCR ESD PROTECTION CIRCUIT

The schematic cross–sectional view of the proposed ESD protection circuit is shown in Fig.1(a), where the n–substrate p–well CMOS process is used to demonstrate the complementary SCR structures. They can also be implemented in p–substrate n–well or twin–well CMOS processes as well if appropriate modifications are made. The corresponding lumped equivalent circuit of the complementary SCR structures is shown in Fig.1(b). There are two lateral SCR structures and two diodes in this complementary –SCR ESD protection circuit. The SCR1 device is arranged between VDD node and the I/O pad with its anode connected to VDD node, and the SCR2 device is arranged between the I/O pad and VSS(GND) node with its anode connected to I/O pad. The SCR1 (SCR2) device is basically formed by the parasitic lateral p–n–p bipolar junction transistor (BJT) Q1 (Q3) and the parasitic vertical n–p–n BJT Q2 (Q4). Q1 and Q3 are the parasitic lateral p–well/ n–substrate/p–well BJT devices whereas Q2 and Q4 are the parasitic vertical N+ diffusion/p–well/n– substrate BJT devices.

The two diodes, D1 and D2, are merged into the base–emitter junctions of the BJTs Q2 and Q3 to save the layout area and also to offer a voltage–clamping effect on the input/output signals. The diode D1 is formed by a N+ diffusion in a p–well, whereas the diode D2 is formed by a p–well in the n–substrate.

The parasitic device resistances and capacitances in the complementary SCR structures are also shown in Figs.1(a) and 1(b). Rw1, Rw2, Rw3, and Rw4 represent the inherent p–well resistances. Rsub1 and Rsub2 are the substrate resistances. Ce1, Cc1+Cc2, Ce3, and Cc3+Cc4 are the p–well/n–substrate junction capacitances. Ce2 and Ce4 are the N+ diffusion/p–well junction capacitances. The device capacitances have important effects to lower the ESD–trigger voltage of the lateral SCR device.

The SCR1 (D1) device is designed to be turned on when an ESD stress occurs at the I/O pad with negative (positive) polarity to VDD node, whereas the SCR2 (D2) device is turned on when an ESD stress with positive (negative) polarity to VSS node.

The equivalent circuit of VDD–to–VSS latchup path in Fig.1(a) is shown in Fig.2, and the emitter–shorting method is used to reduce the shunt resistances Rsub1 and Rw4 so as to overcome the VDD–to–VSS latchup problem. Reducing the Rsub1 and Rw4 also

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reduces the latching capability of the lateral SCR1 and SCR2 devices in Figs.1(a) & 1(b). The latching capability of the SCR1 and SCR2 can be further improved by scaling down the p—well to p—well spacings of the lateral BJTs Q1 and Q3 in the lateral SCR1 and SCR2 devices, respectively. To experimentally investigate the effect of p—well to p—well spacing on the SCR1 and SCR2 devices, this spacing varies from 1.2μm to 3.0μm in the test chip.

III. Experimental Results

A microphotograph of the complementary—SCR ESD protection circuit with the layout of interdigital—finger style is shown in Fig.3, which is fabricated by a 0.6—μm twin—well n—substrate CMOS SRAM technology with LDD process. The layout area of SCR1 and D1 is 108μm × 44μm. The layout area of SCR2 and D2 is 108μm × 76μm, which includes the surrounding N+ diffusion latchup guard ring with the ring width of 10 μm.

With the emitter—shorting method and the 10—μm latchup guard ring, the dc I—V characteristics of the VDD—to—VSS latchup path in the fabricated complementary—SCR ESD protection circuit is shown in Fig.4, where its dc holding voltage is as high as 17.5V. Thus, this proposed ESD protection circuit can be free of VDD—to—VSS latchup problem under the 5—V VDD power supply. Fig.5 shows a photograph of the I—V curve of the lateral SCR device in the fabricated ESD protection circuit. The dc switching characteristics of the lateral SCR device are shown in Fig.6 with the variation of different p—well to p—well spacings. The pulse—type trigger voltage of the lateral SCR device is shown in Fig.7. The turn—on (ESD—trigger) voltage is around 9—11 V, so that it can protect the gate oxide of 150Å in the 0.6—μm CMOS ICs.

The ESD testing results of this proposed ESD protection circuit under the human—body—mode (HBM) and machine—mode (MM) ESD stresses are shown in Figs.8(a) and 8(b), respectively, with different p—well to p—well spacings. As the p—well to p—well spacing is reduced to 1.8μm, the complementary—SCR ESD protection circuit can sustain above ±6500V HBM and ±400V MM ESD stresses in a small active area.

High—frequency operation of input signals on the input pad with the proposed complementary—SCR ESD protection circuit has been verified by a voltage pulse string with the rise time around 200pS generated by HP8131A 500MHz pulse generator. The voltage pulse with sharp rise time of 200pS does not trigger on the SCR1 and SCR2 devices in the fabricated ESD protection circuit because the high/low voltage level is clamped by the diodes D1 and D2. Failure analysis on this fabricated ESD protection circuit has also been done to further improve its ESD protection capability.

IV. Conclusion

A robust ESD protection circuit with complementary SCR structures and junction diodes has been designed and fabricated by 0.6—μm CMOS SRAM technology. Using the emitter—shorting method, this proposed complementary—SCR ESD protection circuit can be free of VDD—to—VSS latchup problem under 5—V VDD operation. To compensate the degradation on the latchup capability of the lateral SCR devices in the ESD protection circuit caused by the emitter—shorting method, the p—well to p—well spacing of the lateral BJTs in the lateral SCR devices is reduced to lower the trigger—on voltage and to enhance their turn—on speed of positive—feedback regenerative process in the lateral SCR devices. The experimental results show that the fabricated ESD protection circuit with p—well to p—well spacing from 1.4 to 1.8 μm can sustain above ± 6500V human—body —mode ESD and ± 400V machine—mode ESD stresses with the total layout area of 108μm × 242 μm. The diodes D1 and D2 in the ESD protection circuit also offer voltage clamping effect on input or output signals when the CMOS ICs are in their normal operation conditions with 5—V VDD power supply.

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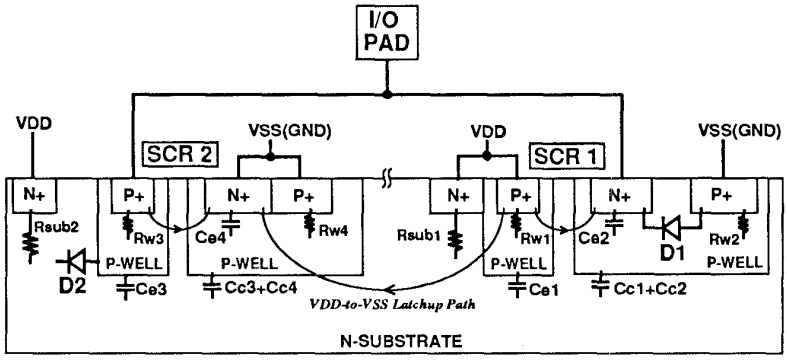

Fig.1(a) The schematic cross-sectional view of the complementary-SCR ESD protection circuit.

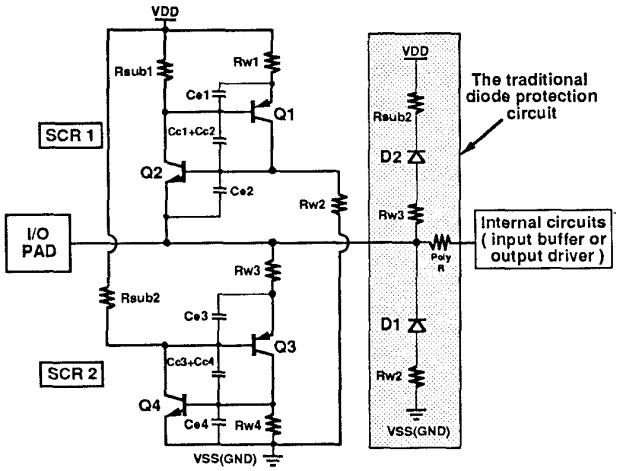

Fig.1(b) The proposed complementary-SCR ESD protection circuit.

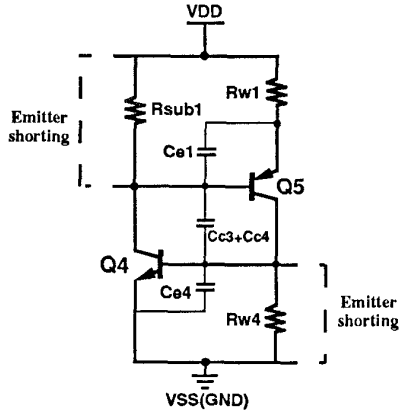

Fig.2 The lumped equivalent circuit of VDD-to-VSS latchup path in Fig.1(a).

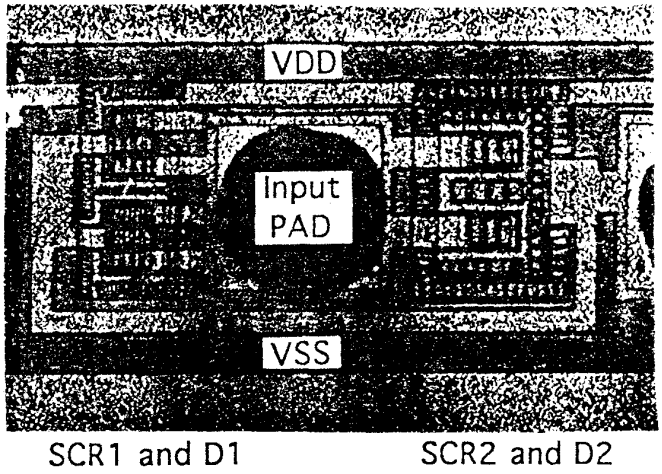

Fig.3 A microphotograph of the complementary-SCR ESD protection circuit fabricated by a 0.6-μm CMOS SRAM process.

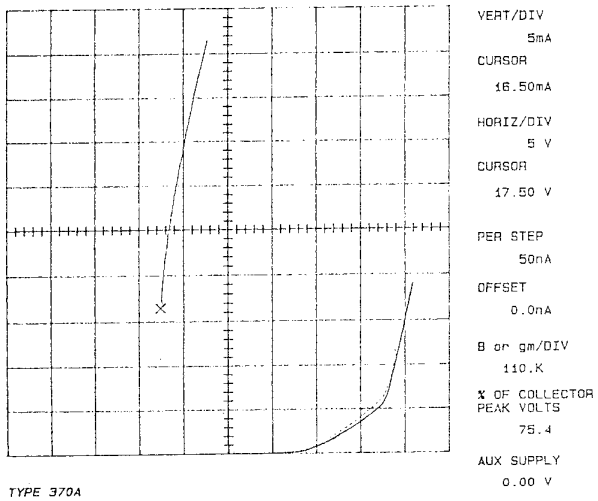

Fig.4 The measured dc I–V characteristics of the VDD-to-VSS latchup path in the fabricated complementary–SCR ESD protection circuit with emitter–shorting method and latchup guardring.

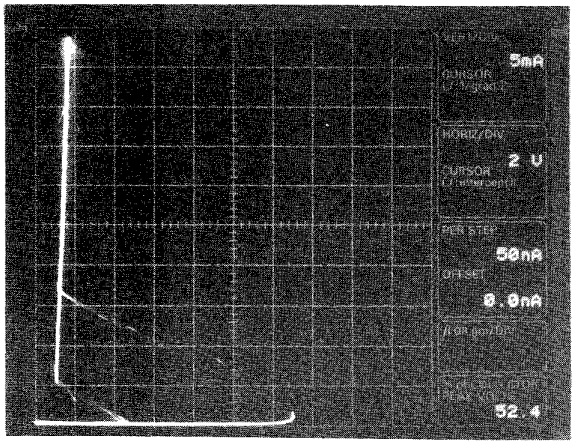

Fig.5 The I–V curve of the lateral SCR device in the fabricated complementary–SCR ESD protection circuit.

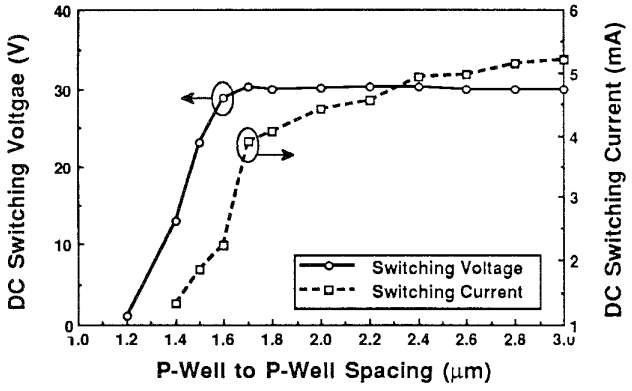

Fig.6 The dc switching characteristics of the lateral SCR device under the variation of p-well to p-well spacings.

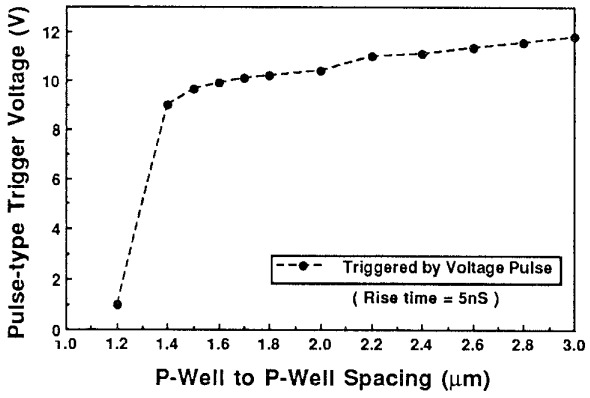

Fig.7 The pulse–type trigger voltage of the lateral SCR device tested by a voltage pulse of 5–nS rise time under the variation of p-well to p-well spacings.

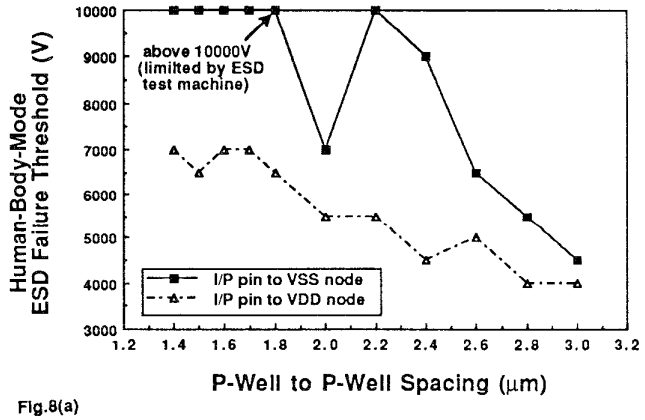

Fig.8(a)

The HBM ESD testing results of the fabricated complementary–SCR ESD protection circuit with the variation of p-well to p-well spacings.

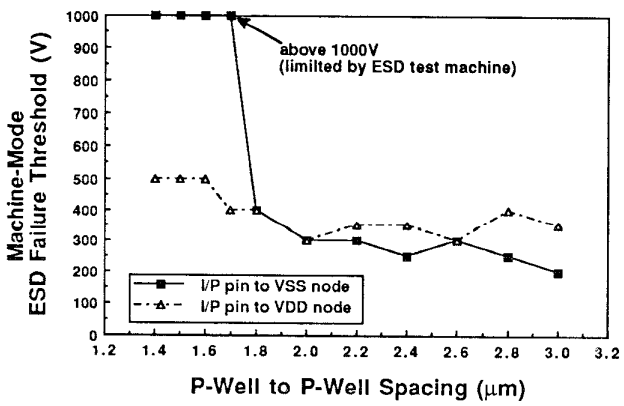

Fig.8(b)

The MM ESD testing results of the fabricated complementary–SCR ESD protection circuit with the variation of p-well to p-well spacings.