Whole-Chip ESD Protection for CMOS VLSI/ULSI With Multiple Power Pins

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Abstract — An anomalous phenomenon of ESD failure in CMOS ICs with multiple VDD and VSS power-supply pins is discovered and investigated. A method of whole-chip ESD protection to overcome this anomalous ESD failure is proposed with experimental verification.

I. Introduction

The electrostatic discharge (ESD) damage is the most insidious failure to electronic devices and systems. It had been reported that the ESD damages was up to 50% of the electrical failures on CMOS ICs. In CMOS ICs, on-chip ESD protection circuits are demanded to be made around each pad to avoid ESD damages. The ESD protection has become one of the main reliability issues for IC products fabricated by advanced submicron CMOS technologies with LDD structure and silicide diffusion [1].

The ESD protection circuits are generally arranged from the input and output pads to the VDD and VSS power lines [2]. To fully protect CMOS ICs against ESD damages, not only the input ESD protection for each input pad and the output ESD protection for each output pad but also the VDD-to-VSS ESD protection are necessary to be designed in CMOS ICs to avoid unexpected ESD damages beyond the ESD protection circuits [3]-[5].

But, some CMOS ICs may have multiple VDD and VSS power-supply pins for advanced design considerations, especially in VLSI chips. In the mixed-mode ICs, the VDD and VSS pins of digital circuits are separated from those of analog circuits to avoid noise coupling. A digital VLSI chip also has multiple VDD and VSS pins to ensure uniform power distribution in the whole chip and to reduce the transient current on each power line. The ESD stresses may occur among the input, output, and multiple VDD or VSS pins to cause unexpected ESD damages in the internal circuits. Thus, whole-chip ESD protection is especially important for VLSI/ULSI with multiple VDD and VSS power pins.

II. Concepts of CMOS on-chip ESD protection

The ICs or wafers inside the container could develop ESD charges. When a grounded operator or object touches these ICs or wafers, the ESD damage could occur. In a manufacturing environment, it is not possible to completely eliminate static electricity and its deleterious effects. Therefore, it becomes necessary to offer an adequate on-chip ESD protection to the ICs. The function of ESD protection circuits is to bypass ESD stress before it damages the active devices of the ICs which are protected. The protection devices must be sufficiently robust to dissipate the energy of the ESD pulse without being destroyed themselves. These protection circuits must conduct only during the ESD events, and should remain inactive in normal CMOS operations

The input gates of CMOS ICs need to be well protected because the gate oxide is so thin to be ruptured. The drains of CMOS devices connected to output pins are also vulnerable to ESD damages. Thus, both input and output pins must be protected with adequate ESD protection devices. Furthermore, VDD and VSS lines are routed everywhere in a chip to support the power for internal circuits operation. The ESD pulses may occur at VDD or VSS pins of an IC and flow along the power lines to destroy the internal circuits. Thus, the protection circuits must also be employed between VDD and VSS pins. A schematic arrangement of on-chip fully-protected ESD protection circuits in a CMOS IC is shown in Fig.1 [6]. An efficient ESD protection circuit must offer direct and effective discharging paths to bypass the ESD stresses with any polarity of ESD voltages to both VDD and VSS nodes, especially for the faster discharge modes such as MM (machine-mode) and CDM (charged-device-mode) ESD events.

The protection circuits also introduce extra delay in the paths of the I/O signals. It is necessary to minimize this delay if the IC is to be operated at higher frequencies. However, this also reduces the robustness of the ESD protection circuits. Therefore, it is important that proper tradeoffs should be made between the speed performance and the ESD protection in the advanced CMOS VLSI/ULSI.

In general, the design specifications for CMOS on-chip ESD protection circuits can be summarized as [6] :

(1) To provide ESD protection with efficient discharging paths to bypass any ESD stress;
(2) To protect themselves against ESD damages with specified degree of robustness during ESD transitions;
(3) To pass normal I/O signals and remain inactive during the normal operations of ICs;
(4) To cause acceptable I/O signal delays (as short as possible) due to the ESD protection circuits added around the I/O pads;

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(5) To offer high ESD protection capability within small layout area (as small as possible);
(6) To maintain the same high latchup immunity of CMOS ICs;
(7) To produce the ESD protection circuits without adding extra steps or masks to the fabrication process.

III. Several commonly-used CMOS on-chip ESD protection circuits

The semiconductor devices used in various on-chip ESD protection circuits for CMOS ICs can be classified as :
(1) resistor (diffusion or poly resistors);
(2) diode;
(3) thin-oxide MOS (NMOS or PMOS);
(4) thick-oxide (field-oxide) device;
(5) parasitic bipolar junction transistor;
(6) parasitic lateral SCR device (the p-n-p-n structure).

The on-chip ESD protection circuits combine above components to offer ESD protections in many different styles. Several commonly-used on-chip ESD protection circuits for CMOS ICs are shown in Fig.2.

The ESD protection capability of an ESD protection circuit varies with different CMOS technologies and different layouts. A comparisons of the measured ESD-failure-threshold voltages for different protection elements is listed in Table I to investigate their ESD protection capability. These protection elements are fabricated by the same 0.8-μm twin-well bulk CMOS process with both LDD and silicide technologies. The diode is made by the N+ diffusion in a p-well. The zener diode has the same layout structure of the diode but with an extra P+ implantation around the N+ diffusion. It is shown that the lateral SCR device has very well ESD protection capability within the smallest layout area in the submicron CMOS technologies.

IV. ESD protection for CMOS ICs with multiple VDD/VSS power pins

In this section, an unexpected ESD damages occurring in the internal circuits of a CMOS product with multiple VDD/VSS power pins are investigated. A tranceiver CMOS IC for the personal computer to connect the interface of RS232 specification has the multiple power pins of +12V VCC, -12V VSS, +5V VDD, and 0V GND. The ± 12V power pins are used for the RS232 driver/receiver, whereas those of 5V and 0V are for the 5-V personal computer. The circuits of ± 12V and 5V/0V CMOS output buffers are shown in Fig.3(a), where the corresponding cross-sectional views are shown in Fig.3(b). The parasitic junction diodes in the output buffers are also shown in Figs.3(a) & 3(b). The results of ESD testing from the output pad OUT1 to its associated +12V VCC and -12V VSS power pins show that the ± 12V output buffer can pass above ± 2KV human-body-mode (HBM) ESD stresses. The output pad OUT2 with ESD testing to its associated +5V VDD and 0V GND power pins can also pass above ± 2KV HBM ESD stresses.

In general, the ESD stress may occur between every two pins of a CMOS IC. The ESD stress may occur from the OUT1 pin of ± 12V output buffer to the 5V VDD or 0V GND pins. The ESD stress may also occur from the OUT2 pin of 5V/ 0V output buffer to the +12V VCC or -12V VSS pins. Under these ESD-stress conditions, some unexpected ESD damages may occur in the internal circuits. A microphotograph of the ESD damages in the internal circuits due to a +1KV HBM ESD stress from the OUT1 pin to a GND pin is shown in Fig.4. The ESD current at OUT1 pin is first diverted through the parasitic junction diode Dp1 to the +12V VCC power line which is connected to the internal circuits. The GND pin is also connected to the internal circuits. If there is no ESD protection circuit between the +12V VCC and 0V GND, the ESD current goes into the internal circuits through the VCC and GND lines and causes the unexpected ESD damages in the internal circuits or in the interconnection lines. This is the reason why the ESD damages (burn-out) appear almost everywhere in Fig.4. The above unexpected ESD damages may occur in other CMOS ICs with multiple VDD/VSS power pins under some ESD-stress conditions.

To avoid the unexpected ESD damages in the multiple VDD/VSS CMOS ICs, the on-chip ESD protection circuits between the multiple power pins should be made. Fig.5 shows the ESD-protection solution for this case of a CMOS IC with ± 12V and 5V/0V power pins. With the additional ESD protection elements of MP3, MN3, MN4, MN5, MN6, and MN7 devices between the power lines in Fig.5, the ESD protection capability of the whole chip can pass above ± 2KV HBM ESD stresses again.

V. Conclusion

The on-chip ESD protection circuits of a CMOS IC with multiple VDD and VSS power pins are necessary to be made not only around each input/output pad to its associated VDD and VSS pins but also between the multiple VDD and VSS power pads to achieve whole-chip ESD protection without unexpected ESD stresses on the internal circuits.

Questions and Answers

- *Q1: Had you any degradation within normal circuit operation due to additional protection ?*
- **Ans**: The additional ESD protection elements of MP3, MN3, MN4, MN5, MN6, and MN7 devices between the power lines in Fig.5 are kept off in normal operations of CMOS ICs by their gates shorted to their sources, so there is no degradation in normal circuit operation of a chip after added above ESD protection elements.
- *Q2: Why not consider Charged Device Model (CDM) ?*
- **Ans**: The standard for CDM ESD testing is still under development. The industrial standards of HBM and MM ESD testing have been matured, so they are used in this paper to verify the proposed whole-chip ESD protection concept.
- *Q3: In the table you gave, why the device with silicide?*
- **Ans**: In Table I, the elements are made by a 0.8-μm CMOS process with LDD (Lightly-Doped Drain) and silicide technologies. The silicide technology has been widely used in submicron CMOS processes to reduce the parasitic

drain and source resistances of MOS devices so as to improve the operating speed of CMOS ICs.

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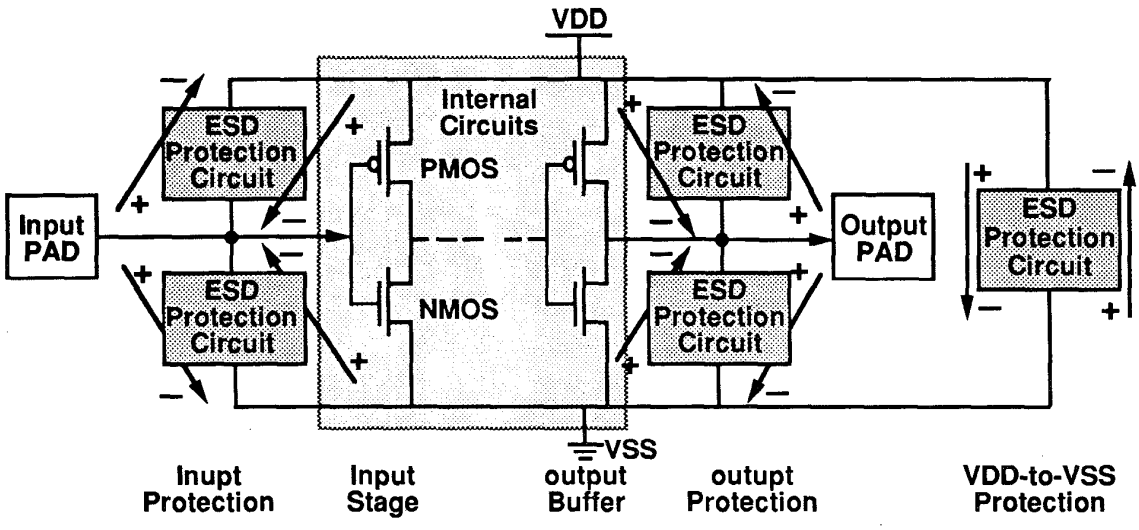

Fig.1 A schematic arrangement of on-chip ESD protection circuits in a CMOS IC.

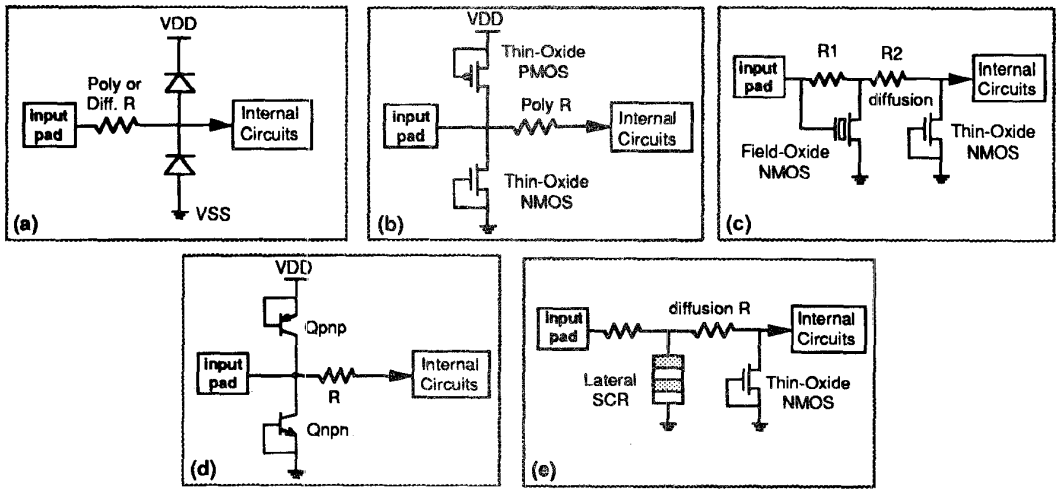

Fig.2 Several commonly-used on-chip ESD protection circuits in CMOS ICs ESD protection circuit formed by (a) resistor and diodes; (b) thin–oxide PMOS and NMOS devices; (c) thick–oxide and thin-oxide NMOS devices; (d) parasitic BJTs; (e) parasitic lateral SCR device.

Table I
Comparisons of ESD–failure–threshold voltages among the CMOS on-chip ESD protection elements made by the same 0.8–μm bulk CMOS process with LDD and silicide technologies.

	The Protection Elements in Submicron CMOS On-Chip ESD Protection Circuits				
	Diode N+ / P-well	Zener Diode	Thin-Oxide NMOS (PMOS)	Thick-Oxide Device	Lateral SCR
Layout Area (μm X μm)	20 X 150	20 X 150	180 X 200	60 X 100	42 X 100
HBM ESD Failure Threshold (Volt)	500	2000	7000	4000	8000
MM ESD Failure Threshold (Volt)	50	200	700	300	500
$\frac{\text{HBM ESD}}{\text{Layout Area}}$ $(\frac{\text{Volt}}{\mu\text{m x }\mu\text{m}})$	0.167	0.667	0.194	0.667	1.9

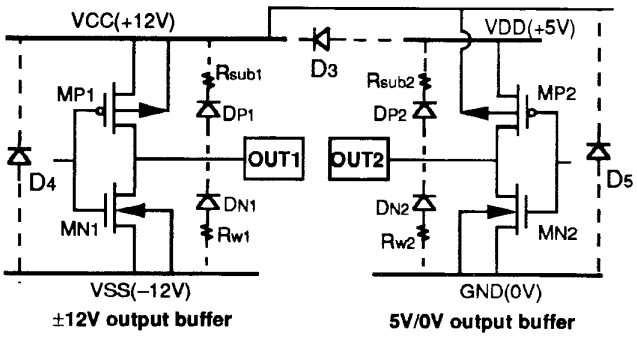

Fig.3(a) The circuits of ±12V and 5V/0V CMOS output buffers in a multiple VDD/VSS CMOS IC.

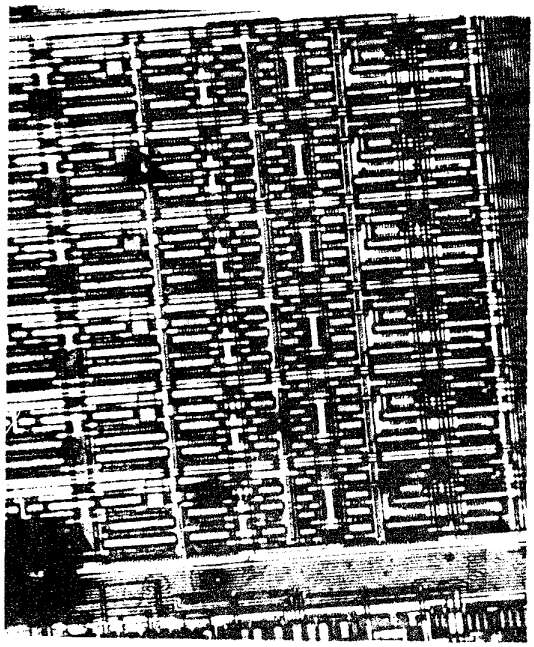

Fig.4 A microphotograph of the unexpected ESD damages in the internal circuits of a multiple VDD/VSS CMOS IC.

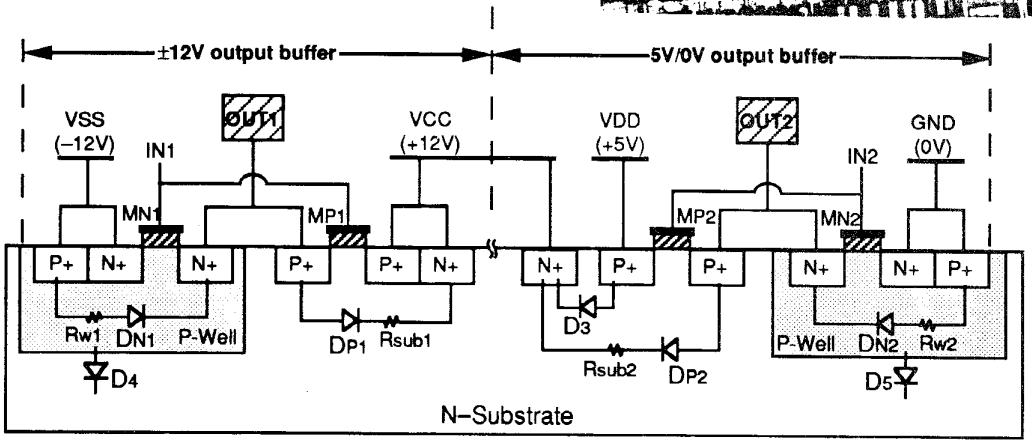

Fig.3(b) The cross-sectional view of the ±12V and 5V/0V output buffers in the n-substrate p-well CMOS technology.

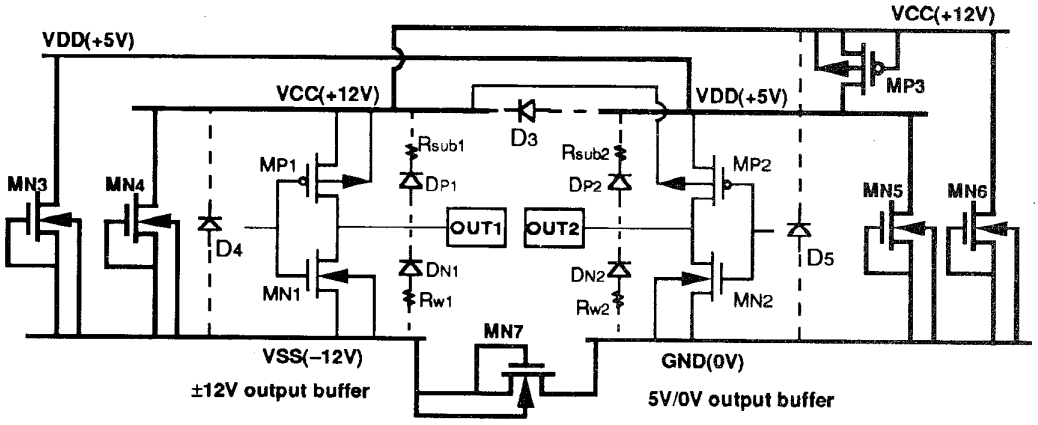

Fig.5 The solution of on-chip ESD protection for the CMOS IC with multiple VDD/VSS power pins corresponding to the output buffers of Fig.1(a).