Area-Efficient CMOS Output Buffer with Enhanced High ESD Reliability for Deep Submicron CMOS ASIC

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Abstract – There are one PTLSCR and one NTLSCR devices in parallel with output PMOS and NMOS devices, respectively, to improve ESD robustness of CMOS output buffer in deep submicron CMOS IC's. PTLSCR (NTLSCR) is merged together with output PMOS (NMOS) device to save layout area for high-density applications. Experimental results show that this proposed CMOS output buffer can sustain up to 4000V (700V) Human-Body-Mode (Machine-Mode) ESD stresses with small layout area in a 0.6-μm CMOS technology with LDD and polycide processes.

I. Introduction

In deep submicron CMOS technologies, the advanced processes such as thinner gate oxide, shorter channel length, shallower source/drain junction, LDD(Lightly-Doped Drain) structure, and silicided diffusion, much degrade ESD robustness of submicron CMOS IC's [1]-[2]. Especially, the drains of NMOS and PMOS devices in CMOS output buffer are often directly connected to the output pad to drive external heavy load, so CMOS output buffer is more sensitive to ESD stress in submicron CMOS technology. To improve ESD protection capability of CMOS output buffer and also to perform enough driving/sinking capability to external load, the NMOS and PMOS in CMOS output buffer are generally designed with much large device dimensions. Even with such large device dimension, the ESD protection capability of CMOS output buffer is still much degraded by advanced submicron CMOS technologies [1]-[2]. To improve ESD robustness of submicron CMOS output buffer, some submicron CMOS technologies offer an additional "ESD Implant" mask into processes to make a stronger device structure for CMOS output buffer against ESD damage. The cost of IC fabrication is also increased by the additional mask and process steps.

In some works [3]-[8], extra ESD protection elements are added between CMOS output buffer and the output pad to improve ESD robustness of submicron CMOS output buffer. In [5]-[7], series resistors are added between the output node of CMOS output buffer and the output pad. These series resistors could effectively improve ESD robustness of submicron CMOS output buffer, but they limit the driving/sinking capability of CMOS output buffer. The timing for output signal is also delayed by the series resistors. Thus, the output driving/sinking capability and output timing may become out of design specifications. In [8], a modified structure of lateral SCR device (called as LVTSCR) was reported to effectively protect the output NMOS device in submicron CMOS IC's.

Since ESD voltages may have positive or negative polarities on a pin to both VDD and VSS(ground) pins, there are four different ESD-stress cases at an output pad with CMOS output buffer. In [3]-[8], the ESD protection is emphasized from the output pad to VSS(GND). The additional ESD protection elements in [3]-[8] are all placed from the output pad to ground in parallel with output NMOS device. There is no additional ESD protection element arranged between the output pad and VDD node. The PMOS device of CMOS output buffer (or the output device between VDD and output pad) is sensitive to ESD damage. The overall ESD failure threshold voltage may be not effectively improved. Thus, an effective ESD protection circuit for output buffer of advanced submicron CMOS ASIC in high-reliability applications should perform strong ESD discharging path from the output pad to both VSS and VDD power lines.

To effectively improve ESD protection capability of output buffer in deep submicron CMOS ASIC and to employ the advantage of highest ESD protection capability of lateral SCR device within small layout area, a new ESD protection circuit for CMOS output buffer is proposed in this work.

II. High ESD-Protection CMOS Output Buffer

The schematic circuit of CMOS output buffer with enhanced ESD protection capability for deep submicron CMOS IC's is shown in Fig.1. There are one PTLSCR device (PMOS trigger lateral SCR) and one NTLSCR device (NMOS trigger lateral SCR) used to effectively protect CMOS output buffer against the four-mode ESD stresses. The PTLSCR (NTLSCR) device is arranged in parallel with the thin-oxide PMOS (NMOS) of CMOS

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output buffer between the output pad and VDD (VSS) power line.

The schematic cross-sectional view of PTLSCR (NTLSCR) device with thin-oxide PMOS (NMOS) in CMOS output buffer is shown in Fig.2 (Fig.3), where the P-substrate N-well CMOS process is used to demonstrate these structures. The PTLSCR (NTLSCR) and output PMOS (NMOS) devices are merged together to save layout area. Fig.4 shows the whole view in layout for the proposed CMOS output buffer with PTLSCR and NTLSCR devices, which is realized in a 0.6-μm three-metal single-poly CMOS technology with LDD and polycide processes.

In PTLSCR (NTLSCR) structure, there is a short-channel thin-oxide PMOS (NMOS) device inserted into the lateral SCR structure as shown in the right-hand part of Fig.2 (Fig.3). This PMOS (NMOS) device with its drain made across the junction between N-well and P-substrate is used to triggered on the lateral SCR structure at its drain snapback-breakdown voltage under the ESD-stress conditions. In normal operation conditions of CMOS IC's, PTLSCR (NTLSCR) is kept off because the gate of thin-oxide PMOS (NMOS) device in it is connected to VDD (VSS). Thus, the PTLSCR and NTLSCR are only active as the output pin is stressed by ESD voltage.

In Fig.1, there also exit two parasitic diodes Dp and Dn. Dp (Dn) is formed by the inherent junction between drain and bulk of PMOS (NMOS) device in the CMOS output buffer. These two diodes also work as ESD protection elements to protect CMOS output buffer.

The trigger voltage of PTLSCR (NTLSCR) device is equivalent to the snapback-breakdown voltage of short-channel thin-oxide PMOS (NMOS) device rather than the original switching voltage (about 30~50V) of lateral SCR structure in commercial CMOS processes. To protect the drain of thin-oxide NMOS and PMOS in CMOS output buffer, the channel length of thin-oxide PMOS (NMOS) in PTLSCR (NTLSCR) structure should be designed shorter than that of thin-oxide PMOS (NMOS) in CMOS output buffer. Thus, the trigger voltage of PTLSCR (NTLSCR) can be lower than the breakdown voltage of PMOS (NMOS) device in the CMOS output buffer.

As ESD events occur on an output pin, there are PS, NS, PD, and ND four different ESD-stress cases. In PS-mode (NS-mode) ESD stress, a positive (negative) ESD voltage occurs at the output pin with relatively grounded VSS pin but VDD pin floating. In PD-mode (ND-mode) ESD stress, a positive (negative) ESD voltage occurs at the output pin with relatively grounded VDD pin but VSS pin floating. In this proposed CMOS output buffer, the PS-, NS-, PD-, and ND-mode ESD stresses are one-by-one protected by the NTLSCR, Dn, Dp, and PTLSCR devices.

In conventional CMOS output buffer, the PS-mode (ND-mode) ESD stress causes PMOS (NMOS) device of the CMOS output buffer into breakdown to bypass ESD current. Under such breakdown conditions, the PMOS and NMOS devices in submicron CMOS output buffer are hard to sustain ESD-stress voltage above 2000V (ESD specification of commercial products in Human-Body-Mode (HBM) ESD testing). So, the PTLSCR and NTLSCR are used in parallel with the PMOS and NMOS in CMOS output buffer to enhance ESD robustness of CMOS output buffer above the 2000-V specification.

As ND-mode (PS-mode) ESD event occurs at the output pin, PTLSCR (NTLSCR) is first turned on by the negative (positive) ESD voltage at the pad to bypass ESD current without the thin-oxide PMOS (NMOS) of CMOS output buffer broken down by the ESD voltage. If PTLSCR (NTLSCR) is triggered on, it can clamp the voltage on the pad as low as its holding voltage of lateral SCR device. Thus, PTLSCR and NTLSCR devices can effectively protect CMOS output buffer against ESD damages.

III. Experimental Results

One set of testkeys fabricated by a 0.6-μm three-metal single-poly CMOS technology with LDD and polycide processes is measured and tested. The typical ESD testing results are shown in Table I, in which a conventional CMOS output buffer with device width/length in PMOS and NMOS devices of 500/1.2 (μm) is also fabricated in the same testchip as a comparing reference. The ESD-stress voltage is set to begin with the initial voltage of 2000V and increase up to 8000V with each step of 250V in HBM ESD testing. The Machine-Mode (MM) ESD stress is also used to test the ESD robustness of CMOS output buffer under the faster ESD-transient condition. The four modes of ESD stresses are applied to the testchips. The lowest (absolute value) ESD failure voltage among the four modes at the same output pin is adopted as the ESD failure threshold of the pin. The results show that this work can sustain ESD failure threshold up to above 4250V (750V) in HBM (MM) ESD testing within smaller layout area.

The turn-on characteristics of PTLSCR and NTLSCR are also measured and shown in Figs.5 and 6, respectively. In Fig.5 (Fig.6), it is clear shown that the trigger voltage of PTLSCR (NTLSCR) is lowered to -13.68V (12.76V) and its holding voltage is still as low as -1.20V (1.12V). These measured results verify that PTLSCR (NTLSCR) is triggered on by the short-channel thin-oxide PMOS (NMOS) device, which inserted into the lateral SCR structure, in its drain snapback-breakdown condition. After drain snapback breaks down, PTLSCR (NTLSCR) is into the low-impedance latching state of lateral SCR structure. A typical snapback-breakdown characteristics of thin-oxide PMOS device with channel length of 0.8μm in the CMOS output buffer is shown in Fig.7. The snapback-breakdown voltage of 0.8-μm PMOS device is -13.94V, and its holding voltage is as high as -9.18V. Comparing the I-V curves between Figs. 5 and 7, it can guarantee that PTLSCR can be first turned on before the PMOS device of CMOS output buffer breaks down under ESD-stress condition. The holding voltage of PTLSCR is also much smaller (in absolute value) than that of PMOS device in CMOS output

buffer. Similar characteristics can be also found between NTLSCR and NMOS device of CMOS output buffer. Thus, this PTLSCR (NTLSCR) can effectively protect the PMOS (NMOS) device of CMOS output buffer against ESD stresses.

This ESD-enhanced CMOS output buffer has been successfully used in some IC's to perform its output function. For example, it has performed the output function for a 5-V 32-bits adder with operating frequency of 25MHz.

IV. Conclusion

With high ESD protection capability in small layout area and without adding extra series resistor between output pad and CMOS output buffer, this proposed CMOS output buffer is very suitable for advanced deep submicron CMOS IC's in high-reliability, high-density, and high-speed applications. The fabrication of this proposed output buffer can be fully compatible to both CMOS and BiCMOS technologies with N-well/P-substrate, P-well/N-substrate, or twin-well processes.

References

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Table I

	Conventional CMOS Output Buffer with Large Dimension (W/L)				This Work			
	PMOS (500/1.2)		NMOS (500/1.2)		PTLSCR + PMOS		NTLSCR + NMOS	
Layout Area ($\mu m \times \mu m$)	158 X 92		166 X 100		107.4 X 86.0		111.4 X 86.0	
ESD-Sress Condition	PD-Mode	ND-Mode	PS-Mode	NS-Mode	PD-Mode	ND-Mode	PS-Mode	NS-Mode
HBM ESD Failure Voltage (V)	above 8000	-3250	below 2000	above -8000	above 8000	above -8000	4250	above -8000
MM ESD Failure Voltage (V)	450	-350	400	-850	above 1000	above -1000	750	above -1000

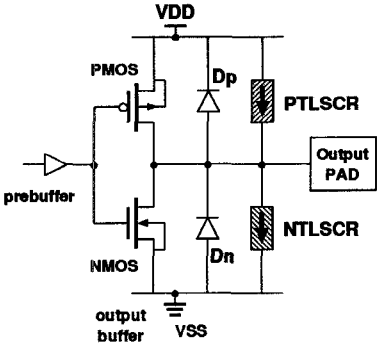

Fig.1 Schematic circuit of CMOS output buffer with enhanced ESD protection capability.

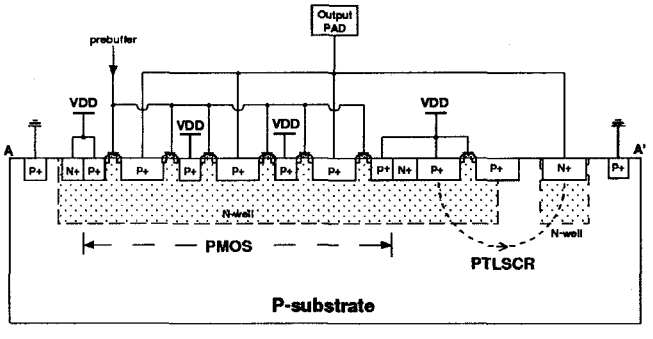

Fig.2 Cross-Sectional view of thin-oxide PMOS with PTLSCR device. (N-well/P-substrate CMOS Process)

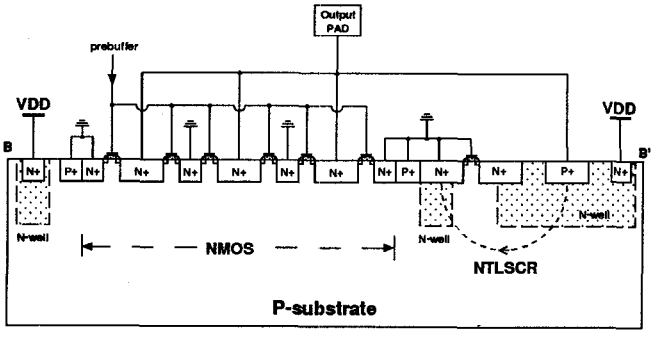

Fig.3 Cross-Sectional view of thin-oxide NMOS with NTLSCR device. (N-well/P-substrate CMOS Process)

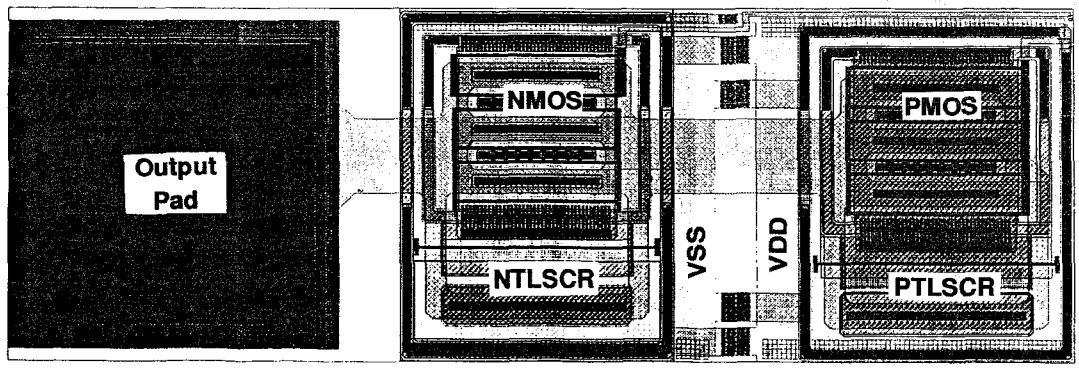

Fig.4 Layout example of the proposed CMOS output buffer with enchanced ESD protection.

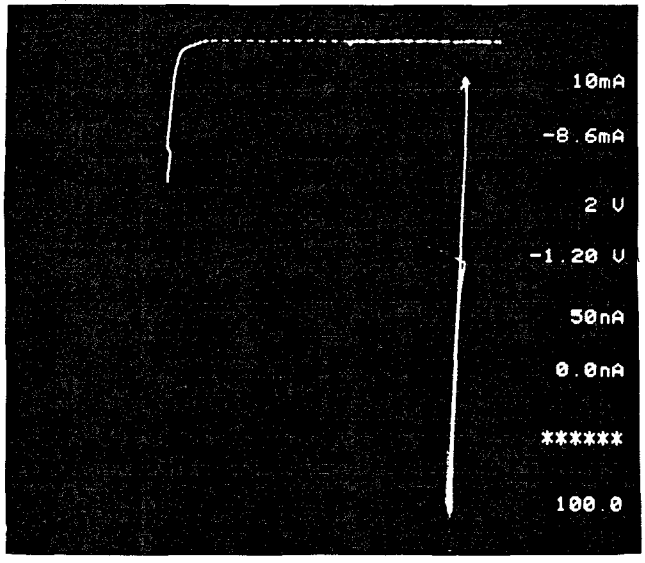

Fig.5 The I-V characteristics of PTLSCR.
(X axis: 2V/div.; Y axis: 10mA/div.)

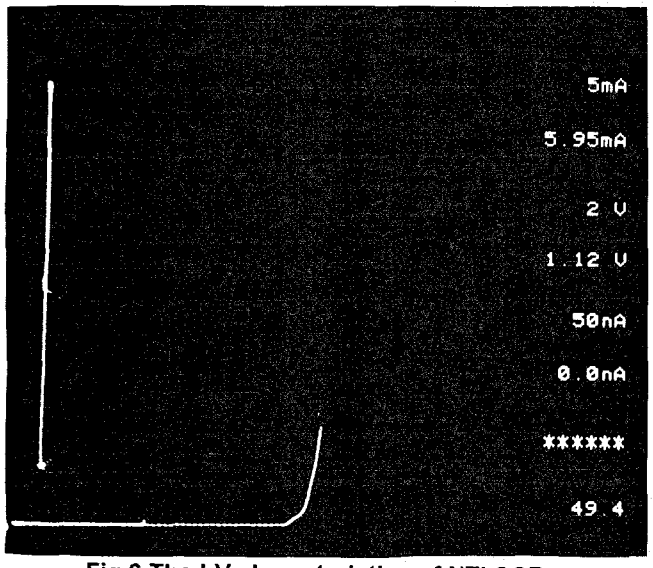

Fig.6 The I-V characteristics of NTLSCR.
(X axis: 2V/div.; Y axis: 5mA/div.)

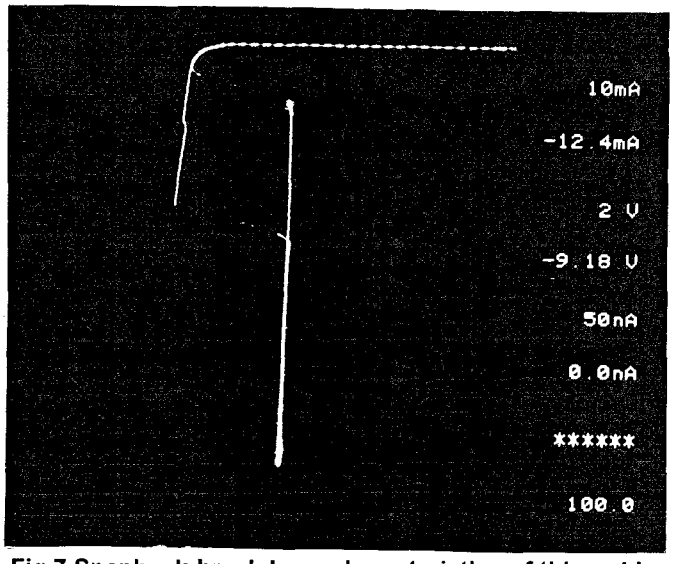

Fig.7 Snapback-breakdown characteristics of thin-oxide PMOS device with channel length of 0.8μm.
(X axis: 2V/div.; Y axis: 10mA/div.)