Complementary–LVTSCR ESD Protection Scheme for Submicron CMOS IC's

Ming-Dou Ker, Chung-Yu Wu, Hun-Hsien Chang, Tao Cheng, and *Tain-Shun Wu

Integrated Circuits and Systems Laboratory
Institute of Electronics, National Chiao-Tung University
Hsinchu, Taiwan, R.O.C., FAX :886-35-715412
E-mail: mdker@alab06.ee.nctu.edu.tw

*VLSI Design Dept.
Computer & Communication Research Lab.
Industrial Technology Research Institute
Chutung, Hsinchu, Taiwan, R.O.C.

Abstract – There are one LVTSCR device merged with short-channel NMOS and another LVTSCR device merged with short-channel PMOS in complementary style to offer effective and direct ESD discharging paths from the input or output pads to Vss and VDD power lines. The dc switching voltage of LVTSCR devices is lowered to the snapback voltage of short-channel NMOS and PMOS devices. Experimental results show that it can perform excellent ESD protection capability in a smaller layout area.

I. INTRODUCTION

Electrostatic discharge (ESD) protection for submicron CMOS IC's is much degraded due to both the smaller feature size of scaled-down devices and the advanced CMOS technologies of LDD (Light-Doped Drain) structure and silicide-diffusion process [1]. To improve ESD protection capability of CMOS on-chip ESD protection circuit, the lateral SCR device had been used as a main protection element to bypass ESD stress. The dc switching voltage of lateral SCR device in the submicron CMOS process is around 30 ~ 50V. But, the gate-oxide thickness in 0.6~0.8 μm CMOS process is only around 150~200 Å. This gate oxide will be damaged by a voltage about 15 ~ 20V across it because the dielectric breakdown strength of SiO_2 is about 10MV/cm. Thus, the lateral SCR device with switching voltage of 30~50V can not protect the gate oxide of CMOS input stage alone without other secondary-protection elements.

If the switching voltage of lateral SCR device can be reduced below the gate-oxide breakdown voltage of CMOS devices, the lateral SCR device can perform the highest ESD protection capability in a smallest layout area (compared with other ESD protection elements such as diode, thick-oxide device, gate-oxide device, and parasitic bipolar device in CMOS IC's). To lower the switching voltage of lateral SCR device in submicron CMOS technologies, some efforts had been contributed to modify the structure of lateral SCR device [2], [3]. In [2], a modified structure of lateral SCR device called as LVTSCR (Low-Voltage Trigger SCR) had been reported with its trigger voltage lower than the gate-oxide breakdown voltage.

Since the ESD voltages may have positive or negative polarities to both VDD and Vss(ground) nodes, there are four different ESD-stress cases at each input or output pins:

(1) PS mode: ESD stress at a pin with positive voltage polarity to VSS(GND) pin when VDD pin is floating;
(2) NS mode: ESD stress at a pin with negative voltage polarity to VSS(GND) pin when VDD pin is floating;
(3) PD mode: ESD stress at a pin with positive voltage polarity to VDD pin when VSS(GND) pin is floating;
(4) ND mode: ESD stress at a pin with negative voltage polarity to VDD pin when VSS(GND) pin is floating.

These ESD voltages could damage both NMOS and PMOS devices in the input stage or output driver of CMOS IC's. In [2], the LVTSCR device is only arranged between the output or input pad to VSS(GND) node. There is no ESD protection element arranged between the pad and VDD node. For the ND-mode or PD-mode ESD stresses, the ESD current/voltage is first diverted from the input pin to Vss power line of CMOS IC through the LVTSCR device, and then this ESD current/voltage flows through the VDD-to-Vss ESD protection element to VDD power line. Finally, the ESD current/voltage goes out of CMOS IC from the VDD pin. Due to the parasitic resistance and capacitance of Vss/VDD power lines in CMOS IC's as well as voltage drops on the input-to-Vss and VDD-to-Vss ESD protection elements, such non-direct ESD discharging path had been reported to cause some unexpected ESD damages on internal circuits beyond ESD protection circuits [4]-[6]. Thus, an effective ESD protection circuit for advanced submicron CMOS IC's should perform direct ESD discharging path from input and output pads to both Vss and VDD power lines.

To overcome above problem of non-direct ESD discharging path and to employ the advantage of high ESD protection capability of lateral SCR device with small layout area, a new complementary-LVTSCR ESD protection circuit is proposed in this paper.

II. COMPLEMENTARY-LVTSCR ESD PROTECTION SCHEME

A. Circuit Configuration

The complementary-LVTSCR ESD protection scheme for submicron CMOS IC's is shown in Fig.1. The corresponding schematic cross-sectional view of complementary-LVTSCR device is shown in Fig.2, where

the P-substrate N-well CMOS process is used to demonstrate the complementary-LVTSCR structures. They can also be implemented in N-substrate P-well CMOS process as well if appropriate modifications are made. The LVTSCR1 device is arranged between V_{DD} power line and input (or output) pad with its cathode connected to the input (or output) pad. The LVTSCR2 device is arranged between input (or output) pad and $V_{SS(GND)}$ power line with its anode connected to the pad.

The LVTSCR1 device is formed by a lateral SCR device (composed by BJT's Q1 and Q2) with a short-channel thin-oxide PMOS which are merged together to lower the trigger-on voltage of lateral SCR device, as shown in the right-hand part of Fig.2. The thin-oxide PMOS is composed by a non-connection P+ diffusion cross the N-well/P-substrate junction as its drain, N-well connected to V_{DD} as its bulk, and a P+ diffusion in the N-well of bulk as its source. The gate of thin-oxide PMOS is connected to V_{DD} to ensure itself off in the normal-operation conditions of CMOS IC's. The purpose of inserting a thin-oxide PMOS into the lateral SCR structure is to use the drain of thin-oxide PMOS in the snapback-breakdown condition to trigger on the lateral SCR structure during ESD stress. The trigger-on voltage of LVTSCR1 device is equivalent to the snapback-breakdown voltage of the short-channel thin-oxide PMOS rather than the original switching voltage (about 30 ~ 50V) of the lateral SCR device.

Similarly, the LVTSCR2 device is formed by a lateral SCR device with a short-channel thin-oxide NMOS merged together to lower the trigger-on voltage of lateral SCR device. The gate of thin-oxide NMOS is connected to $V_{SS(GND)}$. The trigger-on voltage of LVTSCR2 device is equivalent to the snapback-breakdown voltage of short-channel thin-oxide NMOS. The turn-on holding voltage of LVTSCR1 and LVTSCR2 devices is equivalent to the original holding voltage (about 1 ~ 2V) of lateral SCR device.

There also exist two junction diodes D1 and D2 which are merged into the complementary-LVTSCR structure to save layout area. The anode of D1 diode is connected to $V_{SS(GND)}$ and its cathode is connected to input (or output) pad. The anode of D2 diode is connected to the pad and its cathode is connected to V_{DD}. Diode D1, formed by an N-well in P-substrate, can clamp the low voltage level of input (or output) signals on the pad to about $V_{SS(GND)}$-0.6V. Diode D1 also performs an ESD discharging path from $V_{SS(GND)}$ to input (or output) pad. Diode D2, formed by a P+ diffusion in an N-well, can clamp the high voltage level of input (or output) signals on the pad to about V_{DD}+0.6V. Diode D2 also performs an ESD discharging path from the pad to V_{DD}.

A typical layout example of this complementary-LVTSCR ESD protection circuit is shown in Fig.3 with guard rings to prevent V_{DD}-to-Vss latchup.

B. Circuit Operating Principles

When PS-mode ESD events occur, ESD voltage is diverted to the drain (N+ diffusion cross the N-well / P-substrate junction) of thin-oxide NMOS through the P+ diffusion / N-well / N+ diffusion forward-conducting path. The thin-oxide NMOS in LVTSCR2 is turned on by means of drain snapback breakdown to first clamp positive ESD voltage on the pad to the voltage level of snapback voltage (about 13 ~ 16 V) of thin-oxide NMOS. The discharging current from the N+ diffusion in N-well to P-substrate due to the snapback-breakdown drain of thin-oxide NMOS helps and leads to latchup happen in the lateral LVTSCR2 device. Once the latchup happens in the lateral LVTSCR2 device, ESD current is mainly discharged through the lateral SCR structure. The ESD voltage on the pad is clamped by the holding voltage of turn-on lateral SCR structure to about 1 ~ 2V so as to protect the internal circuits which are connected to this pad. Thus, this LVTSCR2 device can effectively protect CMOS IC's against PS-mode ESD damages alone without other secondary protection elements as those shown in [3].

In NS-mode ESD-stress condition, diode D1 is forwardly conducting. So, the NS-mode ESD current can be directly discharged through diode D1.

In PD-mode ESD events, ESD stress occurs at the input (or output) pins with positive polarity to V_{DD} pin. The PD-mode ESD current can be directly discharged through forward-conducting diode D2.

When ND-mode ESD events occur, negative ESD voltage is diverted to the cathode of LVTSCR1 device, through the P-substrate, and then to the drain (P+ diffusion cross the P-substrate/N-well junction) of thin-oxide PMOS. The drain of thin-oxide PMOS is broken down and leads to latchup happen in the lateral LVTSCR1 device. Once the latchup happens in LVTSCR1 device, the ESD current is mainly discharged through the lateral SCR structure. The negative ESD voltage on the pad is clamped by the holding voltage of turn-on lateral SCR structure to about -1 ~ -2V so as to protect the internal circuits.

In normal CMOS operations with 5-V V_{DD} and 0-V Vss power supply, diodes D1 and D2 clamp voltage level on the pad between 5.6V and -0.6V. Thus, these diodes also prevent LVTSCR1 and LVTSCR2 devices to be triggered on in variable normal operating conditions of CMOS IC's.

III. EXPERIMENTAL RESULTS

A test chip to realize this complementary-LVTSCR ESD protection circuit has been designed and fabricated by a 0.8-μm CMOS technology with LDD and silicide processes. One of test pads is shown in Fig.4(a), which is corresponding to the layout example in Fig.3. In Fig.4(b), a conventional CMOS ESD protection circuit composed by

a PMOS (from pad to VDD) and an NMOS (from pad to Vss) with gate shorted to source is also fabricated in the same test chip as a comparing reference. In Fig.4(a), the channel width/length of PMOS and NMOS inserted in LVTSCR1 and LVTSCR2 is 75/1.0 μm, and total layout area of LVTSCR1 (LVTSCR2) is 66.7x108.6 (65.2x107.0) μm^2 which including a 4-μm guard ring of N+ (P+) diffusion. The channel width/length of PMOS and NMOS in the conventional ESD protection circuit of Fig.4(b) is 500/1.0 μm, and the total layout area of each PMOS and each NMOS is 145.2x94.0 μm^2, respectively. The HBM (Human-Body Mode) and MM (Machine Mode) ESD testing results are shown in Table I by the ESD failure criterion of 1-μA leakage current increase below 7.1V bias. The results show that the ESD failure threshold of conventional PMOS/NMOS ESD protection circuit is only 3250V (200V) but that of complementary-LVTSCR ESD protection circuit within a smaller layout area is up to 8000V (650V) in HBM (MM) ESD testing.

The turn-on characteristics of fabricated LVTSCR2 device is shown in Fig.5(a), where the switching voltage is 15.50V and its holding voltage is 1.02V. The snapback turn-on characteristics of fabricated NMOS in the conventional ESD protection circuit is shown in Fig.5(b), where the snapback voltage is 15.64V.

Fig.6 shows the I-V curve measured from the VDD to Vss nodes in the complementary-LVTSCR ESD protection circuit to monitor the VDD-to-Vss latchup issue. It is shown that the holding voltage of VDD-to-Vss latchup is as high as 11.90V. So, this complementary-LVTSCR ESD protection circuit can be free of VDD-to-Vss latchup problem.

IV. CONCLUSION

A robust ESD protection scheme with complementary-LVTSCR structures and junction diodes has been designed, fabricated, and measured in submicron CMOS technologies. From the experimental results, the LVTSCR1 and LVTSCR2 devices with enough lower trigger-on voltage can sustain much higher ESD stress within a smaller layout area than other conventional ESD protection circuits in submicron CMOS IC's with LDD and silicide diffusion technologies. This complementary-LVTSCR ESD protection circuit is also free of VDD-to-Vss latchup problem in 5-V CMOS IC's.

The fabrication of this proposed complementary-LVTSCR ESD protection scheme is fully process compatible to both CMOS and BiCMOS technologies with N-well/P-substrate, P-well/N-substrate, or twin-well structures.

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Table I

	Conventional ESD protection circuit				Complementary-LVTSCR ESD protection circuit			
	PMOS		NMOS		LVTSCR1		LVTSCR2	
Layout Area (μmXμm)	94.0x145.2		94.0x145.2		66.7x108.6		65.2x107.0	
ESD-Stress condition	PD-mode	ND-mode	PS-mode	NS-mode	PD-mode	ND-mode	PS-mode	NS-mode
HBM ESD failure voltage (V)	above 8000 *	-3250	5500	above -8000 *	above 8000 *	-8000	above 8000 *	above -8000 *
MM ESD failure voltage (V)	400	-200	300	-500	700	above -800 *	650	above -800 *

* limited by the ESD testing machine (ESD Simulator : HANWA HED-S5000)

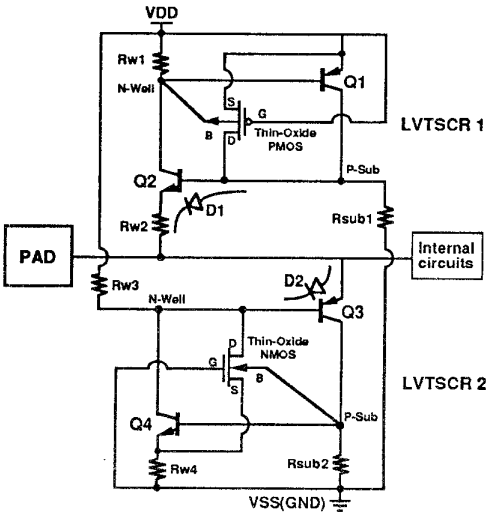


Fig.1 Complementary-LVTSCR ESD Protection Circuit for Submicron CMOS ICs

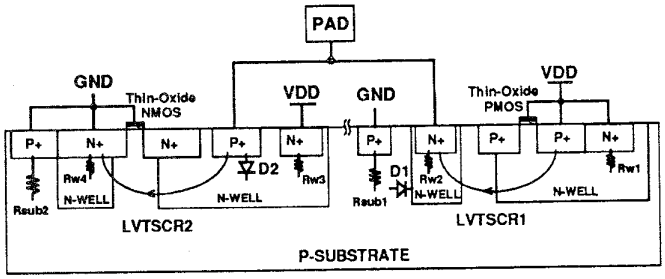


Fig.2 Schematic Cross-Sectional View of Complementary-LVTSCR Device

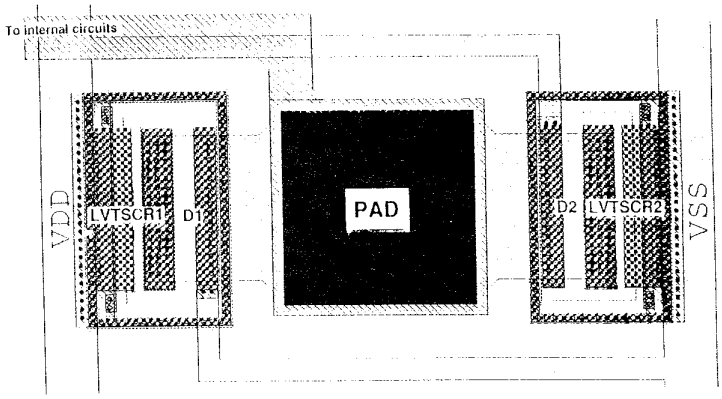
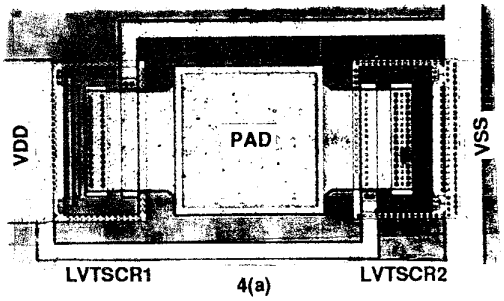
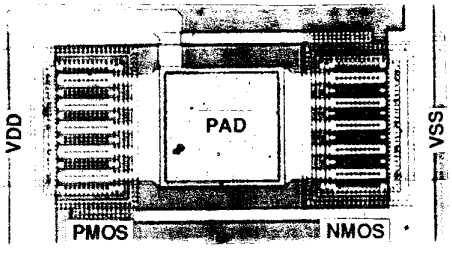


Fig.3 A layout example of complementary-LVTSCR ESD protection circuit.

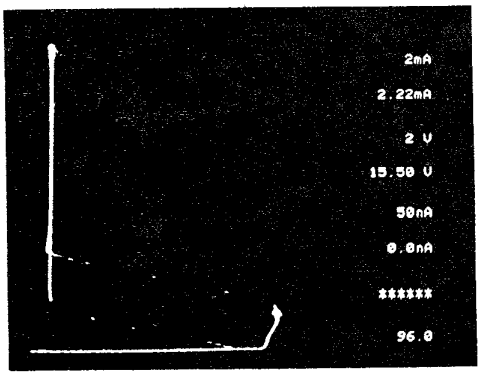


4(a)

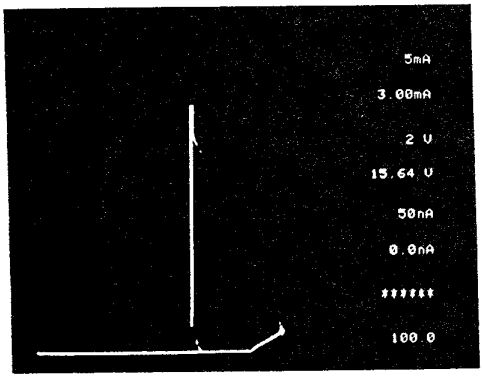


4(b)

Fig.4 Microphotograph of (a) the complementary-LVTSCR ESD protection circuit; (b) the conventional PMOS/ NMOS ESD protection circuit.



5(a)



5(b)

Fig.5 Turn-on characteristics of (a) the LVTSCR2 device; (b) NMOS device in the conventional ESD protection circuit, which are fabricated by a 0.8–μm CMOS process.

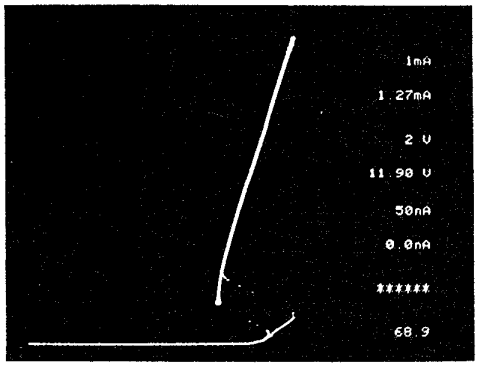


Fig.6 The I-V characteristics of VDD-to-VSS latchup path in the fabricated complementary-LVTSCR ESD protection circuit.