ESD Protection for Deep-Submicron CMOS Technology Using Gate-Couple CMOS-Trigger Lateral SCR Structure

Ming-Dou Ker, Hun-Hsien Chang*, and Chung-Yu Wu*

VLSI Design Department
Computer & Communication Research Laboratories (CCL)
Industrial Technology Research Institute (ITRI)
Chutung, Hsinchu, Taiwan 310, R.O.C.
Fax: 886-35-820025, E-mail: mdker@u1th3.ccl.itri.org.tw

* Integrated Circuits and Systems Laboratory
Institute of Electronics, National Chiao-Tung University
Hsinchu, Taiwan 300, R.O.C.
Fax: 886-35-715412

Abstract

A novel ESD protection circuit, which first combines the advantages of complementary low-voltage-trigger SCR devices and the gate-couple technique, is proposed to more effectively protect the thinner gate oxide of deep submicron CMOS IC's without adding extra ESD-implant mask. Experimental results have verified its excellent ESD-protection capability.

Introduction

In deep submicron CMOS technologies, the advanced processes such as thinner gate oxide, shorter channel length, shallower drain/source junction, LDD structure, polycide, and silicided diffusion, much degrade ESD robustness of CMOS IC's [1]-[2]. Recently, there are three approaches to improve ESD robustness of submicron CMOS IC's. One is to add an extra mask of "ESD implant" into the process flow to make a stronger structure for input/output devices [3]-[4]. But, the cost of chip fabrication is increased. Another approach is to adopt the "gate-couple" technique to achieve uniform power distribution among the multiple fingers of output NMOS device. This technique has been reported to effectively improve ESD reliability in submicron CMOS technology [5]-[7]. Due to the inherent capability of high power delivery, the lateral SCR device had been used as a main protection element to bypass ESD stress. Experimental results have shown that the lateral SCR device can sustain highest ESD stress within smallest layout area as compared to other traditional ESD protection elements [8]. Thus, the third approach is to use low-voltage-trigger lateral SCR (LVTSCR) devices to protect submicron CMOS IC's [9]-[10].

Moreover, in deep submicron CMOS technology, the thickness of gate oxide is scaled down to be thinner [2]. This much thinner gate oxide is more sensitive to ESD stresses. For ESD protection of input pad, gate-grounded NMOS device is often used as the secondary protection element to clamp ESD voltage to the gate oxide of input devices by its drain snapback breakdown. But, the voltage margin between gate-oxide breakdown and drain snapback breakdown is also much reduced in deep submicron CMOS technology. Therefore, the thinner gate oxide may be ruptured by ESD voltage before drain of secondary-protection NMOS into snapback breakdown. To overcome this issue, a gate-couple technique has been reported to successfully lower drain snapback-breakdown voltage of protection devices to effectively protect the thinner gate oxide of 90 ±10Å in a 0.5-μm 3-V CMOS technology [11].

In this paper, a novel ESD protection circuit, which combines both advantages of complementary-LVTSCR devices in highest ESD protection capability within smallest layout area [10] and the lowered drain snapback-breakdown voltage by gate-couple technique [11], is first proposed to more effectively protect the thinner gate oxide of deep submicron CMOS IC's without adding extra ESD-implant mask.

The Proposed ESD Protection Circuit

A. Circuit Configuration and Device Structures

Fig.1 shows the proposed ESD protection circuit with its corresponding schematic cross-sectional view shown in Fig.2. A practical layout example is shown in Fig.3. In Fig.1, there are one PMOS-trigger lateral SCR (PTLSCR) device is arranged between pad and VDD, and one NMOS-trigger lateral SCR (NTLSCR) device is arranged between pad and VSS. PTLSCR and NTLSCR are made by inserting a short-channel PMOS (Mp1) and NMOS (Mn1) into lateral SCR structures to lower their trigger voltages, respectively. The trigger voltage of PTLSCR (NTLSCR) is equivalent to the drain snapback-breakdown voltage of Mp1 (Mn1) [10].

But, in deep submicron CMOS technology with much thinner gate oxide, the drain snapback-breakdown voltage could be near to or even higher than the gate-oxide breakdown voltage. Thus, the gate-couple technique [11] is used to much lower the ESD-trigger voltage of PTLSCR and NTLSCR to effectively protect the gate of input stage in CMOS IC's. The gate-couple technique is realized by the coupling capacitor Cp (Cn) for PTLSCR (NTLSCR). In Fig.3, Cp (Cn) is realized by a poly layer right under the metal pad without increasing total layout area. By modifying

0-7803-2700-4 $4.00 ©1995 IEEE

the overlap area between poly layer and the metal pad, the capacitance of Cp (Cn) can be adjusted.

B. Operating Principles

Since ESD voltages may have positive or negative polarities to VDD or VSS pins, there are four modes of ESD stresses at each pin of a CMOS IC :

(1) PS mode: positive ESD voltage occurs to a pin with relatively grounded VSS pin but VDD pin is floating;
(2) NS mode: negative ESD voltage occurs to a pin with relatively grounded VSS pin but VDD pin is floating;
(3) PD mode: positive ESD voltage occurs to a pin with relatively grounded VDD pin but VSS pin is floating;
(4) ND mode: negative ESD voltage occurs to a pin with relatively grounded VDD pin but VSS pin is floating.

In ND-mode (PS-mode) ESD stress, there is some negative (positive) ESD-transient voltage coupled to the gate of Mp1 (Mn1) through the capacitor Cp (Cn). This coupled negative (positive) voltage on the gate of Mp1 (Mn1) can much lower its drain snapback-breakdown voltage [11]. As the drain of Mp1 (Mn1) is broken down, PTLSCR (NTLSCR) will be triggered on to mainly bypass ESD current. When PTLSCR (NTLSCR) is triggered on, its holding voltage is only around -1~-2V (1~2V). The negative (positive) ESD-stress voltage on the pad is clamped to around -1~-2V (1~2V), so the thinner gate oxide of input stage in deep submicron CMOS IC's can be fully protected. With suitable design on capacitor Cp (Cn), the ESD-transient voltage coupled to the gate of Mp1 (Mn1) can be controlled so as to adjust the ESD-trigger voltage of PTLSCR (NTLSCR) for different practical applications.

In NS-mode (PD-mode) ESD stress, the parasitic diode D1 (D2) is forward biased and turned on to bypass ESD current from the pad to VSS (VDD). The negative (positive) ESD-stress voltage on the pad is clamped to around -0.6~ -0.8V (0.6~0.8V), so the thinner gate oxide of input stage in deep submicron CMOS IC's can be also fully protected.

In normal CMOS operating conditions with VDD and VSS power supplies, the Mp2 (Mn2) with its gate connected to VSS (VDD) through a resistor Rp (Rn) is used to turn off Mp1 (Mn1). The voltage level of input signals on the pad is also clamped, by the parasitic diodes D1 and D2, between VDD+0.6V and VSS-0.6V. Thus, PTLSCR and NTLSCR are guaranteed to be off in normal CMOS operating conditions.

Experimental Results

Experimental test chip has been fabricated by a 0.6-μm CMOS technology. A microphotography of a pad with the proposed ESD protection circuit is shown in Fig.4, which is corresponding to the layout of Fig.3. ESD testing results are summarized in Table I, where a conventional CMOS ESD protection circuit formed by PMOS and NMOS of W/L=500/1.2 (μm) is also made and tested as a reference for comparison in the same test chip. It is shown that this proposed ESD protection circuit can sustain up to 5750 V of human-body-mode ESD stresses in a smaller layout area, but the ESD failure threshold of conventional CMOS ESD protection circuit is only 1200 V even with much larger layout area. This verifies the excellent ESD-protection capability of the proposed ESD protection circuit.

Fig. 5 shows the measured I-V curves of PTLSCR as the gate of Mp1 is applied with different negative voltage. Fig. 6 shows the measured I-V curves of NTLSCR as the gate of Mn1 is applied with different positive voltage. The effect of trigger voltage of PTLSCR (NTLSCR) lowering by the coupled voltage on the gate of Mp1 (Mn1) is shown in Fig. 7 (Fig.8). The larger (in absolute value) voltage coupled to the gate of Mp1 and Mn1, this leads to the lower trigger voltage of PTLSCR and NTLSCR. The voltage coupled to the gate of Mp1 (Mn1) in order to trigger on PTLSCR (NTLSCR) can be adjusted by the capacitor Cp (Cn).

A negative (positive) voltage pulse is direct applied to the pad with relatively grounded VDD (VSS) to find the ESD-trigger voltage of the gate-couple PTLSCR (NTLSCR) in ND-mode (PS-mode) ESD-stress condition, and the measured voltage waveform is shown in Fig.9 (Fig.10). It is found in Fig.9 (Fig.10) that a negative (positive) voltage pulse of -7.562 (7.031)V can trigger on the gate-couple PTLSCR (NTLSCR), but the dc trigger voltage of PTLSCR (NTLSCR) is as high as -16.80 (13.24)V. This verifies the efficiency of gate-couple technique to lower the ESD-trigger voltage of PTLSCR and NTLSCR, so this proposed ESD protection circuit can effectively protect the thinner gate oxide of input stage.

Conclusion

From above experimental verification, this proposed ESD protection circuit is very suitable for deep submicron CMOS IC's in low-voltage (with thinner gate oxide), low-cost (without ESD implant), high-density (within smaller layout area), high-speed (minimum input delay), and high-reliability (high ESD failure threshold) applications. This proposed ESD protection circuit is also suitable to effectively protect the output pad of deep submicron CMOS IC's.

References

[1] C. Duvvury and A. Amerasekera, "ESD: A pervasive reliability concern for IC technologies," *Proc. of IEEE*, vol.81, no.5, pp.690-702, May 1993.

[2] A. Amerasekera and C. Duvvury, "The impact of technology scaling on ESD robustness and protection circuit design," 1994 *EOS/ESD Symp. Proc.*, EOS-16, pp. 237-245.

[3] S. Daniel and G. Krieger, "Process and design optimization for advanced CMOS I/O ESD protection devices," 1990 *EOS/ESD Symp. Proc.*, EOS-12, pp. 206-213.

[4] C. Diaz, T. Kopley, and P. Marcoux, "Building-in ESD/EOS reliability for sub-halfmicron CMOS processes," *Proc. of IRPS*, 1995, pp.276-283.

[5] C. Duvvury and C. Diaz, "Dynamic gate coupling of NMOS for efficient output ESD protection," *Proc. of IRPS*, 1992, pp. 141-150.

[6] C. Duvvury, C. Diaz, and T. Haddock, "Achieving uniform nMOS device power distribution for submicron ESD reliability," 1992 *Tech. Dig. of IEDM*, pp.131-134.

[7] S. Ramaswamy, C. Duvvury, and S.-M. Kang, "EOS/ESD reliability of deep sub-micron NMOS protection devices," *Proc. of IRPS*, 1995, pp.284-291.

[8] M.-D. Ker, C.-Y. Wu, *et al.*, "Whole-chip ESD protection for CMOS VLSI/ULSI with multiple power pins," *Proc. of IEEE International Integrated Reliability Workshop*, 1994, pp.124-128.

[9] A. Chatterjee and T. Polgreen, "A low-voltage triggering SCR for on-chip ESD protection at output and input pads," *IEEE Electron Device Letters*, vol.12, no.1, pp. 21-22, Jan. 1991.

[10] M.-D. Ker, C.-Y. Wu, *et al.*, "Complementary-LVTSCR ESD protection scheme for submicron CMOS IC's," *Proc. of IEEE International Symposium on Circuits and Systems*, 1995, pp.833-836.

[11] M.-D. Ker, C.-Y. Wu, *et al.*, "On-chip ESD protection using capacitor-couple technique in 0.5-μm 3-V CMOS technology," *IEEE International ASIC Conference*, 1995, in press.

Table I Comparison of ESD testing results.

	Conventional CMOS ESD Protection Circuit with Large Dimension (W/L)				This Work			
	PMOS (500/1.2)		NMOS (500/1.2)		Gate-Couple PTLSCR		Gate-Couple NTLSCR	
Layout Area ($\mu m \times \mu m$)	158 X 92		166 X 100		110.2 X 68.3		107.0 X 65.2	
ESD-Sress Condition	PD-Mode	ND-Mode	PS-Mode	NS-Mode	PD-Mode	ND-Mode	PS-Mode	NS-Mode
HBM ESD Failure Voltage (V)	above 8000	-3000	1200	above -8000	above 8000	-5750	above 8000	above -8000
MM ESD Failure Voltage (V)	450	-350	150	-850	750	-500	600	-700

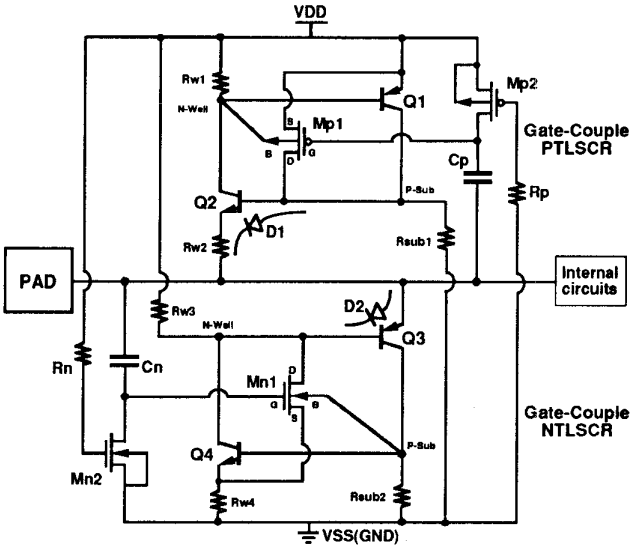

Fig.1 The proposed ESD protection circuit.

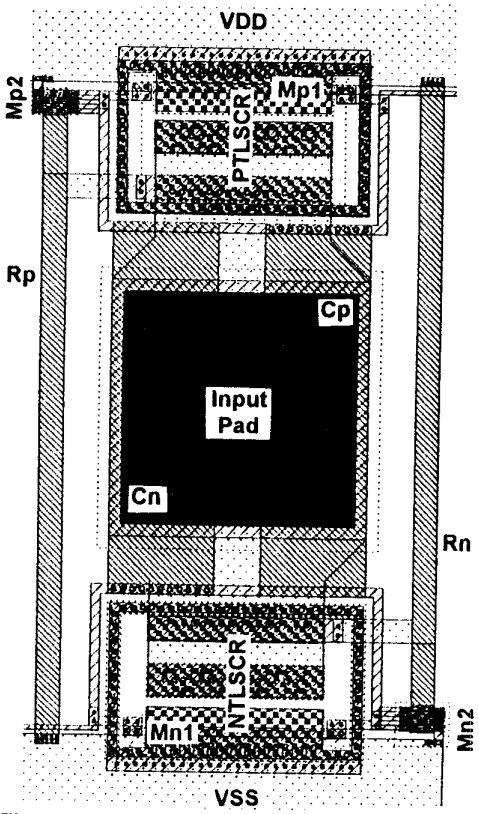

Fig.3 A practical layout example of the proposed ESD protection circuit.

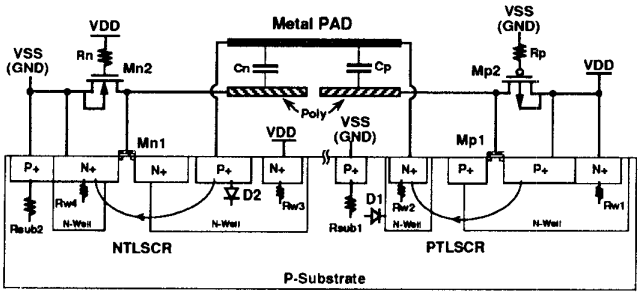

Fig.2 Schematic cross-sectional view of the gate-couple PTLSCR and NTLSCR devices.

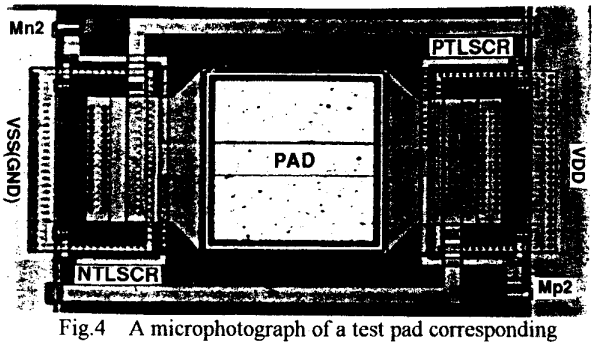

Fig.4 A microphotograph of a test pad corresponding to the layout of Fig.3.

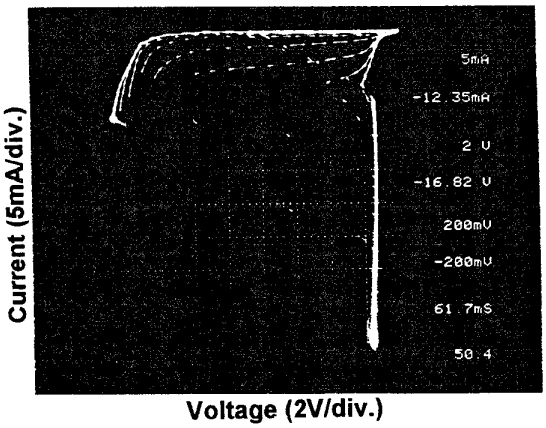

Fig.5 The I-V characteristics of PTLSCR with different negative voltage on the gate of Mp1.

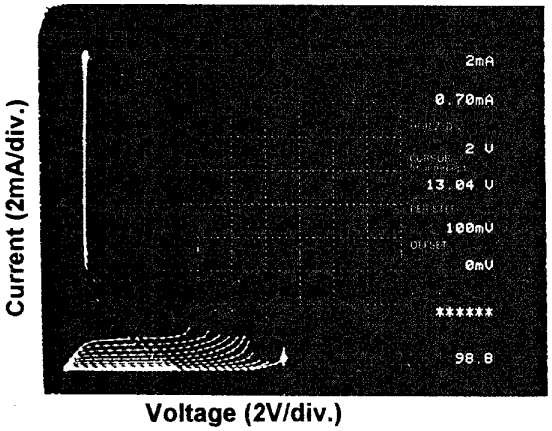

Fig.6 The I-V characteristics of NTLSCR with different positive voltage on the gate of Mn1.

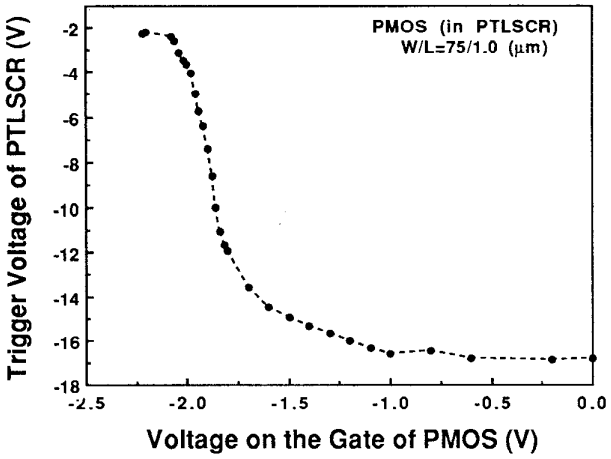

Fig.7 The dependence between the trigger voltage of PTLSCR and the voltage on the gate of Mp1.

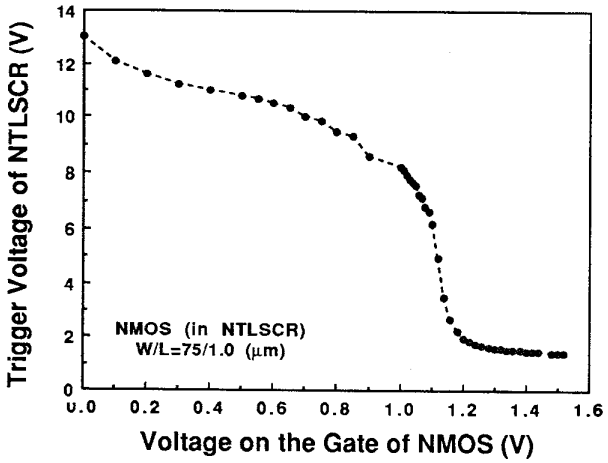

Fig.8 The dependence between the trigger voltage of NTLSCR and the voltage on the gate of Mn1.

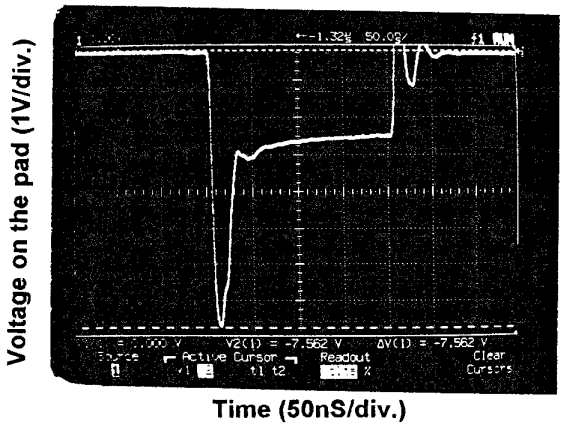

Fig.9 Measured voltage waveform to find the ESD-trigger voltage of gate-couple PTLSCR.

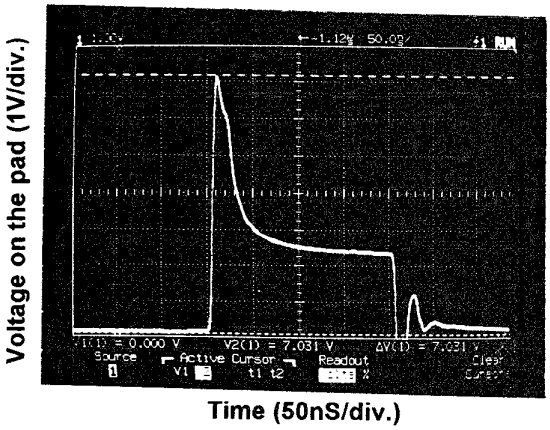

Fig.10 Measured voltage waveform to find the ESD-trigger voltage of gate-couple NTLSCR.