EFFICIENT LAYOUT STYLE OF CMOS OUTPUT BUFFER TO IMPROVE DRIVING CAPABILITY OF LOW–VOLTAGE SUBMICRON CMOS IC's

Ming-Dou Ker, Chung-Yu Wu, Tao Cheng, Hun-Hsien Chang,
Michael J.-N. Wu*, and T.-L. Yu*

Integrated Circuits and Systems Laboratory
Institute of Electronics, National Chiao-Tung University
Hsinchu, Taipei, China
Fax:886-35-715412, E-mail: mdker@alab.ee.nctu.edu.tw

*Winbond Electronics Corporation
Science-Based Industrial Park, Hsinchu, Taipei, China

ABSTRACT

A novel square-type layout style is proposed to efficiently implement CMOS output buffer with larger W/L ratio into a smaller silicon layout area than that of conventional finger-type layout style. Using this proposed layout style, the driving capability of CMOS output buffer in low-voltage submicron CMOS IC's can be effectively improved without increasing more layout area.

INTRODUCTION

As CMOS technologies developed into submicron regime, the LDD (Light-Doped Drain) structure has been well used to overcome the hot-carrier injection problem. Moreover, the VDD power supply in deep submicron CMOS technology is also scaled down for better reliability concerns. With scaled-down VDD supply, the current driving/sinking capability of output buffer is also much degraded. But, the external (off-chip) loading effect does not be reduced in the most applications of CMOS IC's. Thus, for high-driving or heavy-loading output buffer, the NMOS and PMOS of the output buffer with scaled-down VDD power supply need much larger W/L ratio to offer the required driving/sinking currents to meet the specifications of applications. The device with larger W/L ratio occupies larger layout area, so the finger-type layout style has been conventionally used to reduce layout area of CMOS output buffer. However, in high-integration submicron IC's with high pin count, the layout area for each metal pad with the output buffer and ESD protection devices is much limited in order to reduce total die size of the IC.

In this work, a novel layout style is proposed to implement CMOS output buffer with higher driving/sinking capability than that implemented by the conventional finger-type layout style within the same layout area. Thus, the

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driving/sinking capability of a low-voltage CMOS IC can be improved without increasing its die size to save cost.

SQUARE-TYPE LAYOUT FOR CMOS OUTPUT BUFFER

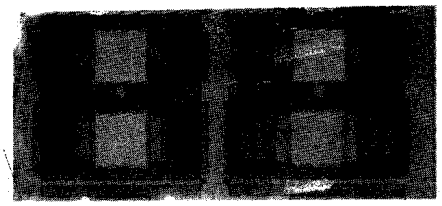
One set of output buffers with different W/L ratios in conventional finger-type layout style and this proposed square-type layout styles has been designed and fabricated by a 0.5-μm 3-V CMOS SRAM process to verify the layout area efficiency. Fig.1 is a microphotograph of the part of output buffers with both finger-type and square-type layout styles. The zoomed microphotographs of the NMOS device in output buffer with conventional finger-type and square-type layout styles are shown in Fig.2(a) and 2(b), respectively. In Fig.2(b), the large-dimension NMOS device is separated into 15 small-dimension NMOS devices. Each small-dimension NMOS is schematically drawn in square-type layout.

EXPERIMENTAL RESULT

The driving/sinking capability of output buffer can be shown by the measured I-V curves of NMOS and PMOS devices in the output buffer, as shown in Fig.3(a) and 3(b), respectively. In Fig.3(a), the channel width/length of NMOS device is 300/0.8 (320/0.8) μm for finger-type (square-type) layout style and its maximum drain current is 66.41(90.31) mA with 3.0-V VDD power supply. So, the maximum NMOS sinking current density per channel width is about 0.2214 (0.2822) mA/μm for finger-type (square-type) output buffer. In Fig.3(b), the channel width/length of PMOS device is also 300/0.8 (320/0.8) μm for finger-type (square-type) layout style and its maximum drain current is 29.62 (39.95) mA with 3.0-V VDD power supply. So, the maximum PMOS driving current density per channel width is about 0.0987 (0.1248) mA/μm for finger-type (square-type) output buffer. From above data, it is clear shown that the maximum driving (sinking) capability of output buffer with square-type layout style is improved 26.44% (27.46%) more than that with conventional finger-type layout style.

CONCLUSION

A novel square-type layout style of output buffer has been experimentally verified to show about 27% improvement on area efficiency than that of conventional finger-type layout style. This proposed square-type CMOS output buffer can provide CMOS IC's with higher driving/sinking capability in a smaller layout area. It will be very suitable for high-density low-voltage submicron CMOS VLSI/ULSI in high-driving or heavy-loading applications.



finger-type square-type

Fig.1 A microphotograph of CMOS output buffers with finger-type and square-type layouts.

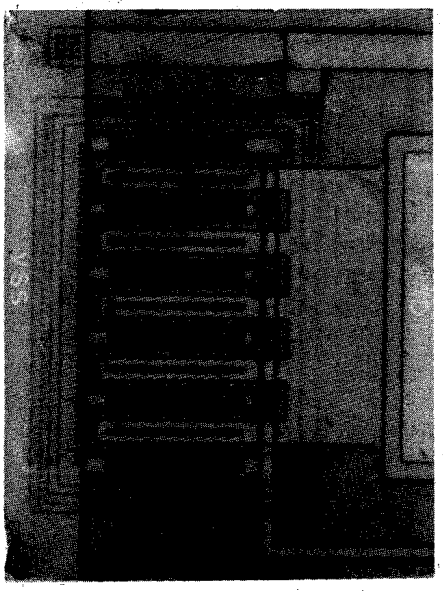


Fig.2(a) Zoomed microphotograph of NMOS device in finger-type layout style.

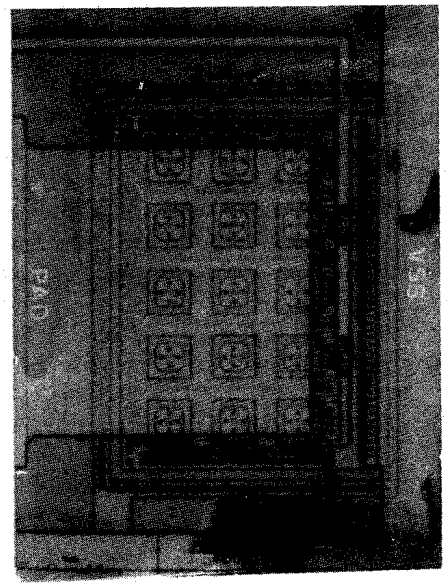


Fig.2(b) Zoomed microphotograph of NMOS device in square-type layout style.

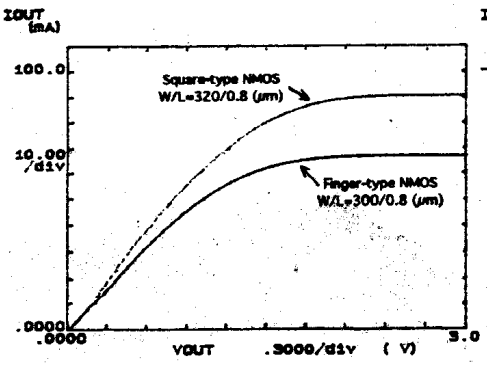


Fig.3(a) Measured I-V curves of finger-type and square-type NMOS devices in the output buffers under Vgs=VDD=3V condition.

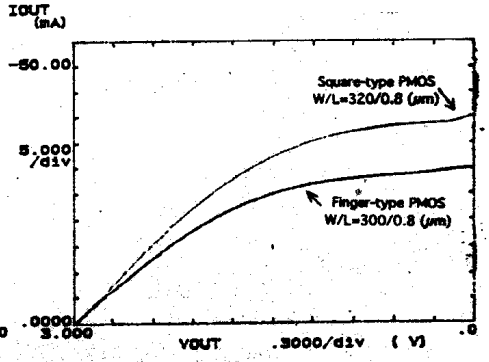


Fig.3(b) Measured I-V curves of finger-type and square-type PMOS devices in the output buffers under Vgs=-VDD=-3V condition.