On-Chip ESD Protection Using Capacitor–Couple Technique in 0.5–μm 3–V CMOS Technology

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Abstract – Capacitance-coupling effect used to lower snapback voltage and to ensure uniform ESD current distribution in the NMOS/PMOS devices of submicron CMOS on-chip ESD protection circuits is proposed. The couple capacitor is made by a ploy layer right under the wire-bonding metal pad without increasing extra layout area to the pad. By using this technique, ESD robustness of submicron CMOS IC's can be significantly improved.

I. Introduction

As CMOS technology is scaled down into deep submicron regime, the advanced processes, such as thinner gate oxide, shorter channel length, shallower source/drain junction, LDD structure, and silicided diffusion, much degrade ESD robustness of deep submicron CMOS IC's [1]-[2]. To achieve the same required ESD robustness, the protection devices in submicron CMOS ESD protection circuits often need to be designed with much larger dimensions than those in traditional long-channel CMOS technologies. But from the practical viewpoint of submicron CMOS IC's in high-integration applications, the pin counts of a submicron CMOS IC are often more than 200. In such high-pin-count submicron CMOS IC's, the pad pitch is reduced to around 100 μm. The layout area available for each input (or output) pad with the ESD protection circuit including latchup guard rings is also seriously limited. Hence, an ESD protection circuit requested to offer better ESD protection performance within smaller layout area becomes more difficult to be designed in submicron CMOS technology.

Recently, some efforts have been contributed to improve ESD robustness of thin-oxide NMOS device in submicron CMOS technology by ensuring uniform ESD current distribution among the fingers of device with large dimension [3]-[6]. In [4], a thin-oxide NMOS device is arranged to couple ESD transient voltage through a parasitic drain-to-gate capacitance to the main ESD-discharging thin-oxide NMOS device to ensure uniform ESD charge flow in ESD events. A "GCnMOS" structure [5]-[6], in which a field-oxide NMOS device was used to couple ESD transient voltage to the gate of thin-oxide NMOS device, was designed to uniformly turn on the multiple fingers of thin-oxide NMOS during ESD transition. By the gate-couple method, the ESD failure threshold of submicron thin-oxide NMOS device in output buffer was effectively improved [5]-[6]. But, the field-oxide or thin-oxide devices used to couple ESD transient voltage to the gate of main discharging devices occupy more extra layout area to the pads with such ESD protection circuits.

Moreover, the gate oxide is scaled down to only 90±10Å in a 0.5-μm 3-V CMOS technology which could be ruptured by a voltage only about 9~12V across it. The initial turn-on voltage of NMOS/PMOS with its gate shorted to its source is related to the snapback voltage due to punchthrough or avalanche breakdown at the drain [7]. But, the snapback voltage of short-channel NMOS/PMOS device which is used to protect the input gate is in the range of 10~11V. This leads to possible damage on the input gate. Thus, the voltage different between the gate-oxide and snapback breakdown of NMOS/PMOS is an important voltage margin for ESD design. In some submicron CMOS process, an extra ESD-implant step is inserted into the process flow to lower snapback voltage and to improve ESD protection capability. This also increases the cost and complexity of submicron CMOS technology.

In this paper, a capacitor-couple ESD protection scheme is proposed not only to ensure uniform ESD current distribution but also to lower snapback voltage of NMOS/PMOS devices in submicron CMOS ESD protection circuits. This proposed ESD protection circuit can provide better ESD-protection effectiveness with NMOS/PMOS devices in deeper submicron CMOS IC's without increasing extra layout area to the pad.

II. Capacitor-Couple ESD Protection Circuit

The curves shown in Fig.1 are I-V characteristics of drain breakdown of a short-channel NMOS in a 0.8-μm CMOS technology under various gate voltage biasing. It can be obviously seen that the snapback voltage of NMOS decades as the gate voltage increases. The short-channel PMOS also has similar I-V characteristics to those of NMOS. Fig. 2 shows the effect of snapback voltage lowering by gate voltage, which is measured from a NMOS device of W/L=50/0.8 μm. This effect lights us a way to protect the thinner gate oxide of deeper submicron CMOS IC's more effective even without ESD-implant process.

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The capacitor-couple ESD protection scheme to ensure uniform ESD current flow, as well as, to much lower the initial turn-on voltage of ESD-protection NMOS/PMOS devices is shown in Figs.3(a)-(c). Fig.3(a) shows the capacitor-couple CMOS ESD protection circuit by using additional Cn and Cp capacitors arranged from the input pad to the gates of NMOS and PMOS, respectively. If a positive (negative) ESD voltage occurs at the input pad with relatively grounded VDD (VSS) and floating VSS (VDD), the parasitic diode Dp1 in PMOS (Dn1 in NMOS) will forward conduct to bypass ESD current. But, the positive (negative) ESD transient voltage will be coupled to the gate of NMOS (PMOS) through capacitor Cn (Cp) under PS-(ND-) mode ESD stress [Positive (Negative) ESD voltage at the pad with grounded VSS (VDD) but floating VDD (VSS)]. The coupled positive (negative) voltage on the gate of NMOS (PMOS) is sustained longer in time by the Rn (Rp) resistor to effectively lower the snapback voltage of NMOS(PMOS). Thus the NMOS and PMOS devices can be more uniformly turned on with much lower initial turn-on voltage under ESD transitions. The magnitude and holding time of ESD-transient coupled voltage on the gate of NMOS (PMOS) can be adjusted by Cn and Rn (Cp and Rp) to make the ESD protection device active only in ESD-stress events but inactive in normal operating conditions of CMOS IC's.

To achieve the capacitor-couple effect without increasing total layout area to the pad, a schematic cross-sectional view of ESD protection circuit with the capacitors is shown in Fig.3(b) where Cn and Cp are realized by inserting the ploy layers right under the metal pad. Rn and Rp are also realized by ploy lines with sheet resistance in a 0.5-μm CMOS technology. A layout example is drawn in Fig.3(c) with NMOS and PMOS of W/L=500/1.0 μm as well as the ploy lines to realize Cn, Cp, Rn, and Rp.

III. Experimental Results

One set of ESD protection circuits with and without capacitor-couple effect has been designed and fabricated by a 0.5-μm 3-V CMOS technology. A microphotograph of the fabricated capacitor-couple ESD protection circuit corresponding to the layout in Fig.3(c) is shown in Fig.4.

An NMOS (PMOS) device with W/L=20/1.0μm is also designed with its gate connected to the gate of ESD-protection NMOS (PMOS) to monitor this capacitor-couple effect. The setup to measure this effect is shown in Fig.5 with the ESD-protection NMOS, Mn1, and a monitor NMOS, Mn2. The gate voltage of Mn1 will rise from zero if an sharp-rising ESD-like positive voltage pulse is applied to the input pad. The voltage coupled to the gate of Mn1 can be monitored by the Mn2 device due to their gates are connected together. If the gate of Mn1 (also of Mn2) is coupled to some voltage level through the designed Cn and Rn, this coupled gate voltage will turn Mn2 on and cause current flowing through the external resistor R. Thus, the voltage at the node "x" will drop down from 5V synchronously when the input voltage pulse is applied.

A typical measured result is shown in Fig.6, where an input pulse with rising peak of 5.625V (CH1) can cause a maximum voltage drop (at x node) of 1.687V (CH2) from 5V of external biased voltage source. This 1.687-V voltage drop on the external R of 9.11KΩ will cause a drain current of 0.185mA into Mn2. By measured the I-V characteristics of a separated NMOS device the same as Mn2 in the same test chip, the corresponding gate voltage due to capacitor-couple effect can be found out to be 1.003V. Fig.7 shows the efficiency of voltage coupling to the gate of ESD-protection NMOS due to pulse-type trigger voltage applied to input pad with different peak voltage level.

In Fig.6, the dashed lines are used to show the holding time as long as 2.37μs as the coupled voltage at the gate is sustained higher than 0.8V (the corresponding voltage drop at CH2 is 0.5V). From above measured results, the coupling effect of Cn (Cp) and voltage holding capability of Rn (Rp) can be verified. For practical applications in different submicron CMOS technologies, the Cn (Cp) and Rn (Rp) can be designed by *HSPICE* simulation to meet the required specifications of voltage coupled on the gate and voltage holding time.

The ESD failure threshold of ESD-protection NMOS (PMOS) of W/L=500/1.0 μm with this proposed capacitor-couple design is 5000V (3500V) in Human-Body-Mode (HBM) ESD testing. In Machine-Mode (MM) ESD testing, it can sustain 450V (250V) ESD stress. In general, ESD specifications for commercial products are set at 2000V (200V) in HBM (MM) ESD testing.

IV. Conclusion

A capacitor-couple ESD protection circuit has been successful designed, fabricated, and verified in a 0.5-μm 3-V CMOS technology. The experimental results show that it can offer more effective ESD protection for the much thinner gate oxide, not only to ensure uniform ESD current flow among the multiple fingers of ESD protection devices but also to much lower the initial turn-on voltage of ESD protection devices. This proposed ESD protection scheme is very suitable for deeper submicron CMOS IC's to against ESD damages without increasing extra layout area to the pad.

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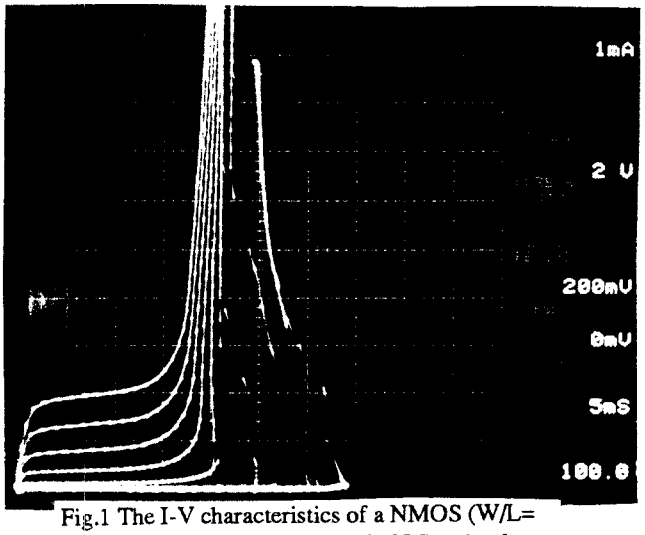

Fig.1 The I-V characteristics of a NMOS (W/L= 50/0.8 μm) in a 0.8-μm CMOS technology.

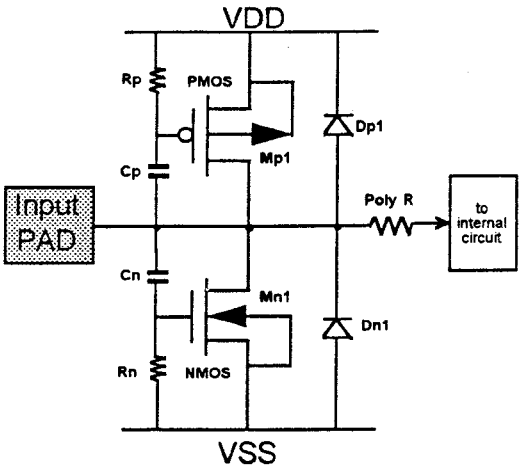

Fig.3(a) The Capacitor-Couple CMOS ESD protection circuit.

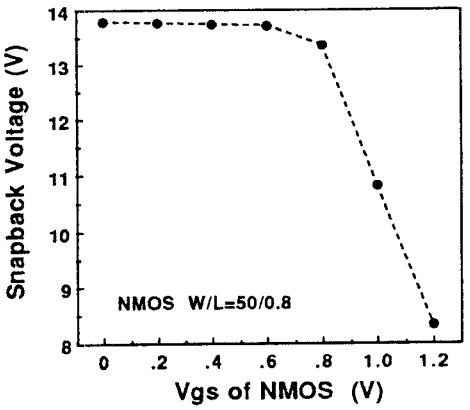

Fig.2 The effect of snapback voltage lowering by gate voltage increasing.

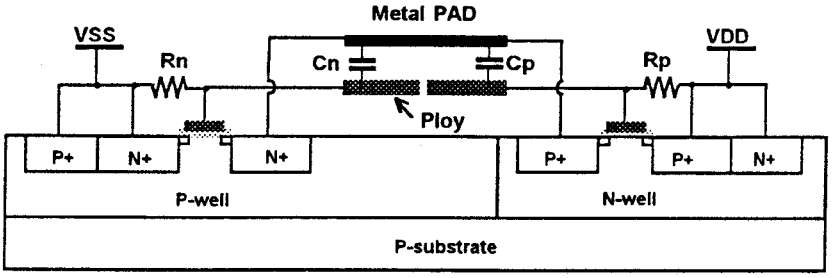

Fig.3(b) Schematic cross-sectional view of the proposed circuit in Fig.3(a).

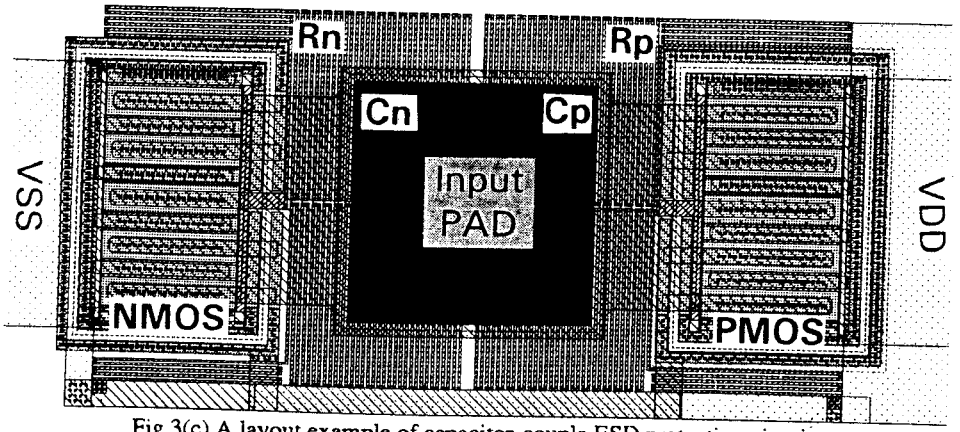

Fig.3(c) A layout example of capacitor-couple ESD protection circuit. The dimensions of NMOS and PMOS are 500/1.0 μm. Cn, Cp, Rn, and Rp are realized by ploy layers.

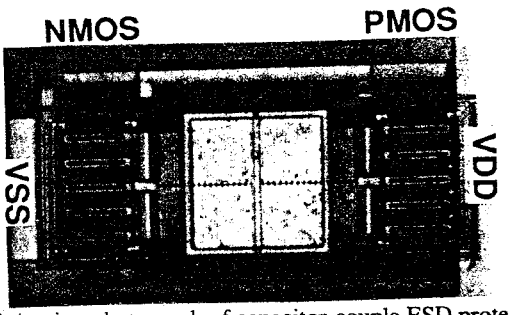

Fig.4 A microphotograph of capacitor-couple ESD protection circuit corresponding to the layout of Fig.3(c).

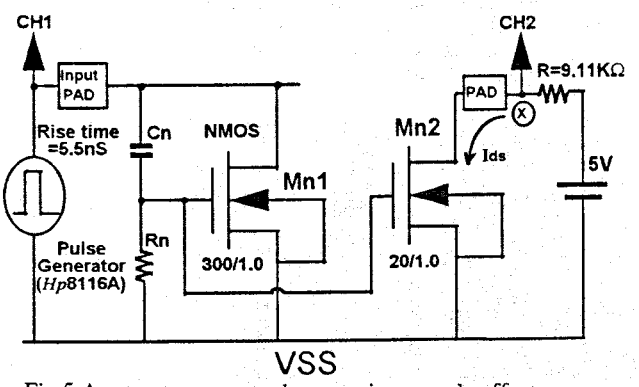

Fig.5 A setup to measure the capacitor-couple effect. An oscilloscope with two channels is used to monitor the variation of voltage waveforms.

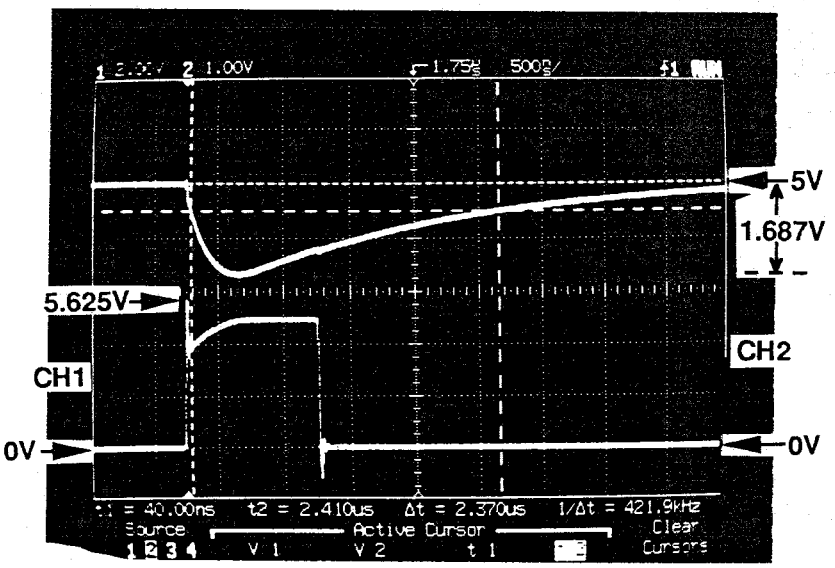

Fig.6 Measured results of capacitor-couple effect.
CH1 (2V/div) is the voltage pulse applied to the input pad.
CH2 (1V/div) is the voltage at node "x" of Fig.5.
The time scale is 500nS/div.

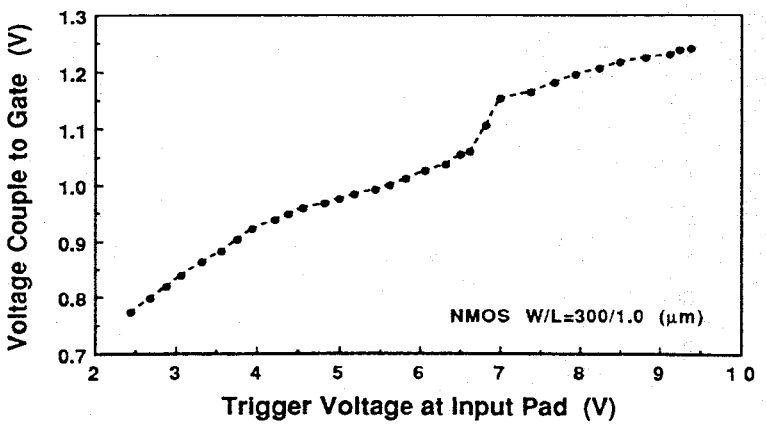

Fig.7 The measured results of capacitor-couple efficiency.