Area-Efficient Layout Design for Output Transistors with Consideration of ESD Reliability

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Abstract

A novel hexagon-type layout is proposed to realize large-dimension CMOS output transistors with smaller layout area but higher ESD reliability. The drain parasitic capacitance of hexagon-type layout is also smaller than that of traditional finger-type layout. Experimental results have shown that the maximum driving capability per layout area of output transistor with hexagon-type layout is improved 40% more than that with finger-type layout. This hexagon-type layout is very suitable for deep-submicron low-voltage CMOS IC's in high-density applications.

I. Introduction

As CMOS technology is scaled down into deep submicron regime, advanced processes much degrade ESD robustness of CMOS IC's [1]-[3]. To achieve the required ESD robustness, output transistors in deep-submicron CMOS IC's often need to be designed with larger device dimensions for ESD-protection consideration. Besides, in order to offer enough driving/sinking capability of CMOS output buffer in low-voltage applications (VDD= 3.3V, 2.5V, ...), the width/length (W/L) ratios of output NMOS and PMOS devices are generally enlarged up to several hundreds. But from practical viewpoint of high-integration applications in high-pin-count CMOS IC's, the pad pitch is reduced to around 100 μm. Layout area available for each output pad with output transistors including latchup guard rings is seriously limited.

In 1989, *Baker* proposed a *waffle*-type layout to enhance ESD hardness of NMOS output transistor [4]. In [4], the *waffle*-type layout had shown to offer better ESD protection capability than that in finger-type layout within the same layout area. In 1992, *Vemuru* made a comparison between the finger-type and *waffle*-type layout [5]. He found that *waffle*-type layout contributes about 10% area reduction to that of finger-type, as well as the *waffle*-type layout produces lower gate resistance suitable for wide-band or low-noise applications.

Recently, some efforts have contributed to investigate the relations between layout parameters and ESD hardness in CMOS devices of deep submicron technologies. It is found that the spacing from drain contact to the edge of gate oxide is an important layout parameter to affect ESD reliability of CMOS devices [6]-[7]. Larger spacing from drain contact to gate-oxide edge leads to higher ESD robustness. This minimum spacing is found to be about 5~6 μm in submicron CMOS technologies to sustain better ESD protection without much increasing layout area. But in *waffle*-type layout, the spacing of source contact and drain contact to the edge of gate oxide are required to be the same. In traditional finger-type layout, the spacing of drain contact to the gate-oxide edge can be different to the spacing of source contact to the gate-oxide edge. Due to this spacing constraint of drain contact to its gate-oxide edge for ESD-reliability consideration in deep submicron CMOS technologies, the *waffle* type will occupy more layout area than the traditional finger type under the same W/L ratio.

In this paper, a new layout method is proposed with ESD-reliability consideration to realize CMOS devices of output buffer in smaller layout area.

II. Traditional Finger-Type Layout

The traditional finger-type layout for NMOS device is shown in Fig.1. Its cross-sectional view along the line A--A' in Fig.1 is shown in Fig.2, which is demonstrated in n-well/p-substrate CMOS process. In Fig.1, a large-dimension NMOS device is separated as four parallel small-dimension NMOS devices. There are four fingers of poly gate, two fingers of drain, and three fingers of sources. The spacing from drain contact to poly-gate edge is marked as "d". The spacing from source contact to poly-gate edge is marked as "S". For better ESD robustness of CMOS output buffer in submicron CMOS technologies, this "d" spacing is found to be about 5~6 μm. But, the "S" spacing has no important effect on ESD reliability of CMOS output buffer. This "S" spacing is often used as 1 μm in practical layout. Outside the source region, there are two latchup guard rings surrounding whole NMOS device. One is P+ diffusion connected to ground(GND) to offer substrate bias. The other is N+ diffusion connected to VDD as a dummy collector to prevent CMOS latchup. In CMOS output buffer, double guard rings for NMOS and PMOS devices are often specified in the design rules of CMOS technologies to prevent CMOS latchup problem.

But in traditional finger-type layout, there is an important spacing denoted as "S2" in Fig.1, which often degrades ESD robustness of CMOS output buffer. To explain this "S2" spacing, a schematic cross-sectional view along the line B--B' is shown in Fig.3. In Fig.3, there exists a parasitic diode D1 between the P+ diffusion (connected to GND) and N+ diffusion of drain.

The spacing from the edge of P+ diffusion to the edge of N+ diffusion is marked as "S2". If S2 spacing is too small, diode D1 will be first broken down to conduct ESD current by a positive ESD voltage occurred on the output pad, before the NMOS drain is broken down. Because the spacing of drain in this side is much smaller than that of drain to its source side, this diode D1 is very weak to ESD stress if S2 is too small. Thus, with consideration of ESD reliability, this S2 spacing has better to be greater than the spacing from the drain-contact edge to source-contact edge. But, the total layout area will be increased.

III. Novel Hexagon-Type Layout

To reduce layout area for cost saving and to overcome the parasitic diode D1 in traditional finger-type layout of CMOS output transistors, a multiple-cell hexagon-type layout design is proposed. The schematic multiple-cell hexagon-type layout of output NMOS device is shown in Fig.4. The schematic cross-sectional view along the line A--A' in Fig.4 is also the same as that shown in Fig.2. This multiple-cell hexagon-type layout can be implemented in any CMOS or BiCMOS technologies. It can be also used to implement PMOS devices. In Fig.4, there are four small-dimension hexagon cells to form a large-dimension NMOS device. Each small-dimension hexagon cell is identical to each other. The black hexagon region in the center of a hexagon cell is the drain contact of NMOS device. The poly gate in each hexagon cell is also drawn in hexagon shape. The N+ diffusion of source is also drawn in hexagon shape and surrounds the gate and drain regions. The contacts at source side are also placing in hexagon-shape arrangement. Outside NMOS device, there is a P+ diffusion in p-substrate connected to ground to offer substrate bias for normal CMOS operations. This P+ diffusion is surrounding whole NMOS device. Besides, there is an N+ diffusion surrounding this P+ diffusion. This N+ diffusion connected to VDD works as latchup guard ring for output NMOS device. All layout elements in a hexagon cell, including the placement of contacts, have to be made as symmetrically as possible to ensure uniform current flow in the NMOS device so as to increase its ESD reliability. In Fig.4, the NMOS device is assembled by four basic hexagon cells. An NMOS device with larger dimension can be assembled by this way. The number of hexagon cells can be designed for different device dimensions (W/L ratios).

With this proposed layout technique, there is no "S2" spacing in the hexagon-type layout. The layout area due to "S2" spacing in the traditional finger-type layout can be saved. Moreover, there is no parasitic diode D1 to directly close the edge of drain region, so ESD robustness of output devices is not degraded.

To verify area efficiency, comparisons of total layout area between traditional finger-type layout and hexagon-type layout are made. Fig.5 shows a comparison of total layout area between finger-type and hexagon-type layout under the spacing "d" (drain contact to poly-gate edge) of 5μm. The total layout area includes double latchup guard rings of "S1=14.2μm" in both finger-type and hexagon-type layout. In hexagon-type layout, the edge "C" of drain contact is 2μm. In traditional finger-type layout, the "S2" spacing is 4μm. The length of each poly finger in the traditional finger-type layout is equal to each other, but this poly-finger length is limited below 50μm in most CMOS design rules for better ESD reliability. In Fig.5, as the spacing "d" is 5μm, the area of hexagon-type layout with larger device width (W) is significantly reduced as compared to that of finger-type layout. In Fig.5, as device dimension (W/L) is 840/0.8 (μm), the total layout area in traditional finger-type layout is 11484 μm^2, but that in hexagon-type layout is only 10296 μm^2. This shows the excellent area efficiency of hexagon-type layout about 11% reduction on total layout area of finger-type layout. Fig.6 shows the relations between device width (W) and the percentage of hexagon-type to finger-type area ratio under different spacings of "d". It is clear shown that the hexagon-type layout can significantly reduce total layout area as spacing "d" is required to be larger.

Moreover, the drain-to-bulk parasitic capacitance at output node is also reduced by this multiple-cell hexagon-type layout. Fig.7 shows a comparison of total drain capacitance between finger-type and hexagon-type layout under spacing d of 5μm. Drain parasitic capacitance in hexagon-type layout is only about 65% of that in finger-type layout under the same device dimension. With lower drain capacitance, this hexagon-type layout is more suitable for CMOS output buffer in high-frequency applications.

IV. Experimental Results

One set of output buffers with different W/L ratios in finger-type layout and the proposed hexagon-type layout has been designed and fabricated by a 0.6-mm CMOS process. A microphotograph of NMOS device in output buffer with hexagon-type layout is shown in Fig.8. The hexagon-type output NMOS in Fig.8 has 14 basic hexagon cells to form total device dimension (W/L) of 588/1.0 (mm).

The measured drain current of output NMOS between finger-type and hexagon-type layout is shown in Fig.9 under different channel widths. The measured condition is with Vgs=3V and Vds=3V or 0.4V to find the sinking current from the output pad. To verify area efficiency, the drain current of output NMOS between finger-type and hexagon-type layout is also compared with parameter of total layout area in Fig.10. From experimentally measured data, the maximum drain current per layout area of output NMOS with hexagon-type layout is improved 40% more than that with finger-type layout. This verifies excellent advantage of hexagon-type layout on area reduction to save silicon cost of CMOS IC's.

The ESD failure voltage of output NMOS with hexagon-type layout is also tested in Human-Body Model (HBM) ESD. The minimum HBM ESD failure voltage of hexagon-type output NMOS with device

dimension (W/L) of 336/1.0 (μm) is as high as 4500V. Larger device dimension leads to higher ESD failure voltage. The ESD failure voltage of hexagon-type layout is much higher that of 2000-V commercial specification.

V. Conclusion

With theoretical calculation and experimental verification, a multiple-cell hexagon-type layout design has been proposed to realize output transistors in deep-submicron low-voltage CMOS IC's within much smaller layout area. By applying this hexagon-type layout to output buffers of CMOS IC, total layout area of a high-pin-count chip can be significantly reduced. The drain-to-bulk parasitic capacitance at the output pad is also reduced by this hexagon-type layout. This hexagon-type layout can be realized in any CMOS and BiCMOS technologies to save silicon cost.

References

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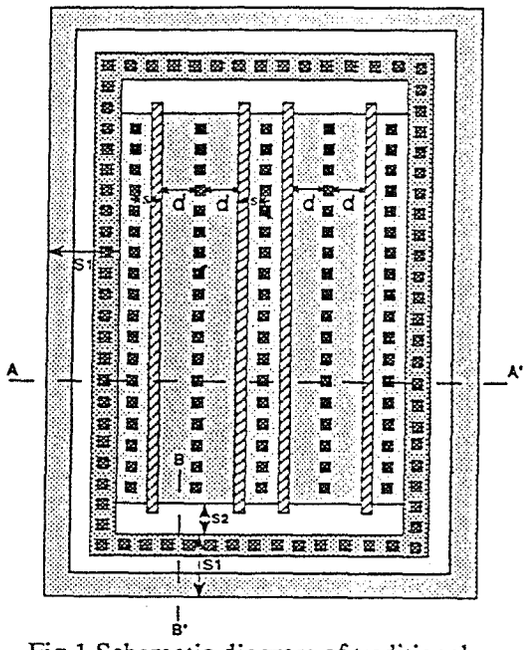

Fig.1 Schematic diagram of traditional figner-type layout.

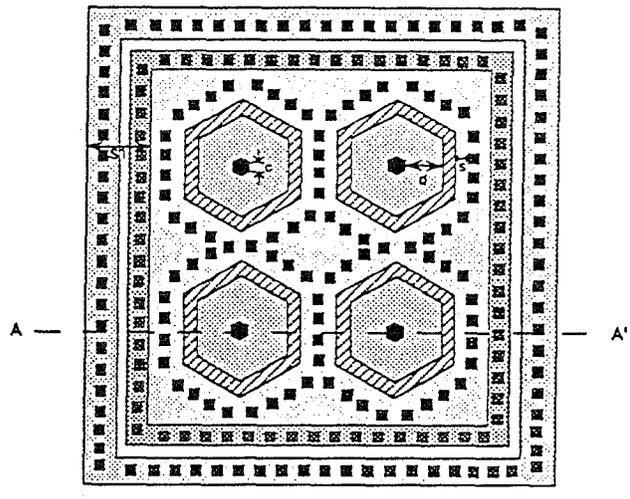

Fig.4 Schematic diagram of the proposed hexagon-type layout.

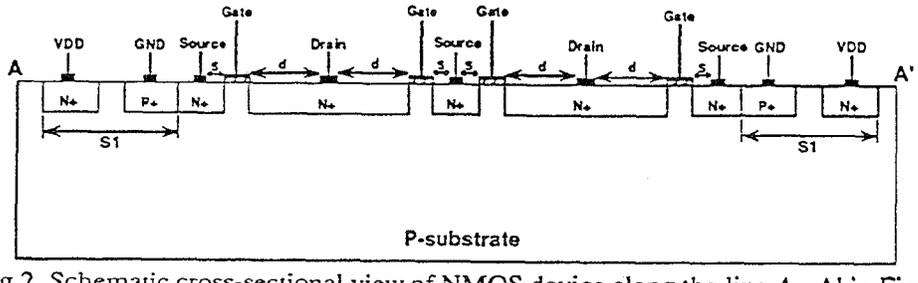

Fig.2 Schematic cross-sectional view of NMOS device along the line A--A' in Fig.1.

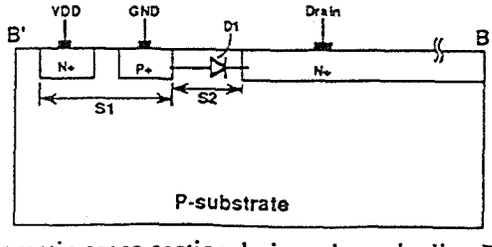

Fig.3 Schematic cross-sectional view along the line B--B' in Fig.1.

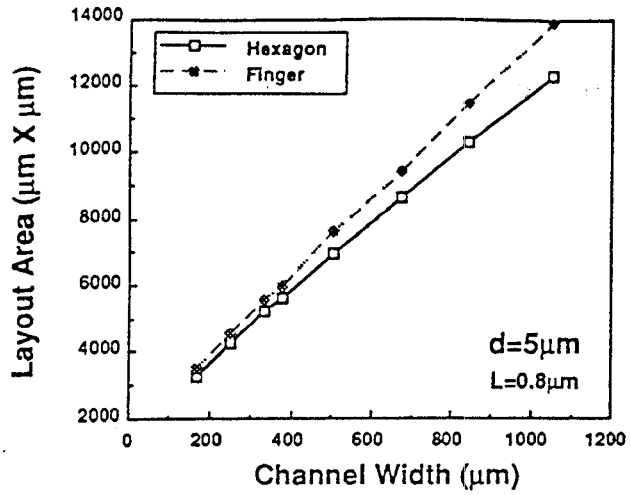

Fig.5 Comparison of layout area between traditional finger-type layout and hexagon-type layout with spacing d of 5μm under different device widths.

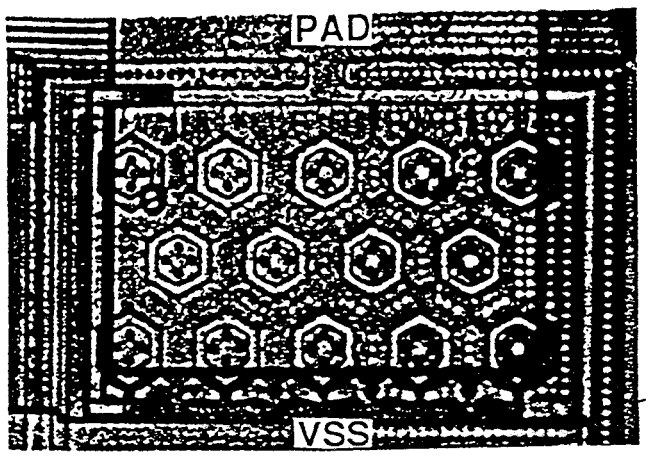

Fig.8 A microphotograph of NMOS device in output buffer with hexagon-type layout.

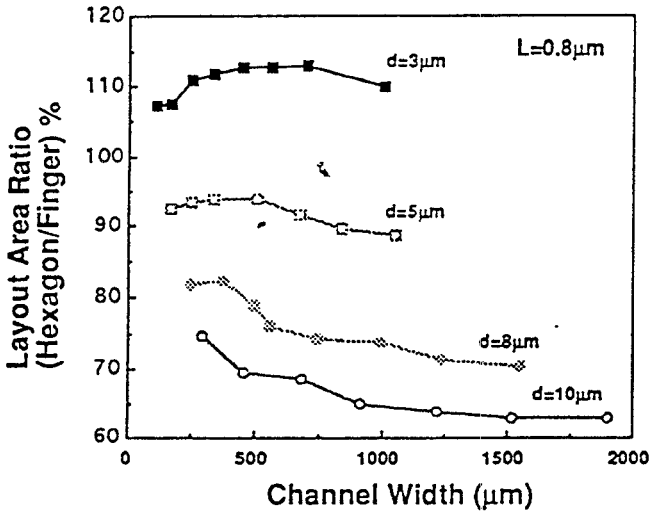

Fig.6 Relation between device width and the percentage of hexagon-to-finger area ratio under different spacing of "d".

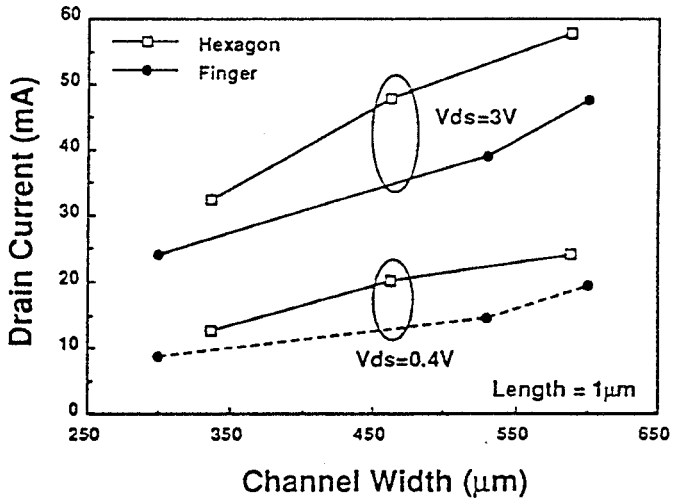

Fig.9 Measured drain current of output NMOS between finger-type and hexagon-type layout under different channel widths. (Vgs=3V, Vds=3V or 0.4V)

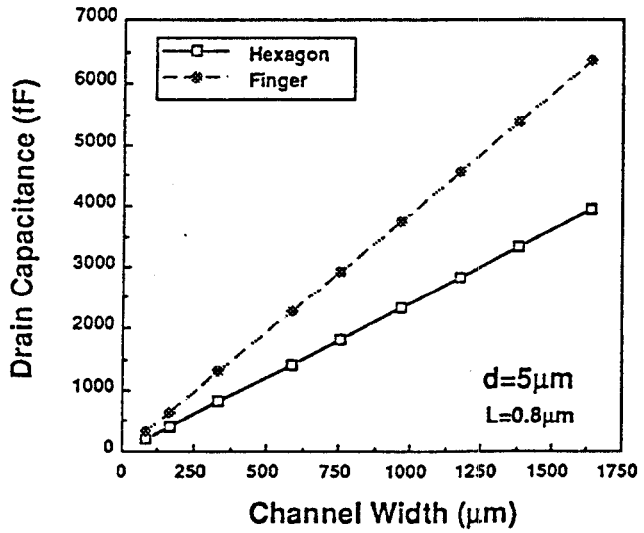

Fig.7 Comparison of total drain capacitance between finger-type and hexagon-type layout under spacing d of 5μm.

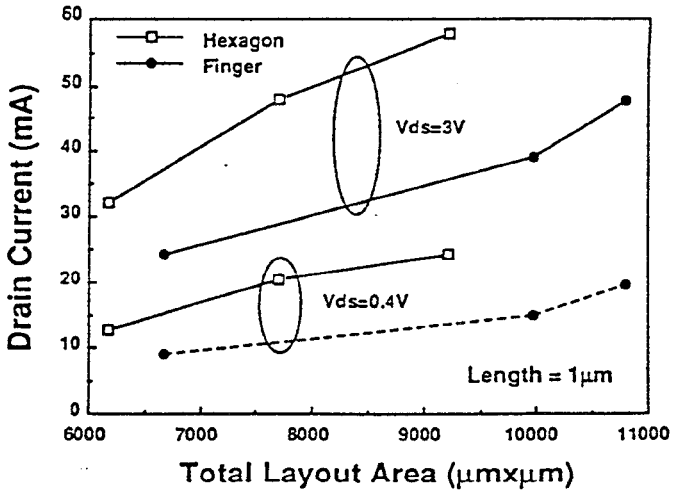

Fig.10 Comparison of drain current of output NMOS between finger-type and hexagon-type layout with total layout area consideration.