ESD Reliability of Thinner Gate Oxide in Deep-Submicron Low-Voltage CMOS Technology

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Abstract

Capacitor-couple technique used to early turn on CMOS on-chip ESD protection circuit and to ensure uniform ESD current distribution is proposed. A timing-original design model is also derived to calculate capacitor-couple efficiency for the ESD protection circuit. Using this capacitor-couple technique, ESD reliability of thinner gate oxide in deep-submicron low-voltage CMOS IC's can be effectively improved.

I. Introduction

Electrostatic discharge (ESD) has become a challenging issue on reliability of IC products in deep submicron process. The advanced processes of deep submicron CMOS technologies much degrade ESD reliability of CMOS IC's [1]-[2]. Moreover, in low-voltage applications, thickness of gate oxide is scaled down to be thinner and thinner. For example, the gate-oxide thickness in a 0.5-μm 5-V CMOS technology is 140Å, but it is reduced to only 90Å in a 0.5-μm 3-V CMOS technology. This much thinner gate oxide is more sensitive to ESD stress.

In traditional ESD protection circuit for input pad, as shown in Fig.1, gate-grounded NMOS device is often used as a protection element to limit overstress voltage across the gate oxide of input devices by its drain snapback breakdown. But, the voltage margin between gate-oxide breakdown and drain snapback breakdown is also much reduced in deep-submicron low-voltage CMOS technology. Therefore, the thinner gate-oxide may be ruptured by ESD voltage before drain of protection NMOS into snapback breakdown. Recently, an extra mask of "ESD implant" is added into process flow to make a heavy-doped structure for input/output devices [3]-[4]. With extra ESD-implant process, drain breakdown voltage may be reduced to protect such thinner gate oxide. But, the cost of chip fabrication is also increased.

Since ESD voltage on a pad may have positive or negative polarities to both VDD and VSS(ground), there are four ESD-stress cases at each input or output pins as shown in Fig.2 [5]. These four modes of ESD stress can cause damage on both NMOS and PMOS devices in input stage or output buffer of CMOS IC's. In Fig.1, traditional ESD protection circuit is only arranged from the pad to VSS(GND). There is no ESD protection element arranged between the pad and VDD. Under ND-mode or PD-mode ESD stress, internal circuits are dangerous to ESD damage [6]-[7].

In this paper, a complementary capacitor-couple ESD protection circuit is proposed to effectively protect the thinner gate oxide and to avoid unexpected ESD damage on internal circuits of deep-submicron low-voltage CMOS IC's without extra ESD-implant process.

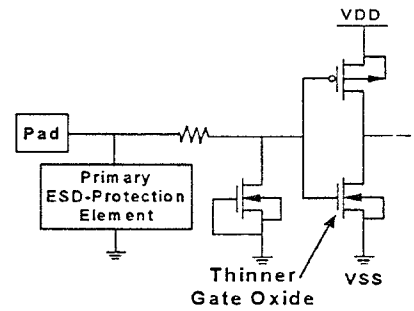

Fig.1 A traditional input ESD protection circuit with gate-grounded NMOS to clamp ESD voltage across the gate oxide of input stage.

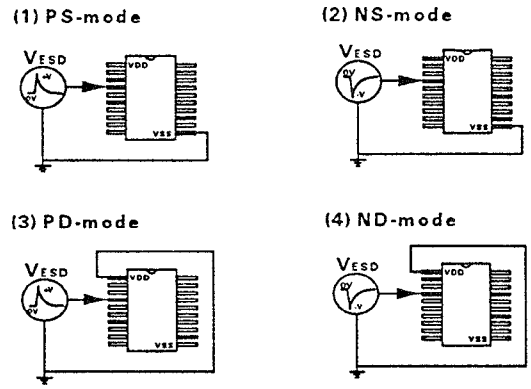

Fig.2 The four modes of ESD stress on an input (or output) pin of CMOS IC.

II. Capacitor-Couple ESD Protection Circuit

The ESD protection using complementary capacitor-couple technique is shown in Fig.3, where the capacitor-couple technique is realized by using additional Cn and Cp capacitors arranged from input pad to the gates of NMOS and PMOS devices in the ESD protection circuit, respectively. To achieve capacitor-couple effect without increasing total layout area to the pad, a schematic cross-sectional view of ESD protection circuit with the capacitors is shown in Fig.4, where Cn and Cp are realized by inserting poly layers right under the metal pad. Rn and Rp can be also realized by poly lines.

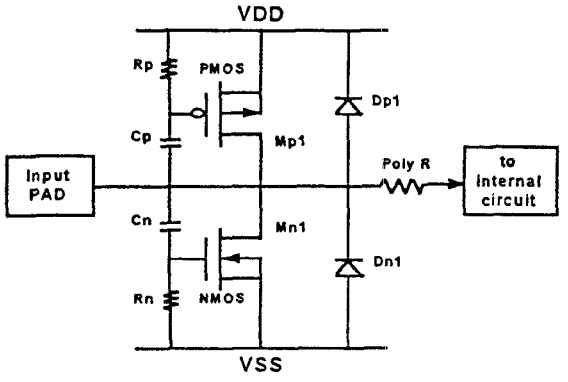

Fig.3 The capacitor-couple ESD protection circuit.

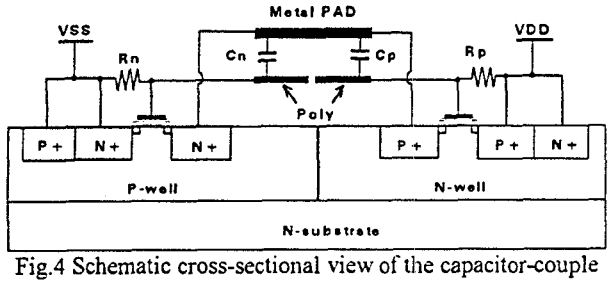

Fig.4 Schematic cross-sectional view of the capacitor-couple ESD protection circuit.

As NS-mode (PD-mode) ESD stress occurs on the input pad, diode Dn1 (Dp1) is forward biased to bypass ESD current. The negative (positive) ESD voltage on the input pad will be clamed to about -0.6V (+0.6V), so the internal circuits can be protected against ESD damage. Diode under forward-biased condition can sustain high ESD stress.

Under PS- (ND-) mode ESD stress, positive (negative) ESD transient voltage will be coupled to the gate of NMOS (PMOS) through capacitor Cn (Cp). The coupled positive (negative) voltage on the gate of NMOS (PMOS) is sustained longer in time by resistor Rn (Rp) to effectively turn on ESD-protection NMOS (PMOS). ESD current is bypassed through the early turned-on NMOS (PMOS), so the thinner gate oxide can be protected.

The four modes of ESD stress on the input pad are one-by-one protected by the capacitor-couple Mn1, diode Dn1, diode Dp1, and capacitor-couple Mp1, respectively. Thus, the internal circuit which is connected to this input pad can be fully protected against ESD damage in deep-submicron low-voltage CMOS IC's. The magnitude and holding time of ESD-transient voltage coupled to the gate of Mn1 (Mp1) can be adjusted by Cn and Rn (Cp and Rp) to make ESD-protection device active only in ESD-stress conditions but inactive in normal operating conditions of CMOS IC's.

III. Design of Capacitor-Couple Efficiency

A timing-original design model has been developed to find the suitable value for Cn (Cp) and Rn (Rp). The coupled gate voltage Vgs(t) on the gate of NMOS due to triggering of 10-V ramp voltage with rise time of 10ns on the input pad is calculated by the developed design model, and the result is shown in Fig.5. As Vgs is higher than Vtn (threshold voltage of NMOS), NMOS is turned on to bypass ESD current. The coupled gate voltage Vgs(t) is discharged through Rn, so the protection NMOS will become off again if Vgs drops below Vtn. The *ton* in Fig.5 is the turn-on time of NMOS. By adjusting Cn and Rn, *ton* becomes tunable for different applications.

The dependence of Cn and Rn on the turn-on time from 50 to 200 ns of protection NMOS under PS-mode stress condition with 10-V ramp input voltage is shown in Fig.6, in which model-calculation results agrees very well to HSPICE-simulation results. The undesired design region in Fig.6 means that Cn or Rn are over-designed in capacitor-couple ESD protection circuit. This causes voltage degradation on normal input signal, because voltage coupled to the gate of protection NMOS is above its threshold voltage. So, Rn and Cn in this undesired region should be avoided. In the adequate design region of Fig.6, protection NMOS is not triggered on by the normal input signal, but it can be triggered on by the 10-V 10-ns ramp voltage.

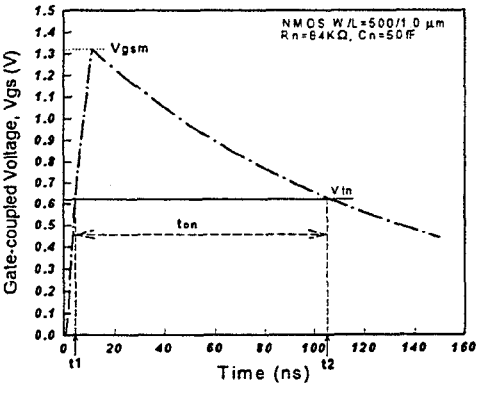

Fig.5 The coupled voltage waveform of Vgs(t) under the triggering of a 10-V ramp voltage with rise time of 10ns, which is calculated by the derived design model.

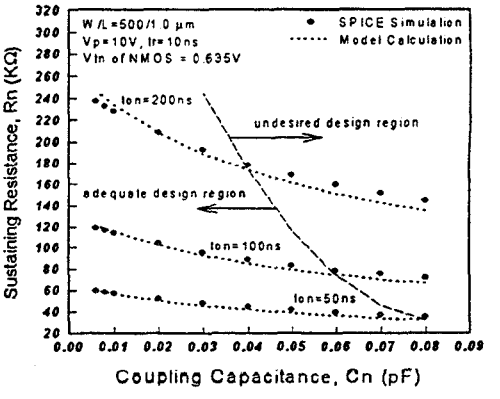

Fig.6 Overall relation between Cn and Rn under different NMOS turn-on time with both model-calculated and *HSPICE*-simulated results.

Another issue on capacitor-couple technique is the rise time of 10-V ramp voltage, which is used to simulate the ESD-transient voltage before gate oxide of input stage is ruptured. Rise time *tr* has been considered in the design model. The sensitivity of rise-time effect on the design of Cn and Rn is analyzed in Fig.7, where the NMOS turn-on time is kept as a constant of 100 ns to find the dependence of different rise time from 1 to 10 ns. In Fig.7, it is shown that the variation between different curves due to different rise time of 10-V input ramp voltage is below 5%. With suitable design on Rn and Cn, this capacitor-couple ESD protection circuit can perform effective ESD protection.

The dependence of PMOS turn-on time on Cp and Rp is also calculated by the design model and compared with *HSPICE*-simulated results. The adequate design region and undesired design region about Rp and Cp for protection PMOS to accurately operate in CMOS IC's is shown in Fig.8.

With wide-range verification and consideration on different turn-on time of protection NMOS/PMOS, device dimension of protection NMOS/PMOS, and different rise time of ESD-transient voltage before gate-oxide breakdown, suitable design of capacitor-couple ESD protection circuit can be easily obtained by this design model instead of iterative trial-and-error *HSPICE* simulation.

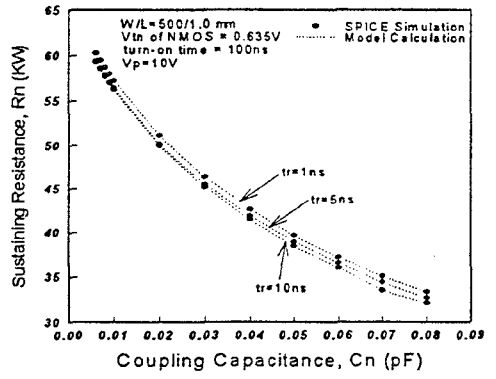

Fig.7 The relation of Cn and Rn to keep NMOS turn-on time of 100 ns under different rise time of the 10-V ramp voltage.

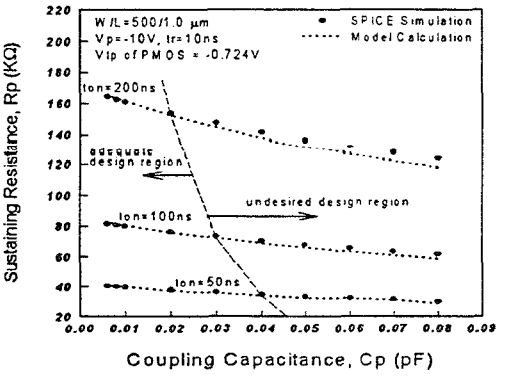

Fig.8 Overall relation between Cp and Rp under different PMOS turn-on time with both model-calculated and *HSPICE*-simulated results.

IV. Experimental Results

A microphotograph of the fabricated capacitor-couple ESD protection circuit is shown in Fig.9, which is fabricated by a 0.5-μm 3-V CMOS technology. The HBM (human-body-mode) and MM (machine-mode) ESD testing results with failure criterion of 1-μA current leakage under 5-V bias are shown in Figs.10 and 11, respectively. It is found that ESD pass voltage is almost linearly increased as channel width is increased either in HBM or MM ESD testing.

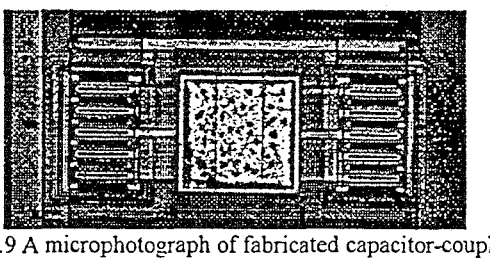

Fig.9 A microphotograph of fabricated capacitor-couple ESD protection circuit.

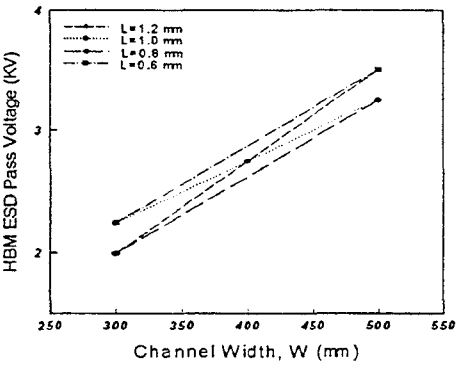

Fig.10 HBM ESD testing results of capacitor-couple ESD protection circuit with different device dimension.

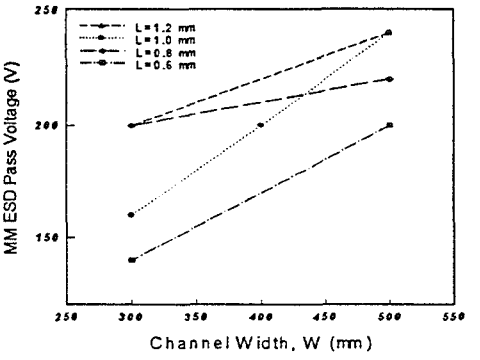

Fig.11 MM ESD testing results of capacitor-couple ESD protection circuit with different device dimension.

To monitor capacitor-couple efficiency, an NMOS (PMOS) device with W/L=20/1.0 (μm) is also designed with its gate connected to the gate of ESD-protection NMOS (PMOS). The setup to measure capacitor-couple efficiency under PS-mode and ND-mode ESD-stress conditions is shown in Figs.12 and 13, respectively. In Fig.12, a positive pulse-type voltage waveform with rise time of 5ns generated by pulse generator *Hp8116A* is

used to simulate PS-mode ESD-transient voltage and applied to the input pad. An oscilloscope is used to monitor voltage waveform in time domain to investigate capacitor-couple effect. The gate voltage of Mn1 will arise from zero if a sharp-rising ESD-like positive voltage pulse is applied to the input pad. The voltage coupled to the gate of Mn1 can be monitored by Mn2 device due to their gates are connected together. This coupled gate voltage will turn Mn2 on and cause current flowing through the external resistor Rext. Thus, the voltage at node "x" will be pulled down from 5V synchronously when the input voltage pulse is applied. Similar measuring principle is also applied in Fig.13 to verify capacitor-couple efficiency under ND-mode ESD-stress condition.

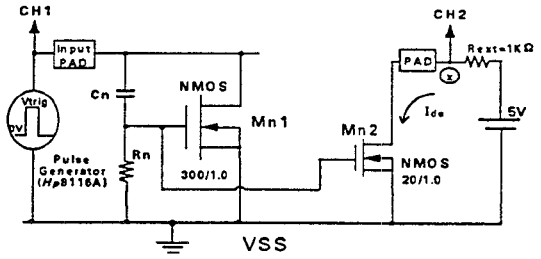

Fig.12 Experimental setup to measure capacitor-couple efficiency in PS-mode ESD-stress condition.

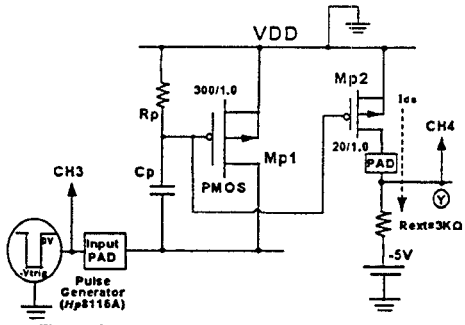

Fig.13 Experimental setup to measure capacitor-couple efficiency in ND-mode ESD-stress condition.

Typical measured voltage waveforms of capacitor-couple efficiency, which is coupled through Cn (Cp) to the gate of NMOS (PMOS) as a positive (negative) pulse-type trigger voltage is applied to the input pad, are shown in Figs.14 and 15, respectively.

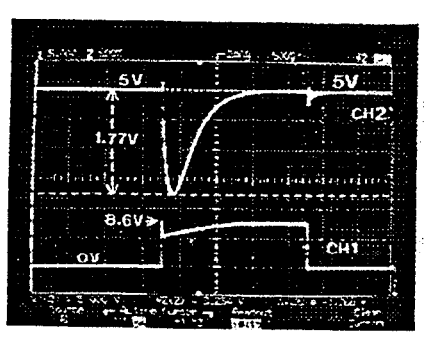

Fig.14 Typical measured voltage waveforms in Fig.12. (X axis: 500ns/div.; CH1: 5V/div.; CH2: 0.5V/div.).

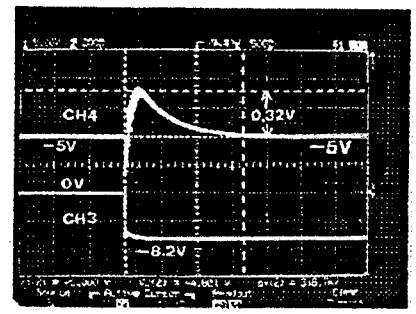

Fig.15 Typical measured voltage waveforms in Fig.13. (X axis: 500ns/div.; CH3: 5V/div.; CH4: 0.2V/div.).

From above measured results, the coupling effect of Cn (Cp) and voltage holding capability of Rn (Rp) have been verified. For applications in different deep-submicron low-voltage CMOS technologies, Cn (Cp) and Rn (Rp) can be designed to meet practical requirement by the developed design model.

V. Conclusion

A capacitor-couple ESD protection circuit has been successful designed, fabricated, and verified in a 0.5-μm 3-V CMOS technology. With poly layer inserting under metal pad to realize the coupling capacitance and poly lines extending around the pad to realize the sustaining resistance, a small layout area of capacitor-couple ESD protection circuit has been shown. A timing-original design model has been also derived to calculate capacitor-couple efficiency without trial-and-error *HSPICE* simulation. Not only to ensure uniform ESD current flow among the multiple fingers of ESD-protection NMOS/PMOS but also to earlier turn on ESD-protection NMOS/PMOS to bypass ESD current, experimental results have verified that it can offer more effective ESD protection for thinner gate oxide.

Thus, this proposed capacitor-couple ESD protection circuit can effectively improve ESD reliability of IC products in deep-submicron low-voltage CMOS technologies

References

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