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EFFICIENT OUTPUT ESD PROTECTION FOR 0.5-μm HIGH-SPEED CMOS SRAM IC WITH WELL-COUPLED TECHNIQUE

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Abstract: This work reports an effective ESD protection circuit design for CMOS IC's by using well-coupled field-oxide device (WCFOD). The bipolar action of the field-oxide device is triggered by well-coupling technique. The ESD-trigger voltage of WCFOD is lowered below the snapback-breakdown voltage of an output transistor, so it can perform efficient ESD protection for output transistors. A 0.5-μm high-speed 256K SRAM product had been fabricated with this proposed well-coupled technique to practically verify the excellent efficiency for output ESD protection. The ESD failure voltage of this SRAM product has been improved up to above 6KV without any extra ESD-Implant process, whereas the original output buffer just can sustain the HBM ESD stress of 1KV only.

INTRODUCTION

Advanced submicron or deep-submicron CMOS technologies had been reported to degrade ESD robustness of CMOS IC's [1]-[2]. Especially, the drains of output transistors in output stages are directly connected to the output pad, so the output transistors are more sensitive to ESD stress. In [3], a field-oxide device is placed from the output pad to VSS to protect thin-oxide output NMOS devices. The drain of the thin-oxide output NMOS is modified with a series N-well resistor. Due to the series resistor between output transistor and output pad, the output driving/sinking capability and output timing are degraded by the series resistor. If the turn-on voltage of the field-oxide device can be lowered below the snapback-breakdown voltage of the short-channel output transistor, the series resistor between the output transistor and the output pad can be removed.

In this paper, a well-coupled technique is proposed to reduce the turn-on voltage of the field-oxide device. With lower turn-on voltage, this well-coupled field-oxide device (WCFOD) can offer excellent ESD protection for output pad alone without the series resistor between the output transistor and the output pad.

OUTPUT ESD PROTECTION WITH WCFOD

The proposed ESD protection with WCFOD for the output stage is shown in Fig.1, and the schematic cross-sectional view of this WCFOD is shown in Fig.2. In Fig.1, the field-oxide device

is formed by the N+ diffusions which close together in a separated P-well. This separated P-well is connected to VSS through a resistor Rp. A capacitor Cp is connected from output pad to the separated P-well to perform the well-coupled action in the ESD stress. The output stage in Fig.1 includes a pull-up NMOS device MN1 and a pull-down NMOS device MN2. A resistor R1 of 30Ω connected between the drain of MN1 device and VDD is used to limit the short-circuit transient current when MN1 and MN2 are both turned on during logic transition.

There are four different modes of ESD stresses on a pin of an IC [4]. The PS-mode ESD stress, a positive ESD voltage on the output pad with relatively grounded VSS pin but floating VDD pin, has been found to be the worst case of ESD stress on the output stage due to the snapback breakdown of an output NMOS with the LDD structure.

As a PS-mode ESD voltage occurs on the output pad, some positive ESD-transient voltage will be coupled to the separated P-well through the capacitor Cp. This coupled positive ESD-transient voltage in the separated P-well is sustained longer in time by the resistor Rp. Due to the positive voltage in the separated P-well, the bulk-to-source junction in the field-oxide device is forward biased. This leads to the lateral bipolar action in the field-oxide device to happen earlier with much lower breakdown voltage. Thus, the WCFOD can be fully turned on to bypass ESD current before the output transistor is damaged by the PS-mode ESD voltage.

The capacitor Cp of about 0.86pF in WCFOD can be realized by inserting the poly layer right under the wire-bonding metal pad, without increasing layout area to the output pad. The resistor Rp of about 10KΩ can be realized by the poly line around the output pad without increasing total layout area of chip size. The Cp and Rp are designed to keep the field-oxide device off in the normal operating condition of SRAM output buffer with 5-V VDD and 0-V VSS bias, but to turn on the field-oxide device in the PS-mode ESD-stress condition. The field-oxide device is realized in a long-finger-type layout with device dimension (width/length) of 173/0.9 (μm).

EXPERIMENTAL RESULTS

This output ESD protection design has been verified by an SRAM product. A single separated WCFOD device with the same layout as that in the output ESD protection circuit of Fig.1 is also fabricated in the same wafer to find its device characteristics. The initial breakdown voltage of the field-oxide device is 12.8V, and the minimum holding voltage of its snapback region is 7.9V.

If there is some voltage bias added to the P-well of the field-oxide device, the breakdown behavior becomes different. The bulk (P-well) of the field-oxide device is biased with different voltages and the measured results are shown in Fig.3. As the P-well bias is increased above 0.6V which is near to the cut-in voltage of the p-n junction, the breakdown voltage is significantly reduced. If the P-well bias is increased above 0.8V, the lateral bipolar action in the field-oxide device is first turned on when its drain bias is in the low voltage region. The relation between the P-well bias and the trigger voltage for the field-oxide device entering into snapback region is shown in Fig.4.

The output ESD protection with WCFOD implemented in 256K high-speed SRAM chip is tested by ESD simulator of human-body model (HBM) to investigate the efficiency of ESD protection. The ESD tester is the *Zapmaster* produced by KeyTek corp. The ESD failure criterion is defined as that the leakage current of the I/O pad with output buffer and ESD protection circuit in its high-impedance state is above 1 μA under VDD (VSS) bias of 6V (0V).

The PS-mode ESD failure voltage of output pad protected by WCFOD is improved up to 6.5KV in the SRAM test chip. The PS-mode ESD failure voltage of the output stage in Fig.1 without the protection of WCFOD is only around 1KV. Because the ESD-transient voltage is coupled to the P-well of the field-oxide device to trigger on the lateral bipolar action, the WCFOD can be turned on with lower snapback-trigger voltage to early bypass ESD current from

the output pad to VSS. Therefore, the output transistor can be effectively protected by WCFOD.

To verify the well-coupled efficiency of the WCFOD for output ESD protection, a voltage pulse generated from *HP8116A* (pulse generator) with pulse width of 400 nS is applied to the output buffer (in its high-impedance state) under the bias of 5-V VDD and 0-V VSS. If the peak voltage is increased more than 7.125V, the WCFOD can be triggered on and the voltage waveform on the output pin is degraded. The typical measured voltage waveform to verify the well-coupled efficiency is shown in Fig.5. With the experimental verification, this WCFOD in the output ESD protection circuit of the output pin is not triggered on by the normal operating voltage of 5-V input/output signals. The dc snapback-trigger voltage of the field-oxide device is 12.8V. The snapback-breakdown voltage of the output NMOS transistor in the SRAM chip is 11.9V. But, the pulse-type trigger voltage of the proposed WCFOD is lowered to only about 7.1V. Thus, the unexpected overstress current, such as ESD, can be bypassed by the early turn-on WCFOD to protect output transistors.

Another concern for the P-well of field-oxide device connected to VSS through a poly resistor is the off-state leakage current as the WCFOD is applied to protect an I/O pad. A chip-selected pin in the SRAM test chip, which can keep all the I/O pins in the high-impedance state, is used to turn off the output transistor. An input voltage sweeping from 0~5V generated by *HP4145* is applied to the I/O pin under the high-impedance condition, and then the input current is observed as the leakage current of the pin. The I/O pin with the WCFOD is found to have the maximum leakage current of 1.8 pA, whereas the maximum leakage current in the original output buffer without the WCFOD is 1.7 pA. The non-direct P-well bias leads to increase of maximum leakage current about 0.1 pA only. So, this WCFOD does not cause degradation on the circuit performance of the output buffer.

CONCLUSION

A new ESD protection technique for output pad with the well-coupled field-oxide device has been successfully verified and practically applied in a 0.5-μm 256K high-speed SRAM product. This WCFOD has the benefits of a lower snapback-trigger voltage, a higher ESD protection capability, and without adding a series resistor into the drain of output NMOS transistors. The ESD reliability of an output pad can be effectively improved without causing any degradation on the circuit performance of the high-speed SRAM IC. By only inserting the field-oxide device in the empty layout region with the realization of poly capacitor under the pad and poly resistor around the pad, the total chip size of the SRAM IC with WCFOD is not increased. The HBM ESD reliability of this SRAM product has been improved up to 6.5KV, whereas the original output buffer without WCFOD just can sustain the PS-mode ESD stress of 1KV only.

With obvious advantages of the lower trigger voltage and the higher ESD robustness, this proposed WCFOD is also very suitable to protect the thinner gate oxide of input stage of CMOS IC's in deep-submicron technology.

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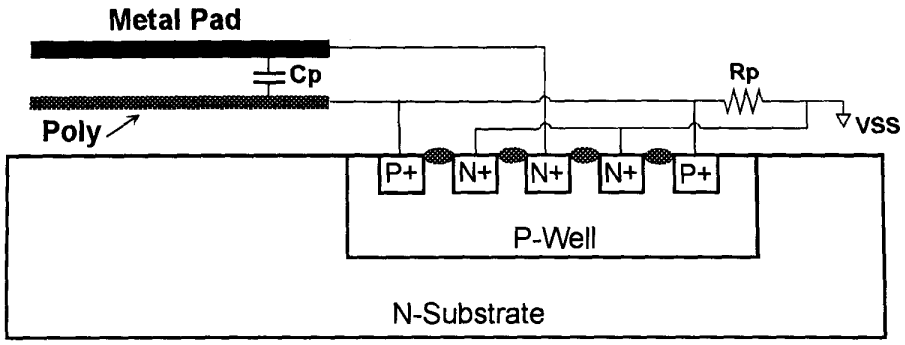

Fig.2 The schematic cross-sectional view of the proposed WCFOD structure.

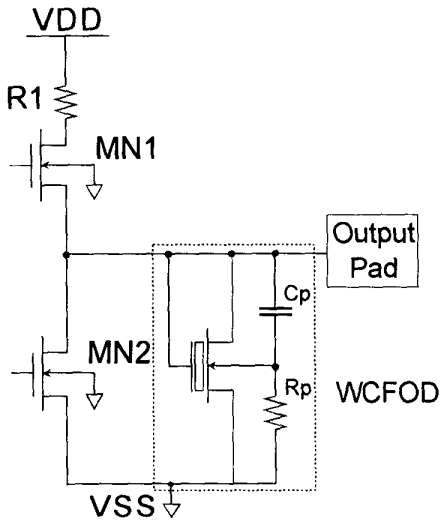

Fig.1 Output ESD protection with the proposed WCFOD structure.

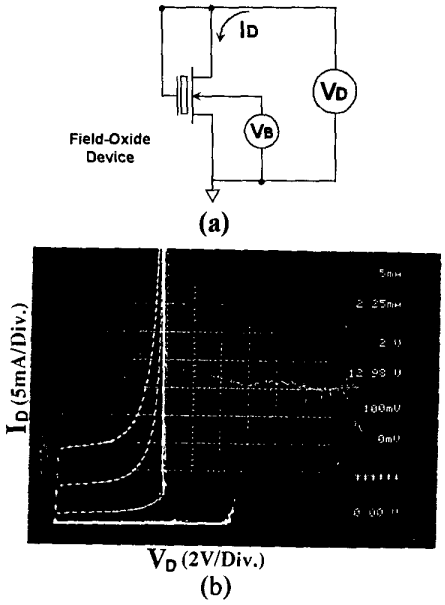

Fig.3 The measured snapback-breakdown characteristics of a field-oxide device with different bulk (P-well) biases. (a) The measurement setup; (b) the measured I-V curves.

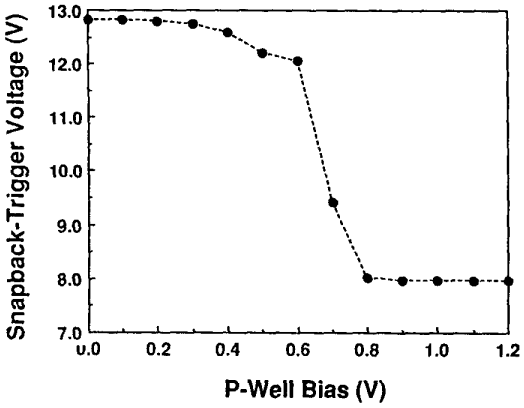

Fig.4 The dependence of the P-well bias on the snapback-trigger voltage of a fabricated field-oxide device in a 0.5-μm SRAM process.

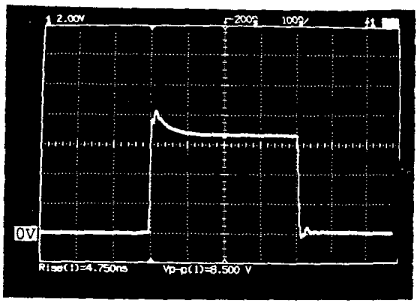

Fig.5 The typical voltage waveform of the pulse-type voltage on the I/O pin with triggered-on WCFOD ESD protection circuit.