Novel Octagonal Device Structure for Output Transistors in Deep-Submicron Low-Voltage CMOS Technology

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Abstract

A novel device structure to effectively reduce the layout area of CMOS output buffers with higher ESD reliability is proposed. Experimental results have shown that the output driving (sinking) current of output buffers in per unit layout area is increased 47.7% (34.3%) by this octagon-type design. The HBM (MM) ESD robustness of this octagon-type output buffer in per unit layout area is also increased 41.5% (84.6%), as comparing to the traditional finger-type output buffer.

Introduction

In deep-submicron low-voltage CMOS technology, VDD is scaled down to save power consumption and to provide better device reliability. To offer enough output driving/ sinking currents as well as to provide stronger ESD reliability, the W/L ratios of output transistors are often enlarged up to several hundreds. But in high-integration applications, especially in the high-pin-count or pad-limited CMOS VLSI, the layout area available for each output pad with output buffer including latchup guard rings is seriously limited. So, an area-efficient output buffer with high driving capability and high ESD robustness is much requested by deep-submicron low-voltage CMOS IC's.

To save the layout area of output buffers, the output devices are often drawn in a finger-type structure as shown in Fig.1. Recently, it has been found that the spacing from the drain contact to the poly-gate edge (marked as "d" in Fig.1) is an important layout parameter to affect ESD reliability of output devices [1]. This minimum spacing is found to be about 5~6 μm to provide a preferable ESD reliability. But this spacing only has ESD improvement in a non-silicided process. In the advanced CMOS process with silicided diffusion, a modified drain structure for output NMOS (shown in Fig.2) can be used to effectively improve ESD reliability without modifying the process steps or adding the extra silicided-block mask. This also much increases the spacing "d" in Fig.2. Due to the ESD-reliability consideration with a larger spacing "d", the layout area of a finger-type output device is significantly increased. Besides, in the finger-type output devices, the ESD damage has been found to easily locate on the finger's end of a drain finger as shown in Fig.3. This unexpected ESD damage is due to the parasitic diode (as shown in Fig.4) breakdown during the fast ESD transition and causes a very weak ESD reliability.

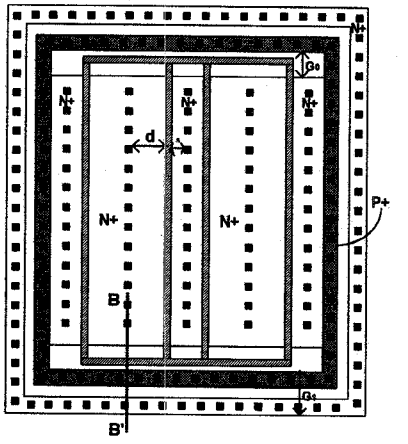

Fig.1 The traditional finger-type output NMOS device.

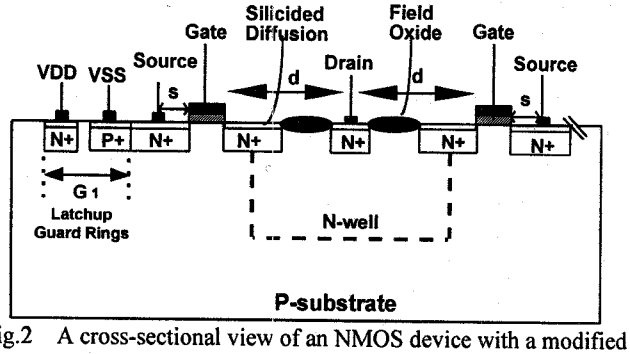

Fig.2 A cross-sectional view of an NMOS device with a modified N-well drain structure in a CMOS process with silicided diffusion.

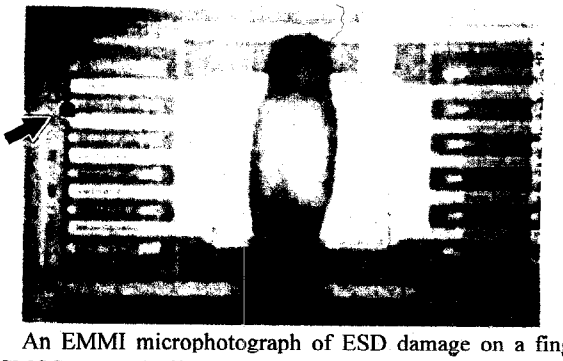

Fig.3 An EMMI microphotograph of ESD damage on a finger-type CMOS output buffer after a PS-mode ESD stress. Only a hot spot is observed at the end of a drain finger, which is indicated by an arrow.

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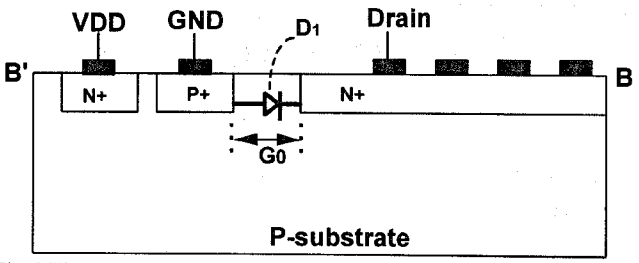

Fig.4 The cross-sectional view to show the parasitic diode along the line B--B' in Fig.1.

In this paper, a novel octagon-type device structure is proposed to realize the output transistors within smaller layout area but with higher driving capability and better ESD robustness [2].

Octagonal Device Structure

The basic octagonal cell to assemble an output NMOS device is shown in Fig.5. Its cross-sectional view is shown in Fig.6, where an n-well/p-substrate CMOS process is used to demonstrate this device structure. This octagonal device structure can be implemented by any CMOS or BiCMOS technologies.

In Fig.5, the black octagonal region in the center of a cell is the drain contact for the NMOS device. A dashed line of octagonal shape enclosing the drain contact is an n-well, which is made to avoid ESD-induced contact spiking. The poly gate, N+ diffusion of source, and the placement of source contacts in the octagonal cell are also drawn or arranged in a octagonal shape. Outside the NMOS device, there is a P+ diffusion connected to VSS to offer the p-substrate bias for normal CMOS operations. All the layout in an octagonal cell is made as symmetrical as possible to ensure uniform ESD current flow in the NMOS device so as to increase its ESD robustness. An NMOS device with larger dimension can be assembled by a plurality of the basic octagonal cells. Fig.7 shows a practical layout of an output NMOS with double latchup guard rings in a 0.6-μm SPTM CMOS technology. There are 15 basic NMOS octagonal cells used to assemble the output NMOS device with a total W/L of 804/0.8 (μm), which only occupies a layout area of 110×74 μm^2.

Theoretical calculations of the layout area and the drain capacitance between the octagon-type and finger-type devices are shown in Figs.8 and 9 with d=5 μm. In Fig.8, the total layout area of an octagon-type device is only 80% of that of a finger-type device with the same device channel width. In Fig.9, the drain capacitance of an octagon-type device is only 62.6% of that in the finger-type device. The layout-area ratios and drain-capacitance ratios (octagon-type/finger-type) under different d spacings are shown in Figs.10 and 11, respectively. The layout area and drain capacitance can be significantly reduced by this octagon-type device structure, as the spacing "d" is large.

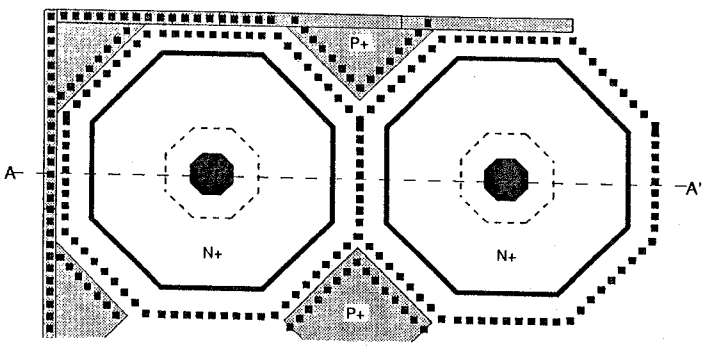

Fig.5 A schematic diagram of the proposed octagonal cell.

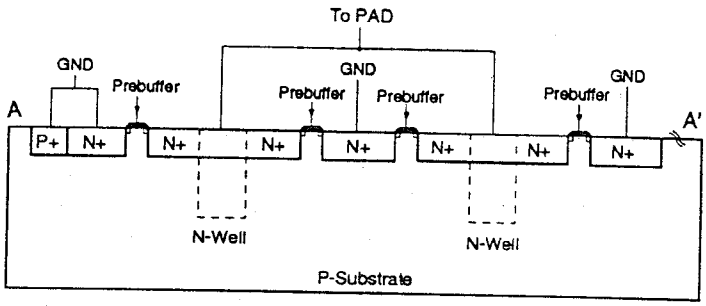

Fig.6 A cross-sectional view of the octagonal cell along the line A--A' in Fig.5.

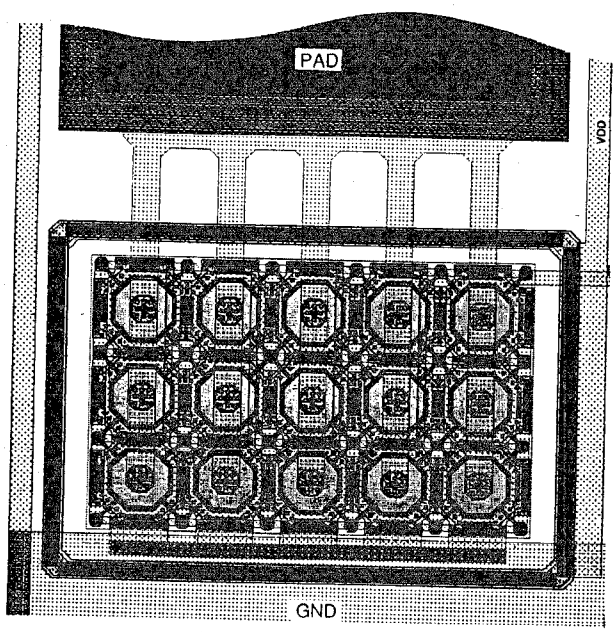

Fig.7 A practical layout example of an octagon-type output NMOS with the device dimension (W/L) of 804/0.8 (μm).

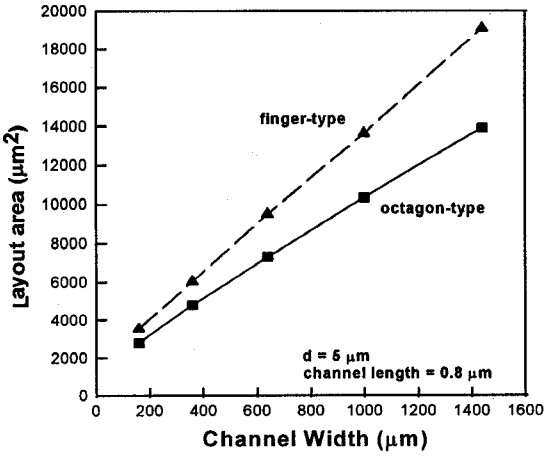

Fig.8 Comparison of the layout area between the octagon-type and the finger-type devices with the spacing d of 5μm.

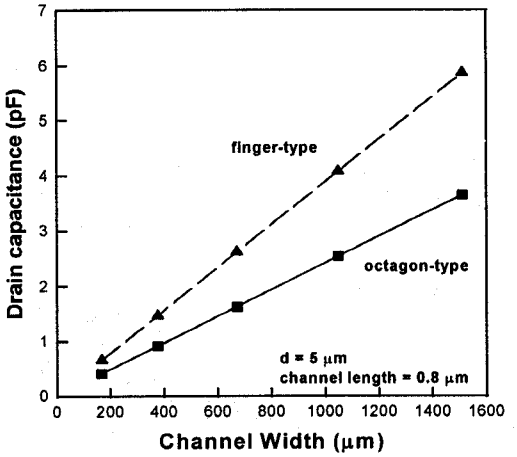

Fig.9 Comparison of the drain parasitic capacitance between the octagon-type and the finger-type devices with d=5μm.

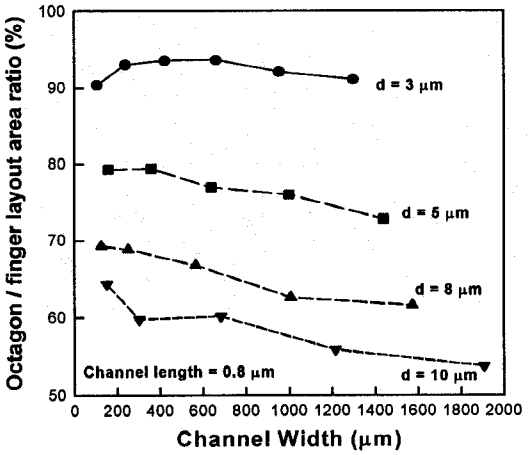

Fig.10 The dependence of the area ratios (octagon-type vs. finger-type) on the device channel width under different d spacings.

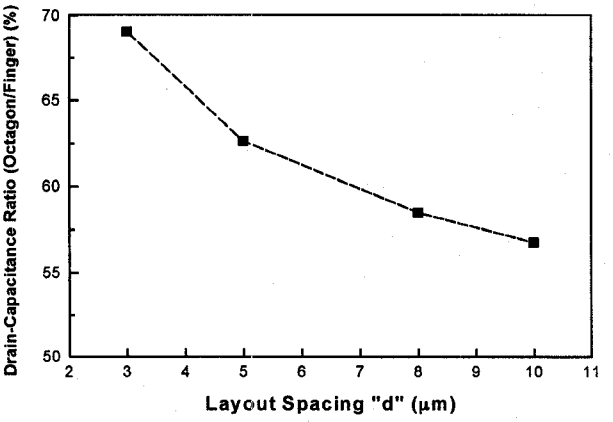

Fig.11 The relations between the drain-capacitance ratios (octagon-type vs. finger-type) and the spacing d.

Experimental Results

A microphotograph of a fabricated octagon-type output buffer is shown in Fig.12. The I-V curves of an octagon-type output NMOS corresponding to the layout of Fig.7 are measured in Fig.13. A finger-type NMOS with W/L= 720/0.8 (μm) is also fabricated in the same CMOS process as a reference, which occupies a layout area of 112×100 μm^2.

A. Output Driving/Sinking Current

The output driving/sinking capability is summarized in Table I to verify the area efficiency. The maximum output sinking (driving) current in per unit layout area of the octagon-type output NMOS (PMOS) device is 13.12 (6.59) μA/μm^2, but that in the finger-type device is only 9.77 (4.46) μA/μm^2. So, the octagon-type NMOS (PMOS) device provides an increase of 34.3% (47.7%) on the output sinking (driving) current in per unit layout area, as comparing to the finger-type devices.

Table I

Comparison of output driving/sinking current between the finger-type device and this octagon-type device.

	Finger-type Device	Octagon-type Device
W/L (μm)	720/0.8	804/0.8
Layout Area (μm^2)	112×110	110×74
NMOS Ids (Vds=Vgs=3V)	120.4 mA	106.8 mA
PMOS Ids (Vds=Vgs= -3V)	-54.95 mA	-53.69 mA
NMOS Ids in per unit Layout Area	9.77 μA/μm^2	13.12 μA/μm^2
PMOS Ids in per unit Layout Area	-4.66 μA/μm^2	-6.59 μA/μm^2

B. Output ESD Robustness

The ESD test results including the HBM (Human Body Model), MM (Machine Model), and CDM (Charged Device Model) ESD tests are listed in Table II. There are four modes of ESD stresses on a pin with respect to VDD and VSS pins [3]. The ESD pass voltage of a pin is defined as the highest ESD voltage that the pin can sustain without causing any damage among the four ESD-stress modes. The octagon-type device structure can effectively improve the uniform turn-on characteristics of the output devices during ESD stresses. Thus, it improves the ESD robustness of output buffers. The HBM (MM) ESD robustness of per unit layout area in the octagon-type output buffer is 0.74 (0.12) V/μm^2, but that in the finger-type output buffer is only 0.53 (0.065) V/μm^2. Thus, this octagon-type output buffer provides an increase of 41.5% (84.6%) in the HBM (MM) ESD robustness of per unit layout area. The CDM ESD robustness in per unit layout area of an octagon-type output buffer can be greater than 0.25V/μm^2.

Table II

Comparison of ESD robustness between the finger-type device and this octagon-type device.

	Finger-type Device	Octagon-type Device
W/L (μm)	720/0.8	804/0.8
Layout Area (μm^2)	112×110	110×74
HBM ESD pass voltage	6500 V	6000 V
MM ESD pass voltage	800 V	950 V
CDM ESD pass voltage	> ±2000 V	> ±2000 V
HBM pass voltage in per unit Layout Area	0.53 V/μm^2	0.74 V/μm^2
MM pass voltage in per unit Layout Area	0.065 V/μm^2	0.12 V/μm^2

Conclusion

An octagon-type layout used to realize the thin-oxide NMOS and PMOS devices in the CMOS output buffer has been successfully verified in a 0.6-μm CMOS process. Both higher output driving/sinking capability and better ESD robustness within a smaller layout area can be practically achieved by the proposed octagon-type CMOS output buffer. This octagon-type layout is very suitable for deep-submicron low-voltage CMOS VLSI in high-density and high-speed applications.

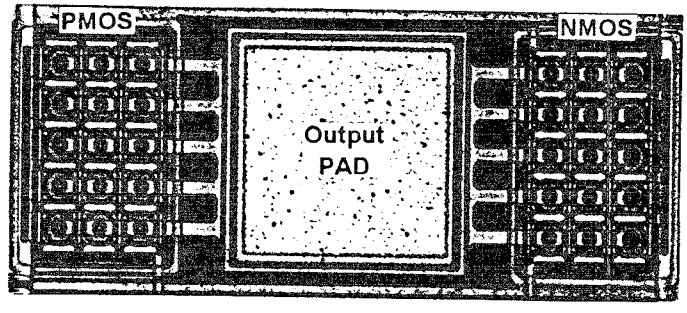

Fig.12 A microphotograph of a fabricated octagon-type CMOS output buffer.

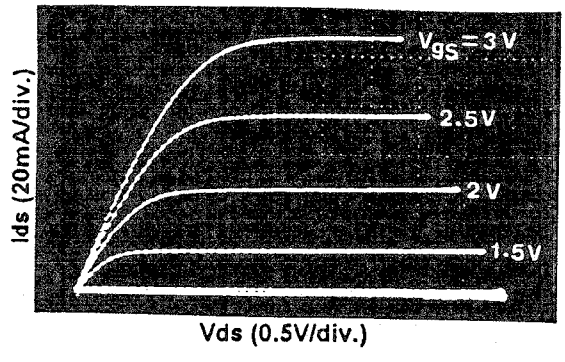

Fig.13 The measured I-V curves of an octagon-type output NMOS transistor.

Acknowledgment

The authors wish to thank Mr. Kuo-Feng Wang for his expert art to draw the layout of this octagonal device structure.

References

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[2] M.-D. Ker, T.-S. Wu, and K.-F. Wang, "N-sided polygonal cell layout for multiple cell transistor," ROC Patent #076087.

[3] M.-D. Ker, C.-Y. Wu, and H.-H. Chang, "Complementary-LVTSCR ESD protection circuit for submicron CMOS VLSI/ULSI," *IEEE Trans. Electron Devices*, vol. 43, no. 4, pp.588-598, 1996.