

Area-Efficient VDD-to-VSS ESD Clamp Circuit by Using Substrate-Triggering Field-Oxide Device (STFOD) for Whole-Chip ESD Protection

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Abstract

A novel substrate-triggering field-oxide device (STFOD) is proposed to form an area-efficient ESD clamp circuit for whole-chip ESD protection in submicron CMOS technology. Experimental results in a 0.6- μm CMOS process have verified that this STFOD can provide four-times higher ESD robustness in per unit layout area as comparing to the previous works with the NMOS device. This design has been practically implemented in an 8-bits DAC chip to provide a real whole-chip ESD protection of above 4KV.

Introduction

Whole-chip ESD protection has become an important reliability issue of submicron CMOS IC's, because there exists the unexpected ESD damage on the internal circuits of IC's beyond the input or output ESD protection circuits [1]-[4]. ESD current may enter into any pin and go out from another pin of an IC. Two additional ESD-testing conditions, which are shown in Figs.1(a) and 1(b), have been used to practically verify the whole-chip ESD reliability [5]. In Fig.1(a), the ESD voltage is stressed on an input (or output) pin while the other input and output pins are grounded but all the VDD and VSS pins are floating. In Fig.1(b), the ESD voltage is directly stressed on the VDD pin with relatively grounded VSS pin but all the input and output pins are floating. The CMOS IC's are more vulnerable to internal ESD damage in Fig.1(b) even if there are ESD protection circuits on the input and output pads [6]. So, suitable ESD clamp circuits should be added between the VDD and VSS power lines of the CMOS IC's. In [7]-[9], a RC -based circuit was used to turn on an NMOS to bypass ESD current from VDD to VSS. In order to sustain the ESD discharging current, the NMOS was designed with a very large W/L ratio ($\mu\text{m}/\mu\text{m}$) such as 8000/0.8 in [7], 3000/0.7 in [8], and $(800/0.8) \times 8$ in [9]. With such huge device dimensions, the layout areas are much increased to realize these designs. In [10]-[11], the SCR's were used as ESD-clamping device between VDD and VSS, but such SCR's may cause the VDD-to-VSS latchup in the normal operating conditions of a CMOS IC due to the

unexpected voltage spikes on the power lines (such as the board-level arcing test or the power-line surging test). So, the protection design with the SCR's between VDD and VSS is very dangerous and not practical in the most applications of CMOS IC's.

In this paper, an ESD clamp circuit with a novel substrate-triggering field-oxide device (STFOD) [12] is proposed to provide the whole-chip ESD protection within a much smaller layout area. The concept and design of whole-chip ESD protection scheme is also described in this paper.

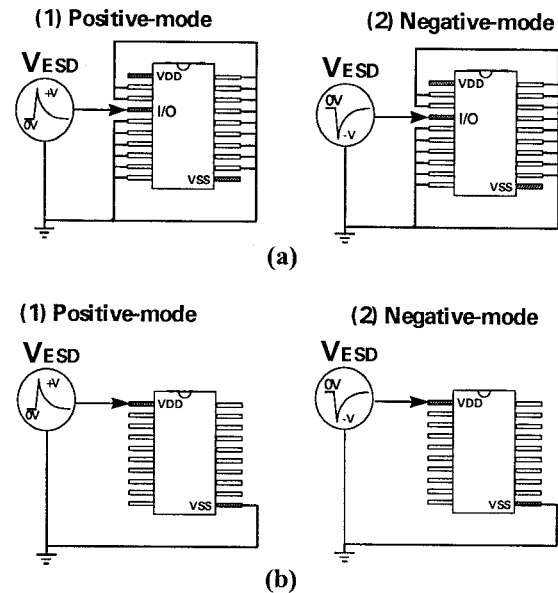


Fig.1 Two additional ESD-testing methods, (a) pin-to-pin ESD stress; (b) VDD-to-VSS ESD stress, to verify the whole-chip ESD reliability.

VDD-to-VSS ESD Clamp Circuit

The proposed ESD clamp circuit with the STFOD is shown in Fig.2. This ESD clamp circuit is designed to be turned on under the ESD-stress condition, but it is kept off as the IC is under the normal power-on condition.

The RC time constant in Fig.2 is designed in the range about 0.1 μs . With such R and C , the ESD-transient detection circuit in Fig.2 can detect the ESD voltage pulse across the VDD and VSS power lines. And then, the Mp device is turned

on by the ESD voltage to send a high voltage to the substrate of the STFOD. As the voltage on the node VB is greater than 0.6V, the lateral bipolar action in the STFOD is triggered on. Thus, the ESD voltage on the VDD power line is quickly discharged to VSS through the turned-on STFOD. The turned-on STFOD, which provides a near short-circuit path between the VDD and VSS power lines, can clamp the ESD voltage across the VDD and VSS power lines to a very low voltage level. So, the internal circuits can be effectively protected without any ESD damage. A schematic voltage waveform on the node of VB (in Fig.2) under the ESD-stress condition is shown in Fig.3. The VB(t) is the voltage to the base of the STFOD which is used to bypass ESD current. In Fig.3, the turn-on time of the STFOD is designed as long as 200ns to meet the half-energy discharging time of the HBM (Human-Body Model) ESD event

Under the normal power-on condition of the IC, the VDD power-on transition has a rise time in the range of microsecond (μ s) order on the VDD voltage waveform. With such a rise time of μ s order, the ESD-transient detection circuit with the RC time constant of 0.1 μ s keeps the VB node with a voltage level of 0V. So, the STFOD is guaranteed to be kept off, as the IC is under the power-on conditions or the normal operating conditions. In Fig.4, it shows the schematic voltage waveform of VB(t) in the time domain under the power-on condition for a CMOS IC to be normally operated. In this power-on condition, the VB(t) should not be greater than 0.6V (the cut-in voltage of STFOD) to keep the STFOD off.

The typical operation of pin-to-pin ESD protection with this VDD-to-VSS ESD clamp circuit is illustrated in Fig.5. In Fig.5, a positive ESD voltage is stressed on an input pin with a grounded output pin while the VDD and VSS pins are floating. The positive ESD voltage will be first diverted to the floating VDD power line through the forward-biased diode Dp1. The floating VSS power line is also biased at a voltage close to the ground through the drain-to-substrate diode Dn2 in the output NMOS device. So, the ESD-stress voltage from the input pin to the output pin becomes across the VDD and VSS power lines. If such an ESD voltage across the power lines can not be effectively bypassed, the internal circuits often drawn with the minimum design rules and minimum spacing are vulnerable to ESD damages. The VDD-to-VSS ESD clamp circuit (in Fig.2) is designed to detect this condition and to turn on the STFOD by the substrate-triggering technique. As the STFOD is turned on, it provides a short-circuit path between the VDD and VSS power lines. The ESD current can be quickly bypassed through the discharging path as shown by the dashed line in Fig.5. So, the

CMOS IC's can be effectively protected by this design without causing the internal ESD damages.

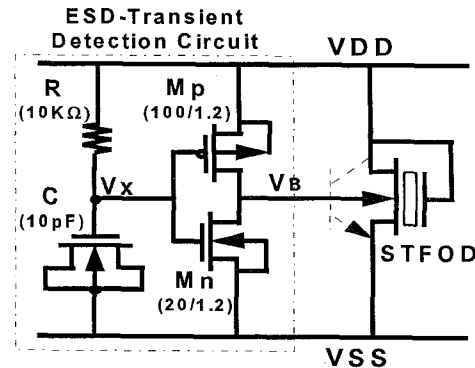


Fig.2 The area-efficient VDD-to-VSS ESD clamp circuit by using the substrate-triggering field-oxide device (STFOD).

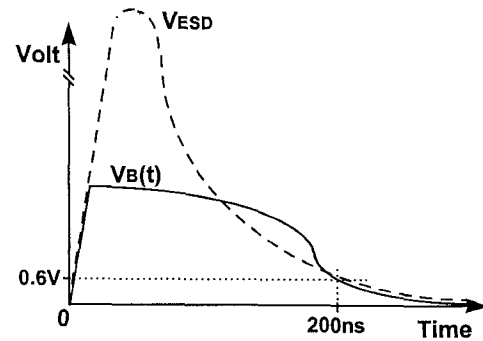


Fig.3 A schematic voltage waveform on the node VB in Fig.2 under the ESD-stress conditions.

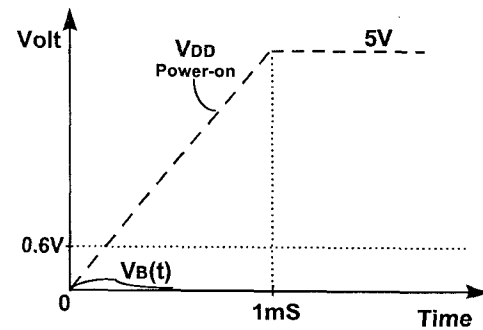


Fig.4 A schematic voltage waveform on the node VB in Fig.2 under the VDD power-on condition.

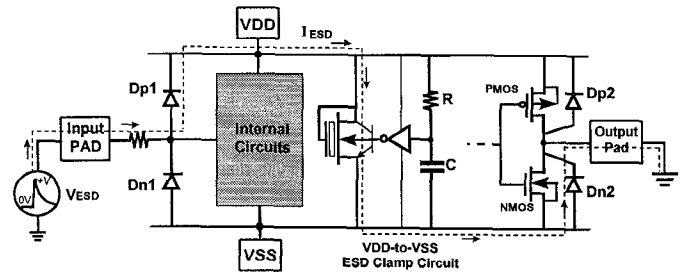


Fig.5 A schematic diagram to show the ESD current path through the VDD-to-VSS ESD clamp circuit under a pin-to-pin ESD-stress condition.

Substrate-Triggering Field-Oxide Device (STFOD)

The STFOD structure is shown in Fig.6, where a P+ diffusion connected to VB of Fig.2 is inserted in the center to provide the substrate-triggering current (I_{trig}) to this STFOD. An N-well in the source region surrounding the whole STFOD is used to enhance its lateral bipolar action. The substrate-triggering current coming from the node VB can be efficiently collected by the N-well structure to forward bias the base-emitter junction of the lateral bipolar transistor in the STFOD. With the forward-biased substrate voltage under the ESD-stress condition, the STFOD can sustain much higher ESD voltage as comparing to the NMOS devices. The STFOD is triggered on by the substrate-triggering design to significantly improve its ESD robustness in per unit layout area. So, the STFOD can provide high ESD robustness for whole-chip ESD protection within a much smaller layout area. Therefore, the device dimension of this STFOD to sustain the required ESD level can be effectively reduced.

ESD performance of the STFOD can be investigated by the relations between the I_{t2} (second breakdown current) and the forward-biased substrate voltage. The relations of I_{t2} (measured by the TLP method [13]) versus different substrate biases of a field-oxide device in a 0.5- μm CMOS process are shown in Figs.7 and 8. The I_{t2} (of per unit channel width) can be significantly improved by the forward-biased substrate voltage [14]. The I_{t2} of an NMOS with 0-V substrate bias, shown in Figs.7 and 8, is about 4.8 mA/ μm . The I_{t2} of the filed-oxide device with a 0-V substrate bias is 9.0 mA/ μm , but the I_{t2} is increased to 18.2 mA/ μm when the field-oxide device has a substrate bias of 0.8V. The field-oxide device with a 0.8-V substrate bias can provide a four-times higher I_{t2} than the NMOS device. So, this STFOD can provide higher ESD robustness within a much smaller layout area as comparing to the previous works [7]-[9], as well as this STFOD is free to the problem of VDD-to-VSS latchup in the SCR devices [10]-[11].

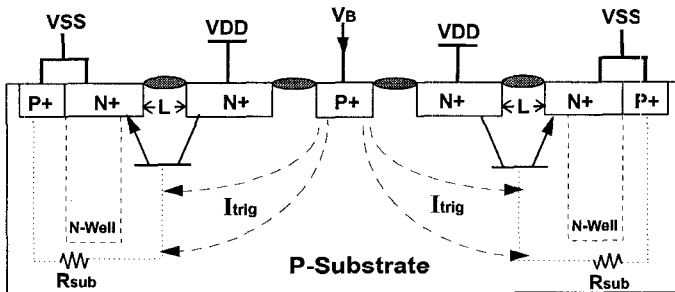


Fig.6 The device structure of the substrate-triggering field-oxide device (STFOD).

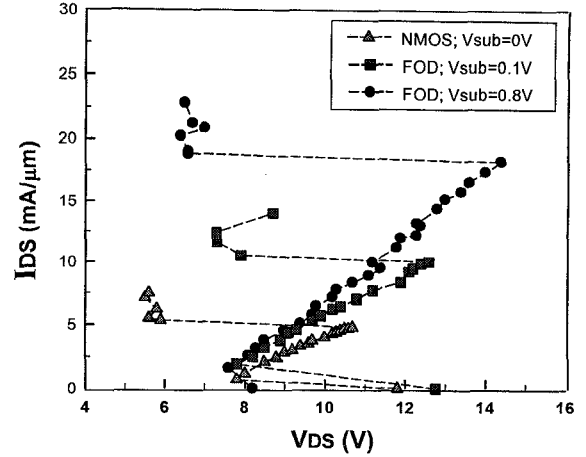


Fig.7 The TLPG-measured I_{t2} under different substrate biases of a field-oxide device (FOD) and an NMOS in a 0.5- μm CMOS process.

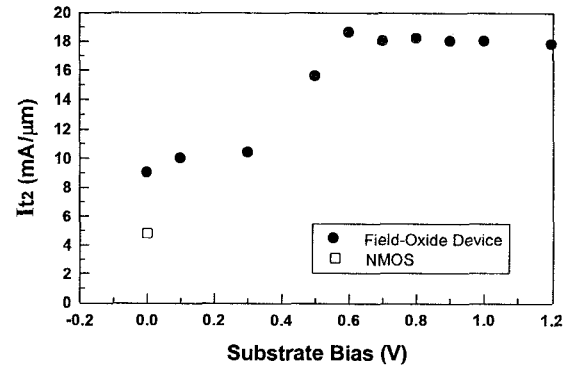


Fig.8 The dependence of I_{t2} (per unit channel width) on the forward-biased substrate voltage in a field-oxide device and an NMOS.

Experimental Results

A microphotograph of the fabricated ESD clamp circuit with the proposed STFOD in a 0.6- μm CMOS process is shown in Fig.9. The previous design by using the NMOS device [7]-[9], as shown in Fig.10, is also made in the same test chip as a reference. The ESD current discharging through the NMOS device in the previous VDD-to-VSS ESD clamp circuit of Fig.10 is focused at the LDD peak of the drain region due to the positive VB on the gate, so the NMOS is easily damaged by the ESD current and often causes a low ESD-sustained level.

The measured I-V characteristics of the STFOD is shown in Fig.11, and the beta gain of the lateral bipolar action in the STFOD is shown in Fig.12. The KeyTek ZapMaster is used to evaluate the ESD robustness of the proposed design with a failure criterion of 1- μA current leakage under a 5-V VDD bias. The HBM ESD testing results are summarized in Table I. This new design with the STFOD can provide 4-times higher ESD robustness in per unit layout area than the NMOS.

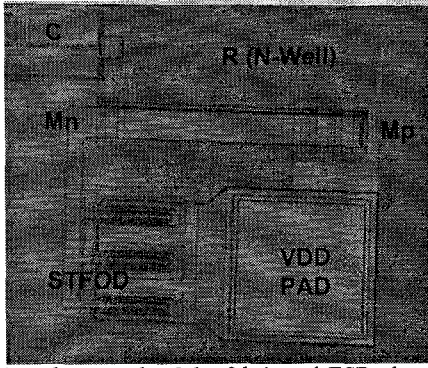


Fig.9 A microphotograph of the fabricated ESD clamp circuit in a 0.6- μm CMOS process.

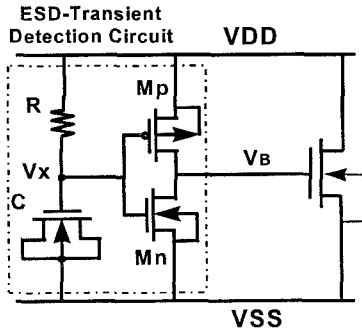


Fig.10 The previous VDD-to-VSS ESD clamp circuit using an NMOS ($W/L=500/0.8$) as the ESD discharging device.

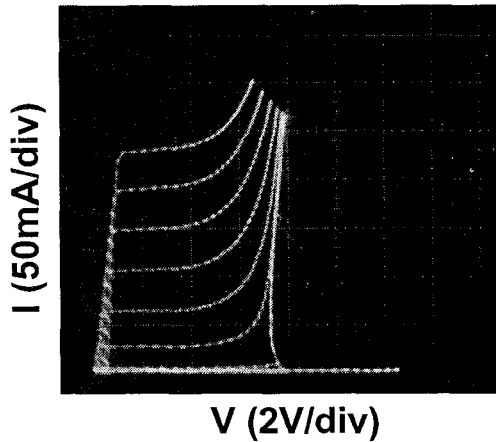


Fig.11 The measured I-V characteristics of the STFOD with different substrate biases from 0 to 2V in a voltage step of 0.2V.

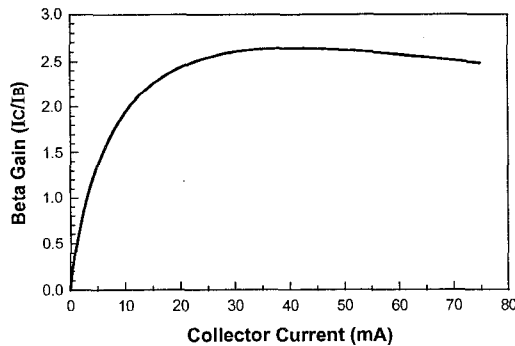


Fig.12 The measured beta gain of the lateral bipolar action in the STFOD. The maximum lateral beta gain is about 2.65.

Table I

	This Work (Fig.2)	Previous work (Fig.10)
ESD Protection Device (W/L, $\mu\text{m}/\mu\text{m}$)	STFOD (439.2/1.2)	NMOS (500/0.8)
Device Layout Area (μm^2)	102.9×78.8	93.6×74.05
HBM ESD Pass Level (V)	4500	1000
ESD Level in per unit Layout Area ($\text{V}/\mu\text{m}^2$)	0.55	0.14

To verify the efficiency of the ESD-transient detection circuit in Fig.2, an 8-V voltage pulse with a rise time of about 5.5ns and a pulse width of 400ns is applied to the ESD clamp circuit with the STFOD to simulate the ESD-stress condition. The voltage waveform on the VDD is measured and shown in Fig.13(a). The voltage pulse has been indeed degraded in the first 200ns because the STFOD is designed to be turned on about 200ns as that shown in Fig.3. A 5-V ramp voltage with a rise time of 0.1ms to simulate the VDD power-on condition is also applied to the VDD (with the VSS grounded) to verify the RC design in the ESD-transient detection circuit. The 5-V ramp voltage waveform on the VDD is observed and shown in Fig.13(b), where no degradation is found on the voltage waveform. This has actually verified the suitable RC design in the ESD-transient detection circuit.

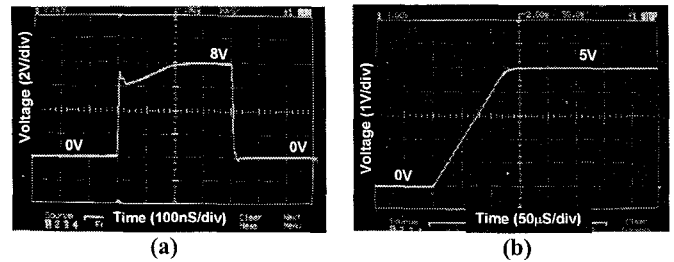


Fig.13 (a) The degraded waveform due to the turn-on of STFOD in the ESD clamp circuit, while a 8-V voltage pulse is applied to VDD with a rise time of 5.5ns; (b) The power-on VDD waveform (5-V ramp voltage with a rise time of 0.1ms) has no degradation because the STFOD is kept off in this power-on condition.

Whole-Chip ESD Protection Scheme

A whole-chip ESD protection scheme for the mixed-mode IC's with multiple VDD and VSS power pins is illustrated in Fig.14 with the proposed STFOD in the ESD clamp circuit. The ESD-connection diodes (D1, D2, D3, and D4) in Fig.14 provide a bi-directional discharging paths between the digital

and analog power lines to avoid the ESD stress on the digital-analog interface. While an ESD voltage occurs on a pin with any pin relatively grounded, the ESD current can be bypassed through the ESD-connection diodes and the area-efficient ESD clamp circuits to limit the ESD voltage across the VDD1 (or VDD2) and VSS1 (or VSS2) power lines. Thus, the ESD voltage across the VDD and VSS power lines can be effectively clamped without causing any ESD damage on the internal circuits.

An application example (layout) of the whole-chip ESD protection scheme with the ESD-connection diodes in an 8-bits DAC (Digital-to-Analog Converter) chip with two ESD clamp circuits between the analog and digital power lines is shown in Fig.15. By using this STFOD in the whole-chip ESD protection design, this DAC can pass the HBM ESD stress of above 4KV in any pin-to-pin ESD-stress conditions. This pin-to-pin ESD level is guaranteed without any internal ESD damage by full function testing after the IC is subjected to the ESD stresses.

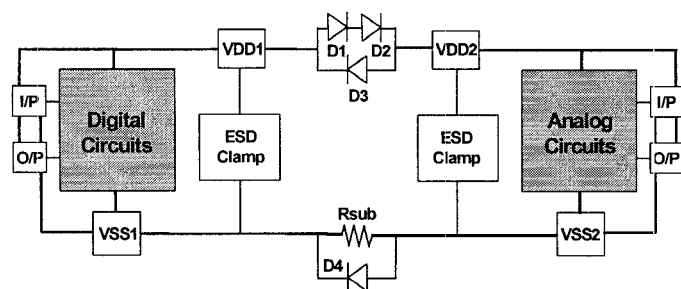


Fig.14 Whole-chip ESD protection design with the area-efficient ESD clamp circuits and the ESD-connection diodes in a mixed-mode IC.

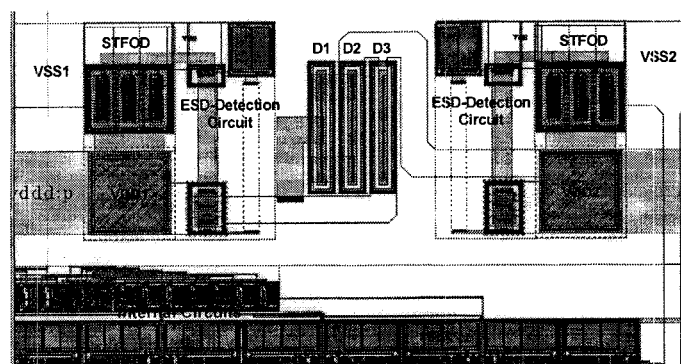


Fig.15 A layout example of the area-efficient ESD clamp circuits and the ESD-connection diodes in an 8-bits DAC chip.

Conclusion

An area-efficient VDD-to-VSS ESD clamp circuit with the novel STFOD has been successfully verified in a mixed-mode IC to provide a real whole-chip ESD protection. By using the substrate-triggering technique, the STFOD can provide four-times higher ESD robustness in per unit layout area as comparing to the previous works with the NMOS device. The whole-chip ESD protection scheme with the area-efficient VDD-to-VSS ESD clamp circuits can be expanded into the CMOS IC's with multiple VDD and VSS power pins.

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