Design of Cost-Efficient ESD Clamp Circuits for the Power Rails of CMOS ASIC's with Substrate-Triggering Technique

Ming-Dou Ker, Tung-Yang Chen*, and Chung-Yu Wu*

VLSI Design Division
Computer & Communication Research Laboratories (CCL)
Industrial Technology Research Institute (ITRI)
Hsinchu, Taiwan, R.O.C.

*Integrated Circuits & Systems Laboratory
Institute of Electronics, National Chiao-Tung University
Hsinchu, Taiwan, R.O.C.

Abstract --- Four new device structures for power-rail ESD clamp circuits by using the substrate-triggering technique are investigated in submicron CMOS technology to improve ESD level of the protection device within a smaller silicon area. Experimental results in a 0.6-μm CMOS process have verified that the ESD clamp circuit with the double-BJT structure can provide 200% higher ESD robustness in per unit layout area as comparing to the previous design with the NMOS device.

Introduction

Whole-chip ESD protection has become an important reliability issue of submicron CMOS ASIC's. Even if there are suitable ESD protection circuits around the input and output pads, the internal circuits are still vulnerable to the ESD damages [1]-[4]. To overcome this unexpected ESD damage on the internal circuits beyond the input or output ESD protection circuits, some ESD clamp circuits had been proposed to be added between the V_{DD} and the V_{SS} power rails [5]-[9].

In [5]-[7], a *RC*-based circuit had been used to turn on an NMOS to bypass the ESD current from V_{DD} to V_{SS}. The schematic circuit diagram of such design is illustrated in Fig.1 with the NMOS device structure shown in the cross-sectional view. If the gate of the NMOS is biased at a positive voltage, the NMOS device with the LDD (lightly-doped drain) peak structure and the silicided diffusion in the advanced CMOS technologies is very weak to ESD stress. The positive gate voltage causes the turn-on of the channel and leads to the ESD current focus at the LDD peak structure. Due to the very shallow junction depth of the LDD peak structure, the ESD current flowing through the LDD peak and the turned-on channel often causes a very low ESD level of the NMOS. In order to sustain a high ESD level, the NMOS had been designed with a huge device dimension (such as 8000/0.8 driven by a three-stage tapped buffer [5]) and occupied a much more silicon area. This causes a cost issue to the general CMOS ASIC's.

In [8]-[9], the parasitic lateral SCR device in CMOS processes were used as the current-discharging device between the V_{DD} and the V_{SS} power lines. Although the lateral SCR can provide high ESD level with a much smaller layout area as comparing to other ESD-protection devices, the lateral SCR may be triggered on by the overshooting noise pulses across the power rails [10]-[12]. In the system-level ESD testing [10] or the transient latchup testing [11]-[12] while the IC is in the normal operating conditions with the V_{DD} and V_{SS} power supplies, the ESD-protection lateral SCR between the power rails may be triggered on and causes a serious short-circuit problem between the power rails. Either the ESD-protection SCR or the power supplies may be burned out in such a system-level reliability testing for the CMOS ASIC's. So, a cost-efficient but latchup-free ESD clamp circuit is much urged by the CMOS ASIC's to provide the high-reliability performance in the scaled-down CMOS technologies.

In this paper, four types of ESD clamp circuits with the substrate-triggering technique on different device structures are investigated to find the cost-efficient design for the practical applications of CMOS ASIC's.

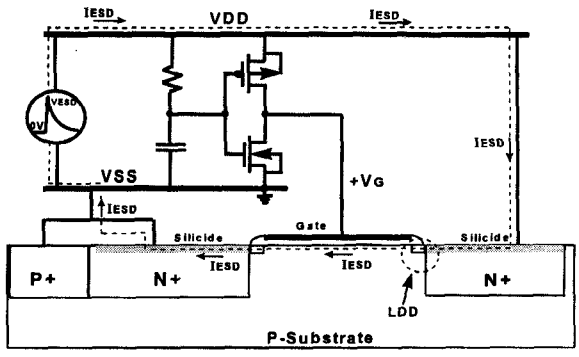


Fig.1 The schematic diagram of the *RC*-based ESD clamp circuit with an NMOS as the current discharging device between the V_{DD} and V_{SS} power rails.

Cost-Efficient ESD Clamp Circuits

If the ESD current is discharged through the parasitic lateral bipolar junction transistor (BJT) in the MOS device, the ESD current is discharged away from both the shallow channel and the LDD peak of the MOS device and therefore leads to a higher ESD level. To induce the ESD current flowing through the lateral BJT of the MOS device, the substrate-triggering technique is used to initiate the bipolar action of the MOS device during the ESD transition. Four types of substrate-triggering ESD clamp circuits with different device structures are investigated in this work.

1063-0988/97/$10.00 © 1997 IEEE.

*A. Substrate-Triggering Lateral BJT (**STLB**) Structure* :

The proposed ESD clamp circuit with the STLB structure is shown in Fig.2(a), and the schematic cross-sectional view of the STLB structure is illustrated in Fig.2(b). During the ESD transition between the power rails, the voltage on the capacitor C is initially kept at a low voltage level due to the large *RC* charging delay in the circuit [5]-[7]. The *RC* value is often designed around 0.1~1 μs to distinguish the ESD transition and the V_{DD} power-on transition. The inverter in Fig.2(a) is self-biased by the ESD energy and provides a trigger current to the V_B node. The parasitic lateral n-p-n BJT in the gate-grounded NMOS device is triggered on through the p-substrate. Therefore, the ESD current is discharged through the lateral n-p-n BJT, which is away from the channel and the LDD peak of the gate-grounded NMOS. To improve the lateral bipolar action in the gate-grounded NMOS, an N-well structure is inserted into the source region of the NMOS, as that shown in Fig.2(b), to collect the substrate-triggering current and to early initiate the bipolar action.

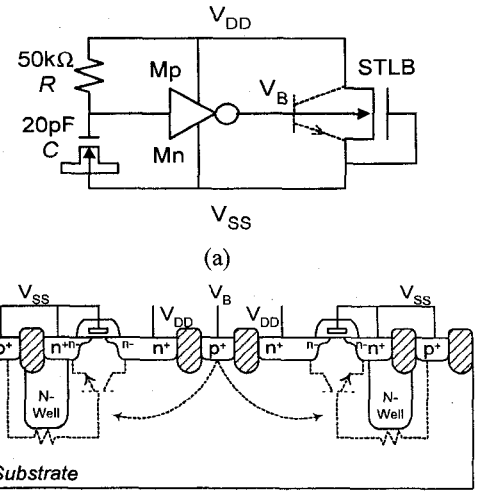


Fig.2 (a) The circuit, and (b) the device structure, of the ESD clamp circuit with the substrate-triggering lateral BJT (STLB) structure.

*B. Substrate-Triggering Vertical BJT (**STVB**) Structure* :

The vertical p-n-p BJT is also designed to bypass the ESD current between the power rails. The circuit and schematic cross-sectional view of the STVB structure are shown in Figs.3(a) and 3(b), respectively. To trigger on the vertical p-n-p BJT, the base node of the BJT has to be kept at a low-voltage level during the ESD transition. To achieve such design, two-stage inverters are connected between the *RC* and the vertical BJT, as shown in Fig.3(a). The two inverters are self-biased by the ESD energy to keep the V_B node at a low voltage level in the ESD-stress condition, but the V_B node is biased at V_{DD} when the IC is in the normal operation condition.

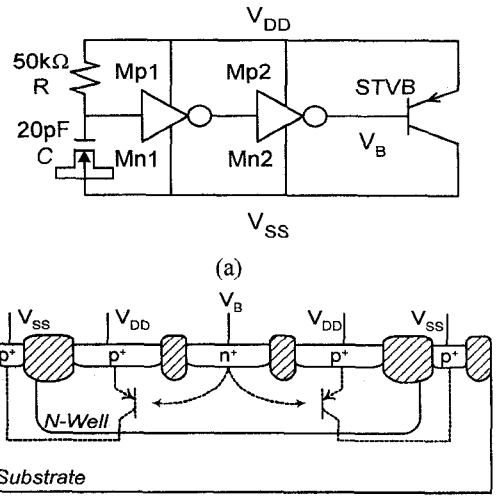


Fig.3 (a) The circuit, and (b) the device structure, of the ESD clamp circuit with the substrate-triggering vertical BJT (STVB) structure.

*C. Substrate-Triggering Double BJT (**STDB**) Structure* :

To make a complementary design to the STLB (with NMOS), the parasitic p-n-p BJT in the PMOS device is designed to bypass the ESD current between the power rails. The circuit and schematic cross-sectional view of such design are shown in Figs.4(a) and 4(b). In Fig.4(b), there is a vertical p-n-p BJT within the device structure to constitute the *double BJT* structure. The substrate-triggering technique is also used to trigger on the *double BJT* structure, as shown in Fig.4(a). With two p-n-p BJT's in the device structure, more current path can be formed in the device to discharge ESD current.

*D. Double-Triggering Double BJT (**DTDB**) Structure* :

To provide more current-discharging path in per unit silicon area of the ESD-protection device, a double-triggering design is shown in Fig.5(a) with the DTDB device structure illustrated in Fig.5(b). The double-triggering design is achieved by applying the trigger voltage to the gate of the ESD-protection PMOS and concurrently applying the trigger current to the *double BJT* structure. Both the PMOS device and the *double BJT* structure can be turned on to provide more ESD current-discharging path in the device structure.

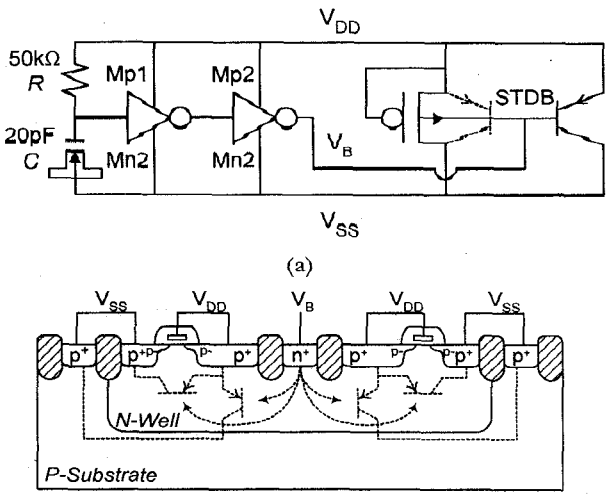
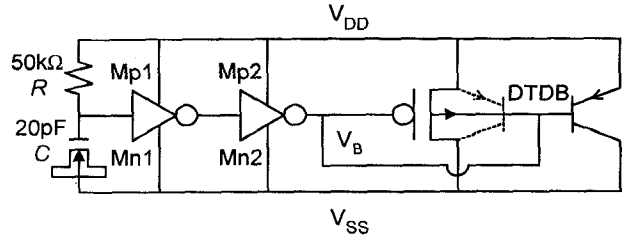
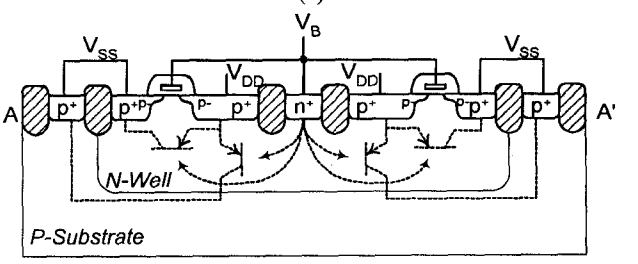


Fig.4 (a) The circuit, and (b) the device structure, of the ESD clamp circuit with the substrate-triggering double BJT (STDB) structure.

In order to cause a more uniform turn-on behavior in the ESD-protection device to improve the ESD level [13], a cell-based square-type layout design is used to realized the DTDB device structure. The practical cell layout of the DTDB device structure is shown in Fig.6(a). The cross-sectional view along the line A--A' of Fig.6(a) is corresponding to that of Fig.5(b). The layout example of such ESD clamp circuit with 4 cells of DTDB is shown in Fig.6(b). The DTDB triggered on by the double-triggering design and realized by the cell-based square-type layout can significantly improve its ESD level in per unit silicon area. The concept of cell-based layout is also applied to realize the other three designs.

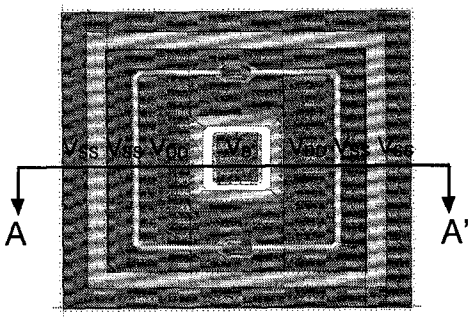


(a)

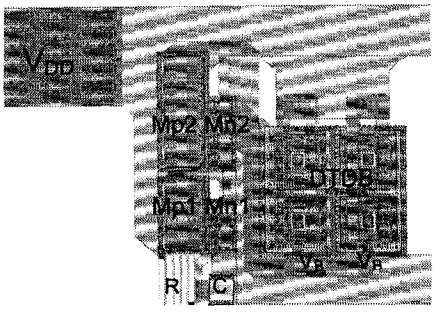


(b)

Fig.5 (a) The circuit, and (b) the device structure, of the ESD clamp circuit with the double-triggering double BJT (DTDB) structure.



(a)



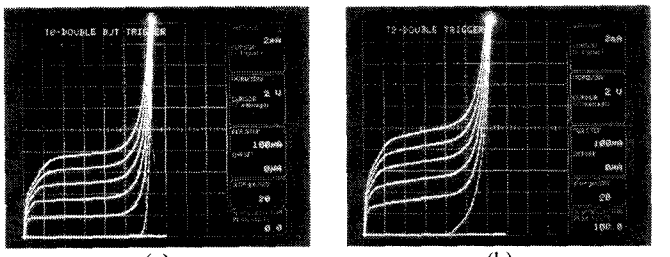
(b)

Fig.6 The layout for (a) the unit cell of DTDB device structure, and (b) the ESD clamp circuit with 4 cells of the DTDB structure.

Experimental Results

A. Device Characteristics

The ESD clamp circuits with different device sizes of the four ESD-protection devices had been fabricated in a 0.6-μm CMOS process. The unit cells of the four device structures are also fabricated independently to find their device characteristics. The measured I-V curves of the bipolar action in the STDB and the DTDB structures are shown in Fig.7. The beta gains among the four device structures are measured and shown in Fig.8. The DTDB structure has a highest beta gain among these four structures. In the low I_C region, the DTDB structure still provides a high gain because the PMOS is initially turned on.



(a) (b)

Fig.7 The I-V curves of (a) the STDB structure, and (b) the DTDB structure. (X scale : 2V/div.; Y scale : 2mA/div.)

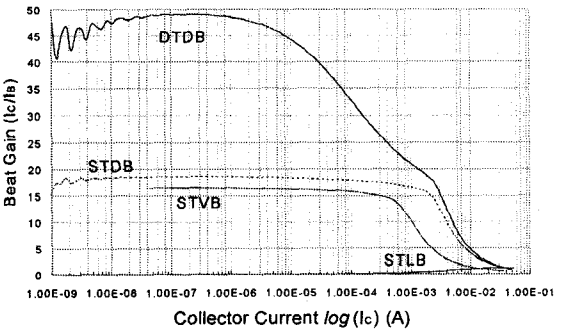


Fig.8 The dependence of the beta gains on the collector currents among the STLB, STVB, STDB, and DTDB device structures.

B. ESD Performance

The *KeyTek ZapMaster* ESD simulator is used to evaluate the ESD robustness of the proposed ESD clamp circuits with a failure criterion of 1-μA current leakage under a 5-V V_{DD} bias. The HBM (human-body model) ESD testing results are summarized in Fig.9. As expected, the ESD clamp circuits with the STDB and DTDB structures can sustain higher ESD level in per silicon area. The ESD robustness in per unit area of the STDB and DTDB structures is about 0.31 V/μm^2, and that of the STLB is about 0.22 V/μm^2. The ESD clamp circuit with the STVB structure only sustains a low ESD level of 1000V even with a larger device size. The parasitic vertical bipolar in the 0.6-μm CMOS process is found to sustain a low ESD level. The design in Fig.1 with an NMOS as the current-discharging device is also fabricated in the 0.6-μm CMOS process. With a device dimension (W/L) of 500/1.0 (μm/μm) for the NMOS, which occupies a layout

area of 6931 μm^2, the previous design (Fig.1) sustains an ESD level of 1000V only. The ESD robustness in per unit area of the NMOS is only 0.14 V/μm^2. Therefore, the STDB and DTDB can provide about two times greater ESD level than the NMOS device in per silicon area.

C. Turn-On Verification

To verify the efficiency of the ESD-transient detection design in the ESD clamp circuits, a voltage pulse with a rise time around 5 ns and a pulse width of 400 ns is applied to the V_{DD} node of the ESD clamp circuits with the V_{SS} node grounded to simulate the ESD-stress condition. The voltage waveform on the V_{DD} node is observed to find the turn-on time of the ESD clamp circuits under different pulse levels. The degraded voltage waveform, while an 8-V voltage pulse is applied to the V_{DD} node of the ESD clamp circuit with the DTDB structure, is shown in Fig.10(a). A 5-V ramp voltage with a rise time of 0.1 ms is also applied to the V_{DD} node (with the V_{SS} grounded) to verify the ESD clamp circuits being kept off in the normal power-on condition. The 5-V ramp voltage waveform on the V_{DD} node is observed and shown in Fig.10(b), where no degradation is found on the voltage waveform. This has practically verified the suitable *RC* value in the ESD clamp circuits between the power rails.

The ESD clamp circuits with other three protection devices also have similar voltage waveforms as those of Fig.10. The turn-on time in Fig.10(a) is about 125nS. The turn-on time is varying due to different pulse heights of the applied voltage pulses. The relations between the turn-on time and the pulse height of the applied voltage pulses among the ESD clamp circuits with the four different current-discharging devices are measured and shown in Fig.11.

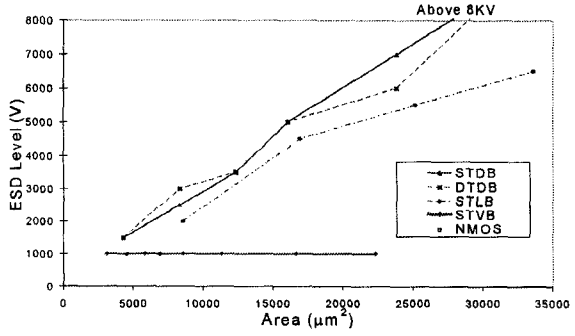
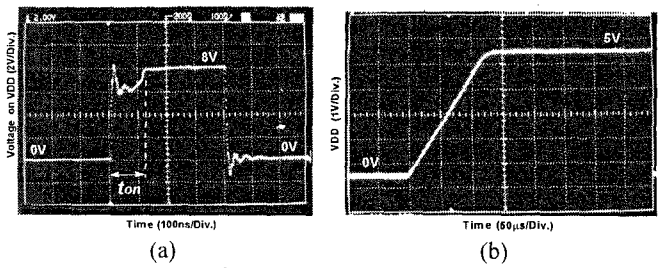


Fig.9 The relation between the HBM ESD-sustained level and the silicon area of the protection device.



(a) (b)

Fig.10 The voltage waveforms on the V_{DD} node of the ESD clamp circuit with the DTDB structure due to the triggering of (a) an 8-V voltage pulse with a rise time of 5ns, and (b) a 5-V ramp voltage with a rise time of 0.1ms.

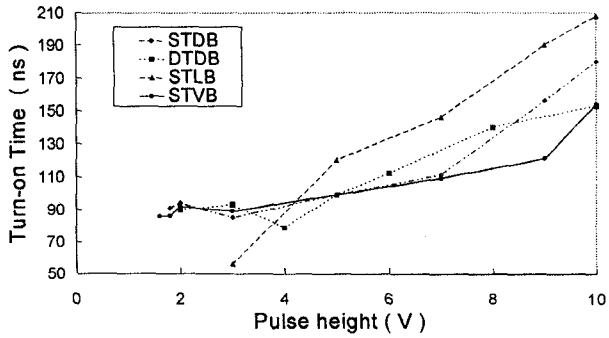


Fig.11 The relations between the turn-on time and the pulse height of the applied voltage pulses on the ESD clamp circuits with different current-discharging devices.

Conclusion

Cost-efficient power-rails ESD clamp circuits with four different device structures have been practically investigated in a 0.6-μm CMOS process. By using the substrate-triggering technique, the DTDB, STDB, and STLB device structures can provide higher ESD robustness within smaller layout area as comparing to the previous design with the NMOS device. But the vertical p-n-p BJT in the 0.6-μm CMOS process even with a large device size still sustains a very low HBM ESD level. With suitable design on the current-discharging device structures, the layout area of the ESD clamp circuit to achieve whole-chip ESD protection can be significantly reduced to save the silicon cost of the CMOS ASIC's.

References

[1] C. Duvvury, R. N. Rountree, O. Adams, "Internal Chip ESD Phenomena Beyond the Protection Circuit," *IEEE Trans. On Electron Devices*, vol. 35, pp. 2133-2139, Dec., 1988.

[2] M. D. Jaffe and P. E. Cottrell, "Electrostatic discharge protection in a 4-Mbit DRAM," *EOS/ESD Symp. Proc.*, 1990, EOS-12, pp.218-223.

[3] C. C. Johnson, T. J. Maloney, and S. Qawami, "Two unusual HBM ESD failure mechanisms on a mature CMOS process," *EOS/ESD Symp. Proc.*, 1993, EOS-15, pp. 225-231.

[4] H. Terletzki, W. Nikutta, and W. Reczek, "Influence of the series resistance of on-chip power supply buses on internal device failure after ESD stress," IEEE Trans. On Electron Devices, vol. 40, pp. 2081-2083, Nov., 1993.

[5] R. Merrill and E. Issaq, "ESD design methodology," EOS/ESD *Symp. Proc.*, 1993, EOS-15, pp. 233-237.

[6] S. Dabral, R. Aslett, and T. Maloney, "Core clamps for low voltage technologies," EOS/ESD *Symp. Proc.*, 1994, EOS-16, pp. 141-149.

[7] E. R. Worley, *et al.*, "Sub-micron chip ESD protection schemes which avoid avalanching junctions," EOS/ESD *Symp. Proc.*, 1995, pp. 13-20.

[8] G. D. Croft, "ESD protection using a variable voltage supply clamp," EOS/ESD *Symp. Proc.*, 1994, EOS-16, pp. 135-140.

[9] J. T. Watt and A. J. Walker, "A hot-carrier triggered SCR for smart power bus ESD protection," IEDM Tech. Digt., 1995, pp.341-344.

[10] J. S. Mass and D. A. Skjeie, "Testing electronic products for susceptibility to electrostatic discharge," EOS/ESD *Symp. Proc.*, 1990, EOS-12, pp. 92-96.

[11] R. Lewis and J. Minor, "Simulation of a system level transient-induced latchup event," EOS/ESD *Symp. Proc.*, 1994, pp. 193-199.

[12] G. Weiss and D. Young, "Transient-induced latchup testing of CMOS integrated circuits," EOS/ESD *Symp. Proc.*, 1995, pp. 194-198.

[13] M.-D. Ker and T.-S. Wu, "Novel octagonal device structure for output transistors in deep-submicron low-voltage CMOS technology," *IEDM Tech. Digt.*, 1996, pp.889-892.