ESD Protection for CMOS ASIC in Noisy Environments with High-Current Low-Voltage Triggering SCR Devices

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Abstract---A practical solution has been proposed to safely apply the LVTSCR (low-voltage-trigger SCR) device for output ESD (electrostatic discharge) protection in the advanced submicron CMOS ASIC's without being accidentally triggered on in the noisy operating environments. By increasing the trigger current of the LVTSCR device up to 200mA, a noise margin greater than VDD+12V (VSS-12V) against the accidental triggering due to the overshooting (undershooting) noise pulses has been practically confirmed by the experimental results. Due to remaining a lower trigger voltage, this solution can still provide effective ESD protection for output transistors but only occupies a small layout area.

Introduction

The lateral SCR device had been used as an effective ESD-protection element for input pins in submicron CMOS IC's [1]-[3]. To effectively protect the CMOS output buffer, the LVTSCR (low-voltage triggering SCR) device had been invented with a much lower trigger voltage [4]-[7]. The trigger voltage of the LVTSCR is equivalent to the snapback-trigger voltage of the short-channel NMOS (or PMOS) device, which is inserted into the lateral SCR structure, rather than the original switching voltage (about 30~50V) of the lateral SCR device. By suitable design, the trigger voltage of the LVTSCR can be lower than the breakdown voltage of the output NMOS (PMOS) [6]. The typical device I-V characteristics of the LVTSCR is shown in Fig.1. The trigger voltage (current) of the LVTSCR in a submicron CMOS technology is about ~10V (~10mA). With such a low trigger voltage, the LVTSCR can provide effective ESD protection for the CMOS output buffer, but the lower trigger current may cause the LVTSCR being accidentally triggered on by the external overshooting noise pulses on the output pins while the CMOS IC is in the normal operating conditions. So, to safely apply the LVTSCR for ESD protection, the LVTSCR must have an enough noise margin for CMOS ASIC's in the noisy environments.

There are two possible methods to avoid the LVTSCR being accidentally triggered on by the noise pulses when the IC's are in the normal operating conditions. As shown in Fig.2(a), one is to increase the holding voltage of the LVTSCR to be greater than the voltage of VDD. But, increasing the holding voltage of LVTSCR leads to more power dissipation (Power ≅ IESD×Vhold) on the LVTSCR during the ESD transition. This will cause a much lower ESD robustness of the LVTSCR. Moreover, to increase the holding voltage of LVTSCR greater than VDD in the bulk CMOS process is difficult and often needs to occupy much more layout area and latchup guardrings. Another method is to only increase the trigger current of the LVTSCR, but the trigger voltage and the holding voltage are kept the same, as shown in Fig.2(b). With higher trigger current, the LVTSCR can have enough noise margin against the overshooting or undershooting noise pulses without either degrading its ESD robustness or occupying a large layout area.

In this paper, a high-current PMOS-trigger lateral SCR (HIPTSCR) and a high-current NMOS-trigger lateral SCR (HINTSCR) with lower trigger voltage but higher trigger current are proposed to safely protect the CMOS ASIC's in the noisy environments.

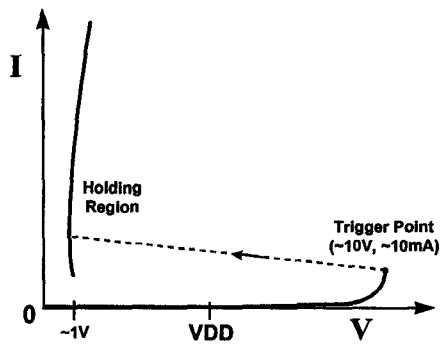

Fig.1 The typical I-V characteristics of the LVTSCR device in submicron CMOS technologies.

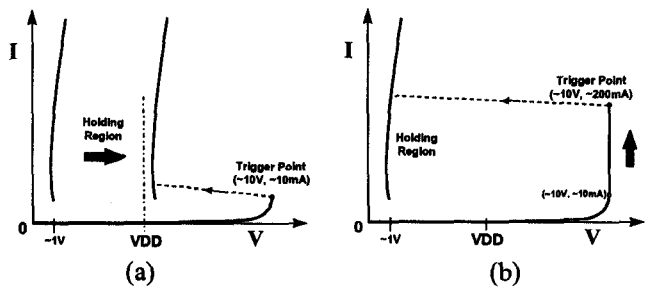

Fig.2 Two possible methods, (a) increasing the holding voltage; (b) increasing the trigger current, to avoid the LVTSCR being accidentally triggered on by the noise pulses.

High-Current Low-Voltage Triggering SCR's

The device structures of the high-current low-voltage triggering SCR's to protect the CMOS output transistors are

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shown in Fig.3. In Fig.3(a), a current-bypass diode Dn2 is added into the latching path of the PMOS-trigger lateral SCR to form the HIPTSCR device. In Fig.3(b), a current-bypass diode Dp2 is added into the latching path of the NMOS-trigger lateral SCR to form the HINTSCR device. The current-bypass diodes Dn2 and Dp2 located in the latching paths of the SCR structures can absorb partial current away from the latchup path, so the trigger current to initiate the regeneration process of latchup in the HINTSCR and HIPTSCR can be significantly increased [8].

The schematic circuit diagram of using the HIPTSCR and HINTSCR to protect the CMOS output buffer is shown in Fig.4. Since ESD voltages may have positive or negative polarities on a pin to the VDD or the VSS pins, there are four ESD-stress conditions (PS, NS, PD, and ND modes [7]) on an output pad with the CMOS output buffer. The ESD failure threshold of an output pin is defined as the lowest (in absolute value) ESD-sustained voltage of the four-mode ESD stresses at the pin. In the CMOS output buffer, there also exist two parasitic junction diodes, Dp1 and Dn1, in the device structures of the output PMOS and NMOS. The Dp1 (Dn1) is forward biased in the PD-mode (NS-mode) ESD-stress condition. The diode in its forward-biased condition can sustain high ESD voltage. So, the CMOS output buffer often has a much higher ESD robustness in the PD-mode and NS-mode ESD stresses than it in the PS-mode and ND-mode ESD stresses. Therefore, the HIPTSCR and HINTSCR are designed to improve the ESD robustness of the CMOS output buffer in the PS-mode and ND-mode ESD stresses, respectively.

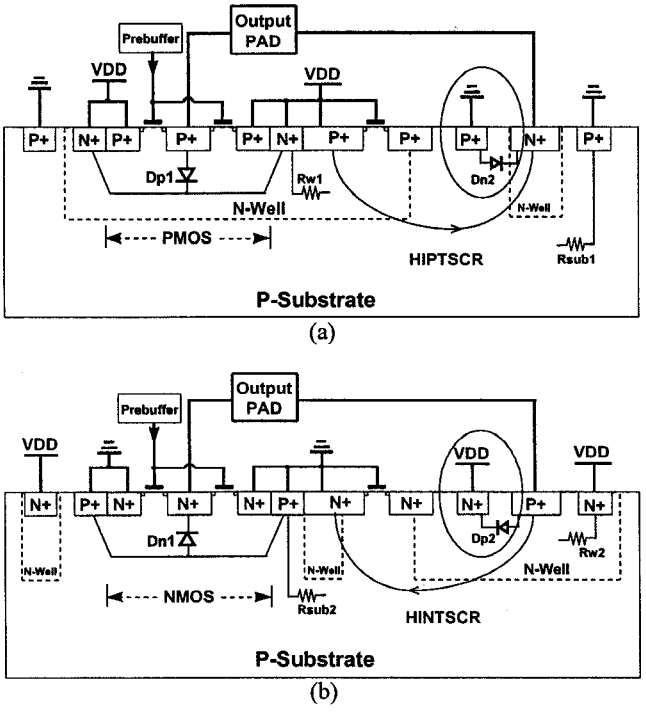


Fig.3 The schematic cross-sectional view of, (a) the HIPTSCR; (b) the HINTSCR, merged with the output transistors in a P-substrate N-well CMOS process.

The HIPTSCR (HINTSCR) can be merged with the output PMOS (NMOS) in the device structure to save the occupied silicon area. A practical layout example of the HIPTSCR and HINTSCR devices merged with the CMOS output buffer in a typical 0.6-μm CMOS technology is shown in Fig.5. The layout area occupied by the HIPTSCR (HINTSCR) in Fig.5 is only $60 \times 37.6\ \mu m^2$.

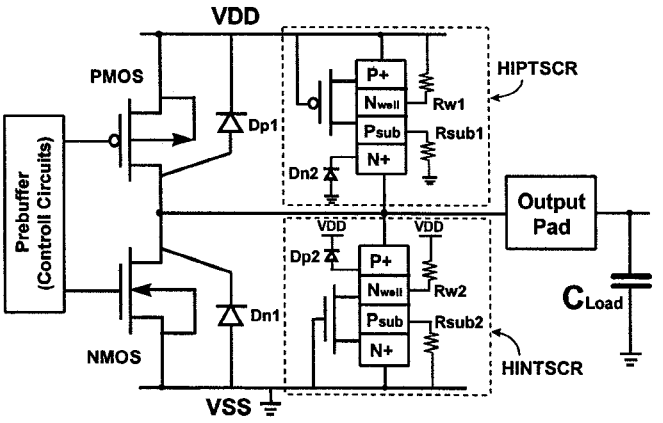


Fig.4 The schematic circuit diagram of a CMOS output buffer protected by the HIPTSCR and HINTSCR devices.

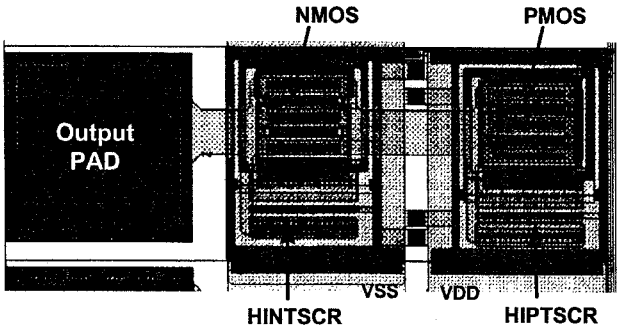


Fig.5 A layout example of the CMOS output buffer merged with the HIPTSCR and HINTSCR devices.

Experimental Results

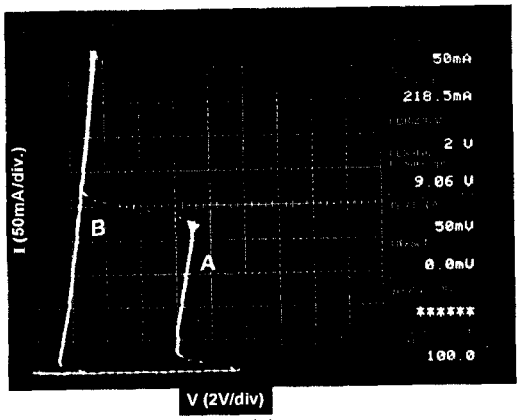
A. Device I-V Characteristics :

One set of testkeys fabricated by a 0.6-μm CMOS technology with LDD and polycide processes is measured and tested. The I-V characteristics of the HINTSCR and HIPTSCR devices are shown in Fig.6. The channel length of the NMOS (PMOS) inserted into the HINTSCR (HIPTSCR) device structure is 0.8μm. The channel length of the output NMOS (PMOS) is 1.0μm.

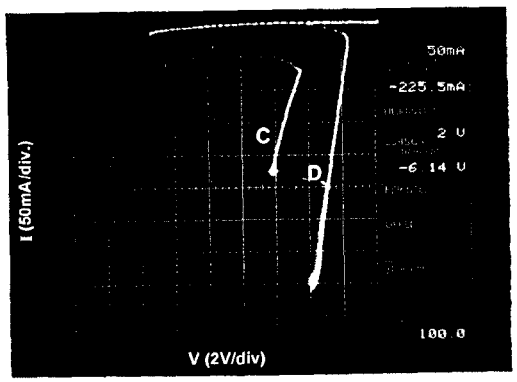
In Fig.6(a), the HINTSCR has two trigger points in its I-V characteristics. The first trigger point in Fig.6(a) is due to the drain snapback breakdown of the inserted short-channel NMOS. Due to the presence of the current-bypass diode Dp2, there is a buffer region in the I-V characteristics marked as "A" in Fig.6(a) before the lateral SCR in the HINTSCR is triggered on. As the applied current is still increased, the lateral SCR in the HINTSCR will be finally triggered on. So, there is the second trigger point in the I-V curves of Fig.6(a). The measured second trigger current (voltage) of the

HINTSCR is as high as 218.5mA (9.06V). After the second trigger point, the I-V curve enters into the latchup holding region "B" in Fig.6(a), which is due to the latching action of the lateral SCR structure in the HINTSCR. The minimum holding voltage (current) of the region B is as low as 1.34V (12.5mA). In the region A, the HINTSCR can be safely operated in this snapback region without causing any damage. With this buffer region A, the HINTSCR is not triggered on by the external noise pulses, but it can be triggered on by the ESD pulses.

Similarly, the HIPTSCR also has two trigger points in its I-V curves of Fig.6(b). The buffer region marked as "C" in Fig.6(b), before the lateral SCR in the HIPTSCR is triggered on, is owing to the presence of the current-bypass diode Dn2 and the inserted short-channel PMOS in the HIPTSCR device structure. As the applied negative current is still increased, the lateral SCR in the HIPTSCR can be finally triggered on and cause a second trigger point in the I-V curves of Fig.6(b). The second trigger current (voltage) in the HIPTSCR is -225.3mA (-6.14V). After the second trigger point, the I-V curve enters into the latchup holding region "D" in Fig.6(b), which is due to the latching action of the lateral SCR structure in the HIPTSCR. In the region C, the HIPTSCR can be safely operated in this snapback region without causing any damage. With this buffer region C, the HIPTSCR is not triggered on by the external noise pulses, but it can be triggered on by the ESD pulses.



(a)



(b)

Fig.6 The measured I-V characteristics of (a) the HINTSCR device, (b) the HIPTSCR device.

B. Noise Margin :

To investigate the noise margin of the HINTSCR against the overshooting voltage pulses, an experimental setup is shown in Fig.7. A positive voltage pulse with a low-level voltage of 3V generated from a pulse generator is used to simulate the overshooting noise on the output pad while the IC is in its normal operating condition with the power supplies of 3-V VDD and 0-V VSS. In Fig.7, the output NMOS is off but the output PMOS is on by its gate grounded to provide a 3-V voltage to the output pad. If the HINTSCR is triggered on by the overshooting noise pulse, the voltage level on the output pad will be dropped down to VSS due to the very low turn-on resistance of the HINTSCR. But, if the HINTSCR is not triggered on, the voltage level on the output pad will be remained at 3V after the transition of the overshooting noise pulses.

The measured results are shown in Fig.8. The voltage waveform in Fig.8(a) is the original overshooting voltage pulse generated from the pulse generator, which has a low-level voltage of 3V and a high-level voltage of up to 15V with a pulse width of 250μS. As this overshooting voltage pulse is applied to the output pad as that shown is Fig.7, the voltage waveform on the output pad is monitored and shown in Fig.8(b). The 15-V high-level voltage is clamped to about only 3.5V by the diode Dp1. After the triggering of the 15-V overshooting voltage pulse on the output pad, the voltage waveform on the output pad is still kept at 3V without any degradation. So, the HINTSCR still remains off. Thus, the noise margin of the HINTSCR has been verified to be greater than VDD+12V.

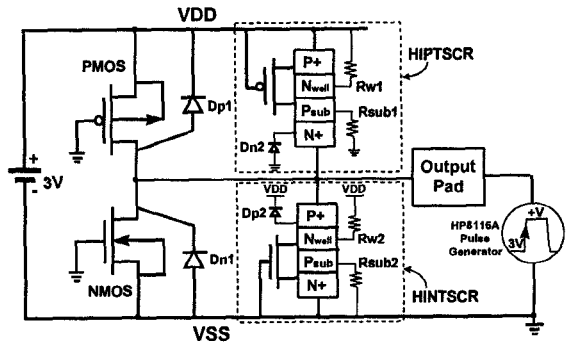
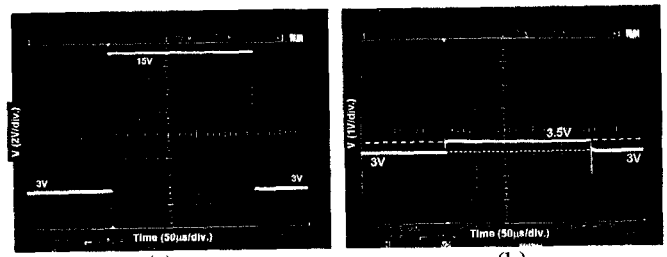


Fig.7 An experimental setup to investigate the noise margin of the HINTSCR in the output overshooting condition with the 3-V VDD and 0-V VSS biases.



(a) (b)

Fig.8 (a) The applied voltage pulse to simulate the overshooting noise pulse on the output pad. (b) The clamped voltage waveform on the output pad without triggering on the HINTSCR.

Similarly, to investigate the noise margin of the HIPTSCR against the undershooting voltage pulses, an experimental setup is shown in Fig.9. An undershooting voltage pulse with a high-level voltage of 0V and a negative low-level voltage is applied to the output pad, while the output PMOS is off but the output NMOS is on to provide a 0-V voltage to the output pad. If this undershooting voltage pulse can accidentally trigger on the HIPTSCR, the voltage on the output pad will be raised up to VDD due to the very low turn-on resistance of the HIPTSCR. So, by monitoring the voltage waveform on the output pad, we can verify whether the HIPTSCR is triggered on by the undershooting voltage pulse or not. The measured results are shown in Fig.10. The original undershooting voltage pulse generated from the pulse generator is shown in Fig.10(a), where the undershooting voltage pulse has a low-level voltage of -12V. As this -12V undershooting voltage pulse is applied to the output pad, the voltage waveform on the output pad is degraded as shown in Fig.10(b). The low-level voltage of -12V in the undershooting voltage pulse is clamped by the diode Dn1 to only about -0.72V. After the transition of the undershooting voltage pulse, the voltage on the output pad is remained at 0V. So, the HIPTSCR is not triggered on by the applied -12V undershooting voltage pulse. This has verified that the HIPTSCR has a noise margin greater than VSS-12V.

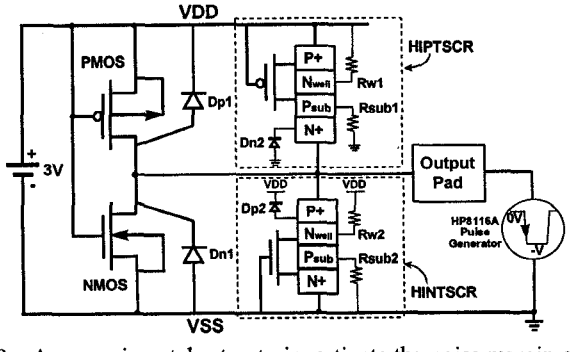
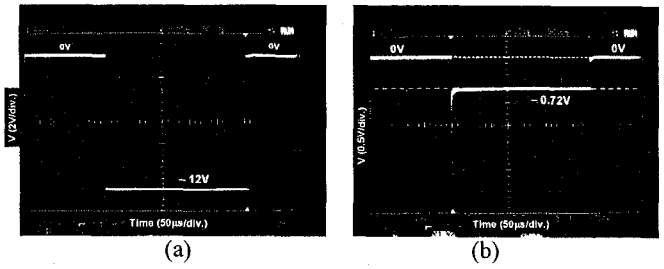


Fig.9 An experimental setup to investigate the noise margin of the HIPTSCR in the output undershooting condition with the 3-V VDD and 0-V VSS biases.



(a) (b)

Fig.10 (a) The applied voltage pulse to simulate the undershooting noise pulse on the output pad. (b) The clamped voltage waveform on the output pad without triggering on the HIPTSCR.

C. ESD Roubstness :

The ESD-stress voltage is set to begin with the initial voltage of ±1000V and increase up to ±8000V in an Human-Body-Model (HBM) ESD tester. The four modes of ESD stresses are applied to the testchip, in which a modified CMOS output buffer with an N-well resistor to improve ESD protection [9] is also tested as a reference. The failure criterion is defined as the leakage current of the CMOS output buffer in its off state becomes above 1μA. The results are listed in Table I, where the CMOS output buffer with the HIPTSCR and HINTSCR devices can provide an ESD failure threshold of 4000V for the output pin in the HBM ESD testing. The modified CMOS output buffer, even with the N-well resistor [9], only sustains an HBM ESD stress of 1250V. This has practically verified the excellent ESD-protection capability of the HIPTSCR and HINTSCR devices for CMOS output buffers.

Table I

	Modified CMOS Output Buffer with N-well Resistor [9]				This Work			
Device Dimension W/L (μm/μm)	PMOS (300/1.0)		NMOS (200/1.0)		HIPTSCR + PMOS (312/1.0)		HINTSCR + NMOS (300/1.0)	
Layout Area (μm × μm)	112.6 X 52		136.2 X 52		114.4 X 86 (60 X 37.6 for HIPTSCR)		117.4 X 86 (60 X 37.6 for HINTSCR)	
ESD-Sress Condition	PD-Mode	ND-Mode	PS-Mode	NS-Mode	PD-Mode	ND-Mode	PS-Mode	NS-Mode
HBM ESD Sustain Voltage (V)	7250	-1750	1250	-4500	above 8000	-5500	4000	above -8000

Conclusion

The accidental triggering of the LVTSCR device, due to the overshooting or undershooting noise pulses, has been successfully overcome by increasing the trigger current of the LVTSCR device. By adding the current-bypass diodes into the device structures, the HIPTSCR and HINTSCR can still provide the CMOS output buffer with high ESD robustness as the LVTSCR does. But, the HIPTSCR and HINTSCR have a much safe margin against the external noise pulses on the output pad. These HIPTSCR and HINTSCR can be also applied to protect the input pins of the CMOS ASIC's in the noisy environments.

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