Efficient Output ESD Protection of High-Speed SRAM IC with Well-Coupled Technique in Sub-μm CMOS Technology

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Abstract

A well-coupled field-oxide device (WCFOD) has been proposed to effectively improve ESD robustness of output buffers in a 0.5-μm CMOS process. ESD-transient voltage is coupled to the bulk of the field-oxide device through a parasitic capacitor to trigger on the lateral bipolar action of the field-oxide device. A 0.5-μm high-speed 256K SRAM product had been fabricated with this WCFOD to practically verify the excellent efficiency for output ESD protection. The HBM ESD failure voltage of this SRAM product has been improved up to above 6.5KV without using any extra ESD-modification process, whereas the original output buffer just can sustain the HBM ESD stress of 1KV only.

Introduction

Due to the rapid development on CMOS technology, CMOS devices have been scaled down into deep-submicron regime with thinner gate oxide, shorter channel length, shallow drain/source junction, LDD (lightly-doped drain) structure, and silicided diffusion. These advanced processes much degrade ESD robustness of CMOS IC's in submicron or deep-submicron technologies [1], [2]. Especially, the drains of output transistors in CMOS output buffers are often directly connected to the pad to drive external load, so the output transistors are more sensitive to ESD stress. But, even with large device dimensions, ESD protection capability of the output transistors is still seriously degraded by the advanced submicron CMOS technologies [3]-[5]. An output buffer with enough driving/sinking capability, higher ESD reliability, but smaller layout area is more requested by CMOS IC's in the advanced CMOS technologies. Therefore, it is necessary to improve ESD protection for output transistors through either process modification [6]-[9] or more effective protection design with extra ESD-protection elements [10]-[13]. In [14], a substrate-triggering technique was used to improve the ESD performance of deep submicron CMOS processes.

In [10]-[13], an n-type field-oxide device (or lateral n-p-n bipolar junction transistor) was placed in parallel with the thin-oxide output NMOS from the output pad to VSS to improve ESD robustness of the output buffer. But the snapback-breakdown voltage of the n-type field-oxide device is generally higher than that of the short-channel thin-oxide NMOS device in the general submicron CMOS technologies, the output NMOS could be still first damaged before the field-oxide device is fully turned on to bypass ESD current. To effective protect the output buffer by using the field-oxide device, a series resistor has to be inserted between the output buffer and the field-oxide device. A schematic circuit of such design is shown in Fig.1. If the series resistor R is too small, the ESD current could be still discharged through the output NMOS rather than the field-oxide device. This series resistor is used to limit the ESD current toward the output transistors, but it also limits the driving/sinking capability of the output transistors. The timing specification of the output signal is also delayed by the series resistor. If the turn-on voltage of the field-oxide device can be lowered below the breakdown voltage of the output transistors, the field-oxide device can perform excellent ESD protection for the output pad within a smaller layout area and without adding the series resistor.

In this paper, a well-coupled technique is proposed to reduce the turn-on voltage of the field-oxide device. With a lower turn-on voltage, this well-coupled field-oxide device (WCFOD) can offer excellent ESD protection for the output transistors alone without any series resistor between the output transistors and the output pad.

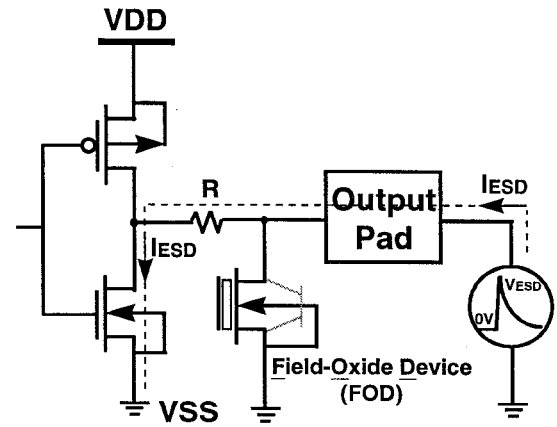


Fig.1 Output ESD protection with the field-oxide device and a series resistor.

WCFOD for Output ESD Protection

A. Original Output Buffer of the SRAM IC

Fig.2 shows the output buffer of a 256K high-speed SRAM IC in a 5-V 0.5-μm n-substrate/twin-well CMOS process. This output buffer includes a pull-up NMOS device,

MN1, and a pull-down NMOS device, MN2. A resistor R1 of 30Ω connected between the drain of MN1 device and VDD is used to limit the short-circuit transient current when MN1 and MN2 are both turned on during the logic transition. An NMOS rather than PMOS device is used as the pull-up transistor to save layout area, as well as to avoid the VDD-to-VSS latchup issue. With both considerations on the output driving capability and the chip size, the device dimensions (W/L) of MN1 and MN2 in this SRAM IC are 281/1.0 and 256/1.0 (μm/μm), respectively.

There are four different modes of ESD stresses on a pin of an IC [15]. The PS-mode ESD stress, a positive ESD voltage on the pad with relatively grounded VSS but floating VDD, has been found to be the worst case of ESD stress on the output buffer due to the snapback breakdown of the output NMOS with LDD structure or silicided diffusion. The PS-mode ESD failure voltage of such an output buffer in Fig.2 is only around 1KV in HBM (human-body model) ESD testing, but its NS-mode ESD failure voltage can pass above 8KV. The greater failure level during the NS-mode ESD stress is due to the lower clamping voltage and greater current handling capability of the parasitic diode between the drain and the bulk of the output NMOS MN2. The ESD failure threshold of an output pad is defined as the lowest ESD failure voltage among the four modes of ESD stresses, so the most important work of ESD protection for such an output buffer is to improve the PS-mode ESD failure voltage.

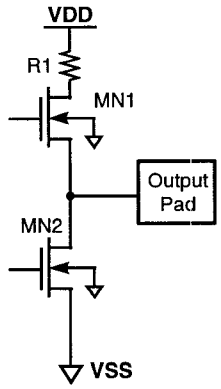


Fig.2 The original output buffer in an SRAM IC.

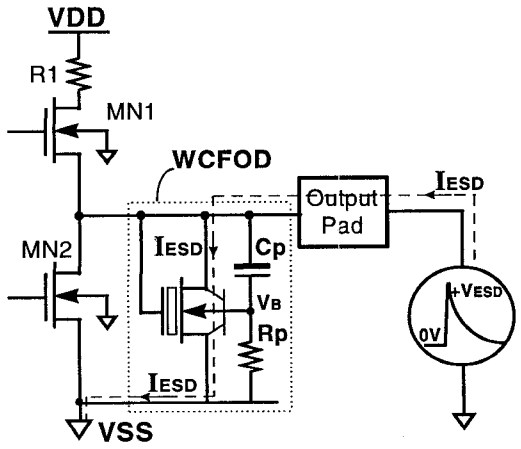


Fig.3 (a) Output ESD protection with the proposed WCFOD.

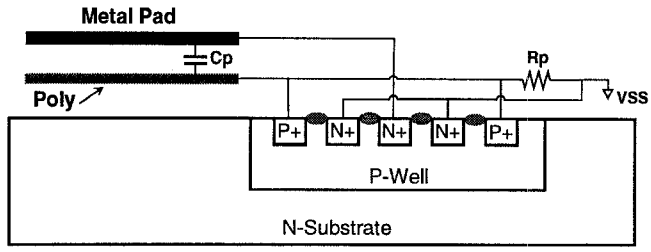


Fig.3(b) Schematic cross-sectional view of the proposed WCFOD.

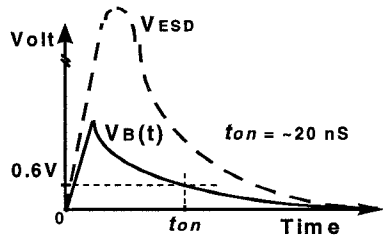


Fig.4 The schematic voltage waveform on the VB node in the WCFOD under the PS-mode ESD-stress condition.

B. Output ESD Protection with WCFOD

The proposed ESD protection with the WCFOD for output buffers is shown in Fig.3(a), and the corresponding schematic cross-sectional view of this WCFOD is shown in Fig.3(b). In Fig.3(b), the field-oxide device is formed by the N+ diffusions which are close together in a separated P-well. This separated P-well is connected to VSS through a resistor Rp. A capacitor Cp is connected from the output pad to the separated P-well to perform the well-coupling action under the PS-mode ESD stress.

As the PS-mode ESD voltage occurs on the output pad, some positive ESD-transient voltage will be coupled to the separated P-well through the capacitor Cp. This coupled positive ESD-transient voltage in the separated P-well is sustained longer in time by the resistor Rp. The schematic voltage waveform on the VB node in the WCFOD, under the PS-mode ESD-stress condition, is illustrated in Fig.4. Due to the positive voltage in the separated P-well, the bulk-to-source junction in the field-oxide device is forward biased. This leads to the lateral bipolar action in the field-oxide device to happen early with a much lower breakdown voltage. Thus, the WCFOD can be fully turned on to bypass ESD current before the output transistor is damaged. So, the output transistors can be effectively protected by the WCFOD.

The capacitor Cp in the WCFOD can be realized by inserting the poly layer right under the wire-bonding metal pad, as that shown in Fig.3(b), without increasing layout area to the output pad. This layout style of the coupling capacitor had been successfully verified in an input ESD protection circuit [16]. The sustaining resistor Rp can be realized by the poly line surrounding the output pad without increasing total layout area of the chip. Cp and Rp are designed to keep the field-oxide device off in the normal operating conditions of the SRAM IC with 5-V VDD and 0-V VSS biases, but to turn on the field-oxide device in the PS-mode ESD-stress condition. Because the voltage level and the rise time between the normal output signals and the

ESD pulses are quite different, the Cp and Rp can be easily selected.

In the practical layout of the output buffer with this WCFOD, the output transistors MN1 and MN2 are realized by the finger-type layout with 5 fingers. The field-oxide device is realized by the strip-line-type layout with a device dimension of 173/0.9 (μm/μm). A square-shape poly layer of 88×88 μm^2 is placed right under the metal pad to constitute the coupling capacitor Cp of 0.86pF. A poly line with a 400-μm length is drawn from the square-shape poly layer and surrounds the output pad to form the resistor Rp about 24KΩ. The other end of this poly line is connected to the VSS power line.

Experimental Results

An SRAM IC is used to verify the ESD-protection efficiency of this design in a 5-V 0.5-μm n-substrate/twin-well CMOS process with LDD structure. An SRAM chip with the original output buffer (as shown in Fig.2) is also fabricated in the same wafer as a basic reference. A single WCFOD device is also fabricated in the same wafer to find its device characteristics. A microphotograph of the fabricated WCFOD around an output pad is shown in Fig.5.

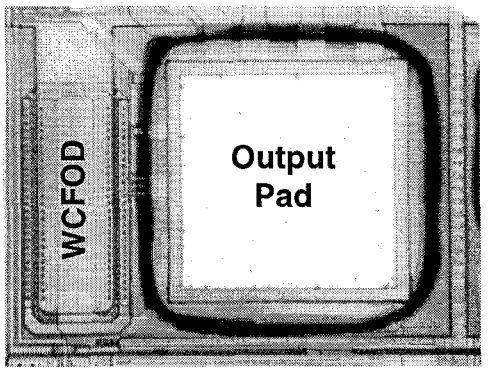
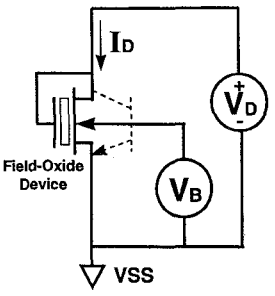


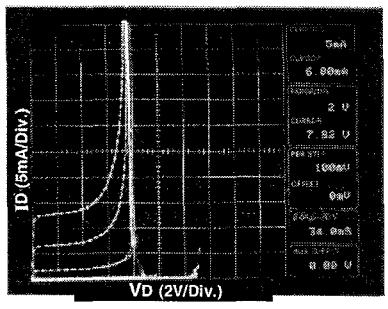
Fig.5 A microphotograph of the WCFOD used to protect the output buffer in an SRAM IC.

A. Device Characteristics of the WCFOD

Fig.6(a) shows the setup to measure the breakdown characteristics of the WCFOD with different P-well bias. The bulk (P-well) of the field-oxide device is biased with different voltages and the measured results are shown in Fig.6(b). As the P-well bias is increased above 0.6V, the snapback-trigger voltage is significantly reduced. If the P-well bias is increased above 0.8V, the lateral bipolar action in the field-oxide device has been fully turned on when its drain bias is in the low voltage region. As the drain bias increases higher, the turned-on field-oxide device finally enters into its snapback region. The relation between the P-well bias and the trigger voltage for the field-oxide device entering into its snapback region is shown in Fig.7. As the bias voltage is up to 0.8V, the snapback-trigger voltage is lowed to only about 7.8V. With such a lower snapback-trigger voltage of the field-oxide device, it can become an effective ESD-protection device to protect the output pad.



(a)



(b)

Fig.6 (a) An experimental setup to measure the snapback-breakdown characteristics of the WCFOD device under different P-well biases. (b) The measured I-V curves of the WCFOD with different P-well biases.

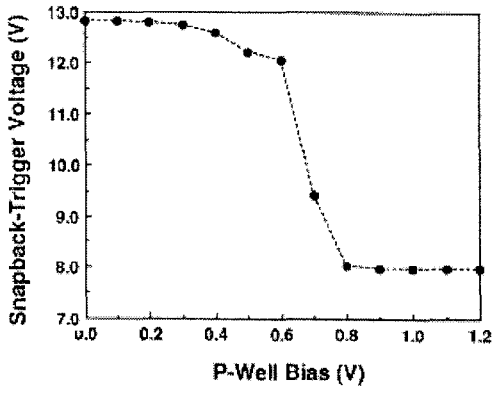


Fig.7 The dependence of P-well bias on the snapback-trigger voltage of the WCFOD in a 0.5-μm SRAM process.

B. ESD Testing Results

The 256K high-speed SRAM chips are tested by the ESD simulator in the human-body model (HBM) to investigate the efficiency of ESD protection. The ESD tester is the *Zapmaster* produced by KeyTek corp. [17]. The ESD failure criterion is defined as that the leakage current of the output pad with the output buffer and ESD protection circuit in its high-impedance state is above 1 μA under VDD (VSS) bias of 6V (0V). The high-impedance state of each output pin can be controlled by a chip-selected pin of the 256K high-speed SRAM IC.

The PS-mode ESD failure voltage of the output buffer with this WCFOD is improved up to 6.5KV in the SRAM test chip. The ESD failure voltage of the original output buffer without WCFOD is only 1KV. Because the ESD-transient voltage is coupled to the P-well of the field-oxide device to trigger on the lateral bipolar action, the WCFOD

can be turned on with a lower snapback-trigger voltage to early bypass the ESD current from the output pad to VSS. This verifies the excellent performance of WCFOD for output ESD protection. Without the series resistor into the drain of output transistors, the output driving/sinking capability of the output buffers is not degraded by the WCFOD. So, this WCFOD is very suitable for CMOS IC's in advanced submicron or deep-submicron CMOS technologies to effectively improve output ESD reliability without causing any degradation on the circuit performance.

C. Well-Coupled Efficiency

To verify the efficiency of the proposed well-coupled technique for output ESD protection with the WCFOD, a voltage pulse generated from HP8116A with a pulse width of 400 nS is applied to the output pin under the biases of 5-V VDD and 0-V VSS. The experimental setup to verify the well-coupled efficiency is shown in Fig.8. An oscilloscope is used to monitor the voltage waveform on the output pin. The chip-selected pin is also used to turn the output transistors off. If the WCFOD is not triggered on by the applied voltage pulse, the voltage waveform of the applied voltage pulse is not degraded on the pin. If enough transient voltage is coupled through the Cp to the P-well of the WCFOD due to the rising edge of the applied voltage pulse on the pin, the voltage waveform of the applied voltage pulse will be degraded by the turned-on WCFOD.

When the voltage peak of the applied voltage pulse is increased up to 7.1V, as shown in Fig.9(a), the WCFOD is still not triggered on. So, there is no degradation on the pulse-type voltage waveform in Fig.9(a). If the voltage peak is increased more than 7.1V, the WCFOD can be triggered on and the voltage waveform on the pin is degraded. A typical degraded voltage waveform is shown in Fig.9(b), where the voltage peak of the applied voltage pulse is 8.5V with its rise time of only 4.75 nS. The rising edge of the applied voltage pulse triggers on the WCFOD, so the voltage waveform in Fig.9(b) is degraded by the turned-on WCFOD after the rising edge.

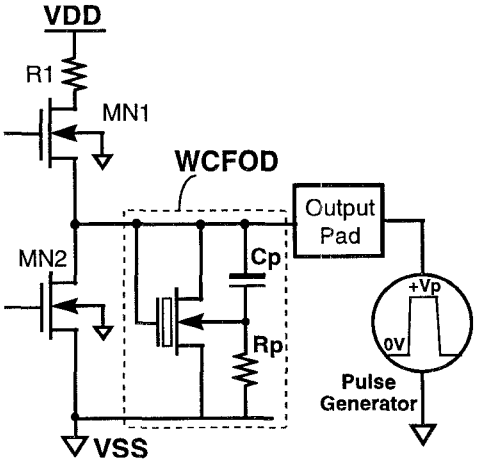
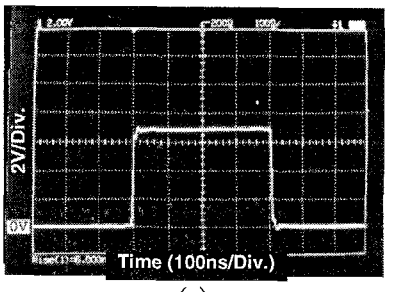
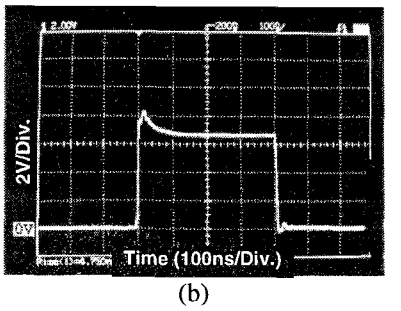


Fig.8 The experimental setup to verify the well-coupled efficiency in the fabricated WCFOD.



(a)



(b)

Fig.9 The voltage waveform of the applied pulse-type voltage on the output pin, (a) without triggering on the WCFOD, (b) with triggering on the WCFOD.

With the practical verification, the WCFOD is not triggered on by the normal 5-V input/output signals. But, the pulse-type trigger voltage of the proposed WCFOD is lowered to only 7.1V. Thus, ESD voltage can be early bypassed by the turned-on WCFOD to effectively protect the output transistors. This verifies the excellent efficiency of the proposed well-coupled technique.

D. Output Leakage Current

Another concern for the P-well of the WCFOD connected to VSS through a poly resistor is the off-state leakage current as the WCFOD is applied to protect the I/O pad. In an I/O pad, it may become an input pad as the output transistors are kept off by the control of internal circuits. The leakage currents on the I/O pads of the SRAM IC with the WCFOD and without the WCFOD are investigated. A chip-selected pin in the SRAM IC, which can keep all the I/O pins in the high-impedance state, is used to turn off the output transistors. An input voltage sweeping from 0 ~ 5 V generated by HP4145 is applied to the I/O pin under the high-impedance condition, and then the input current is observed as the leakage current of the pin. The experimental setup to measure the leakage current of the output pin is shown in Fig.10. A typical measured I-V curves for the leakage current on the output pad without or with the WCFOD are shown in Fig.11. As shown in Fig.11, the leakage current increases as the applied voltage is increased. The maximum leakage current occurs as the applied voltage is increased to 5V. The leakage current could occur in the output transistors or in the WCFOD. The leakage current on the output pin with the original output buffer is shown in Fig.11(a), where the maximum leakage current in the original design is 1.7 pA. The leakage current on the output

pin with the output buffer and the WCFOD is shown in Fig.11(b). The I/O pin with the WCFOD is found to have the maximum leakage current of only 1.8 pA. The maximum leakage current of the I/O pin with the WCFOD is only 0.1-pA greater than that of the original design. This indirect P-well bias leads to the increase of maximum leakage current only about 0.1 pA. The maximum leakage current in the order of only 1.8 pA on the I/O pin is still very small without causing any degradation on the circuit performance of the I/O pin.

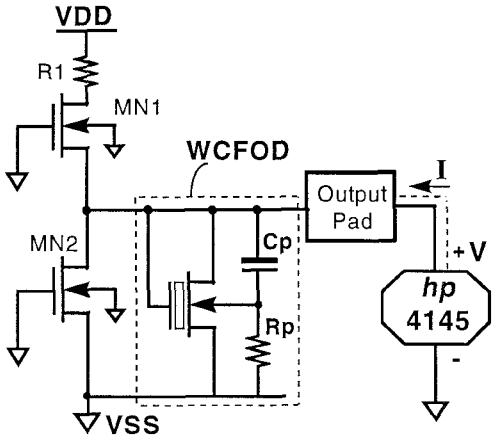
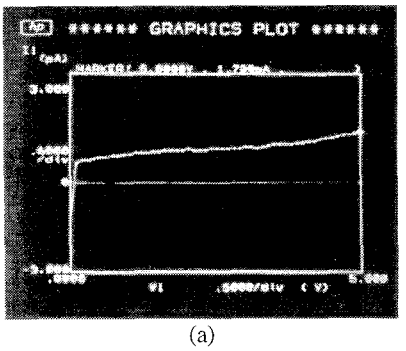
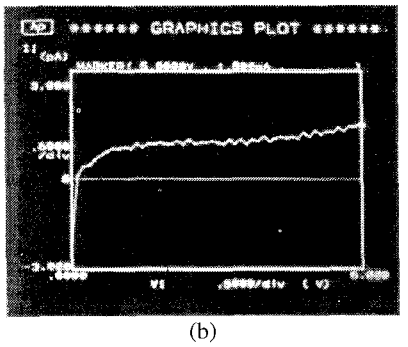


Fig.10 The experimental setup to measure the leakage current of the output pin protected by the WCFOD.



(a)



(b)

Fig.11 The measured leakage current on the output pin (a) without the WCFOD, (b) with the WCFOD.

Conclusion

A new ESD protection technique for the output pad with the well-coupled field-oxide device has been successfully verified and practically applied in a 0.5-μm 256K high-speed SRAM IC. This WCFOD has the benefits of lower snapback-trigger voltage, higher ESD protection capability, and without adding the series resistor between the output NMOS and the output pad. The ESD reliability of output buffers can be effectively improved without causing any degradation on the circuit performance of the high-speed SRAM IC. By only inserting the field-oxide device in the empty layout region with the poly capacitor under the pad and poly resistor around the pad, the total chip size of the SRAM IC with the WCFOD is not increased. The HBM ESD reliability of this SRAM IC has been improved up to 6.5KV, whereas the original output buffer without the WCFOD just can sustain PS-mode ESD stress of 1KV only.

With the obvious advantages of lower trigger voltage and higher ESD robustness, this proposed WCFOD is also very suitable to protect the thinner gate oxide of the input stages of CMOS IC's in deep-submicron technologies.

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