Layout Verification to Improve ESD/Latchup Immunity of Scaled-Down CMOS Cell Libraries

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Abstract --- Layout verification has been proposed to improve the ESD (Electrostatic Discharge) and latchup immunity of scaled-down CMOS cell libraries. By using the DRC (design rules check) and ERC (electrical rules check), the ESD/latchup sensitive layout can be found. By changing the layout in the suggested way of high immunity to ESD and latchup without increasing the layout area of the cells, the ESD and latchup reliability of CMOS IC's assembled by the layout-verified cell libraries can be significantly improved.

Introduction

The CMOS technology had been scaled down into the deep-submicron regime. The minimum spacing or clearance between the P+ or N+ diffusions has been also much reduced to save the layout area. With the scaled-down spacings, the parasitic lateral bipolar action is enhanced. The latchup immunity of submicron or deep-submicron CMOS IC's is seriously reduced if the trench-isolation process or the epi-layer wafer are not used.

Besides the latchup issue, the scaled-down CMOS IC's are also sensitive to ESD stresses [1]. Not only the input or output pins are easily damaged by the ESD, but the internal circuits are still sensitive to ESD damage. Because the ESD events on the input or output pads have been well known by the designers, suitable ESD-protection designs for the input and output cells have been included in the standard CMOS cell libraries. But, in the scaled-down CMOS IC's, some unexpected ESD damages had still been found to locate at the internal circuits beyond the input and output ESD protection circuits [2]-[5]. Especially, the component-level ESD test had caused a failure in the latchup path of the internal circuits [2].

The ESD current may enter into any pin and go out from another pin of the IC. The pin-to-pin ESD-stress condition is illustrated in Fig.1 [1], where a positive ESD voltage is applied to an input pin while another output pin is relatively grounded but the VDD and VSS pins are floating. Such a pin-to-pin ESD stress often causes the ESD voltage to become across the VDD and the VSS power lines. Certainly, the ESD voltage may be directly applied to the VDD pin while the VSS pin is grounded, as illustrated in Fig.2. Because the VDD and VSS power lines are often distributed everywhere in a chip, the ESD voltage across the VDD and VSS power lines is diverted into the internal parts of the IC and easily causes serious ESD damages on the internal circuits. The ESD-induced latchup failure on the internal circuits will become more serious in the scaled-down CMOS IC's if there are latchup-sensitive layouts in the internal circuits. Moreover, some ESD damages have been also found to locate at the parasitic n-p-n bipolar transistor between the VDD and VSS, which is formed by two N+ diffusions with a narrow spacing [5].

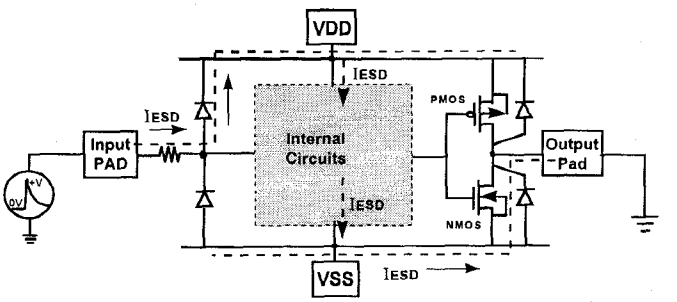

Fig.1 Schematic circuit diagram to show the internal ESD damage due to the pin-to-pin ESD stress.

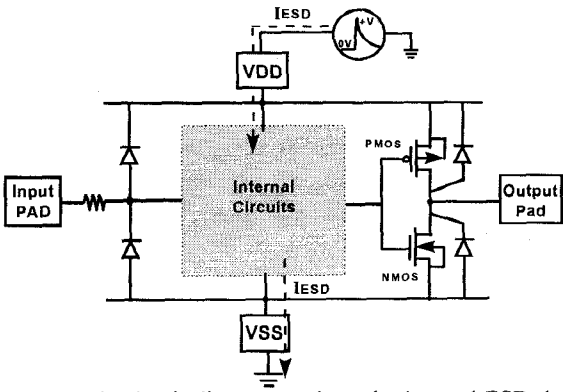

Fig.2 Schematic circuit diagram to show the internal ESD damage due to the VDD-to-VSS ESD stress.

Recently, due to the request of the "CE" mark from the European Community, an ESD gun with the ESD voltage of 8KV or even up to 15KV is used to test the electromagnetic compatibility of the electronic products. The international standard of the electromagnetic-compatibility testing had been specified as "IEC 801-2" by the International Electron-technical Commission in 1991 [6]. Such an electromagnetic-compatibility testing by the ESD gun is the system-level ESD

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testing through the air-discharge or contact-discharge methods [6]. This system-level ESD event can not only cause the electronic system to "freeze" or "upset" , but also can actually "blow out" some of the integrated circuits in the electronic systems [7]-[9]. Such a system-level ESD event easily causes the transient-induced latchup failure on the internal circuits of the CMOS IC's [10]-[12]. Due to the peak-discharging effect of ESD events, the p-n-p-n paths in the internal circuits having the peak structure and narrower spacing in the layout are more vulnerable to system-level ESD-induced latchup failures.

In this paper, a layout verification method is proposed to find the ESD or latchup sensitive layouts in the standard cell libraries. The insensitive layout styles are also proposed to improve the ESD/latchup immunity of the scaled-down CMOS IC's.

The Scaled-Down Spacing

A. The p-n-p-n path

The ESD voltage due to component-level or system-level ESD stresses has been found to be across the VDD and VSS power lines of a CMOS IC. The ESD voltage may be diverted into the internal circuits before the ESD energy is bypassed by the ESD clamp circuits. The fast ESD-transient voltage across the VDD and VSS power lines can initiate the latchup in the internal circuits. The PMOS and NMOS transistors in the I/O circuits which are directly connected to the pads are often surrounded by double guard rings to prevent the latchup in the I/O circuits. The holding voltage of the latchup path (lateral SCR) in the I/O circuits surrounded with the double guard rings can be greater than VDD. But, in order to save the layout area, the PMOS and NMOS transistors in the internal circuits are seldom surrounded by the guard rings. Only the substrate contact (connected to VSS) and well contact (connected to VDD) are located into the internal circuits with a far spacing. For instance, the maximum distance between two substrate (or well) contacts in the design rules of the TSMC 0.6-μm CMOS process is as far as 40 μm. So, the holding voltage of the lateral SCR devices in the internal circuits is as low as 1~2V in the TSMC 0.6-μm CMOS process without using the epi-wafer. If such a latchup path in the internal circuits is triggered on by the system-level or component-level ESD-transient voltage/current spikes, it will cause the damage located in the internal circuits of the IC's. So, the latchup path in the internal circuits becomes a weak point in the IC layout against the ESD-transient voltage/current spikes.

The latchup path in the internal circuits is shown in Fig.3, where a general p-substrate CMOS process is used to demonstrate this latchup path. The p-n-p-n path between the VDD and VSS can be triggered on by the fast ESD-transient spikes. The minimum spacing between the P+ (connected to VDD) in an N-well and the N+ (connected to VSS) in the p-substrate is much reduced in the scaled-down CMOS technologies. The minimum spacings of the p-n-p-n latchup paths in the design rules of the TSMC CMOS technologies are summarized in Table I. The minimum p-n-p-n spacing is reduced from 4.8μm in a 0.8-μm CMOS process to only 2.4μm in a 0.35-μm CMOS process. The reduced p-n-p-n spacing enhances the bipolar action of the parasitic bipolar transistors in the latchup path. Therefore, the scaled-down CMOS IC is sensitive to latchup, especially the ESD-induced latchup. The typical I-V curves of the lateral SCR in the internal circuits fabricated by the TSMC 0.6-μm CMOS process is shown in Fig.4, where the spacing from the anode to the cathode of the lateral SCR (p-n-p-n path) is 12 μm. The holding voltage of the p-n-p-n path in Fig.4 is only 1.12V. If such a latchup path is triggered on by the ESD-transient voltage, a large current will flow through this latched path when the IC is under its operating conditions with the normal biases of VDD and VSS power supplies. Finally, this latched path in the internal circuits will be damaged or even burned out.

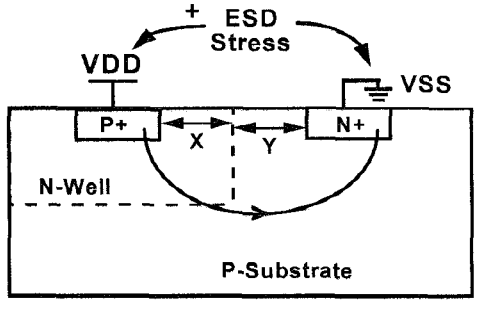


Fig.3 The sensitive latchup path in the internal circuits.

Table I

TSMC Process	X (μm)	Y (μm)	X+Y (μm)
0.8-μm	2.4	2.4	4.8
0.6-μm	1.8	1.8	3.6
0.5-μm	1.5	1.5	3.0
0.35-μm	1.2	1.2	2.4

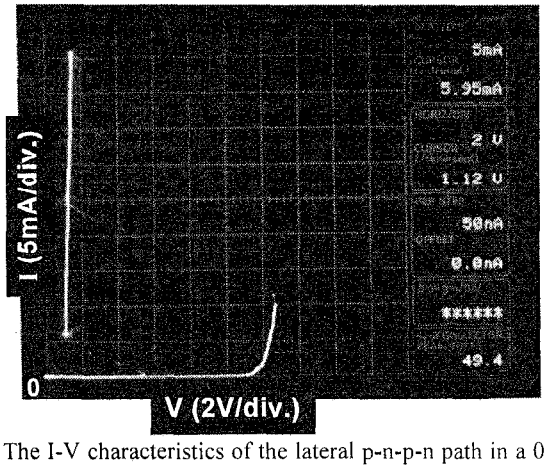


Fig.4 The I-V characteristics of the lateral p-n-p-n path in a 0.6-μm CMOS process with the spacing of 12 μm from the anode to the cathode.

Although the layout of internal circuits is not surrounded by the latchup guard rings as those used in the input and output circuits, there are still several methods to enhance the latchup immunity of the internal circuits. One is to increase the latchup immunity in the layout of the CMOS cell libraries. Three layout styles with different latchup immunity but the same circuit function are shown in Fig.5. If the internal circuit has a layout style as the worst case of Fig.5, the peak to peak structure between the VDD-connected P+ diffusion (in the PMOS) and the VSS-connected N+ diffusion (in the NMOS) is most sensitive to ESD-induced latchup. Because the ESD event to the CMOS IC's is like to the lightning to the buildings, the peak structures between the different potentials are the first discharging points in the layout. So, the corner peak of the VDD-connected P+ diffusion and the corner peak of the VSS-connected N+ diffusion in the layout of the worst case of Fig.5 will be the weakest point of the internal circuits.

The fast ESD-transient voltage across the VDD and VSS power lines, due to the ESD stresses, can trigger on the latchup path in the internal circuits. Especially, the peak structures in the layout of the internal circuits are more sensitive to the ESD-induced latchup. As the latchup path is triggered on by the fast ESD-transient voltage, the ESD current is first discharged through the low-impedance latchup path. Because the device sizes in the internal circuits are often designed with smaller dimensions, the peak structures are much easily damaged by the ESD current and to cause a short-circuit path between the VDD and VSS power lines. This leads to the malfunction of the CMOS IC's. If the peak structures can be avoided in the layout of the internal circuits, the internal circuits have a high immunity against the ESD-induced latchup. The layout as the bad case of Fig.5 also has a peak-to-peak structure between the VDD-connected P+ diffusion in the N-well and the VSS-connected N+ diffusion in the p-substrate. It is still sensitive to the ESD-induced latchup. If the connection for the drain and source of the NMOS can be changed as that of the good case in Fig.5, the peak-to-peak structure is absent between the VDD and VSS. Therefore, the internal circuits can have a higher ESD and latchup immunity.

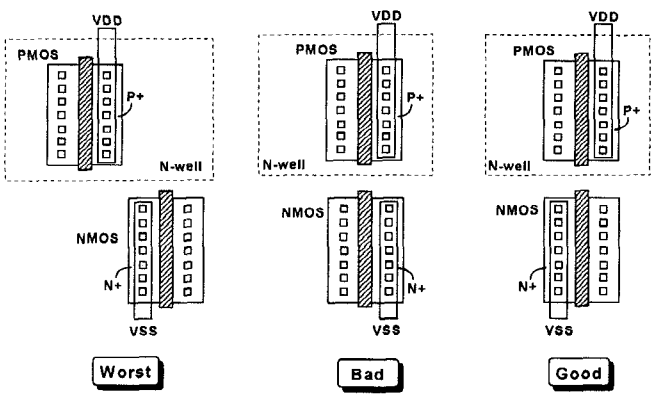


Fig.5 Three layout styles to show the different latchup sensitivity.

B. The lateral n-p-n bipolar device

Another ESD-sensitive layout in the internal circuits is the parasitic lateral n-p-n bipolar, which is formed by a VDD-connected N+ diffusion and a VSS-connected N+ diffusion with a narrow spacing. The schematic diagram of such a parasitic n-p-n bipolar device is shown in Fig.6. The I-V characteristics of the parasitic lateral n-p-n bipolar transistor is illustrated in Fig.7. The narrower spacing between the two N+ diffusions leads to the lower breakdown voltage (Vbd) and snapback voltage (Vsb) of the lateral n-p-n bipolar. The minimum spacings between two N+ diffusions in the design rules of TSMC CMOS processes are summarized in Table II. The spacing is reduced from 1.6 μm in a 0.8-μm process to only 0.6 μm in a 0.35-μm process. With such a narrower spacing, the parasitic lateral bipolar transistor is much easily triggered on by the ESD transition.

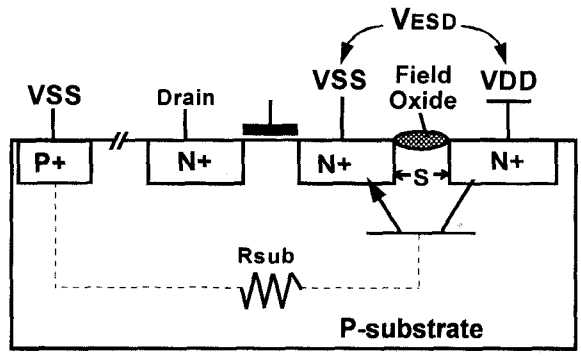


Fig.6 The parasitic lateral n-p-n bipolar transistor between the VDD and VSS power lines, which is sensitive to ESD stress.

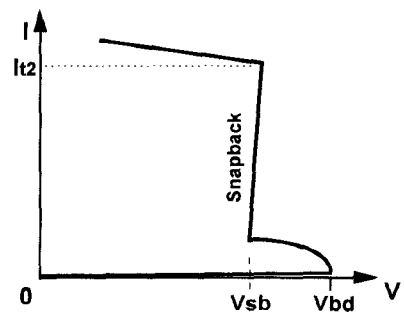


Fig.7 The schematic I-V characteristics of the parasitic lateral n-p-n bipolar transistor in the CMOS processes.

Table II

TSMC Process	Minimum S (μm)
0.8-μm	1.6
0.6-μm	1.2
0.5-μm	0.9
0.35-μm	0.6

When the IC is under the ESD-stress conditions, the ESD voltage will transfer to be across the VDD and VSS power lines of the IC. This ESD-transient voltage can trigger on the parasitic n-p-n bipolar transistor into its snapback region, and therefore causes a short-circuit path between the VDD and VSS. Then, the ESD current is mainly discharged through the snapback n-p-n bipolar transistor. Because the n-p-n bipolar transistor in the internal circuits is parasitically formed by two adjacent N+ diffusions, which often has a device size. So, such a parasitic lateral n-p-n transistor is very easily damaged by the ESD energy.

To reduce the sensitivity of the parasitic lateral n-p-n transistor in the internal circuits, a layout example is shown in Fig.8. In the bad case of Fig.8, two NMOS's are placed with a narrow spacing, but the VSS-connected N+ diffusion closes to the VDD-connected N+ diffusion. In such a way, the lateral n-p-n transistor in the bad-case layout is very easily triggered on and damaged by the ESD energy. To overcome this issue, a good layout case is shown in the right-hand part of Fig.8, where the circuit has the same function and layout area but has no dangerous lateral n-p-n transistor in the layout. So, through a correct layout design, the logic gates in the cell libraries can have better reliability against the component-level and system-level ESD stresses.

Layout Verification

As described in the above sections, the layouts of the logic gates in the cell libraries often have some ESD/latchup sensitive paths. If we can find these sensitive paths in the development of a cell library, the sensitive paths can be amended to become insensitive by suitable layout design without increasing the layout area of the cells. A method to verify the layout having ESD/latchup sensitive paths is illustrated in Fig.9, where the DRACULA [13] is used to check the spacing of the sensitive paths. By using the DRC and ERC functions of the DRACULA, the ESD/latchup sensitive paths can be found and replaced by the way of insensitive layout styles as those shown in Figs.5 and 8. Every cell layout in a cell library can be scanned by this method to find the ESD/latchup sensitive paths under the development of a cell library. Through this layout verification, the scaled-down CMOS IC's assembled by the verified cell libraries can have better immunity to ESD and latchup events.

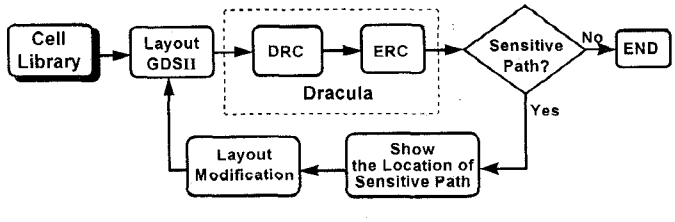


Fig.9 A flow chart to show the layout verification and modification under the development of the cell libraries in the scaled-down CMOS processes.

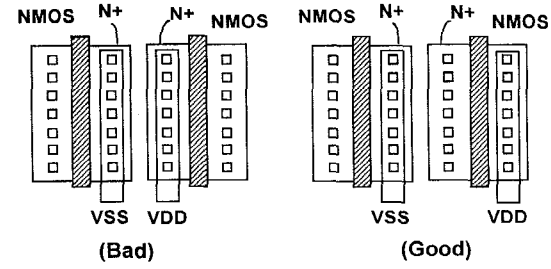


Fig.8 The different layout styles between two NMOS's with and without the parasitic lateral n-p-n bipolar transistor.

Application Examples

A typical circuit in the cell library often has both parasitic lateral n-p-n bipolar transistor and latchup-sensitive path is shown in Fig.10, which is a schmitt trigger circuit with non-inverting output. The original layout of this circuit is shown in Fig.11(a). By using the proposed layout verification method, three latchup-sensitive peak structures (marked as latchup A, B, and C) and one dangerous lateral n-p-n bipolar transistor (marked as npn BJT) are found in the layout. The typical ESD-induced damage on the parasitic lateral n-p-n bipolar transistor in a schmitt trigger circuit had been reported in [14]. These four ESD/latchup sensitive layouts can be amended to become insensitive as those shown in Fig.11(b) without increasing the total cell layout area.

In Fig.11(b), the connection for the drain and the source of an NMOS is changed, and then the peak structures of latchup A and B and the lateral n-p-n BJT are absent in the layout. The peak structure of latchup C is modified by reducing the contacts of the VDD-connected P+ diffusion [2], as shown in the top side of Fig.11(b). This contact-reduced P+ diffusion provides a series resistance along the p-n-p-n path to limit the latchup current [2], so the latchup immunity of this p-n-p-n path in the cell can be improved.

Another example having the latchup-sensitive path is the inverter, and the typical layout of a inverter in the cell libraries is shown in Fig.12(a). By using the proposed layout verification method, the latchup-sensitive path in Fig.12(a) is found to locate from the source of PMOS to the source of NMOS. By redrawing the layout in the way of Fig.12(b), this inverter can practically become latchup-insensitive without increasing the cell layout area.

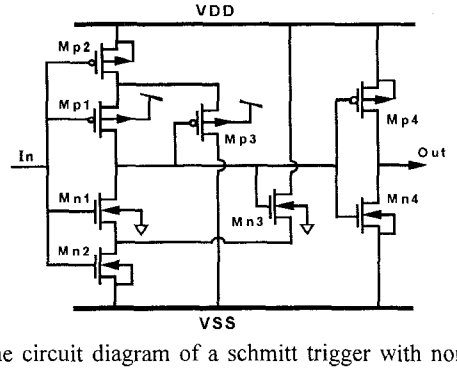
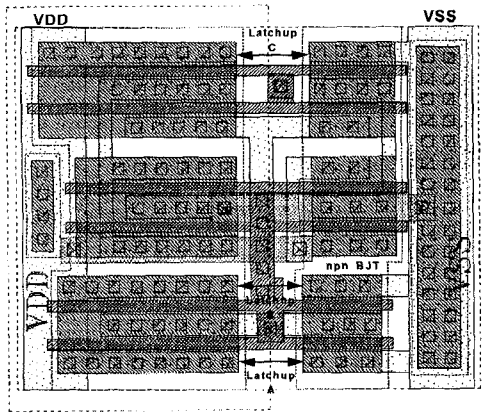
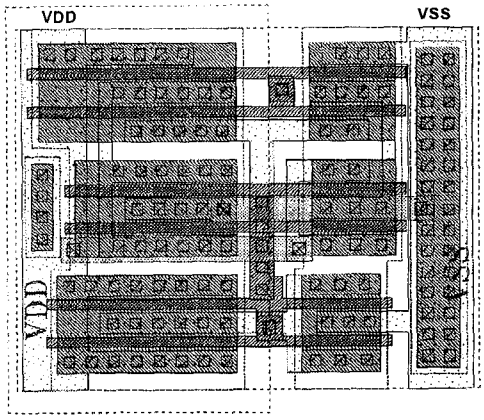


Fig.10 The circuit diagram of a schmitt trigger with non-inverting output.

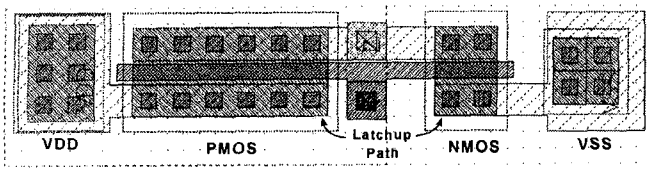


(a)

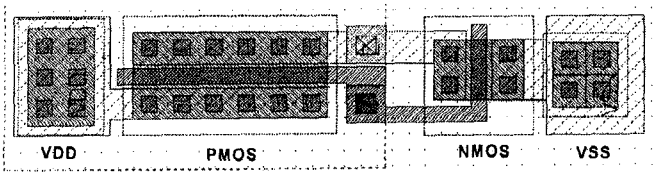


(b)

Fig.11 (a) The original layout of the schmitt trigger circuit of Fig.10 in a cell library; (b) The modified layout of the schmitt trigger circuit with better ESD/latchup reliability by using the proposed layout verification method.



(a)



(b)

Fig.12 (a) The original layout of a inverter in a cell library; (b) The redrawn layout of the inverter with better latchup reliability by using the proposed layout verification method.

Conclusion

A practical layout verification method has been proposed to find and to fix the ESD/latchup sensitive layouts in the development of scaled-down CMOS cell libraries. The ESD/latchup-insensitive layout style has been suggested without increasing the layout area of the cells. The whole chip layout after P&R can be also checked and fixed the sensitive paths by this proposed verification method. By using this proposed layout verification method, the submicron and deep-submicron CMOS IC's can still have enough immunity against the ESD/latchup events.

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