Whole-Chip ESD Protection Design for Submicron CMOS VLSI

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Abstract - A VDD-to-VSS ESD clamp circuit is designed to provide the real whole-chip ESD protection for submicron CMOS IC's. The ESD-protection efficiency is experimentally verified to be dependent on the pin location of a chip. This whole-chip ESD protection design has been successfully implemented in a 0.8-μm CMOS IC product with a real pin-to-pin ESD protection of above 3KV.

I. INTRODUCTION

ESD (electrostatic discharge) protection has become an important task on the reliability of submicron CMOS IC's. Especially in the deep-submicron CMOS technologies, the advanced processes greatly degrade the ESD robustness of CMOS IC's [1]-[2]. Besides the using of input or output ESD protection circuits around each input or output pads, there is still an important issue of unexpected ESD damage on the internal circuits of CMOS IC's beyond the input or output ESD protection circuits [3]-[5]. Even the parasitic capacitance and resistance along the power lines also have an effect on the ESD reliability of CMOS IC's [6].

Since an ESD stress may have positive or negative voltage on an input (or output) pin with reference to the grounded VDD or VSS pins, there are four different ESD-stress modes on an input (or output) pin [7]. Moreover, ESD current could enter into any pin and go out from another pin of an IC. To practically verify the whole-chip ESD reliability, two additional testing conditions have to be considered into the ESD testing. These two additional ESD testing conditions are shown in Fig.1 (a) and 1(b). In these two ESD testing conditions, the CMOS IC's are more vulnerable to internal ESD damage even if there are input and output ESD protection circuits on the input and output pads. So, to really protect a whole chip, a suitable ESD protection circuit should be added between the VDD and VSS power lines [8]-[9].

In this paper, a whole-chip ESD protection is designed with an efficient VDD-to-VSS ESD clamp circuit to protect submicron CMOS IC's without causing the unexpected ESD damage on the internal circuits. This whole-chip ESD protection has been successfully implemented in a product with a real pin-to-pin ESD protection of above 3KV.

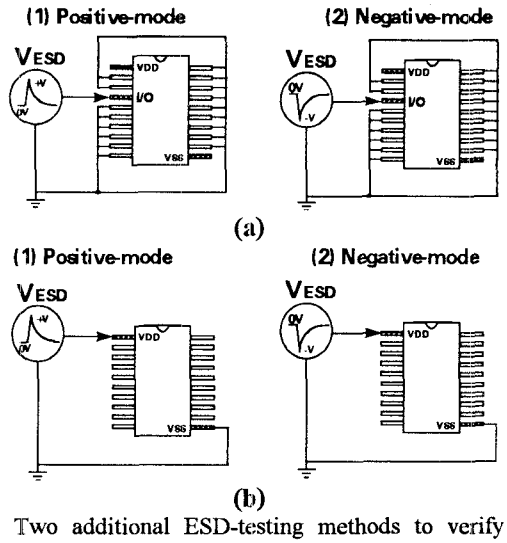

Fig.1 Two additional ESD-testing methods to verify the whole-chip ESD reliability. (a) The ESD voltage is stressed on an input (or output) pin as other input and output pins are grounded but the VDD and VSS pins are floating. (b) The ESD voltage is directly stressed on the VDD pin with grounded VSS pin but all input and output pins are floating.

II. VDD-TO-VSS ESD CLAMP CIRCUIT

The proposed VDD-to-VSS ESD clamp circuit is shown in Fig.2. This ESD clamp circuit is designed to be turned on as an ESD voltage appears between the VDD and VSS power lines. But, this ESD protection circuit is kept off as the IC is under the power-on condition. To meet these requirements, the *RC* time constant in the VDD-to-VSS ESD clamp circuit is designed in the order of μs to achieve aforementioned operations. A schematic voltage waveform on the node of V_B (in Fig.2) under the ESD-stress condition is shown in Fig.3. The $V_B(t)$ is the voltage on the gate of an NMOS which is used to bypass ESD current. In Fig.3, the turn-on time of the NMOS is as long as 200ns to meet the half-energy discharging time of a HBM (Human-Body Model) ESD event In Fig.4, it shows the voltage waveform of $V_B(t)$ in the time

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domain under the power-on condition for a CMOS IC to be normally operated. In this power-on condition, the $V_B(t)$ should not be greater than Vth (the threshold voltage of NMOS) to keep the ESD-discharging NMOS off. To meet such required operations in Fig.3 and Fig.4, the *HSPICE* can be used to find the suitable device sizes for this VDD-to-VSS ESD clamp circuit.

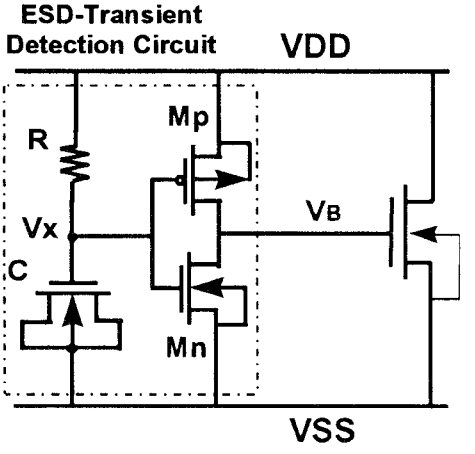


Fig.2 The efficient VDD-to-VSS ESD clamp circuit used to achieve the whole-chip ESD protection.

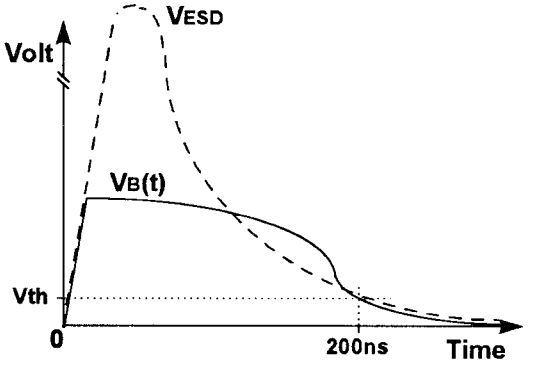


Fig.3 A schematic voltage waveform on the node **VB** in Fig.2 under the ESD-stress conditions.

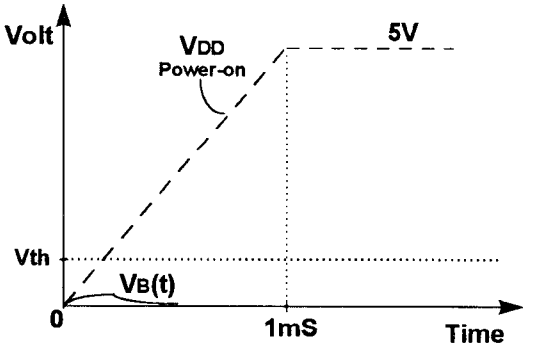


Fig.4 A schematic voltage waveform on the node **VB** in Fig.2 under the VDD power-on condition.

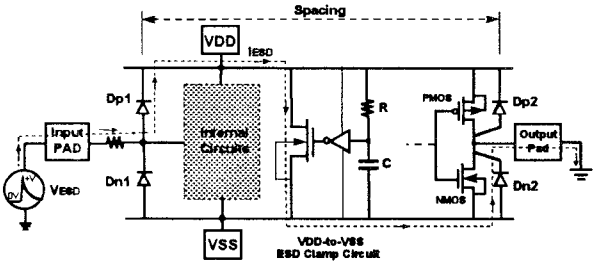


Fig.5 A schematic diagram to show the ESD current path through the VDD-to-VSS ESD clamp circuit under a pin-to-pin ESD-stress condition.

III. PIN-TO-PIN ESD PROTECTION

The operation of pin-to-pin ESD protection with this VDD-to-VSS ESD clamp circuit is shown in Fig.5. In Fig.5, a positive ESD voltage is stressed on an input pin with a grounded output pin while the VDD and VSS pins are floating. The positive ESD voltage will be first diverted to the floating VDD power line through the forward-biased diode Dp1. The floating VSS power line is also biased at a voltage close to the ground through the drain-to-substrate diode Dn2 in the output NMOS device. So, the ESD-stress voltage from the input pin to the output pin becomes across the VDD and VSS power lines. If such ESD voltage across the power lines can not be effectively bypassed, the internal circuits often drawn with the minimum design rules and minimum spacing are vulnerable to ESD damages. The VDD-to-VSS ESD clamp circuit (in Fig.2) is designed to detect this condition and to turn on the discharging NMOS. As the NMOS is turned on, it provides a short-circuit path between the VDD and VSS power lines. The ESD current can be quickly bypassed through the discharging path as shown by the dashed line in Fig.5. So, the CMOS IC's can be effectively protected by this design without causing the internal ESD damages.

But, the parasitic resistance and capacitance along the VDD and VSS power lines may cause a time delay to bypass the ESD current. As the location spacing between the ESD-stressed input pin and the grounded output pin is far, the length of the VDD and VSS power lines between these two pins is longer. With longer power lines, the time delay to bypass the ESD current due to the parasitic resistance and capacitance along the power lines is increased. This may lead to a degradation on the ESD-protection efficiency [6].

IV. EXPERIMENTAL RESULTS

An experimental test chip has been designed to investigate the ESD-protection efficiency of this

proposed VDD-to-VSS ESD clamp circuit and the spacing effect of the pin location. A schematic diagram of the test chip to investigate the spacing effect on the pin-to-pin ESD protection with this VDD-to-VSS ESD clamp circuit is shown in Fig.6.

The output pads are located at the left-hand part of Fig.6 with different spacings to the VDD-to-VSS ESD clamp circuit. The output PMOS and NMOS devices have the same device dimension (W/L) of 150/1.2 (μm). The input pads are located at the right-hand part of Fig.6 with different spacings to the VDD-to-VSS ESD clamp circuit. The diodes Dp and Dn have the same anode perimeter of 120 μm, and the spacing between the anode and cathode of the diodes is 2.4 μm. The device dimension (W/L) of the discharging NMOS used in the VDD-to-VSS ESD clamp circuit is 250/1.4 (μm). The resistor R is about 100 KΩ and the capacitor C is about 2 pF in the VDD-to-VSS ESD clamp circuit. The metal width of both the VDD and VSS power lines is selected as 30 μm to investigate the spacing effect (due to the parasitic resistance and capacitance along the power lines) on the pin-to-pin ESD protection.

This test chip has been fabricated in a 0.8-μm CMOS technology with LDD process. The HBM (Human-Body Model) ESD testing results are illustrated in Fig.7(a) and Fig.7(b) to show the spacing effect on the pin-to-pin ESD-protection efficiency. The pin-to-pin ESD protection performance is decreased as the spacing between the ESD-stressed input pin and the grounded output pin is increased. To provide a 3-KV ESD reliability for a CMOS IC with the power line width of 30 μm and the ESD-protection device dimensions as shown in Fig.6, the VDD-to-VSS ESD clamp circuit have to be repeated between the VDD and VSS power lines in every spacing of 3000 μm. The larger device dimension of the discharging NMOS and the wider metal width of the VDD and VSS power lines will lead to higher pin-to-pin ESD protection.

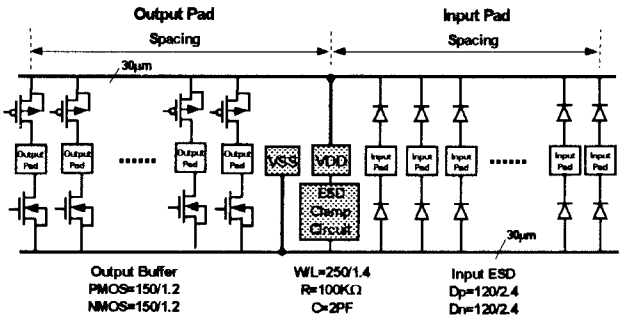
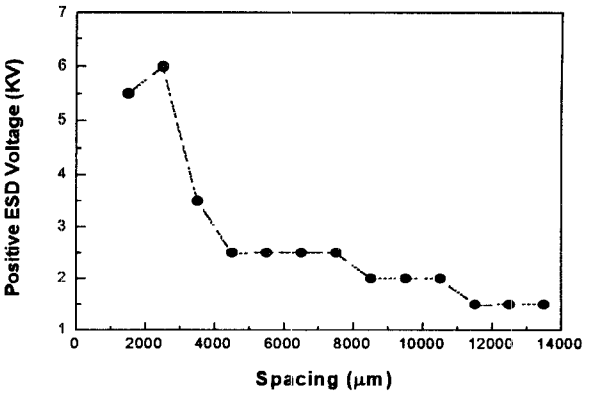
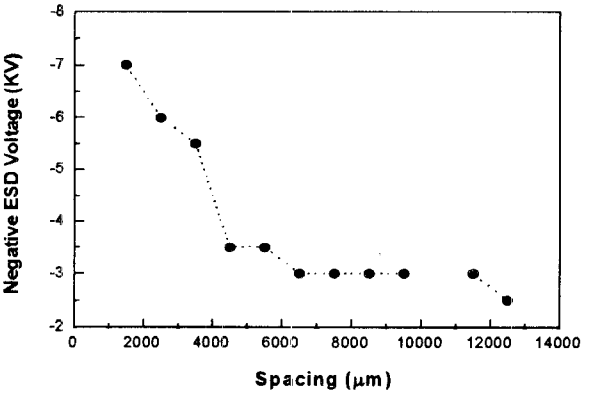


Fig.6 A schematic diagram to show the spacing effect between the input and output pins on the ESD performance of a chip due to the parasitic resistance and capacitance along the VDD and VSS power lines.



(a)



(b)

Fig.7 Experimental results of pin-to-pin ESD reliability with relation to the spacing from an ESD-stressed input pin to another relatively grounded output pin. (a) A positive ESD voltage; (b) a negative ESD voltage; is applied to an input pin while another output pin is grounded, but other pins including the VDD and VSS pins are all floating.

V. APPLICATION

A practical design of whole-chip ESD protection with this proposed ESD clamp circuit is illustrated in Fig.8 to provide a real pin-to-pin ESD protection for an IC without the unexpected ESD damage on the internal circuits under any ESD-stress condition.

This whole-chip ESD protection design has been implemented into a 0.8-μm CMOS product to improve the ESD reliability of the product. In the original ESD design of this product, two gated-NMOS's [8] (W/L=250/2 for each NMOS)) are used as the VDD-to-VSS ESD clamp devices in the chip, but the pin-to-pin ESD level of this IC is only about 0.5 ~ 1 KV in the HBM ESD testing. By using this new design as shown in Fig.9 without increasing the total chip size, the pin-to-pin ESD level is improved up to above 3KV, which is much greater than the commercial specification of 2KV. This pin-to-pin ESD level is guaranteed by full

function testing after the IC is tested under every ESD-stress condition including the conditions of Fig.1. So, the internal circuits of an IC can be fully protected against ESD damage by this proposed whole-chip ESD protection design.

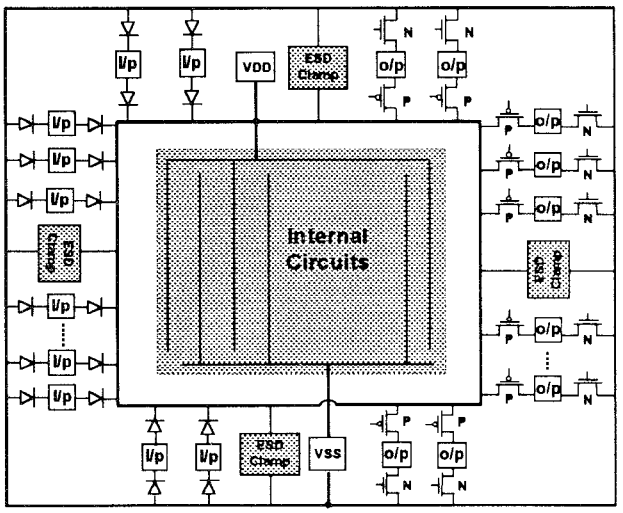


Fig.8 A schematic diagram to show the concept of whole-chip ESD protection with four efficient ESD clamp circuits arranged between the VDD and VSS power lines in an CMOS chip.

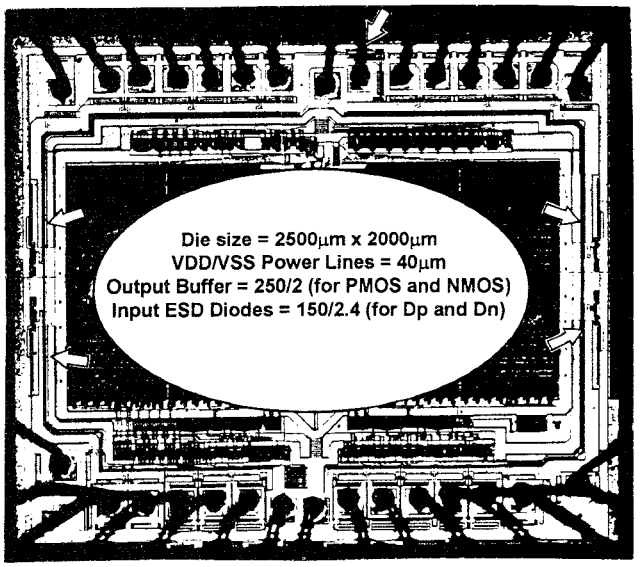


Fig.9 A microphotograph of a 0.8-μm CMOS product using the proposed whole-chip ESD protection design to achieve a real pin-to-pin ESD protection of above 3KV in HBM ESD testing. The added five VDD-to-VSS ESD clamp circuits are indicated by the arrows.

VI. CONCLUSION

A design concept of chip-level ESD protection has been exposed with the experimental verification. An efficient whole-chip ESD protection design has been successfully verified within the submicron CMOS IC products to provide the real pin-to-pin ESD protection. This design concept can be expanded to the CMOS IC's with multiple VDD or VSS power pins.

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