Whole-Chip ESD Protection Scheme for CMOS Mixed-Mode IC's in Deep-Submicron CMOS Technology

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Abstract

A whole-chip ESD protection scheme with the ESD-connection diodes and a substrate-triggering field-oxide device (STFOD) are proposed to protect mixed-mode CMOS IC's against ESD damage. The STFOD is triggered on by the substrate-triggering technique to make an area-efficient VDD-to-VSS ESD clamp circuit. The ESD-connection diodes provide the current discharging paths among the multiple separated power lines to avoid the ESD damage located at the digital-analog interface. This whole-chip ESD protection scheme has been practically verified in an 8-bits DAC chip in a 0.6-μm CMOS process with a pin-to-pin ESD robustness of above 4KV.

Introduction

Whole-chip ESD (Electrostatic Discharge) protection becomes a challenging and emergent task on the reliability of IC products in the deep-submicron CMOS technology, because the internal circuits of CMOS IC's with the scaled-down device sizes and layout spacings are more vulnerable to ESD damage. Even if there are suitable ESD protection circuits around the input and output pads, the internal circuits are still damaged by the ESD voltage [1]-[5].

Actually, the ESD current may enter into any pin and go out from another pin of an IC. Fig.1 shows a pin-to-pin ESD stress condition, where a positive ESD voltage is applied to an input pin while another output pin is relatively grounded but the VDD and VSS pins are floating. Such pin-to-pin ESD stress may cause the ESD voltage to be across the VDD and VSS power lines. Because the VDD and VSS power lines are often distributed everywhere in a chip, the ESD voltage across the VDD and VSS power lines is diverted into the internal parts of an IC and easily causes serious ESD damages on the internal circuits.

Besides, the ESD voltage may directly occur on the VDD pin with the VSS pin grounded [6]. In this direct stress condition, the internal circuits are much vulnerable to ESD damage if there is no effective ESD protection circuit between the VDD and VSS power lines. Especially, the mixed-mode IC's often have multiple separated VDD and VSS power pins. The internal circuits of such mixed-mode IC's with the separated power pins are also vulnerable to ESD damages. An unexpected ESD damage due to VDD-to-VSS ESD stress had been found to locate at the digital and analog interface [7]. The ESD current discharging paths in the mixed-mode IC is illustrated in Fig.2, where a positive ESD voltage is directly applied to the digital VDD with the digital VSS grounded, but the analog VDDA and VSSA are floating. Although there are two gate-grounded NMOS's used to clamp the ESD voltage across the digital and analog power lines, a 2-KV HBM ESD voltage still causes a gate-oxide damage on the digital-analog interface. Thus, suitable whole-chip ESD protection design should be added into the mixed-mode IC's.

In this paper, a whole-chip ESD protection scheme is proposed to fully protect the mixed-mode IC's against the unexpected internal ESD damages by using the area-efficient STFOD and the ESD-connection diodes.

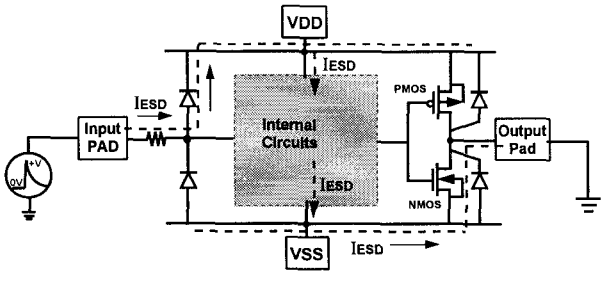

Fig.1 Internal ESD damage due to pin-to-pin ESD stress.

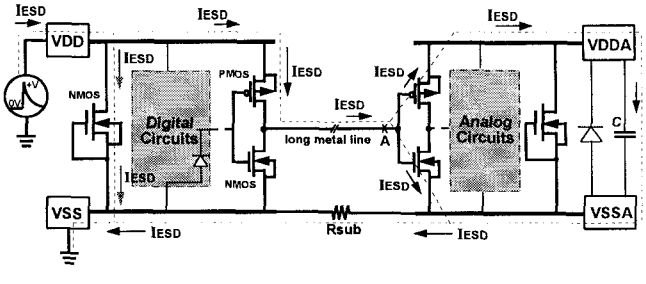

Fig. 2 ESD current discharging paths in a mixed-mode IC with separated analog and digital power pins.

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Whole-Chip ESD Protection Scheme

A. Whole-Chip ESD Protection

The proposed whole-chip ESD protection scheme for a mixed-mode IC with the VDD-to-VSS ESD clamp circuits and ESD-connection diodes is shown in Fig.3. The ESD clamp circuits are designed to be turned on only under the ESD-stress conditions, but they are kept off as the IC is under the normal operating conditions and the power-on condition. The ESD-connection diodes (D1, D2, D3, and D4) provide the discharging paths between the digital and analog power lines to avoid the ESD stress on the digital-analog interface. As an ESD voltage occurs on a pin with any a pin relatively grounded (not limited to the power pins), the ESD current can be bypassed through the ESD-connection diodes and the area-efficient ESD clamp circuits to limit the ESD voltage across the VDD1 (or VDD2) and VSS1 (or VSS2) power lines. So, the ESD voltage across the VDD and VSS power lines can be effectively clamped without causing any ESD damage on the internal circuits.

For example, the ESD current discharging paths in a mixed-mode IC with the whole-chip ESD protection scheme are shown in Fig.4, while a positive ESD voltage is applied to the digital VDD with only the digital VSS grounded. With suitable connection for ESD current discharging paths and efficient ESD clamp circuits, the internal circuits and the digital-analog interface can be free to ESD damage.

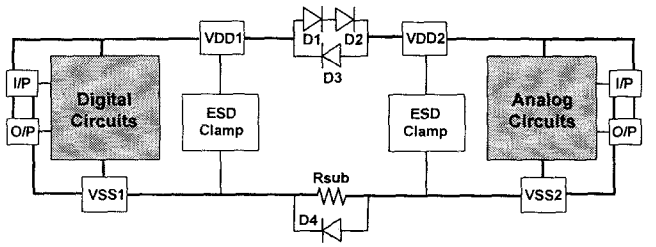

Fig.3 Whole-chip ESD protection scheme for a mixed-mode IC with area-efficient ESD clamp circuits and ESD-connection diodes.

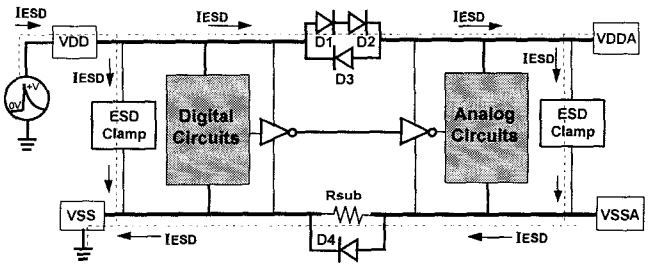

Fig.4 The ESD current discharging paths in a mixed-mode IC with the whole-chip ESD protection scheme, while a positive ESD voltage is applied to the digital VDD with only the digital VSS grounded.

B. VDD-to-VSS ESD Clamp Circuit

The area-efficient VDD-to-VSS ESD clamp circuit, shown in Fig.5, is achieved by using a substrate-triggering field-oxide device (STFOD) to much save layout area. The *RC* time constant in Fig.5 is designed in the range of 0.1~1 μS. With such R and C, the ESD-transient detection circuit can detect the ESD voltage across the VDD and VSS power lines. The Mp device is designed to be turned on by the ESD voltage and sends a high voltage to the substrate of the STFOD. As the voltage on the node V_B is greater than 0.6V, the lateral bipolar action in the STFOD is triggered on. Thus, the ESD voltage across the VDD and VSS power lines is quickly discharged through the turned-on STFOD. The schematic voltage waveform of V_B under the ESD-stress condition is shown in Fig.6(a). The turned-on STFOD, which provides a near short-circuit path between the VDD and VSS power lines, can clamp the ESD voltage to a very low voltage level. So, the internal circuits can be effectively protected without any ESD damage.

Under the normal power-on condition of the IC, the VDD power-on voltage waveform has a rise time in the order of mini-second (ms). With such a rise time of ms, the ESD-transient detection circuit with the *RC* time constant of 0.1~1 μs keeps the V_B node with a voltage level of 0V. The schematic voltage waveform of V_B under the VDD power-on transition is shown in Fig.6(b). So, the STFOD is guaranteed to be kept off, as the IC is under the power-on condition and the normal operating conditions.

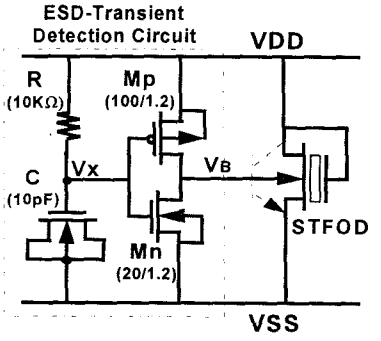

Fig.5 The area-efficient VDD-to-VSS ESD clamp circuit by using a substrate-triggering field-oxide device (STFOD).

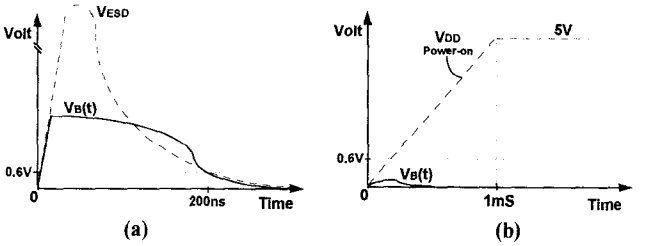

Fig.6 A schematic voltage waveform on the node V_B of Fig.5 under (a) the ESD-stress condition; (b) the VDD power-on condition.

C. Design of the STFOD

The STFOD is triggered on by a substrate-triggering technique to significantly improve its ESD robustness in per unit layout area. The STFOD device structure is illustrated

in Fig.7, where a P+ connected to V_B of Fig.5 is inserted in the center to provide the substrate-triggering current to this STFOD. An N-well in the source region surrounding the whole STFOD is used to enhance its lateral bipolar action. With the forward-biased V_B voltage under ESD-stress condition, the STFOD can sustain much higher ESD voltage within a smaller layout area as comparing to the NMOS devices in deep-submicron CMOS technologies.

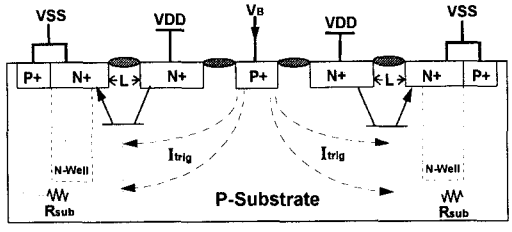

Fig.7 The device structure of the substrate-triggering field-oxide device (STFOD) to improve its lateral bipolar action.

Experimental Results

An experimental test chip has been fabricated to verify the ESD-protection efficiency of the ESD clamp circuit. A microphotograph of the fabricated ESD clamp circuit in a 0.6-μm CMOS process is shown in Fig.8. The previous design by using the NMOS device [8] is also made in the same test chip as a reference.

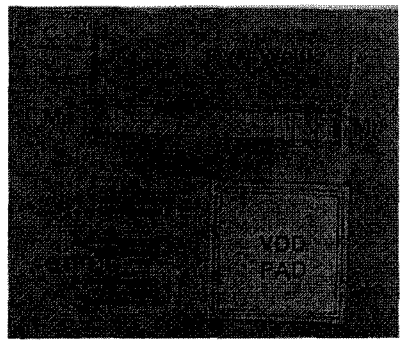

Fig.8 A microphotograph of the fabricated ESD clamp circuit in a 0.6-μm CMOS process.

Table I

	This Work	Previous work
ESD Protection Device (W/L, μm)	STFOD (439.2/1.2)	NMOS (500/0.8)
Device Layout Area (μm^2)	102.9 × 78.8	93.6 × 74.05
HBM ESD Pass Level (V)	4500	1000
ESD Level in per unit Layout Area ($V/\mu m^2$)	0.55	0.14

A. ESD Testing

The *KeyTek* ZapMaster (one of the industrial ESD testers) is used to evaluate the ESD robustness with a failure criterion of 1-μA current leakage under a 5-V VDD bias. The testing results between the ESD clamp circuit with the STFOD and the previous design with the NMOS [8] in the HBM (Human-Body Model) ESD events are summarized in Table I. It is clearly shown that this new design with the STFOD can provide about 4-times higher ESD robustness in per unit layout area than the previous design with the NMOS.

B. VDD-Transient Testing

The operation of this ESD clamp circuit is verified by applying an 8-V voltage pulse with a rise time of 5.5nS, or a 5-V power-on ramp voltage with a rise time of 0.1mS, to the VDD with VSS grounded. The voltage waveforms on the VDD are observed in Figs.9(a) and 9(b) to verify the selective action of the ESD clamp circuit.

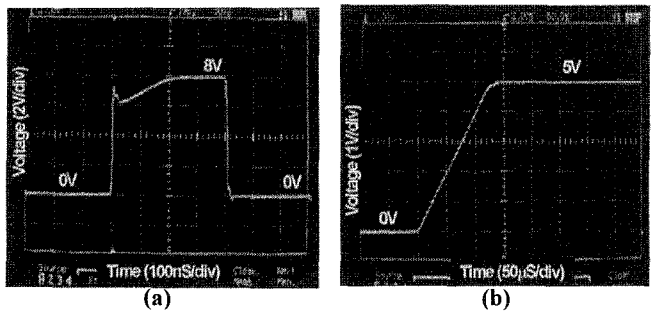

Fig.9 (a) The degraded waveform due to the turn-on of STFOD in the ESD clamp circuit, as a 8-V voltage pulse is applied to VDD with a rise time of 5.5nS; (b) The power-on VDD waveform (5-V ramp voltage with a rise time of 0.1mS) has no degradation because the STFOD is kept off in this power-on condition.

C. Bipolar Action of the STFOD

The bipolar characteristics of the fabricated STFOD is shown in Fig.10, where different base currents are applied into the substrate of the STFOD and the collector current is measured. The beta current gain of the STFOD is calculated and shown in Fig.11. The STFOD has a maximum beta gain of about 2.7, but this gain is still maintained as the collector current is in the high-current range. This leads to an improvement of ESD robustness of the STFOD.

The ESD improvement of the STFOD can be verified by the relations between the It2 (second-breakdown current) and the forward-biased substrate voltage. The relations of It2 measured by TLPG (Transmission-Line Pulse Generator) versus the different substrate biases of a field-oxide device are shown in Fig.12, where the It2 (of per unit channel width) can be significantly improved by the forward-biased substrate voltage. The It2 of an NMOS with a 0-V substrate bias is also shown in Fig.12. The field-oxide device with a 0.8-V substrate bias can provide a four-times higher It2 than the NMOS device. So, this STFOD can provide much higher ESD robustness within a smaller layout area, as well as this STFOD is free to the issue of VDD-to-VSS latchup in the

SCR devices [9]. In [9], the SCR device was used as the ESD-clamping device between VDD and VSS, but such SCR may cause the VDD-to-VSS latchup in the normal operating conditions due to the unexpected voltage spikes on the power lines (such as the board-level arcing test or the power-line surging test).

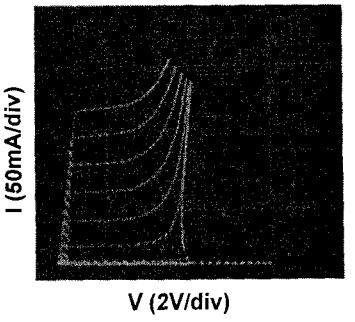

Fig.10 The lateral bipolar characteristics of the STFOD.

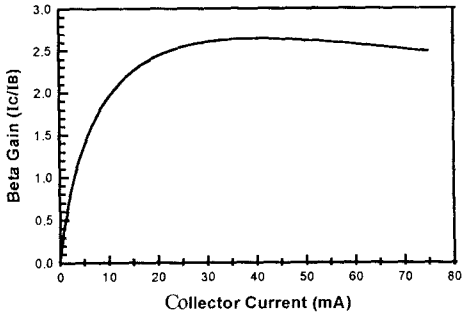

Fig.11 The beta gain of the lateral bipolar action in the STFOD.

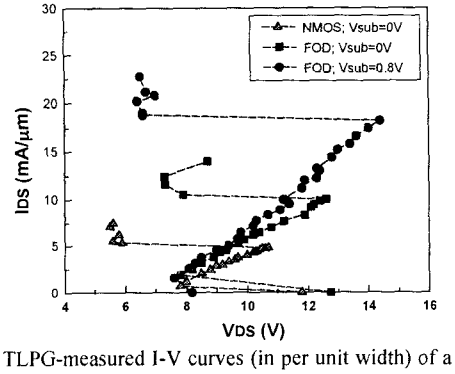

Fig.12 The TLPG-measured I-V curves (in per unit width) of a field-oxide device under different substrate biases and an NMOS device with 0-V substrate bias in the same CMOS process.

D. Practical Application

The proposed whole-chip ESD protection scheme with the STFOD in the ESD clamp circuit has been practically implemented in some mixed-mode IC's to provide a real whole-chip ESD protection. A typical example is shown in Fig.13, where an 8-bits DAC (Digital-to-Analog Converter) chip has two ESD clamp circuits between the analog and digital power lines. The diodes D1, D2 , D3, and D4 in Figs.3 and 13 provide a bi-directional discharging paths to bypass ESD current, as the ESD voltage occurs on a digital pin (or an analog pin) but with an analog pin (or a digital pin) grounded. By using the proposed whole-chip ESD protection scheme with the area-efficient ESD clamp circuit, this 8-bits DAC can pass the HBM ESD stress of above 4KV in any pin-to-pin ESD-testing conditions. This pin-to-pin ESD protection is guaranteed without any internal ESD damage by a full function testing after the IC is subjected to the ESD stresses.

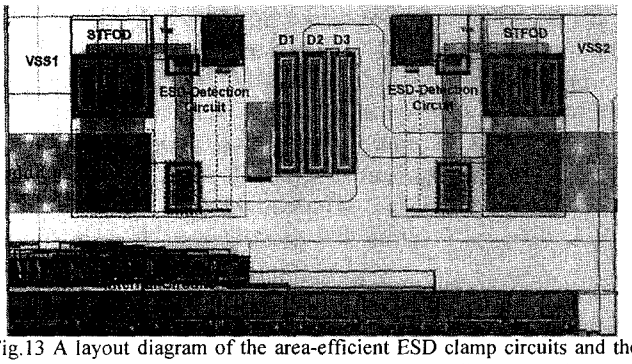

Fig.13 A layout diagram of the area-efficient ESD clamp circuits and the connection diodes in an 8-bits DAC chip, corresponding to the design in Fig.3.

Conclusion

An area-efficient whole-chip ESD protection design has been successfully verified in a mixed-mode CMOS IC to provide the real pin-to-pin ESD protection. By using the substrate-triggering technique, the STFOD can provide four-times higher ESD robustness in per unit layout area as comparing to the previous works with the NMOS device. This whole-chip ESD protection scheme can be expanded to the CMOS IC's with multiple VDD and VSS power pins.

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