Advanced Layout Design for Deep-Submicron CMOS Output Buffer with Higher Driving Capability and Better ESD Reliability

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Abstract

Three new device structures to effectively reduce the layout area of CMOS output buffers with higher driving capability and better ESD reliability are proposed. With theoretical calculation and experimental verification, both the higher output driving/sinking capability and the stronger ESD robustness of CMOS output buffers can be practically achieved by the new proposed layout designs within smaller layout area. The output devices assembled by a plurality of the proposed basic layout cells have a lower ploy-gate resistance and a smaller drain capacitance than that by the traditional finger-type layout.

Introduction

In deep-submicron low-voltage CMOS technology, VDD had been scaled down to save power consumption and to provide better device reliability. To offer enough output driving/sinking currents as well as to provide stronger ESD reliability, the W/L ratios of output transistors are often enlarged up to several hundreds. But in high-integration applications, especially in the high-pin-count and pad-limited CMOS VLSI, the layout area available for each output pad with output buffer including latchup guard rings is seriously limited. So, an area-efficient output buffer with high driving capability and high ESD robustness is much requested by deep-submicron low-voltage CMOS IC's.

To save the layout area of output buffers, the output transistors are traditionally drawn in the finger-type structure as that illustrated in Fig.1. The cross-sectional view along the line A--A' in Fig.1 is shown in Fig.2, which is demonstrated in an n-well/p-substrate CMOS process. In Fig.1, a large-dimension NMOS device is separated as four parallel small-dimension NMOS devices. The spacing from the drain contact to the poly-gate edge is marked as "d". The spacing from the source contact to the poly-gate edge is marked as "S". Recently, it had been found that the spacing from the drain contact to the poly-gate edge is an important layout parameter to affect the ESD reliability of output devices [1]. For better ESD robustness of CMOS output buffers, this spacing d has been found to be about 5~6 μm. But, the "S" spacing has no important effect on the ESD reliability of CMOS output buffers. The spacing S is often used as 1 μm in the practical layout. Outside the source region, there are two latchup guard rings surrounding the whole NMOS device. But this spacing d only has ESD improvement in the non-silicided processes. In the advanced CMOS process with silicided diffusion, a modified drain structure for output NMOS, shown in Fig.3, can be used to improve ESD reliability without modifying the process steps or adding the extra silicided-block mask. This modified drain structure also increases the spacing d. Due to the ESD consideration with a larger spacing d, the layout area of a finger-type output transistor is significantly increased.

Besides, in the finger-type output transistors, the ESD damage has been found to easily locate on the finger's end of a drain finger as that shown in Fig.4. This unexpected ESD damage due to the peak-discharging effect of ESD current on the parasitic diode, shown in Fig.5, often causes a very weak ESD reliability.

In this paper, three new device structures (square [2], hexagon [3], and octagon [4]) are proposed to realize the CMOS output transistors within smaller layout area but with higher driving capability and better ESD robustness.

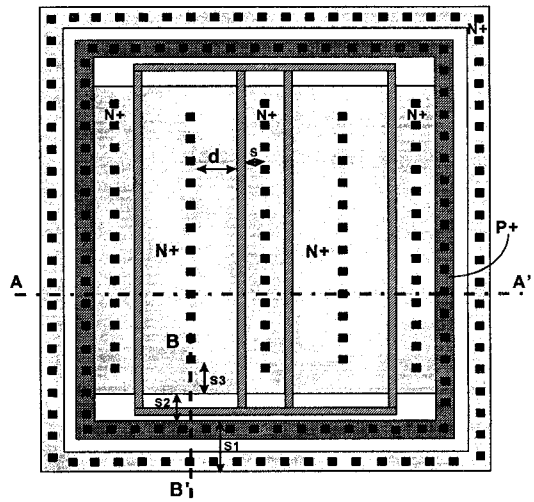


Fig.1 The traditional finger-type output NMOS device.

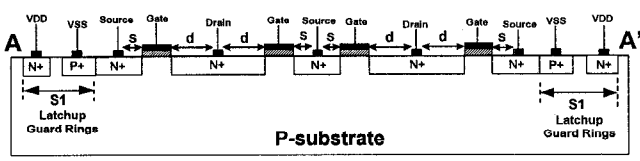


Fig.2 The cross-sectional view of the NMOS device along the line A--A' in Fig.1.

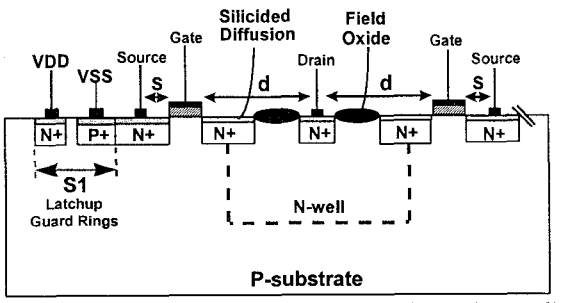


Fig.3 A cross-sectional view of an NMOS device with a modified N-well drain structure in a CMOS process with silicided diffusion.

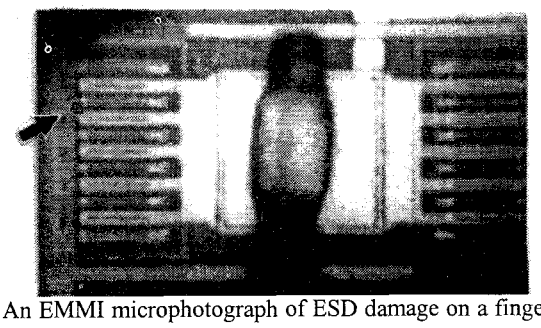


Fig.4 An EMMI microphotograph of ESD damage on a finger-type CMOS output buffer after a PS-mode ESD stress. Only a hot spot is observed at the end of a drain finger, which is indicated by an arrow.

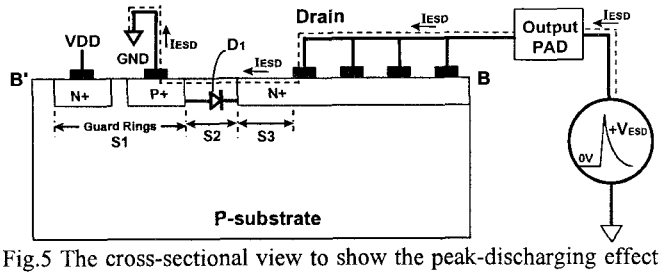


Fig.5 The cross-sectional view to show the peak-discharging effect on the parasitic diode along the line B--B' in Fig.1.

Advanced Layout Designs

A. Square-Type Layout

To reduce the layout area and to overcome the parasitic diode D1 in the traditional finger-type layout of CMOS output transistors, a multiple-cell square-type layout design for the output NMOS is shown in Fig.6. The schematic cross-sectional view along the line A--A' in Fig.6 is also the same as that shown in Fig.2. In Fig.6, there are four small-dimension square cells to form a large-dimension NMOS device. Each small-dimension square cell is identical to each other. The black square region in the center of a square cell is the drain contact of the NMOS device. The poly gate in each square cell is also drawn in a square ring. The N+ diffusion of the source is also drawn in a square shape and surrounds the gate and drain regions. The contacts at the source region are placing in a square-shape arrangement. Outside the NMOS device, there is a P+ diffusion connected to ground to offer the substrate bias. This P+ diffusion surrounds the whole NMOS device. Besides, there is an N+ diffusion surrounding this P+ diffusion. This N+ diffusion connected to VDD works as a latchup guard ring. All the layout elements in a square cell, including the placement of contacts, have to be made as symmetrical as possible to ensure uniform current flow in the NMOS device so as to increase its ESD reliability. An NMOS device with a larger dimension can be assembled by a plurality of the square cells.

To verify area efficiency, the total layout area between the finger-type layout and the square-type layout has been calculated. The total layout area includes the same double latchup guard rings in both the finger-type and the square-type layout. In the square-type layout, the edge "C" of drain contact is 2μm. With a device dimension (W/L) of 432/0.8 (μm/μm) and the spacing d (S) of 5 (1) μm, the total layout area in the finger-type layout is 6982 μm^2, but that in the square-type layout is only 4789 μm^2. This shows the excellent area-saving efficiency of the square-type layout about 30% reduction, as comparing to the finger-type layout. Fig.7 shows the relations between the channel width (W) and the percentage of square-type to finger-type area ratio under different d spacings. It is clearly shown that the layout area can be significantly reduced by the square-type layout, while the spacing d is large.

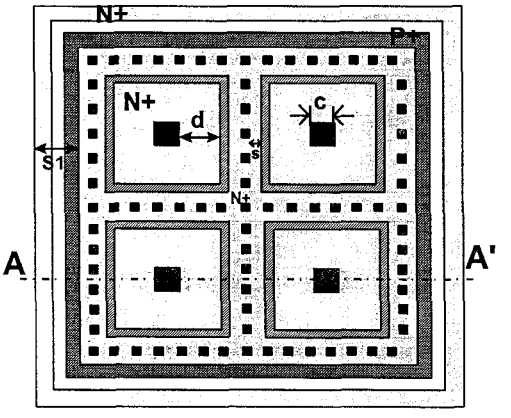


Fig.6 The schematic diagram of the proposed square-type layout.

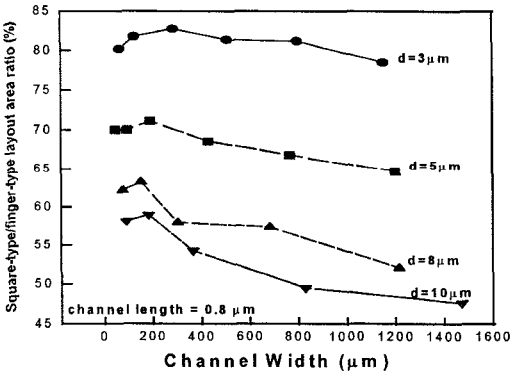


Fig.7 The relations between the percentage of the square-to-finger layout area ratio and the device channel width under different layout parameters of d.

B. Hexagon-Type Layout

The schematic diagram of the multiple-cell hexagon-type layout of an output NMOS is shown in Fig.8. The schematic cross-sectional view along the line A--A' in Fig.8 is also the same as that shown in Fig.2. In Fig.8, there are four small-dimension hexagon cells to form a large-dimension NMOS device. Each small-dimension hexagon cell is identical to each other. The poly gate in each hexagon cell is also drawn in a hexagon ring. The N+ diffusion of the source is also drawn in the hexagonal shape and surrounds the gate and drain regions. The contacts at the source region are also placing in a hexagon-shape arrangement. All the layout elements in the hexagon cell, including the placement of contacts, have to be made as symmetrical as possible to ensure uniform current flow in the NMOS device so as to increase its ESD reliability. An NMOS device with a larger dimension can be assembled by this way. The number of hexagon cells can be designed for different device dimensions.

To verify area efficiency, comparisons of total layout area between the traditional finger-type layout and the hexagon-type layout have been investigated. In the hexagon-type layout, the diameter "C" of drain contact is 2 μm. In the traditional finger-type layout, the "S2" spacing is 4 μm. The length of each poly finger in the traditional finger-type layout is equal to each other, but this poly-finger length is limited below 50μm in most CMOS design rules for better ESD reliability. Fig.9 shows the relations between device channel width (W) and the percentage of the hexagon-type to finger-type area ratio under different d spacings. The hexagon-type layout provides an area reduction about 25% to the total layout area of the finger-type layout, while the spacing d is 5 μm. If the spacing d is required to become larger, the hexagon-type layout can significantly reduce the total layout area.

C. Octagon-Type Layout

An output NMOS device assembled by four basic octagonal cells is shown in Fig.10, where the black octagonal region in the center of a cell is the drain contact for the NMOS device. The poly gate, N+ diffusion of the source, and the placement of source contacts in the octagonal cell are also drawn or arranged in an octagonal shape. Outside the NMOS device, there is a P+ diffusion connected to VSS to offer the p-substrate bias for normal operations. All the layout in an octagonal cell is made as symmetrical as possible to ensure uniform ESD current flow in the NMOS device so as to increase its ESD robustness. An NMOS device with a larger dimension can be assembled by a plurality of the basic octagonal cells.

The layout-area ratios (octagon-type/finger-type) under different d spacings are shown in Fig.11. As the NMOS device dimension of 800/0.8, the total layout area in the traditional finger-type layout is 10842 μm^2, but that in the octagon-type layout is only 8687 μm^2. With the spacing d of 5 μm, the total layout area of an octagon-type device is only 80% of that of a finger-type device with the same device dimension. The layout area can be significantly reduced by this octagon-type device structure, while the spacing "d" is large.

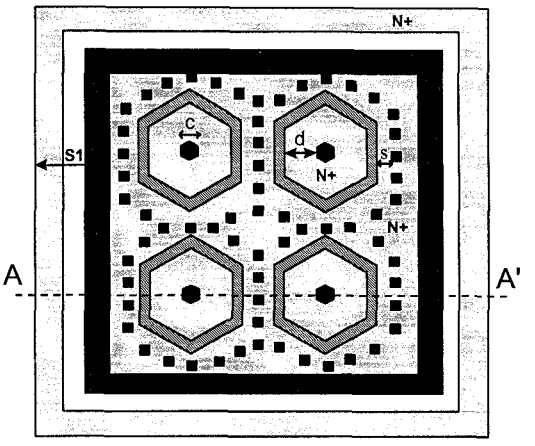


Fig.8 The schematic diagram of the proposed hexagon-type layout.

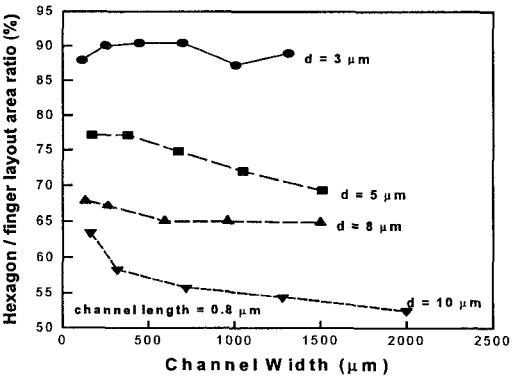


Fig.9 The relations between the percentage of the hexagon-to-finger layout area ratio and the device channel width under different layout parameters of d.

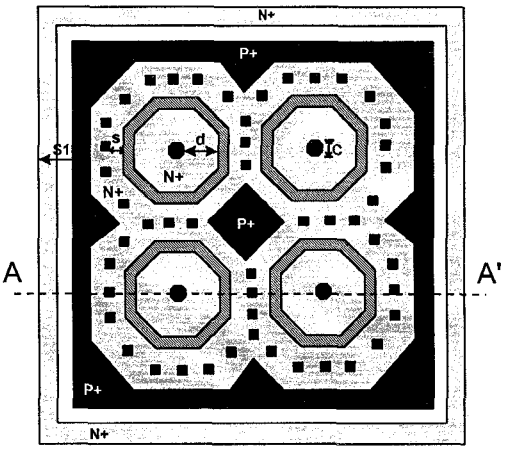


Fig.10 The schematic diagram of the proposed octagonal cell.

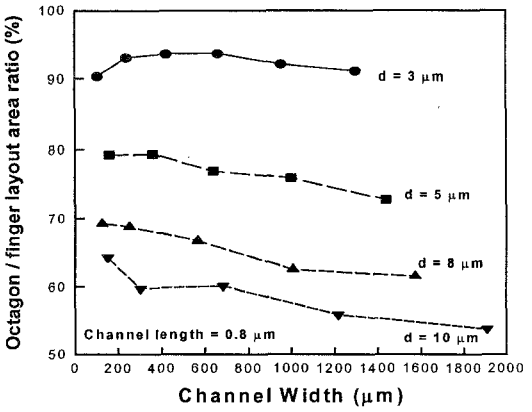


Fig.11 The dependence of the area ratios (octagon-type vs. finger-type) on the device channel width under different d spacings.

D. Area Efficiency and Drain Capacitance

With this proposed layout technique, there is no "S2" spacing in the square-type, hexagon-type, and octagon-type layouts. The layout area due to the spacing "S2" in the traditional finger-type layout can be saved. Moreover, no parasitic diode D1 is directly close to the edge of the drain region. The peak-discharging effect on the end of the drain fingers can be avoided, therefore the ESD robustness of output transistors can be sustained without any degradation. This proposed layout technique can be also used to realize the output PMOS transistors.

The comparison on the layout area of output NMOS transistors with different channel widths, realized by the four kinds of layout styles, is shown in Fig.12. The spacing d and the channel length in Fig.12 are kept as 5 μm and 0.8 μm, respectively. It has obviously shown that the NMOS (or PMOS) transistor realized by the square-type layout can save more layout area than those by the other layout styles.

Moreover, the drain-to-bulk parasitic capacitance at the output node is also reduced by the proposed layout technique. Because the total layout area of the output transistor is reduced by these proposed layout styles, the layout area and perimeter of the drain region in the new layout styles are also reduced. Under the same spacing d of 5μm and the same device dimension, the drain parasitic capacitance of an output NMOS in the square-type (hexagon-type or octagon-type) layout is only about 65% (62%) of that in the finger-type layout. With a lower drain capacitance, this new proposed layout technique is more suitable to realize the CMOS output buffers for high-speed or high-frequency applications.

Experimental Results

The proposed layout designs have been verified in a 0.6-μm CMOS process. The microphotographs of the fabricated CMOS output buffers in the square-type, the hexagon-type, and the octagon-type layout are shown in Fig.13.

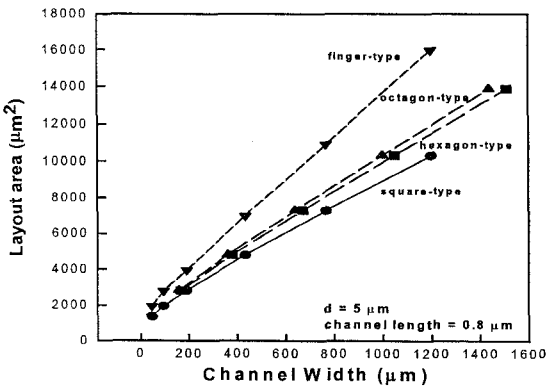


Fig.12 Comparison of layout area among the four different layout styles with the spacing d of 5 μm.

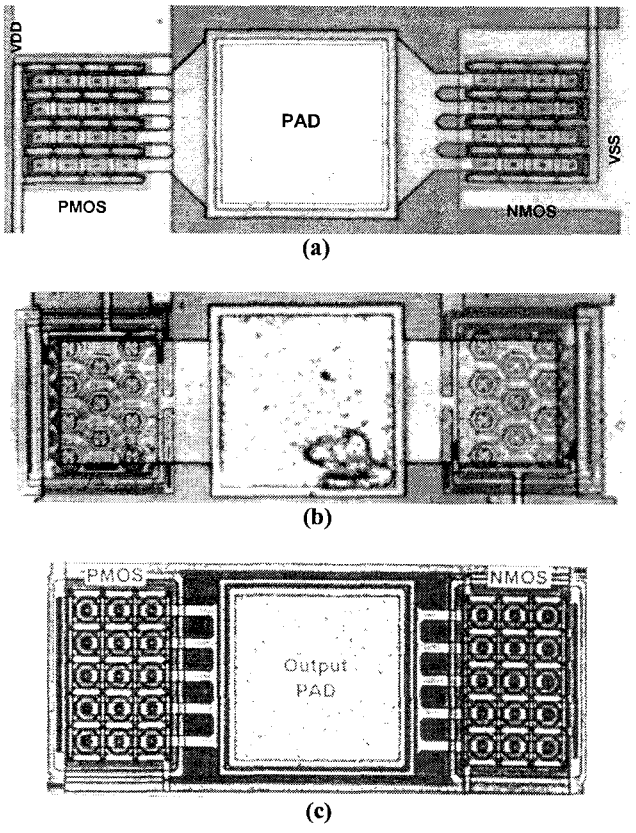


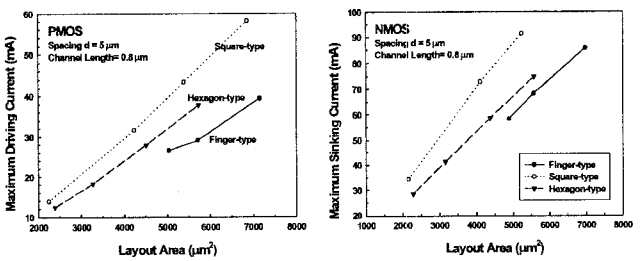
Fig.13 The microphotographs of the fabricated CMOS output buffers in (a) the square-type, (b) the hexagon-type, and (c) the octagon-type, layout styles.

A. Output Driving/Sinking Ability

The current driving/sinking capability of a CMOS output buffer can be investigated by the measured I-V curves of NMOS and PMOS devices in the output buffer. The drain currents of the output NMOS (PMOS) transistors are measured under the bias conditions of Vds=3V and Vgs=3V (Vds=-3V and Vgs=-3V) with their sources grounded. The measured sinking/driving currents of the fabricated output buffers in the square-type and hexagon-type layouts versus

the total layout area, as comparing to the finger-type layout, are shown in Fig.14. The maximum driving (sinking) capability of CMOS output buffers in the square-type layout is improved about 50% (40%) more than that in the finger-type layout under the same layout area. The maximum driving (sinking) capability of CMOS output buffers in the hexagon-type layout is improved about 15% (10%) more than that in the finger-type layout in per unit layout area.

The output driving/sinking capability of the octagon-type layout is summarized in Table I to verify the area efficiency. The maximum output sinking (driving) current in per unit layout area of the octagon-type output NMOS (PMOS) device is 13.12 (6.59) $\mu A/\mu m^2$, but that in the finger-type device is only 9.77 (4.46) $\mu A/\mu m^2$. So, the octagon-type NMOS (PMOS) device provides an increase of 34.3% (47.7%) on the output sinking (driving) current in per unit layout area, as comparing to the finger-type devices.



(a) (b)

Fig.14 Experimental results of the maximum (a) driving current, (b) sinking current, of the CMOS output buffers in the finger-type, square-type, and hexagon-type layouts with a 3-V power supply.

Table I

	Finger-type	Octagon-type
W/L (μm/μm)	720/0.8	804/0.8
Layout Area (μm^2)	112×110	110×74
NMOS **Ids** (Vds=Vgs=3V)	120.4 mA	106.8 mA
PMOS **Ids** (Vds=Vgs= -3V)	-54.95 mA	-53.69 mA
NMOS **Ids** in per unit Layout Area	9.77 $\mu A/\mu m^2$	13.12 $\mu A/\mu m^2$
PMOS **Ids** in per unit Layout Area	-4.66 $\mu A/\mu m^2$	-6.59 $\mu A/\mu m^2$

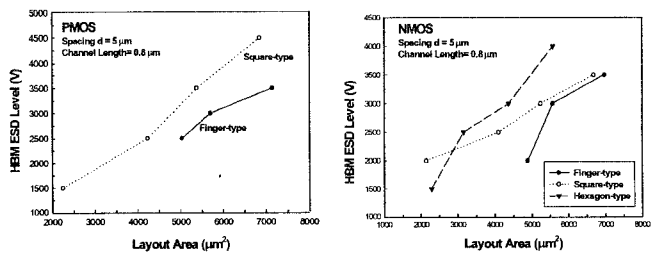
Table II

	Finger-type	Octagon-type
W/L (μm/μm)	720/0.8	804/0.8
Layout Area (μm^2)	112×110	110×74
HBM ESD pass voltage	6500 V	6000 V
MM ESD pass voltage	800 V	950 V
CDM ESD pass voltage	> ±2000 V	> ±2000 V
HBM pass voltage in per unit Layout Area	0.53 $V/\mu m^2$	0.74 $V/\mu m^2$
MM pass voltage in per unit Layout Area	0.065 $V/\mu m^2$	0.12 $V/\mu m^2$

B. Output ESD Robustness

The HBM (Human Body Model) ESD levels of the output PMOS and NMOS devices in different layout styles are tested and the results are shown in Fig.15. Owing to the more uniform layout design, the ESD levels of the square-type and the hexagon-type layouts in per unit area are confirmed to be greater than that in the finger-type layout.

The ESD test results including the HBM, MM (Machine Model), and CDM (Charged Device Model) ESD tests on the octagon-type and finger-type layout are listed in Table II. There are four modes of ESD stresses on a pin [5]. The ESD pass voltage of a pin is defined as the highest ESD voltage that the pin can sustain without causing any damage. The HBM (MM) ESD robustness in per unit silicon area of the octagon-type output buffer is 0.74 (0.12) $V/\mu m^2$, but that in the finger-type layout is only 0.53 (0.065) $V/\mu m^2$. This octagon-type layout provides an increase of 41.5% (84.6%) in the HBM (MM) ESD robustness of per unit layout area. The CDM ESD robustness in per unit layout area of the octagon-type output buffer can be greater than $0.25V/\mu m^2$.



(a) (b)

Fig.15 Testing results of the HBM ESD-sustaining voltage of the (a) output PMOS, (b) output NMOS, in the finger-type, square-type, and hexagon-type layouts.

Conclusion

With theoretical calculation and experimental verification, the total silicon area of the pad-limited VLSI chip can be significantly reduced to save production cost by these proposed layout designs. These area-efficient layout designs are very suitable to the submicron or deep-submicron low-voltage CMOS IC's in the high-density, high-speed, and high-reliability applications.

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