CMOS On-Chip ESD Protection Design With Substrate-Triggering Technique

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Abstract

To increase the ESD robustness and to reduce the trigger voltage of the ESD protection devices, a substrate-triggering technique is proposed to effectively enhance the ESD-protection efficiency of CMOS on-chip ESD protection circuits in submicron CMOS technologies. With suitable substrate bias, the ESD protection devices can sustain much higher ESD-stress voltage within small layout area. Two practical design examples of the input ESD protection circuit and the VDD-to-VSS ESD clamp circuit are designed by using the substrate-triggering technique to verify the ESD protection efficiency.

1. Introduction

ESD (electrostatic discharge) robustness has become the main reliability issue of submicron and deep-submicron CMOS technologies. To avoid the IC products are damaged by the ESD energy during the packaging and assembling phases, the IC's had been generally required to sustain at least an HBM (human-body model) ESD voltage of 2000V. So, the on-chip ESD protection circuits have to be inserted into the IC's against the ESD damages in the IC's. The ESD current enters into the IC's through the metal pins of the IC's, thus the on-chip ESD protection circuits are often made around the input and output bonding pads of the IC's.

To drive the external heavy load, the output buffers connected to the output pad are often designed with large device dimensions. With the large device dimensions, the output buffers can sustain high ESD stress if suitable layout design or ESD-enhanced processes are used [1]-[4]. But the input pads of CMOS IC's are connected to the input stages, the thinner gate oxide of the input stages in submicron CMOS IC's is very sensitive to ESD stress. To protect the thinner gate oxide of the input stages, the on-chip input ESD protection circuits have to be added into the CMOS IC's to clamp the overstress voltage on the input pads. Besides, the ESD current may enter into the IC's through the VDD or VSS power pins. The effective VDD-to-VSS ESD clamp circuits have to be added into the IC's to avoid the ESD current through the VDD or VSS power lines into the internal circuits of the IC's to cause some unexpected ESD damages in the internal circuits of the IC's [5]-[6].

Because the peak discharging current of the HBM ESD events with an ESD voltage of 2000V is as high as ~1.3A [7], the on-chip ESD protection circuits often have huge device dimensions to sustain such large ESD current. With huge device dimensions, the on-chip ESD protection circuits therefore occupy huge layout area in the CMOS IC's. In this paper, the substrate-triggering effect on ESD robustness of the ESD protection devices are investigated and used to increase ESD robustness of the ESD protection circuits within small layout area.

2. Substrate-Triggering Effect

The HBM ESD failure threshold voltage (V_{ESD}) of the ESD protection circuits had been found to be proportional to the pulsed secondary breakdown current (It2) of the ESD protection devices [8]-[9]. The V_{ESD} can be expressed as

$$V_{ESD} = (1500\Omega + R_{device}) \times It2, \qquad (1)$$

where the 1500Ω is the discharge resistance of the HBM ESD events [7]. The R_{device} is the equivalent resistance of the ESD protection device in the ESD-stress condition. Generally, the R_{device} of ESD protection devices is much smaller than 1500Ω. The It2 of the ESD protection devices can be measured by the TLPG (transmission line pulse generator) with a pulse width about 100ns [9]. From equation (1), the V_{ESD} can be improved if the It2 of the ESD protection devices is increased. An ESD protection device with a larger device dimension generally has a larger It2, but it also occupies a larger layout area in the IC's.

Recently, the ESD characteristics of protection devices had been more studied. It was found that the local substrate bias can increase ESD level of the protection devices [6], [10]. To investigate the substrate-triggering effect, the It2 of a lateral bipolar device in a 0.6-μm CMOS technology is measured by the TLPG under different substrate biases. The measured I-V characteristics of the lateral bipolar device in the snapback breakdown region is shown in Fig.1. When the substrate bias is 0V, the It2 of the lateral

bipolar device is only 1.49A. But, the It2 can be increased up to 3.36A, when the substrate bias is 1.5V. The relationship between the substrate bias and the It2 of the lateral bipolar device is shown in Fig.2. The It2 can be effectively increased by the substrate bias under the same device dimension. This has verified the substrate-triggering effect to increase the ESD robustness of ESD protection devices. By using this substrate-triggering technique, the ESD protection devices can sustain higher ESD voltage without occupying much more layout area.
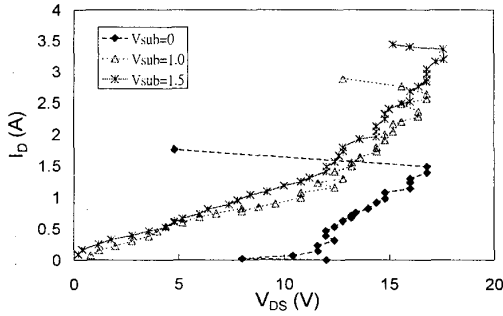
Fig.1 The TLPG-measured I-V characteristics of a lateral bipolar device under different substrate biases.
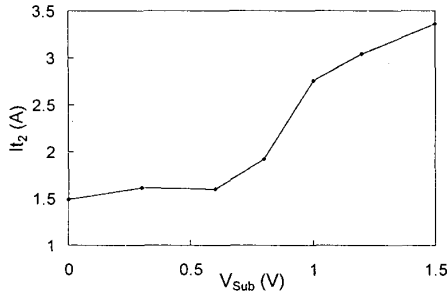

Fig.2 The relationship between the substrate bias and the It2 of a lateral bipolar device in a 0.6-μm CMOS technology.

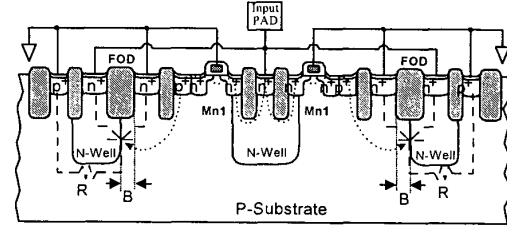## 3. ESD Protection Circuits with the Substrate-Triggering Technique

3.1 Input ESD Protection Circuit

By applying the substrate-triggering technique to improve the ESD-sustained level and to lower its trigger voltage, an input ESD protection circuit is shown in Fig.3. The substrate-triggering input ESD protection circuit is formed by a short-channel NMOS (Mn1), a resistor (R), and a field-oxide device (FOD). The drain of the short-channel NMOS (Mn1) is directly connected to the input pad, and the source of the Mn1 is connected to VSS through the resistor R. The source of the Mn1 is also connected to the substrate of the FOD to trigger on the parasitic lateral bipolar junction transistor (LBJT) in

the FOD. The FOD in Fig.3 is turned on by the LBJT action with a forward-biased base-emitter junction in the FOD. The turn-on voltage of the FOD with a positive substrate bias is lower than its drain breakdown voltage. The Mn1 and resistor R are therefore designed to provide the substrate-triggering current to the FOD during the ESD stresses. This substrate-triggering FOD can sustain higher ESD stress with a lower turn-on voltage, so this substrate-triggering input ESD protection circuit can effectively protect the thinner gate oxide in the deep-submicron CMOS IC's.
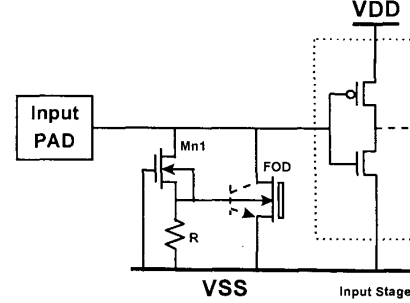
Fig.3 The input ESD protection circuit by using the substrate-triggering technique.

Fig.4 The device structure of the substrate-triggering input ESD protection circuit in Fig.3.

The device structure to realize the substrate-triggering ESD protection circuit of Fig.3 is shown in Fig.4, which includes the Mn1, R, and the FOD in a 0.25-μm shallow-trench-isolation CMOS technology. In the center of Fig.4, an N-well is connected to the input pad, and this N-well is also connected to the drain of Mn1 to protect the Mn1. Because the Mn1 with a shorter channel length, LDD structure, and the silicided diffusion in the deep-submicron CMOS technologies is very weak to the ESD stress, the N-well is added to limit the ESD current through the Mn1 before the FOD is triggered on. Because the Mn1 is designed as a start-up device to initiate the turn-on of the FOD through the substrate, the added N-well structure does not affect the triggering function of the Mn1 in the ESD protection circuit. The resistor R is realized by the parasitic p-type substrate resistance as shown in Fig.4.

While a positive ESD voltage happens to the input pin which is connected to the input pad through the bonding wire, the short-channel Mn1 is snapback broken down and generates a substrate current into the

base of the LBJT in the FOD. The base voltage is increased when the breakdown current flowing through the resistors R to VSS. The LBJT of the FOD is quickly biased by the triggering current in its substrate. Therefore, the FOD can be early triggered on to clamp the ESD voltage across the gate oxide of the input stage.

3.2 VDD-to-VSS ESD Clamp Circuit

To overcome the unexpected ESD damage on the internal circuits beyond the input or output ESD protection circuits, some ESD clamp circuits should be added between the VDD and VSS power lines [5], [6]. A VDD-to-VSS ESD clamp circuit by using the substrate-triggering technique is shown in Fig.5, where the *RC*-based ESD detection circuit is used to turn on the ESD protection device between the VDD and VSS power lines. The ESD protection device in Fig.5 is a novel double-triggering double-BJT (DTDB) device, whose device structure is illustrated in Fig.6. The DTDB device is triggered on by the trigger voltage on the gate of the ESD-protection PMOS and the trigger current in the substrate of the double-BJT structure. Both the PMOS device and the double-BJT structure in the DTDB device can be turned on to provide ESD-current discharging path between the VDD and VSS power lines.

Fig.5 The VDD-to-VSS ESD clamp circuit with the substrate-triggering technique.

Fig.6 The device structure of the DTDB device in Fig.5.

4. Experimental Results

4.1 Input ESD Protection Circuit

The substrate-triggering input ESD protection circuit has been designed and fabricated in a 0.25-μm shallow-trench-isolation CMOS process. The I-V characteristics of the lateral BJT in the FOD is measured and shown in

Fig.7(a). The snapback breakdown voltage of the FOD is as high as 11.9V, but the trigger voltage for the FOD entering into its snapback region is significantly reduced if there is some substrate bias on its base. The I-V characteristics of the whole substrate-triggering input ESD protection circuit in Fig.3 is the combination of the I-V curves of the FOD, the Mn1, and the substrate resistance. The whole I-V characteristics of the substrate-triggering input ESD protection circuit is shown in Fig.7(b), where the trigger voltage of the substrate-triggering input ESD protection circuit is lowered to only 6.4V. The trigger voltage of the FOD has been significantly reduced by the substrate-triggering current generated from the short-channel Mn1. The turn-on speed of the FOD is also enhanced by the substrate-triggering current. So, this substrate-triggering input ESD protection circuit can provide effective and quick voltage-clamping function to protect the thinner gate oxide of 50Å in the 0.25-μm CMOS technology.

(a)

(b)

Fig.7 The measured I-V characteristics of, (a) a field-oxide device with different substrate biases (X-scale: 2V/div.; Y-scale: 5mA/div.), and (b) the whole substrate-triggering input ESD protection circuit in Fig.3 (X-scale: 1V/div.; Y-scale: 2mA/div.).

The secondary breakdown current (It2) of the substrate-triggering input ESD protection circuit is also measured by the TLPG system. When the ESD-stress current on the input pad is greater than the It2 of the substrate-triggering input ESD protection circuit, the

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input ESD protection circuit is permanently damaged by the overstress current. Adjusting the device dimension of the LBJT in the FOD, the It2 can be proportionally increased. Thus, the ESD robustness of the input ESD protection circuit can be adjusted by both the device dimension and the substrate-triggering effect. The dependence of ESD level on the It2 of the substrate-triggering input ESD protection circuit with the FOD is shown in Fig.8.
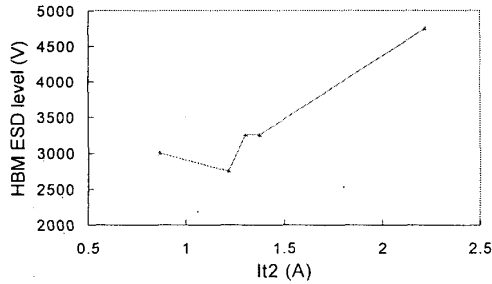

Fig.8 Dependence of the ESD level on the It2 of the substrate-triggering input ESD protection circuit in Fig.3.

4.2 VDD-to-VSS ESD Clamp Circuit

The measured I-V characteristics of the DTDB device of Fig.6 in a 0.6-μm CMOS process with different substrate biases is shown in Fig.9. The HBM ESD robustness of the VDD-to-VSS ESD clamp circuit is summarized in Fig.10 with different device dimensions. The ESD robustness in unit layout area of the DTDB device is about 0.31 V/μm^2. A similar design by using the NMOS as the ESD-current discharging device in the VDD-to-VSS ESD clamp circuit is also fabricated in the same 0.6-μm CMOS process. The NMOS with a device dimension (W/L) of 500/1.0 (μm/μm) occupies a layout area of 6931 μm^2, but only sustains an HBM ESD level of 1000V. The ESD robustness in unit layout area of the NMOS is only 0.14 V/μm^2. Thus, the DTDB device with substrate-triggering design can provide above two-times greater ESD level than that of the NMOS device in the same CMOS process.
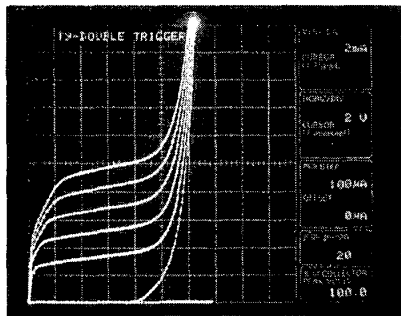

Fig.9 The I-V curves of the DTDB device with different substrate biases (X-scale: 2V/div.; Y-scale: 2mA/div.).
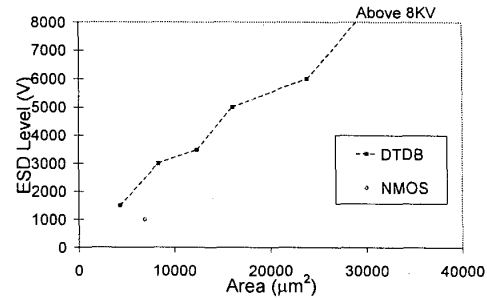

Fig.10 The relation between the HBM ESD level and the layout area of the DTDB and NMOS devices in a 0.6-μm CMOS process.

5. Conclusions

The substrate-triggering effect has been practically verified by the TLPG-measured It2 in the ESD protection devices. The substrate bias can increase the It2 of the ESD protection devices without increasing its layout area. By using the substrate-triggering technique, the input ESD protection circuit with the FOD device or the VDD-to-VSS ESD clamp circuit with the DTDB device have been proved to sustain higher ESD voltage within smaller layout area.

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