DYNAMIC–FLOATING–GATE DESIGN FOR OUTPUT ESD PROTECTION IN A 0.35–μm CMOS CELL LIBRARY

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Abstract

A dynamic-floating-gate design is proposed to improve ESD robustness of the driving-current-programmable CMOS output buffers in a 0.35-μm CMOS cell library. Through suitable design to dynamically float the gates of the output NMOS/PMOS which are originally unused in a 2-mA output buffer, the ND-mode (PS-mode) ESD level of the 2-mA output buffer can be improved from the original 1.5KV (1.0KV) up to greater than 8KV.

1. Introduction

Electrostatic Discharge (ESD) robustness of CMOS IC's had been founded to be seriously degraded by the advanced deep-submicron CMOS technologies [1]-[2]. It is necessary to improve ESD protection for the output buffers through either process modification [3] or more effective ESD protection circuit design. To improve ESD robustness of the output transistors, the symmetrical layout structure is much emphasized to realize the large-dimension output transistors by ensuring the uniform turn-on phenomenon along the multiple fingers of the output transistors [4]-[5]. To more enhance uniform turn-on phenomenon among the multiple fingers of an output NMOS, a dynamic gate-coupling design was reported to achieve uniform ESD power distribution on the large-dimension output NMOS [6].

But in the practical applications, the output buffers in a cell library have different driving specifications. For example, the output buffers may have the driving capability of 2mA, 4mA, 8mA, ..., or 24mA in the tsmc 0.35-μm cell library. But, the cell layouts of the output buffers with different driving capabilities are drawn in the same layout style and area. To provide different output driving currents, different fingers of the poly gates in the output NMOS are connected to the pre-buffer circuit, but the other unused poly-gate fingers are connected to ground. A typical layout example of the finger-type output NMOS with a small driving current is shown in Fig.1(a), whereas the equivalent circuit is shown in Fig.1(b). In Fig.1(a), there are 10 poly-gate fingers in the NMOS layout, but only a poly-gate finger (Mn1) is connected to the pre-buffer circuit to provide the sinking current from the output pad. The other 9 poly-gate fingers (Mn2) are connected to ground to turn off the NMOS (Mn2) which is unused but inside the layout. Due to the asymmetrical connection on the poly-gate fingers of the output NMOS in the layout, the ESD turn-on phenomenon among the fingers are quite different. The Mn1 with a small channel width is often turned on first and damaged by the ESD voltage, whereas the unused Mn2 with a much larger (9X) channel width is always off during the ESD stress. This generally causes a very low ESD level for the output buffer even with a total large device dimension (Mn1 + Mn2).

In this paper, a novel dynamic-floating-gate design is proposed to improve the ESD level of the output buffer with a small driving/sinking current but with a large total layout area. The gate of the unused NMOS/PMOS in the output buffer is dynamically floated during the ESD stress, so such unused NMOS/PMOS can be turned on to bypass the ESD current. The overall ESD level of such output buffers in the cell library can be significantly improved.

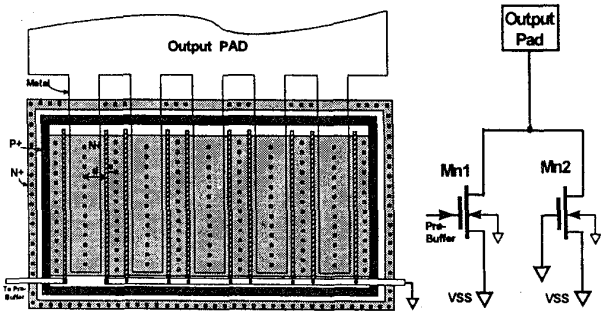

Fig.1 (a) The schematic layout of an output NMOS in a cell library with a small driving specification. (b) The equivalent circuit of the layout in (a) with a small-driving-current NMOS Mn1 and an unused but large-dimension NMOS Mn2.

2. ESD Protection Issue in the Output Buffers

To improve the turn-on uniformity of the output buffers with different driving/sinking currents and also to protect the thinner gate oxide of the output buffers in the tsmc 0.35-μm CMOS cell library, the poly gates of the unused NMOS (PMOS) in the output buffers are connected to VSS (VDD) through a small-dimension NMOS Mdn1 (PMOS Mdp1), as

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shown in Fig.2. The small-dimension Mdn1 (Mdp1) provides a function as a resistor to protect the thinner gate oxide of Mn2 (Mp2), and also sustains the ESD-transient coupling voltage on the gate of Mn2 (Mp2) to help the uniform turn-on phenomenon among the multiples fingers of the Mn1 and Mn2 (Mp1 and Mp2). The small-dimension Mdn1 (Mdp1) cooperated with the parasitic drain-to-gate capacitor in the Mn2 (Mp2) performs a gate-coupling effect to turn on the Mn2 (Mp2) during the ESD stress [6]-[7].

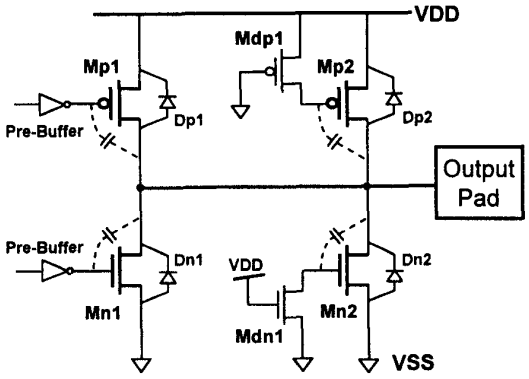

Fig.2 The output buffer in a 0.35-μm cell library with a small driving current. The gate of the unused Mn2 (Mp2) is connected to VSS (VDD) through a small-dimension Mdn1 (Mdp1) to perform the gate-coupling effect for ESD protection.

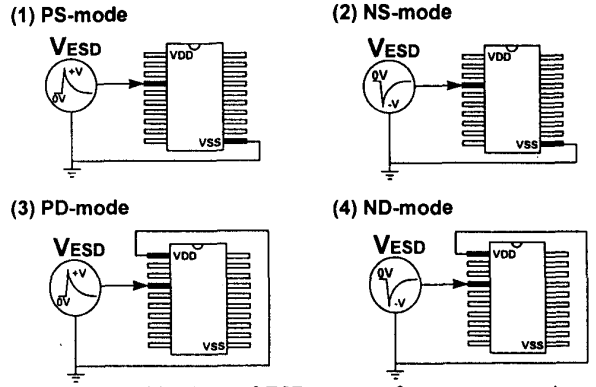

Fig.3 The combinations of ESD stresses from an output pin to the VDD or VSS pins.

Table I

HBM ESD Stress \ Output Buffers	2-mA Buffer	4-mA Buffer	8-mA Buffer	12-mA Buffer	24-mA Buffer
ND-Mode	1.5KV	2KV	2.5KV	> 2.5KV	> 2.5KV
PS-Mode	1.0KV	1.5KV	2.0KV	> 2.5KV	> 2.5KV

The ESD test to verify the ESD level of an output pin is shown in Fig.3, where there are four modes of testing combinations from the output pin to the VDD or VSS pins [8]. In the ND-mode (PS-mode) ESD stress, the output PMOS (NMOS) is reverse biased and broken down by the ESD voltage. But, in the NS-mode (PD-mode) ESD stress, the parasitic drain-to-bulk diode in the NMOS (PMOS) is forward biased to bypass the ESD current. Thus, the worst cases of the ESD stresses on an output buffer are the ND- and PS-mode ESD events.

When a positive ESD voltage attaches the output pad of Fig.2, some transient voltage is coupled through the parasitic drain-to-gate capacitor to the gates of Mn1 and Mn2. The gate of Mdn1 is biased at a high voltage, because the positive ESD voltage on the output pad is also diverted into the VDD power line through the parasitic diode Dp2 (Dp1) in the Mp2 (Mp1). The coupled voltage on the gate of Mn1 is held on its gate, but the coupled voltage on the gate of Mn2 is discharged by the Mdn1. This causes that the Mn1 is triggered on and damaged by the ESD energy before the Mn2 is turned on. Because the Mn1 is designed with a small device dimension for low driving-current specification (for example, 30/0.5 in the 2-mA output buffer), such an output buffer often has a low ESD level.

The HBM (human-body-model) ESD testing results of the cell library with different driving-current output buffers are summarized in Table I. Due to the different connections on the gates of the output Mn1 and the unused Mn2, the PS-mode (ND-mode) ESD level of the 2-mA output buffer is only 1KV (1.5KV). While the driving current of the output buffer is increased with a larger device dimension of Mn1, the output buffer has a higher ESD level. Although the cell layout areas of these output buffers (2mA, 4mA,....) are all the same in the cell library, the ESD level of these output buffers are quite different. Even if using the small-dimension NMOS Mdn1 (PMOS Mdp1) to perform the gate-coupling effect to help the uniform turn-on between the fingers of Mn1 and Mn2 (Mp1 and Mp2), the HBM ESD level of the output buffer with a small Mn1 (Mp1) but a large Mn2 (Mp2) is still below the general industrial ESD specification of 2000V.

3. The Proposed Dynamic-Floating-Gate Design

3.1 Circuit Configuration

The proposed dynamic-floating-gate design to improve ESD level of the small-driving output buffer is shown in Fig.4. As comparing to the output circuit in Fig.2, two additional MR2 and MC2 devices are designed to dynamically float the gate of the Mp2 during the ND-mode ESD-stress condition, but the gate of Mp2 is connected to VDD in the normal operating condition. Two additional MR1 and MC1 devices are also used to dynamically float the gate of the Mn2 during the PS-mode ESD-stress condition, but the gate of Mn2 is connected to VSS in the normal operating condition.

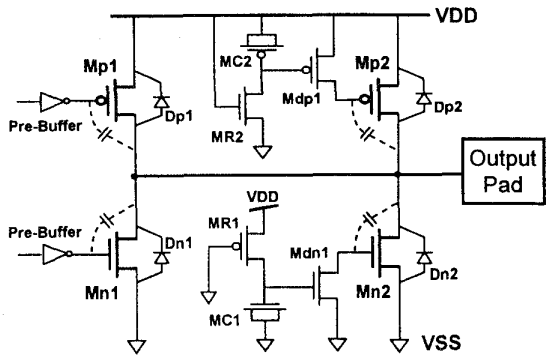

Fig.4 The proposed dynamic-floating-gate design to improve ESD level of the small-driving output buffers in a 0.35-μm cell library.

3.2 The Dynamic-Floating-Gate Mechanism

In the PS-mode ESD stress, the positive ESD voltage is applied to the output pad with the VSS grounded but the VDD floated. Due to the sharp-rising transition of the ESD voltage, the gates of the Mn2 and Mn1 are coupled with some positive voltage through the drain-to-gate parasitic capacitance in the Mn2 and Mn1. During the PS-mode ESD stress, the positive ESD voltage on the pad is also diverted into the floated VDD power line through the parasitic diode Dp2 (Dp1) in the Mp2 (Mp1). The source of MR1 is therefore charged by the ESD voltage on the VDD power line. The MR1 with a grounded gate functions as a resistor to charge the gate of Mdn1. The MC1 functions as a capacitor to store the gate voltage of Mdn1. Initially, the voltage stored on the capacitor MC1 is zero before the ESD voltage is applied to the output pad. But, the voltage stored on the capacitor MC1 is increased through the MR1 after the VDD power line is charged by the ESD current through the Dp2. The speed of the gate voltage increase, which is stored on the MC1, is strongly dependent on the *RC* time constant of the resistor MR1 and the capacitor MC1. The MR1 is especially designed with a high resistance and the MC1 is drawn with a large capacitance. This special design causes the gate voltage of Mdn1 to be kept below its threshold voltage in a long time. Because the Mdn1 is kept off in a long time, the gate of the unused Mn2 is therefore dynamically floating in the time period. A larger resistor MR1 and a lager capacitor MC1 lead to a longer time period to float the gate of the unused Mn2. By using this dynamic-floating design on the gate of the unused Mn2, the ESD-coupled voltage through the drain-to-gate capacitance of Mn2 can be held on the gate of Mn2 in an enough long time period. So, the unused Mn2 with a large device dimension in the small-driving output buffer can be instantaneously turned on to bypass the ESD current from the output pad to VSS. Owing to the effective turn-on of the unused large-dimension Mn2 in the output buffer, the PS-mode ESD level of such a small-driving output buffer can be significantly improved.

In the ND-mode ESD stress, the negative ESD voltage is applied to the output pad with the VDD grounded but the VSS floated. The negative ESD voltage on the output pad is diverted into the floated VSS power lines through the parasitic diode Dn2 (Dn1) in the Mn2 (Mn1). The NMOS MR2 with its gate connected to VDD functions as a resistor, whereas the PMOS MC2 functions as a capacitor. The negative ESD voltage on the VSS power line charges the gate of the Mdp1 through the *RC* delay of the MR2 and MC2. The speed of the decrease on the gate voltage of Mdp1 is strongly dependent on the *RC* time constant of the resistor MR2 and the capacitor MC2. A high-resistance MR2 and a large-capacitance MC2 are also designed to keep the Mdp1 off in a longer time, so the gate of the unused Mp2 can be dynamically floated in a longer time period. Due to this dynamic-floating design on the gate of the unused Mp2, the negative ESD-coupled voltage through the drain-to-gate capacitance of Mp2 can be held on the gate of Mp2 in an enough long time period. So, the unused Mp2 with a large device dimension can be instantaneously turned on to bypass the negative ESD voltage from the output pad to VDD. Owing to the turn-on of the unused large-dimension Mp2 in the output buffer, the ND-mode ESD level of such a small-driving output buffer can be significantly improved.

3.3 HSPICE Simulation on the Turn-On Behavior

To investigate the efficiency of the dynamic-floating-gate design in the small-driving output buffer, the output circuit is simulated by the *HSPICE* in a 0.35-μm CMOS technology. An ESD-like voltage pulse is added to the output pad with a pulse height of 7V and a rise time of 10ns to simulate the PS-mode ESD-stress condition. The transient voltages on the gates of Mn1 and Mn2 are monitored and shown in Fig.5. The discharging currents through the Mn1 and Mn2 in the time domain are shown in Fig.6. As shown in Figs.5 and 6, the unused Mn2 with a large device dimension can provide a much higher discharging current than the output Mn1. The turn-on time of the unused Mn2 in the simulation is about 33.7ns, which can be adjusted by the device dimensions (*RC* time constant) of the MR1 and MC1. A higher ESD voltage will couple a larger voltage to the gate of Mn2 and cause a longer turn-on time on Mn2.

The turn-on behaviors of the output circuit with the dynamic-floating-gate design is also simulated in the ND-mode ESD-stress condition. The ND-mode ESD-like voltage has a pulse height of -7V and a fall time of 10ns. The simulated results are shown in Figs.7 and 8, where the unused Mp2 has a turn-on time of 20.5ns. Due to the large device dimension of the Mp2, the discharging current through the Mp2 is much greater than that through the output Mp1. Therefore, the ESD level of the small-driving output buffer can be significantly improved by the unused Mp2 and Mn2, which are originally unused but placed in the layout of the small-driving output buffer.

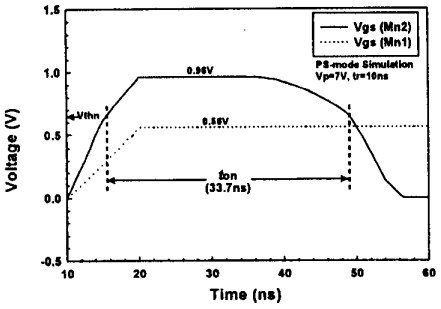

Fig.5 The transient voltages on the gates of the output Mn1 and the unused Mn2 in the PS-mode simulation with a voltage pulse of 7V and a rise time of 10ns.

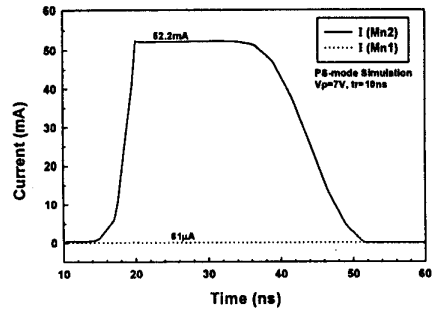

Fig.6 The discharging currents through the output Mn1 and the unused Mn2 in the PS-mode simulation with a voltage pulse of 7V and a rise time of 10ns.

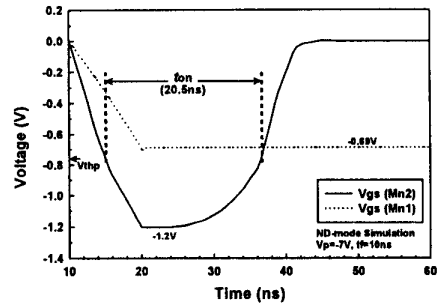

Fig.7 The transient voltages on the gates of the output Mp1 and the unused Mp2 in the ND-mode simulation with a voltage pulse of -7V and a fall time of 10ns.

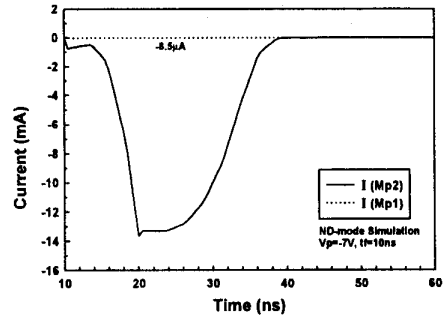

Fig.8 The discharging currents through the output Mp1 and the unused Mp2 in the ND-mode simulation with a voltage pulse of -7V and a fall time of 10ns.

3.4 Experimental Results

The small-driving output buffer with the dynamic-floating-gate design has been fabricated and tested. The additional devices MR2, MC2, MR1, and MC1 are placed in the original-empty region between the output PMOS and NMOS without increasing the total cell layout area of the original output buffer. The ESD test results are compared in Table II. The ND-mode (PS-mode) ESD level of the 2-mA output buffer with the original protection design in Fig.2 is only 1.5KV (1.0KV). But, the 2-mA output buffer with the dynamic-floating-gate design in Fig.4 can sustain the ND-mode (PS-mode) ESD level of greater than 8KV with the same cell layout area of the output buffer. The fabricated 2-mA output buffer is also subjected to the field-induced CDM (charged-device model) ESD events. It can pass the 4-KV CDM ESD stress.

Table II

HBM ESD Stress \ Output Buffers	Original 2-mA Buffer (Fig.2)	2-mA Buffer with Dynamic-Floating-Gate Design (Fig.4)
ND-Mode	1.5 KV	> 8 KV
PS-Mode	1.0 KV	> 8 KV

4. Conclusion

A novel dynamic-floating-gate design has been successfully used to improve ESD level of the small-driving output buffers in a 0.35-μm CMOS cell library. The gates of the unused NMOS/PMOS in the output buffers are dynamically floated during the ESD stress, so the unused NMOS/PMOS with a large device dimension can be instantaneously turned on to bypass the ESD current. By using the proposed dynamic-floating-gate design, the 2-mA output buffer can sustain the HBM, MM (machine-model), and field-induced CDM ESD stresses of greater than 8KV, 800V, and 4KV, respectively.

References

[1] S. Voldman and V. Gross, "Scaling, optimization and design consideration of electrostatic discharge protection circuits in CMOS technology," *1993 EOS/ESD Symp. Proc.*, pp. 251-260.

[2] A. Amerasekera and C. Duvvury, "The impact of technology scaling on ESD robustness and protection circuit design," *1994 EOS/ESD Symp. Proc.*, pp. 237-245.

[3] S. Daniel and G. Krieger, "Process and design optimization for advanced CMOS I/O ESD protection devices," *1990 EOS/ESD Symp. Proc.*, pp. 206-213.

[4] T. L. Polgreen and A. Chatterjee, "Improving the ESD failure threshold of silicided nMOS output transistors by ensuring uniform current flow," *IEEE Trans. Electron Devices*, vol. 39, pp. 379-388, 1992.

[5] S. G. Beebe, "Methodology for layout design and optimization of ESD protection transistors," *1996 EOS/ESD Symp. Proc.*, pp. 265-275.

[6] C. Duvvury and C. Diaz, "Dynamic gate coupling of NMOS for efficient output ESD protection," *Proc. of IRPS*, 1992, pp. 141-150.

[7] M.-D. Ker, *et al.*, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," *IEEE Trans. on VLSI Systems*, vol.4, pp.307-321, 1996.

[8] *EOS/ESD Standard for ESD Sensitivity Testing*, EOS/ESD Association, Inc., NY., 1993.