Electrostatic Discharge Protection Circuits in CMOS IC's Using the Lateral SCR Devices : An Overview

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Abstract

An overview on the electrostatic discharge (ESD) protection circuits by using the lateral SCR devices in CMOS IC's is presented. The history of the lateral SCR devices used for on-chip ESD protection is introduced. The practical problem of using the SCR devices in the ESD protection circuits of CMOS IC's is also discussed. Such SCR devices have been found to be accidentally triggered on by the noisy pulses when the IC's are in the normal operating conditions. To overcome this problem, two solutions are proposed to safely apply the SCR devices for effective ESD protection in the CMOS IC's.

1. Introduction

Due to the low holding voltage (~1V) of the lateral SCR devices, the power dissipation (Power ≅ IESD×Vhold) located on the SCR device during the ESD transition is significantly less than the other ESD protection devices, such as the field-oxide device, thin-oxide NMOS, or diode, in the CMOS technologies. Therefore, the lateral SCR can sustain a very high ESD voltage than the other ESD protection devices in the CMOS technologies. For example, the holding voltage of the SCR device in a typical 0.5-μm CMOS process is about 1V, but the snapback holding voltage of the NMOS in the same process is about 10V. The SCR device can sustain about 10-times larger ESD voltage in unit layout area than the NMOS does. Because the SCR devices can sustain much higher ESD voltage within a smaller layout area, the lateral SCR devices had been invented and used in the on-chip ESD protection circuits to protect the CMOS IC's against the ESD damage.

To provide the effective ESD protection for the whole CMOS IC's, the on-chip ESD protection circuits have to be added around the input, output, and power pads of the CMOS IC's. The location of the ESD protection circuits to achieve whole-chip ESD protection for a CMOS IC is illustrated in Fig.1. The lateral SCR devices were therefore used in the input/output ESD protection circuits and the VDD-to-VSS ESD clamp circuits to effectively protect the CMOS IC against the ESD damage. The overview of the SCR devices for CMOS on-chip ESD protection is first discussed in this paper.

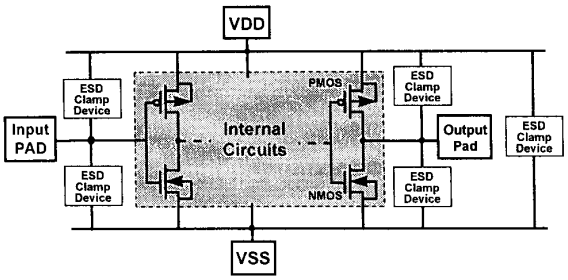

Fig.1 The schematic circuit diagram to show the location of the ESD clamp devices to achieve the whole-chip ESD protection for a CMOS IC.

2. The SCR Devices Using in the CMOS On-Chip ESD Protection Circuits

2.1 The Lateral SCR (LSCR) :

The lateral SCR (LSCR) device was used as an effective ESD-protection element for input pins in submicron CMOS IC's [1]. The application example of the LSCR device in the input ESD protection circuit is shown in Fig.2(a). The device structure of the LSCR is illustrated in Fig.2(b) and the I-V characteristics of the LSCR is illustrated in Fig.2(c). The LSCR has a high trigger voltage (~50V), which is generally greater than the gate-oxide breakdown voltage of the input stage in submicron CMOS IC's. Therefore, the LSCR has to be cooperated with the secondary protection circuit (the series resistor and the gate-grounded NMOS in Fig.2(a)) to perform the overall ESD protection function to protect the input stages. The secondary protection circuit has to sustain the ESD stress before the LSCR is triggered on to bypass the ESD current on the input pad. Because the LSCR is hard to be triggered on in time, the secondary protection circuit was found to be damaged by the ESD energy [2]. So, the secondary protection circuit was designed with a considerable large device dimension and a large series resistor to protect themselves. This secondary protection circuit with large device dimensions often occupies more layout area. If the secondary protection circuit was not properly designed, it had caused the fail window in the ESD test scanning from the low voltage to the high voltage [2]. Such input ESD protection circuit was found to pass the ESD stress with low voltage

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level or high voltage level, but it was failed when the ESD stress with a middle voltage level [2]. So, the design of the secondary protection circuit with the LSCR for the overall input ESD protection circuit is somewhat critical in the CMOS IC's.

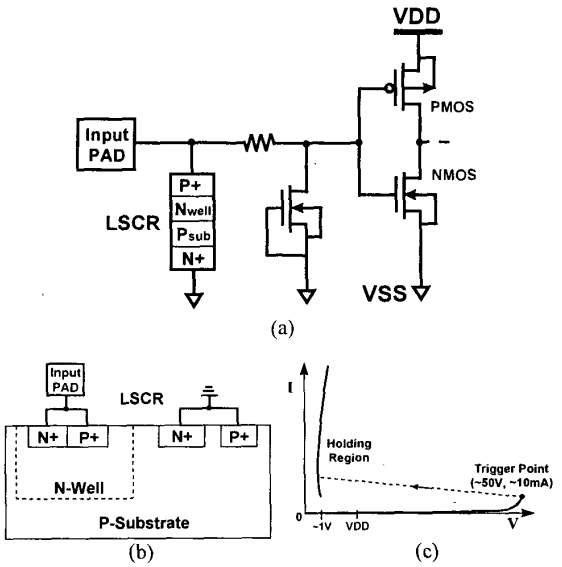


Fig.2 (a) The input ESD protection circuit with the LSCR device. (b) The device structure of the LSCR in CMOS process. (c) The I-V characteristics of the LSCR in a 1.2-μm CMOS process [2].

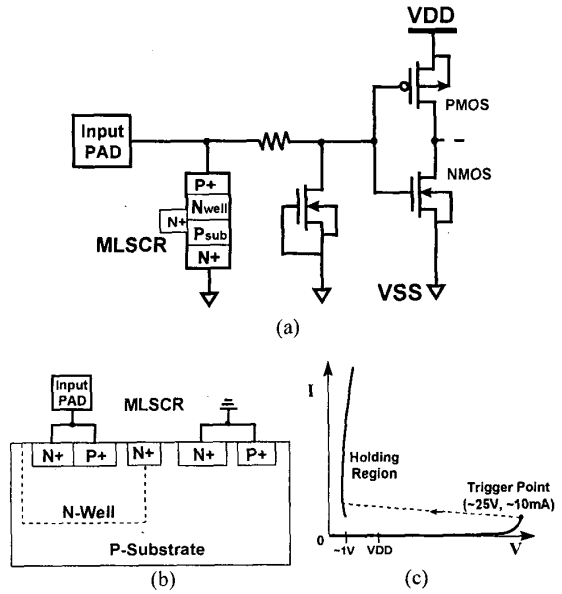


Fig.3 (a) The input ESD protection circuit with the MLSCR device. (b) The device structure of the MLSCR in CMOS process. (c) The I-V characteristics of the MLSCR in a 1.2-μm CMOS process [3].

2.2 The Modified Lateral SCR (MLSCR) :

To provide more effective ESD protection for the input stages, the modified lateral SCR (MLSCR) was invented to reduce the trigger voltage of the lateral SCR [3]. With a lower trigger voltage in the MLSCR, the secondary protection circuit could have smaller device dimensions to save total layout area. The example of using the MLSCR device in the input ESD protection circuit is shown in Fig.3(a). The device structure of the MLSCR is illustrated in Fig.3(b) and the I-V characteristics of the MLSCR is illustrated in Fig.3(c). The MLSCR is made by adding an N+ diffusion across the well-substrate junction to lower the breakdown voltage across the well-substrate junction. Because the N+ diffusion has a much higher doping concentration than the N-well, so the trigger voltage of the MLSCR can be much lower than that of the LSCR in the same CMOS process. The MLSCR was reported to have a trigger voltage about ~25V [3], which is still greater than the gate-oxide breakdown voltage of the input stages in submicron CMOS IC's. Thus, the MLSCR has to be still cooperated with the secondary protection circuit to perform the overall ESD protection function to the input stages. Unsuitable design or layout on the secondary protection circuit still causes the ESD damage located on the secondary protection circuit rather than the MLSCR device [3].

2.3 The Low-Voltage Triggering SCR (LVTSCR) :

To effectively protect the input stages and even the output buffers in submicron CMOS IC's, the LVTSCR (low-voltage triggering SCR) device had been invented with a much lower trigger voltage [4]-[7]. The example of using the LVTSCR device as the output ESD protection circuit is shown in Fig.4(a). The device structure of the LVTSCR is drawn in Fig.4(b) and the I-V characteristics of the LVTSCR is illustrated in Fig.4(c). The trigger voltage of the LVTSCR is equivalent to the snapback-trigger voltage of the short-channel NMOS device, which is inserted into the lateral SCR structure, rather than the original switching voltage (about 30~50V) of the lateral SCR device. By suitable design, the trigger voltage of the LVTSCR can be lowered below the breakdown voltage of the output NMOS [4]-[6]. The trigger voltage (current) of the LVTSCR in a submicron CMOS technology is about ~10V (~10mA). With such a low trigger voltage, the LVTSCR can provide effective ESD protection for the input stages or the output buffers of CMOS IC's without the secondary protection circuit. Therefore, the total layout area of the ESD protection circuits with the LVTSCR can be significantly saved.

2.4 The Gate-Coupled LVTSCR :

To effectively protect the thinner gate oxide in the deep-submicron low-voltage CMOS IC's, the gate-coupling technique was applied to further reduce the

trigger voltage of the LVTSCR [8]. The gate-coupled LVTSCR ESD protection circuit for input or output pads is shown in Fig.5(a). The device structure of the gate-coupled LVTSCR is illustrated in Fig.5(b) and the I-V characteristics of the gate-coupled LVTSCR in a 0.6-μm CMOS process is measured in Fig.5(c). The trigger voltage of the gate-coupled LVTSCR can be much lowered by the coupled voltage on the gate of the short-channel NMOS in the LVTSCR device. Therefore, the thinner gate oxide of the input stages in the deep-submicron low-voltage CMOS IC's can be effectively protected by using the gate-coupled LVTSCR device.

An alternative design by using circuit technique to turn on the LVTSCR rather than by the snapback breakdown in the inserted NMOS of the LVTSCR was reported in [9].

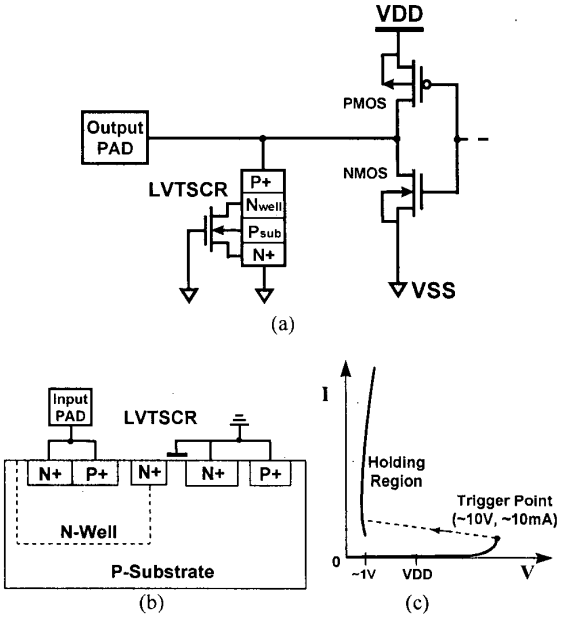


Fig.4 (a) The output ESD protection circuit with the LVTSCR device. (b) The device structure of the LVTSCR in CMOS process. (c) The I-V characteristics of the LVTSCR in a 0.6-μm CMOS process [7].

3. Issue of the SCR Devices in CMOS IC's

Due to the low holding voltage (~1V), the SCR devices in the on-chip ESD protection circuit can sustain much higher ESD voltage within smaller layout area, as comparing to the other ESD protection devices in the CMOS IC's. But, the lower trigger current may cause the LVTSCR being accidentally triggered on by the external noise pulses while the CMOS IC is in the normal operating conditions. In order to safely apply the LVTSCR for ESD protection, the LVTSCR must have an enough noise margin for CMOS IC's in the noisy environments.

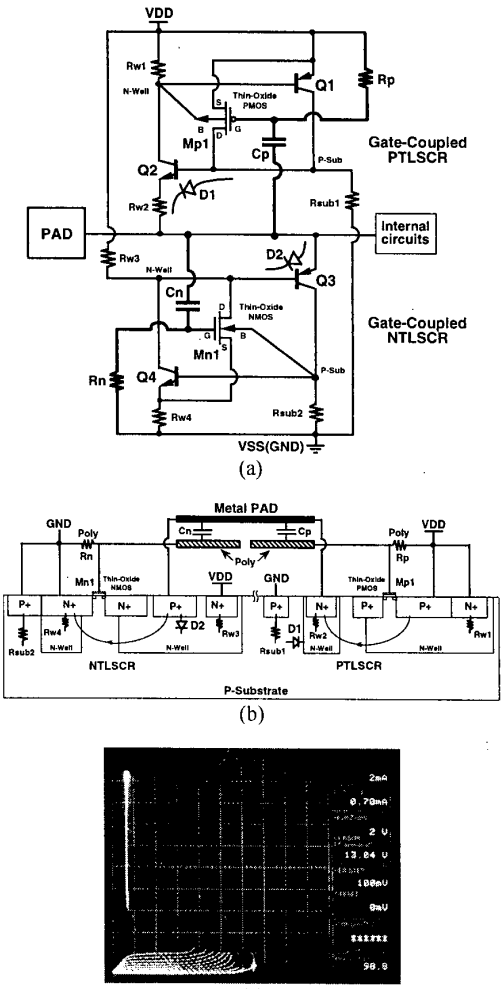
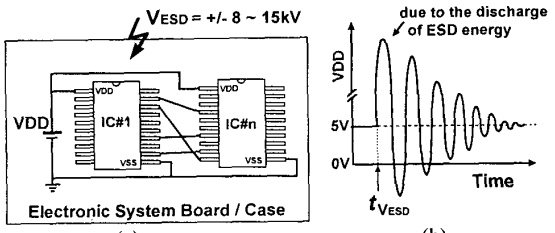


Fig.5 (a) The ESD protection circuit with the gate-coupled LVTSCR device. (b) The device structure of the gate-coupled LVTSCR in CMOS process. (c) The measured I-V characteristics of the LVTSCR in a 0.6-μm CMOS process [8].

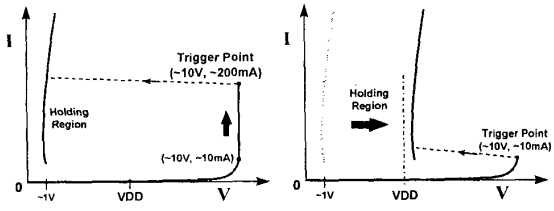
Recently, due to the request of the "*CE*" mark from the *European Community*, an ESD gun with the ESD voltage of 8~15 KV is used to test the electromagnetic compatibility (EMC) of the electronic products [10]. The system-level EMC/ESD test is illustrated in Fig.6(a). Such EMC/ESD test can cause a heavily-transient overshooting and undershooting voltage waveform of several-hundreds volts on the VDD pin of the IC's in the system board, as shown in Fig.6(b). During such system-level ESD/EMC testing, the power lines of the IC's in the system board can be coupled with an overstress voltage even up to several hundreds volts. Such a system-level ESD/EMC event easily causes the transient-induced latchup failure in the CMOS IC's. If the lateral SCR or the LVTSCR devices are used as the ESD clamp devices between the VDD and

VSS power lines of the CMOS IC's [11]-[12], such ESD-protection SCR devices are easily triggered on by the system-level ESD/EMC transient pulses to cause very serious latchup problem in the CMOS IC's.



(a) (b)

Fig.6 (a) The schematic diagram to show the system-level electromagnetic comparability (EMC) ESD test. (b) The transient overshooting/undershooting voltage waveform on the VDD pin of the IC's during the EMC/ESD testing.



(a) (b)

Fig.7 Two solutions, (a) increasing the trigger voltage; (b) increasing the holding current, to avoid the LVTSCR being accidentally triggered on by the noise pulses.

4. Solutions to Safely Applying the SCR Devices for On-Chip ESD Protection

There are two solutions to avoid the LVTSCR being accidentally triggered on by the noise pulses when the IC's are in the normal operating conditions. As shown in Fig.7(a), one to only increase the trigger current of the LVTSCR, but the trigger voltage and the holding voltage are kept the same. With higher trigger current, the LVTSCR has enough noise margin against the overshooting or undershooting noise pulses on the pads. An HINTSCR (high-current NMOS-trigger lateral SCR) device has been successfully designed by adding a bypass diode into the LVTSCR structure to increase its trigger current up to 218.5mA in a 0.6-μm CMOS process [13]. Such HINTSCR has a noise margin greater than VDD+12V in the 3-V application.

Another method is to increase the holding voltage of the LVTSCR to be greater than the voltage of VDD, as shown in Fig.7(b). But, the trigger voltage and current is still kept as low as that of the LVTSCR. Only increasing the holding voltage of an LVTSCR leads to more power dissipation on the LVTSCR during the ESD transition. This will cause a lower ESD robustness on the LVTSCR. To overcome this issue, a novel cascoded-LVTSCR structure has been designed to increase the holding voltage (>VDD) without degrading its ESD robustness in a 0.35-μm silicided CMOS technology [14].

5. Conclusions

An overview on the ESD protection circuits by using the lateral SCR devices in CMOS IC's has been presented. The practical problem of using the SCR devices in the ESD protection circuits of CMOS IC's is also discussed. To overcome such problem, two solutions are proposed to safely apply the SCR devices for effective ESD protection in the CMOS IC's.

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