

# How to Safely Apply the LVTSCR for CMOS Whole-Chip ESD Protection without being Accidentally Triggered On

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**Abstract** - In this paper, the lateral SCR devices used in CMOS on-chip ESD protection circuits are reviewed. Such SCR devices had been found to be accidentally triggered on by noise pulses when the IC's are in the normal operating condition. A cascode design is therefore proposed to safely apply the LVTSCR devices for whole-chip ESD protection in CMOS IC's without causing unexpected operation errors or latchup danger. Such cascoded LVTSCR's with a holding voltage greater than VDD of an IC can provide CMOS IC's with effective component-level ESD protection but without being accidentally triggered on by system-level overshooting or undershooting noise pulses.

## 1. Introduction

Due to the low holding voltage ( $\sim 1V$ ) of the lateral SCR device, the power dissipation ( $\text{Power} \cong I_{\text{ESD}} \times V_{\text{hold}}$ ) of the SCR device during the electrostatic discharge (ESD) transition is less than that of other ESD protection devices (such as the field-oxide device, thin-oxide NMOS, or diode) in CMOS technologies. Thus, the lateral SCR device can sustain very high ESD stress as compared to other ESD protection devices in CMOS technologies. For example, the holding voltage of an SCR device in a  $0.35\text{-}\mu\text{m}$  bulk CMOS process is about  $1V$ , but the snapback holding voltage of an NMOS device in the same process is about  $6V$ . The SCR device can sustain about 6-times larger ESD current per unit layout area than does the NMOS. Because the SCR device can sustain much higher ESD stress within a smaller layout area, the lateral SCR devices had been used in the on-chip ESD protection circuits to protect CMOS IC's against ESD damage [1]-[20].

To provide effective ESD protection for a whole CMOS IC, the on-chip ESD protection circuits are added around the input, output, and power pads of a CMOS IC. Because some ESD damage had been

found on the internal circuits beyond the input or output ESD protection circuits [21]-[24], the ESD clamp circuit has to be also placed between the VDD and VSS power lines to provide the real whole-chip ESD protection [25]-[29]. The location of ESD clamp circuits in a CMOS IC to achieve whole-chip ESD protection is illustrated in Fig.1. Therefore, the lateral SCR devices had been used in input/output ESD protection circuits [1]-[16], [18]-[20] and VDD-to-VSS ESD clamp circuits [17], [29] to effectively protect CMOS IC's against ESD damage.

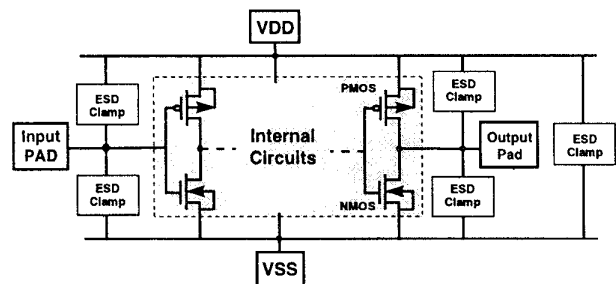


Fig.1 The schematic circuit diagram to show the location of ESD clamp circuits in a CMOS IC to achieve whole-chip ESD protection.

In this paper, the lateral SCR devices used in CMOS on-chip ESD protection circuits are reviewed. The latchup danger of using SCR devices in CMOS on-chip ESD protection circuits is discussed. Such SCR devices had been found to be accidentally triggered on by the noise pulses when the IC's are in the normal operating conditions. To overcome this problem, a cascode configuration has been proposed to safely apply the SCR devices for effective ESD protection in CMOS IC's.

## 2. The SCR Devices Used in CMOS On-Chip ESD Protection Circuits

### 2.1 The Lateral SCR (LSCR) :

The lateral SCR (LSCR) device had been used as an effective ESD protection element for input pins in submicron CMOS IC's [1]-[3]. The typical application example of the LSCR device in an input ESD protection circuit is shown in Fig.2(a). The device structure of the LSCR is illustrated in Fig.2(b) and the I-V characteristics of the LSCR is illustrated in Fig.2(c). The LSCR has a high trigger voltage (~50V), which is much greater than the gate-oxide breakdown voltage of the input stages in submicron CMOS IC's. Therefore, the LSCR has to be used in conjunction with the secondary protection circuit (the series resistor and the gate-grounded NMOS in Fig.2(a)) to perform the overall ESD protection function to protect the input stages.

The secondary protection circuit has to sustain the ESD stress before the LSCR is triggered on to bypass ESD current on the input pad. Because the LSCR is slow in triggering, the secondary protection circuit was found to be damaged by the ESD energy [3]. So, the secondary protection circuit was designed with a considerably larger device dimension and a large series resistor to protect themselves. This secondary protection circuit with large device dimensions often occupies more layout area. If the secondary protection circuit was not properly designed, it had caused a failure window in the ESD test scanning from the low voltage to the high voltage. Such input ESD protection circuit was found to pass the ESD stress with low voltage level or high voltage level, but it failed when the ESD stress with a middle voltage level [3]. So, the design of the secondary protection circuit with the LSCR for the overall input ESD protection circuit is somewhat critical in CMOS IC's.

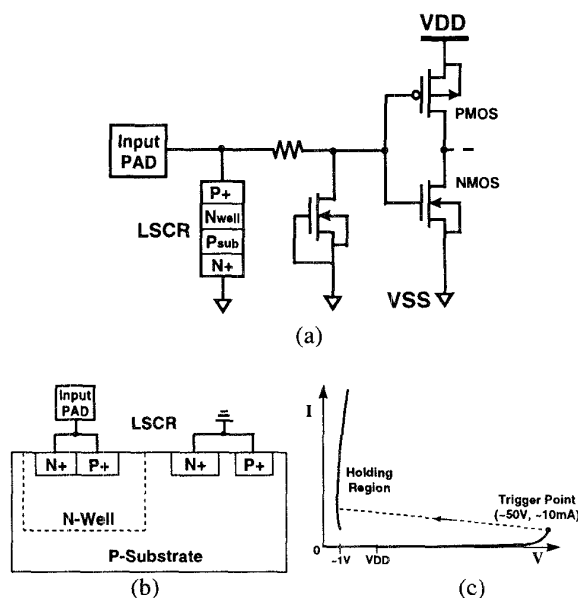


Fig.2 (a) The input ESD protection circuit with the LSCR device. (b) The device structure of the LSCR in CMOS process. (c) The I-V characteristics of the LSCR in a 1.2- $\mu$ m CMOS process [2].

### 2.2 The Modified Lateral SCR (MLSCR) :

To provide more effective ESD protection for the input stages, the modified lateral SCR (MLSCR) was invented to reduce the trigger voltage of the lateral SCR [4]. With a lower trigger voltage in the MLSCR, the secondary protection circuit could have smaller device dimensions to save total layout area. The example of using the MLSCR device in the input ESD protection circuit is shown in Fig.3(a). The device structure of the MLSCR is illustrated in Fig.3(b) and the I-V characteristics of the MLSCR is illustrated in Fig.3(c). The MLSCR is made by adding an N+ diffusion across the well-substrate junction to lower the trigger voltage of the SCR device. Because the N+ diffusion has a much higher doping concentration than the N-well, the trigger voltage of the MLSCR can be significantly lower than that of the LSCR in the same CMOS process. The MLSCR was reported to have a trigger voltage of about ~25V [4], which is still greater than the gate-oxide breakdown voltage of the input stages in submicron CMOS IC's. Thus, the MLSCR has to be still cooperated with the secondary protection circuit to perform the overall ESD protection function for the input stages. Unsuitable design or layout on the secondary protection circuit still causes the ESD damage located on the secondary protection circuit rather than the MLSCR device [4].

To lower the trigger voltage of SCR device, the transient-triggering effect on the SCR device had been studied and used to design the on-chip ESD protection circuit with multiple SCR structures [5]-[9].

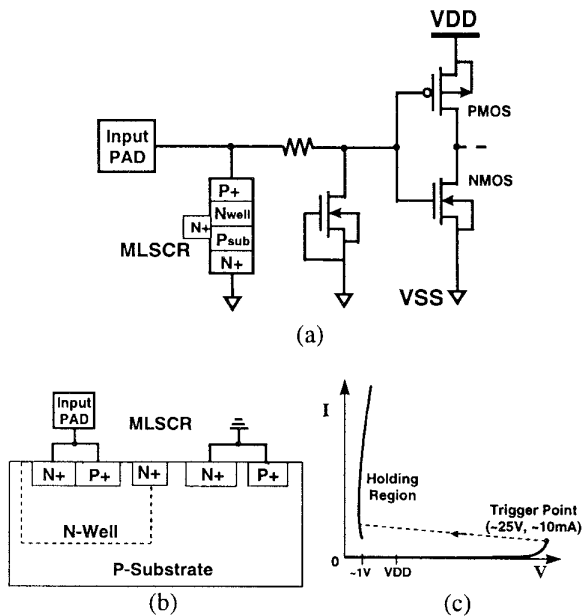


Fig.3 (a) The input ESD protection circuit with the MLSCR device. (b) The device structure of the MLSCR in CMOS process. (c) The I-V characteristics of the MLSCR in a 1.2- $\mu\text{m}$  CMOS process [4].

### 2.3 The Low-Voltage Triggering SCR (LVTSCR) :

To effectively protect the input stages and even the output buffers in submicron CMOS IC's, the LVTSCR (low-voltage triggering SCR) device had been invented with a much lower trigger voltage [10]-[16]. The example of using the LVTSCR device as the output ESD protection circuit is shown in Fig.4(a). The device structure of the LVTSCR is drawn in Fig.4(b) and the I-V characteristics of the LVTSCR is illustrated in Fig.4(c).

The trigger voltage of the LVTSCR is equivalent to the snapback-trigger voltage of the short-channel NMOS device, which is inserted into the lateral SCR structure, rather than the original switching voltage (about 30~50V) of the lateral SCR device. By suitable design, the trigger voltage of the LVTSCR can be lowered below the breakdown voltage of the output NMOS [11]-[16]. The trigger voltage (current) of the LVTSCR in a 0.6- $\mu\text{m}$  CMOS technology is about ~10V (~10mA). With such a low trigger voltage, the

LVTSCR can provide effective ESD protection for both the input stages and the output buffers of CMOS IC's without the support of secondary protection circuit. Therefore, the total layout area of the ESD protection circuits with the LVTSCR can be significantly reduced.

By using another method, the hot-carrier effect in the short-channel NMOS device was also applied to reduce the trigger voltage of the SCR device [17].

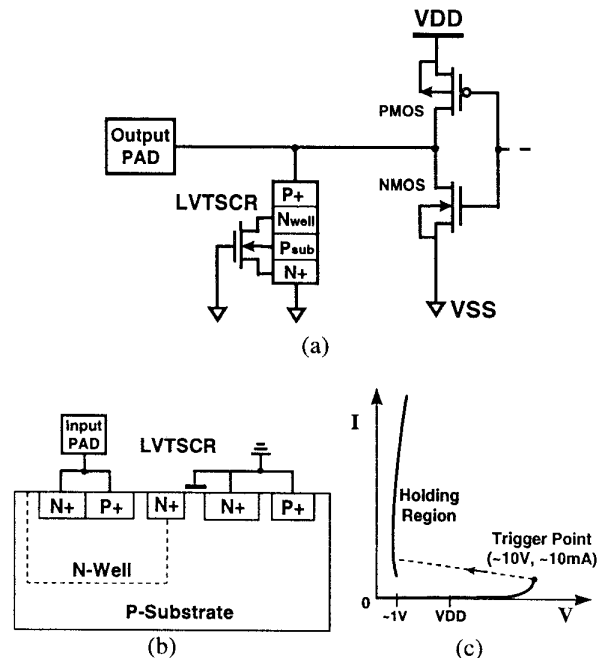


Fig.4 (a) The output ESD protection circuit with the LVTSCR device. (b) The device structure of the LVTSCR in CMOS process. (c) The I-V characteristics of the LVTSCR in a 0.6- $\mu\text{m}$  CMOS process [16].

### 2.4 The Gate-Coupled LVTSCR :

To effectively protect the thinner gate oxide in deep-submicron low-voltage CMOS IC's, the gate-coupling technique was applied to further reduce the trigger voltage of the LVTSCR [18]-[19]. The gate-coupled LVTSCR ESD protection circuit for input or output pads is shown in Fig.5(a). The device structure of the gate-coupled LVTSCR is illustrated in Fig.5(b) and the I-V characteristics of the gate-coupled LVTSCR in a 0.6- $\mu\text{m}$  CMOS process is measured in Fig.5(c). The trigger voltage of the gate-coupled LVTSCR can be significantly lowered by the coupled voltage on the gate of the short-channel NMOS in the LVTSCR device. Thus, the thinner gate oxide of the input stages in deep-submicron low-voltage CMOS

IC's can be effectively protected by the gate-coupled LVTSCR.

An alternative design by using a circuit technique, rather than by using snapback breakdown, is to turn on the LVTSCR device for ESD protection as also reported in [20].

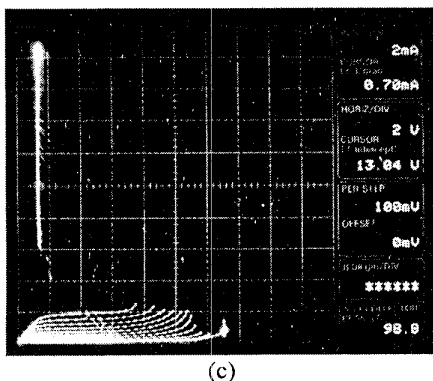
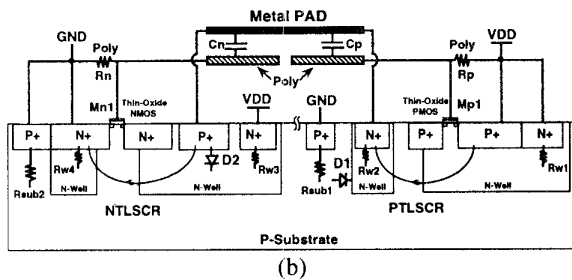
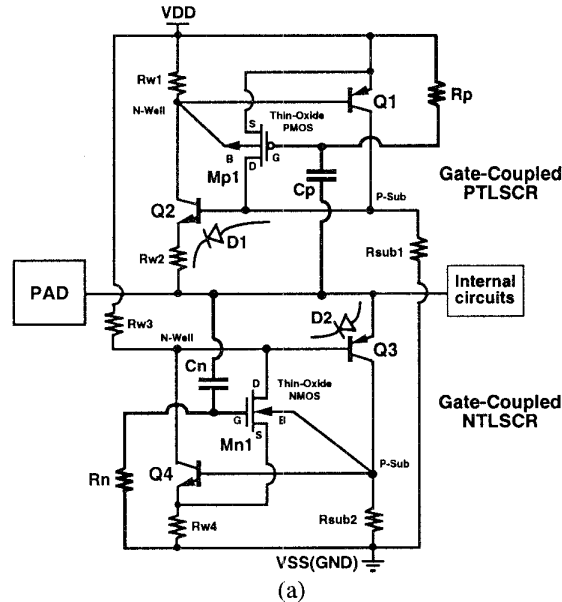


Fig.5 (a) The ESD protection circuit with the gate-coupled LVTSCR devices. (b) The device structure of the gate-coupled LVTSCR in CMOS process. (c) The measured I-V characteristics of the gate-coupled LVTSCR in a 0.6- $\mu\text{m}$  CMOS process [19].

### 3. Issue of the LVTSCR Devices in CMOS IC's

Due to the low trigger voltage ( $\sim 10\text{V}$ ), the LVTSCR device can perform excellent on-chip ESD protection without the support of the secondary protection circuit. But, its low trigger current ( $\sim 10\text{mA}$ ) may cause the LVTSCR to be accidentally triggered on by the external noise pulses while the CMOS IC is in the normal operating condition. In order to safely apply the LVTSCR for on-chip ESD protection, the LVTSCR in CMOS IC's must have an enough noise margin to the noise glitches in the application environments.

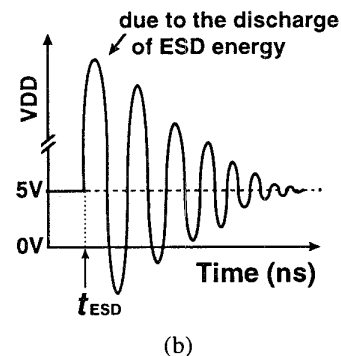
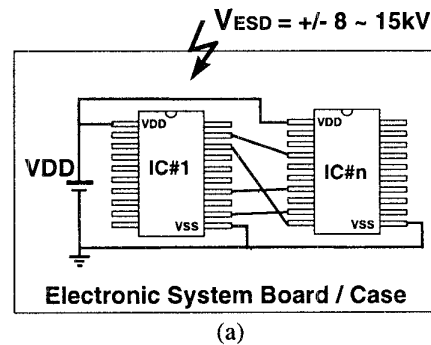


Fig.6 (a) The schematic diagram to show the system-level electromagnetic compatibility (EMC) ESD test. (b) The transient overshooting/undershooting voltage waveform on the VDD pin of the IC's during the EMC/ESD test.

Recently, due to the request of the “CE” mark from the *European Community*, an ESD gun with the ESD voltage of 8~15 KV is used to test the electromagnetic compatibility (EMC) of the electronic products [30]-[32]. The system-level EMC/ESD test is illustrated in Fig.6(a). Such EMC/ESD test can cause a heavily overshooting or undershooting voltage transition on the VDD pins of the IC's in the system board, as shown in Fig.6(b). During such system-level EMC/ESD test, the power lines of IC's in the system board can be coupled with

an overstress voltage even up to several hundreds volts. Such a system-level EMC/ESD event easily causes the transient-induced latchup failure in CMOS IC's [33]-[35]. If the lateral SCR or the LVTSCR devices are used as the ESD clamp devices between the VDD and VSS power lines of CMOS IC's [17], [29], such ESD-protection SCR devices are easily triggered on by the system-level EMC/ESD transient pulses to cause very serious latchup problem in CMOS IC's.

The LVTSCR devices in the input or output ESD protection circuits are also susceptible to such system-level noise pulses. Because the holding voltage of the LVTSCR is only  $\sim 1\text{V}$ , the voltage levels of the input or output signals can be destroyed if the LVTSCR in the ESD protection circuits is accidentally turned on when the IC is in the normal operating condition [36]. For example, in Fig.7(a), the output buffer of Chip 1 is used to drive the input pad of Chip 2, where the input ESD protection circuit in Chip 2 is formed by the LVTSCR. While the output buffer in Chip 2 sends an output signal of logic "1" to the input pad of Chip 1, the output PMOS in Chip 1 is turned on by the pre-buffer circuit with a logic "0". Therefore, the voltage level on the input pad of Chip 2 is charged up to VDD, and the LVTSCR is initially kept off. But, if there is a board-level noise pulse coupled to the interconnection line between the output pad of Chip 1 and the input pad of Chip 2, the LVTSCR in Chip 2 may be triggered on by the overshooting noise pulse and the voltage level on the input pad is dropped down to only  $\sim 1\text{V}$ . If the LVTSCR device is used in the output ESD protection circuit, as shown in Fig.7(b), the LVTSCR could be also triggered on by the noise pulse coupled to the output pad.

Because the output PMOS often has a large device dimension to drive an external heavy load, the load line of the output PMOS has a stable intercept point on the I-V curve of the LVTSCR. The intercept point in Fig.7(c) is the operating point of the LVTSCR, where there is a current  $I_L$  flowing from the VDD through the output PMOS and LVTSCR to the VSS. Due to the triggering of noise pulses, the turned-on LVTSCR clamps the voltage level on the input pad of Chip2 (the output pad of Chip 3) from VDD to  $\sim 1\text{V}$ . This changes the logic state from "1" to "0" on the pad and causes an operation error in the application system. Moreover, the board-level leakage current  $I_L$  ( $\sim 100\text{mA}$ , dependent on the device dimension of the output PMOS) from VDD to VSS consumes more system power.

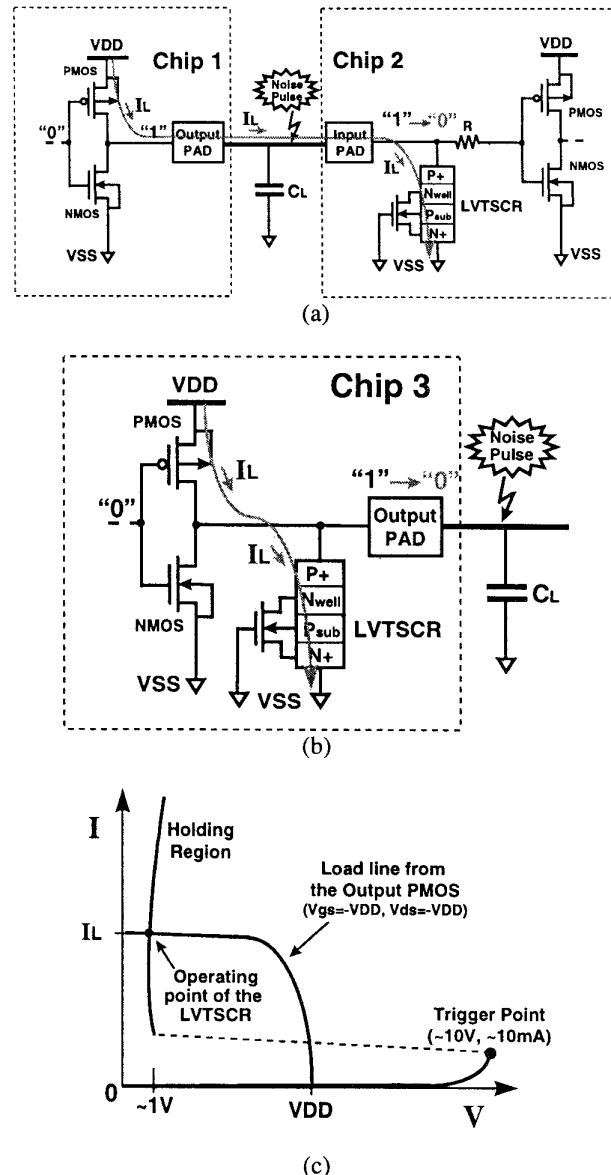


Fig.7 The schematic diagram to show the LVTSCR in (a) an input ESD protection circuit in Chip 2, (b) an output ESD protection circuit in Chip 3, being accidentally triggered on by the system-level overshooting noise pulses. (c) The intercepted point between the I-V curves of the output PMOS and the LVTSCR decides the voltage level on the pad and the leakage current  $I_L$  from VDD to VSS.

#### 4. Solutions to Safely Apply LVTSCR Devices for On-Chip ESD Protection

There are two solutions to avoid the LVTSCR being accidentally triggered on by the noise pulses when the IC's are in the normal operating condition. As shown in Fig.8(a), the first is to only increase the trigger current of the LVTSCR, but the trigger voltage and the holding voltage are kept the same.

With a higher trigger current, the LVTSCR has enough noise margin against the overshooting or undershooting noise pulses on the pads. An HINTSCR (high-current NMOS-trigger lateral SCR) device had been successfully designed by adding a bypass diode into the LVTSCR device structure to increase its trigger current from  $\sim 10\text{mA}$  to  $\sim 200\text{mA}$  in a  $0.6\text{-}\mu\text{m}$  CMOS process [37]-[39]. Such an HINTSCR has a noise margin greater than  $V_{DD}+12\text{V}$  in the 3-V application.

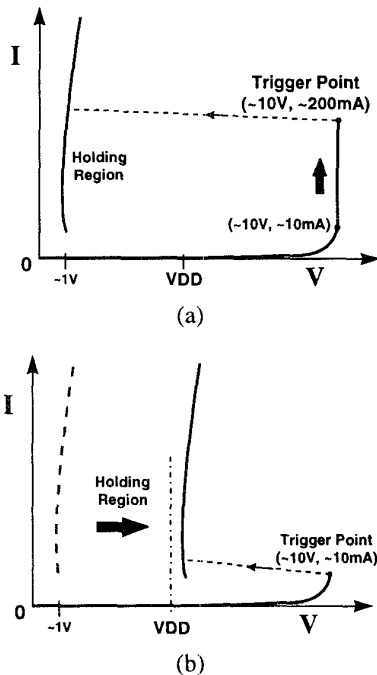


Fig.8 Two solutions, (a) by increasing the trigger current; (b) by increasing the holding voltage, to avoid the LVTSCR being accidentally triggered on by the noise pulses.

The second method is to increase the holding voltage of the LVTSCR greater than the voltage level of  $V_{DD}$  in CMOS IC's, as shown in Fig.8(b). But, the trigger voltage and current is still kept as low as that of an LVTSCR. In the CMOS process with epitaxial substrate, the holding voltage of an SCR device can be easily increased greater than  $V_{DD}$  by extending the anode-to-cathode distance in the SCR structure or by reducing the thickness of the epitaxial layer [40]-[41]. Only increasing the holding voltage of an LVTSCR leads to more power dissipation (Power  $\equiv I_{ESD} \times V_{hold}$ ) of the LVTSCR during the ESD transient. This will cause a lower ESD robustness on the LVTSCR. The dependence of layout spacing on ESD performance of an LVTSCR device with a holding voltage greater than  $V_{DD}$  had been

investigated in a CMOS process with epitaxial substrate [42]. But, most CMOS IC's (especially the consumer IC's) are still fabricated in the low-cost bulk CMOS processes without using the epitaxial substrate. It is difficult to increase the holding voltage of an SCR device greater than  $V_{DD}$  in such bulk CMOS processes. Using the double guard rings to surround both the anode and the cathode of an SCR device can break the latching path and increase its holding voltage. But, the latchup guard rings often occupy much more layout area and wider layout spacing for the bulk CMOS process. Moreover, such SCR devices with double guard rings for the bulk CMOS process take more time to turn themselves on, so they can not be triggered on in time to bypass the fast-transient ESD current.

To overcome this issue, a novel cascoded-LVTSCR structure is designed in this paper to increase its holding voltage ( $>V_{DD}$ ) without much degradation in its ESD robustness for a  $0.35\text{-}\mu\text{m}$  silicided bulk CMOS process.

## 5. Design of the Cascoded LVTSCR's

To increase the holding voltage of the LVTSCR but without increasing the power dissipation in the LVTSCR, a novel cascode configuration is proposed to achieve both high component-level ESD robustness and safe application without the latchup problem during the system-level EMC/ESD test. The device structures of the proposed cascoded NCLSCR's (NMOS-Controlled Lateral SCR's) and PCLSCR's (PMOS-Controlled Lateral SCR's) are shown in Fig.9(a) and 9(b), respectively, in a bulk p-substrate CMOS process. In Fig.9, the cathode of the NCLSCR1 (PCLSCR1) is connected to the anode of the NCLSCR2 (PCLSCR2), and the cathode of the NCLSCR2 is connected to the anode of the next NCLSCR (PCLSCR) device to configure the cascoded NCLSCR's (PCLSCR's). All the gates of the NCLSCR's (PCLSCR's) are connected together and controlled by a control gate.

By using the cascode configuration, the total voltage drop across the cascoded NCLSCR's (PCLSCR's) is the sum of the voltage drop across every NCLSCR (PCLSCR) device. Therefore, the total holding voltage of the cascoded NCLSCR's (PCLSCR's) becomes tunable by changing the number of the NCLSCR's (PCLSCR's) in the cascode configuration. If the cascoded NCLSCR's include 3 NCLSCR devices, its total holding voltage can be

greater than the 3-V VDD. Each NCLSCR device still has a holding voltage of  $\sim 1\text{V}$ , but the cascoded NCLSCR's have a holding voltage greater than VDD. So, the cascoded NCLSCR's (PCLSCR's) design can safely apply the advantages of the LVTSCR's for whole-chip ESD protection but without causing the accidental trigger-on operation error or the latchup danger in CMOS IC's.

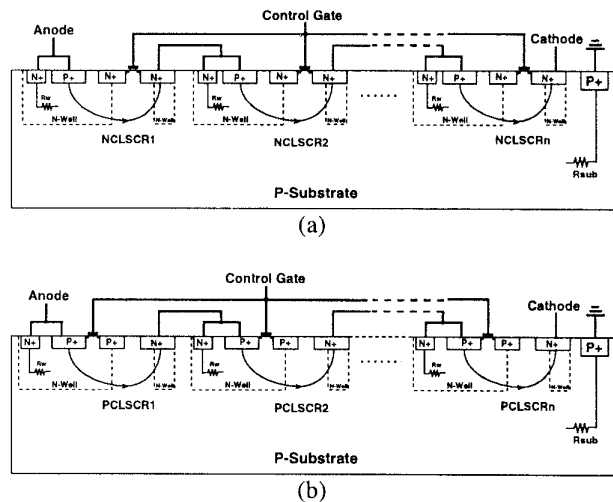


Fig.9 The schematic cross-sectional view of (a) the cascoded NCLSCR's, and (b) the cascoded PCLSCR's.

## 6. Characteristics of the Cascoded LVTSCR's

The cascoded NCLSCR's and PCLSCR's with different number of LVTSCR devices have been fabricated in a  $0.35\text{-}\mu\text{m}$  bulk CMOS process with both silicided diffusion and LDD structure. The device characteristics, especially including the temperature effect, has been measured and investigated in more detail.

### 6.1 The Cascoded NCLSCR's :

The I-V curves of a single NCLSCR with 0-V gate bias are shown in Fig.10(a) and 10(b) under the temperature of  $25^\circ\text{C}$  and  $150^\circ\text{C}$ , respectively. The holding voltage of a single NCLSCR is reduced from the  $1.44\text{V}$  at  $25^\circ\text{C}$  to only  $1.07\text{V}$  at  $150^\circ\text{C}$ , which is much lower than the VDD of CMOS IC's. Such an NCLSCR in the ESD protection circuit is easily triggered on by the system-level EMC/ESD test or by the high-temperature high-voltage reliability test which cause failures or malfunctions in the application systems.

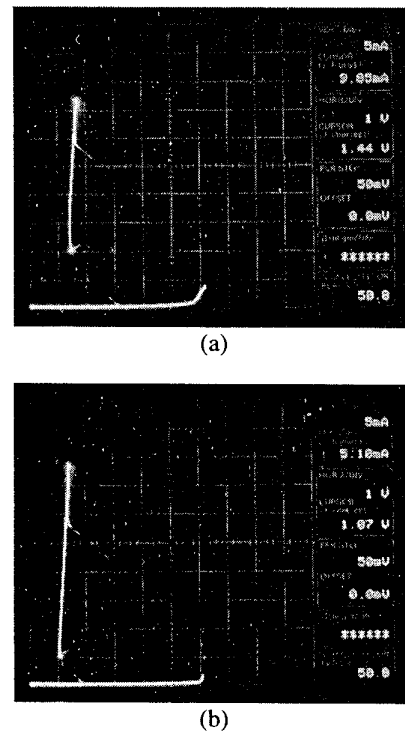
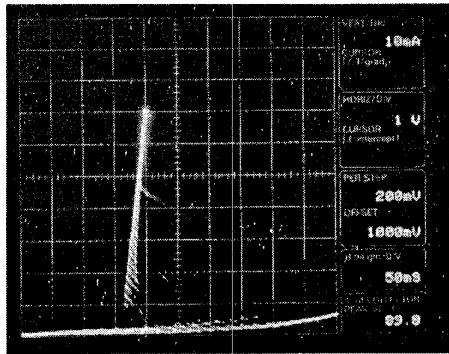


Fig.10 The I-V curves of a single NCLSCR device with 0-V gate bias under the temperature of (a)  $25^\circ\text{C}$ , and (b)  $150^\circ\text{C}$ .

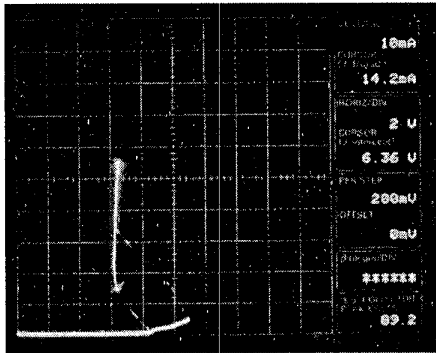
The I-V curves of the cascoded NCLSCR's with three and five NCLSCR's at  $125^\circ\text{C}$  are shown in Fig.11(a) and 11(b), respectively, under different gate biases. The trigger voltage of the NCLSCR can be significantly reduced as its gate voltage is increased. With a positive gate voltage, the cascoded NCLSCR's are easily triggered into the holding region. The dependence of the trigger voltage of the cascoded NCLSCR's on the control-gate voltage under the temperature of  $125^\circ\text{C}$  is shown in Fig.12. The larger gate voltage leads to a lower trigger voltage to turn on the cascoded NCLSCR's.

In Fig.11, the holding voltage of the 3-NCLSCR's is  $3.82\text{V}$ , whereas the holding voltage of the 5-NCLSCR's is  $6.36\text{V}$ . The temperature dependence of the total holding voltage in the cascoded NCLSCR's is shown in Fig.13. The dependence of the holding voltage of the cascoded NCLSCR's on the number of the NCLSCR devices for different temperatures is shown in Fig.14. The holding voltage of the cascoded NCLSCR's is almost linearly increased as the number of the cascoded NCLSCR's is increased. By adjusting the number of the cascoded NCLSCR devices, the holding voltage of the cascoded NCLSCR's becomes tunable to meet the different applications.

For example, to safely apply the cascoded NCLSCR's for ESD protection in 3-V CMOS IC's without causing latchup danger, three cascoded NCLSCR's have to be used. This provides a practical and useful solution to safely apply the LVTSCR for effective ESD protection, especially in the bulk CMOS process.



(a)



(b)

Fig.11 The I-V curves of (a) the 3-NCLSCR's with different gate biases, and (b) the 5-NCLSCR's with 0-V gate bias, under the temperature of 125°C.

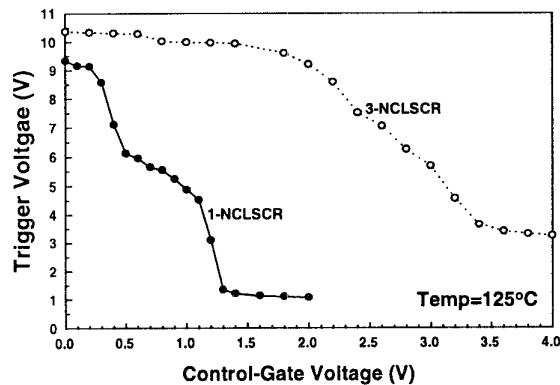


Fig.12 Dependence of the trigger voltage of the cascoded NCLSCR's on the control-gate voltage under the temperature of 125°C.

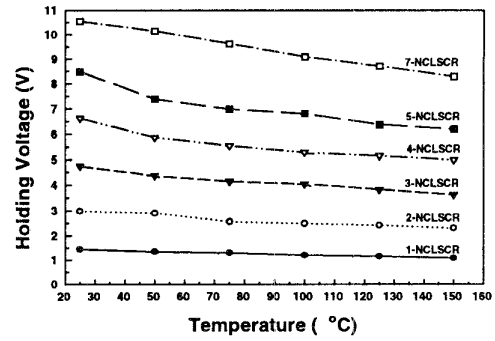


Fig.13 The temperature dependence of the total holding voltage in the cascoded NCLSCR's with different number of NCLSCR devices.

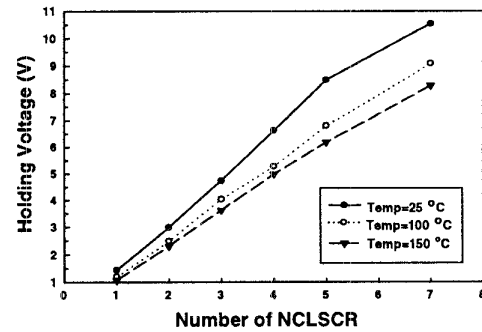
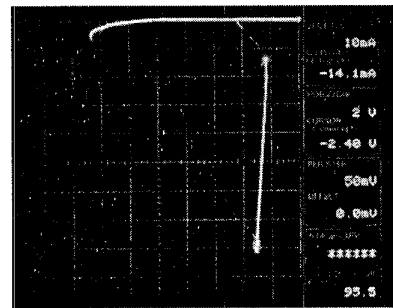
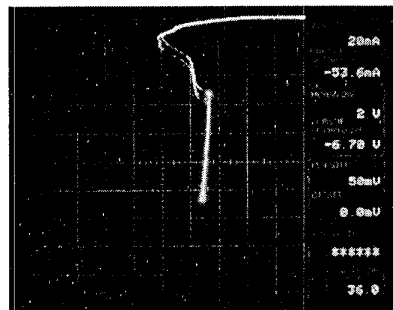


Fig.14 Dependence of the holding voltage of the cascoded NCLSCR's on the number of the NCLSCR devices.



(a)



(b)

Fig.15 The I-V curves of the cascoded PCLSCR's with (a) two PCLSCR devices, (b) five PCLSCR devices, under the temperature of 150°C.



## 6.2 The Cascoded PCLSCR's :

The I-V curves of the cascoded PCLSCR's with two and five PCLSCR's at 150°C are shown in Fig.15(a) and 15(b), respectively, under 0-V gate bias. The holding voltage of the 2-PCLSCR's is -2.4V, whereas the holding voltage of the 5-PCLSCR's is -6.7V. The temperature dependence of the holding voltage of the cascoded PCLSCR's is shown in Fig.16. The dependence of the holding voltage of the cascoded PCLSCR's on the number of PCLSCR devices for different temperatures is shown in Fig.17. The holding voltage of the cascoded PCLSCR's is almost linearly increased as the number of the cascoded PCLSCR's is increased. By adjusting the number of the cascoded PCLSCR devices, the holding voltage of the cascoded PCLSCR's becomes tunable to meet the different applications. For example, to safely apply the cascoded PCLSCR's for ESD protection in the 3-V CMOS IC's without causing latchup danger, three PCLSCR's have to be used in the cascoded PCLSCR's

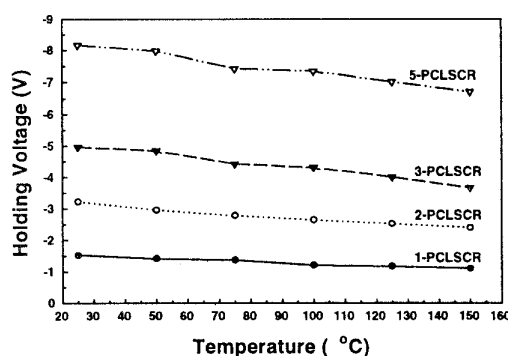


Fig.16 The temperature dependence of the holding voltage of the cascoded PCLSCR's with different number of PCLSCR devices.

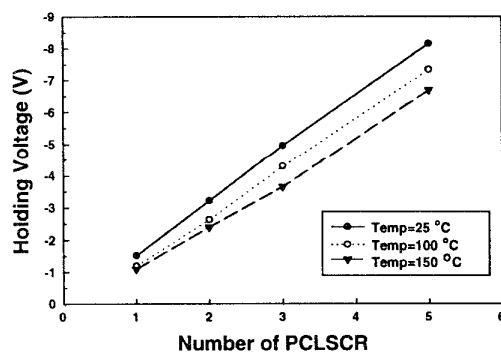


Fig.17 Dependence of the holding voltage of the cascoded PCLSCR's on the number of PCLSCR devices.

## 6.3 Turn-On Resistance :

The slope ( $\Delta V/\Delta I$ ) of the measured I-V curves of the cascoded NCLSCR's and PCLSCR's devices can be defined as the turn-on resistance of the cascoded LVTSCR's in their holding regions. The turn-on resistance in the holding region changes slightly while the operating point is moving along the I-V curves in the holding region. For comparison, the slope ( $\Delta V/\Delta I$ ) between the operating currents of 20 mA and 200mA in the holding region is used to define the turn-on resistance of the cascoded LVTSCR's. The relations between the turn-on resistance and the number of cascoded LVTSCR's are shown in Fig.18. All the cascoded LVTSCR's devices have the same device width of 30  $\mu\text{m}$ . The larger the device width leads to a lower turn-on resistance in the cascoded LVTSCR's. In Fig.18 with the device width of 30  $\mu\text{m}$ , the cascoded 3-NCLSCR's have a turn-on resistance of 9.8  $\Omega$ , but the cascoded 3-PCLSCR's have a turn-on resistance of 12.7  $\Omega$ . More NCLSCR's or PCLSCR's used in the cascode configuration cause a corresponding higher turn-on resistance in the cascoded LVTSCR's. To reduce the turn-on resistance, the cascoded LVTSCR's have to be designed with wider device widths.

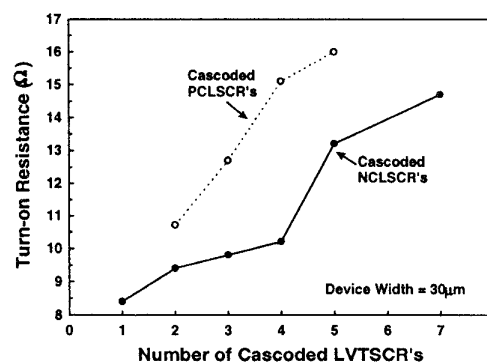


Fig.18 The relations between the turn-on resistance and the number of cascoded LVTSCR's.

## 7. Safe Applications for Whole-Chip ESD Protection

### 7.1 ESD Protection Circuits :

From the detailed investigation of the device characteristics including the temperature dependence, the cascoded LVTSCR's with three NCLSCR's (PCLSCR's) in a 0.35- $\mu\text{m}$  bulk CMOS process were used with a holding voltage of 4.74V (-4.96V) at 25°C and 3.62V (-3.66) at 150°C. To safely apply the

LVTSCR's for ESD protection in 3-V CMOS IC's, three NCLSCR's or PCLSCR's in the cascode configuration are enough. The typical input and output ESD protection circuits using both the cascaded 3-NCLSCR's and cascaded 3-PCLSCR's with the gate-coupled technique [18]-[19] for 3-V CMOS IC's are shown in Fig.19(a) and 19(b), respectively. The gate-coupled technique is used to provide a lower trigger voltage for the cascaded NCLSCR's (PCLSCR's) for more effective ESD protection.

The VDD-to-VSS ESD clamp circuits using the cascaded 3-NCLSCR's or cascaded 3-PCLSCR's with the RC-based control circuit [25]-[28] are shown in Fig.20(a) and 20(b), respectively. The number of the cascaded NCLSCR's or PCLSCR's is dependent on the voltage level of VDD in the CMOS IC. For the 5-V CMOS IC's, 5-NCLSCR's (5-PCLSCR's) have to be used in the VDD-to-VSS ESD clamp circuit to effectively clamp the ESD voltage across the VDD and VSS power lines but without causing the VDD-to-VSS latchup problem.

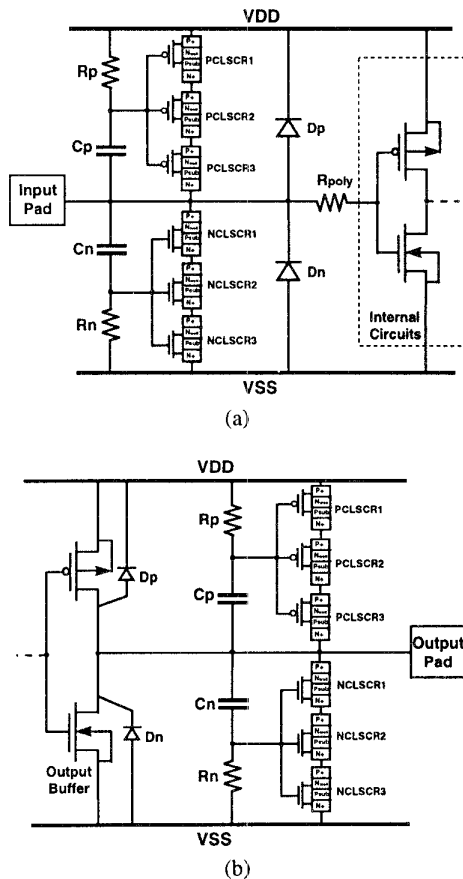


Fig.19 (a) The input ESD protection circuit, and (b) the output ESD protection circuit, using both the cascaded 3-NCLSCR's and the cascaded 3-PCLSCR's with the gate-coupled technique.

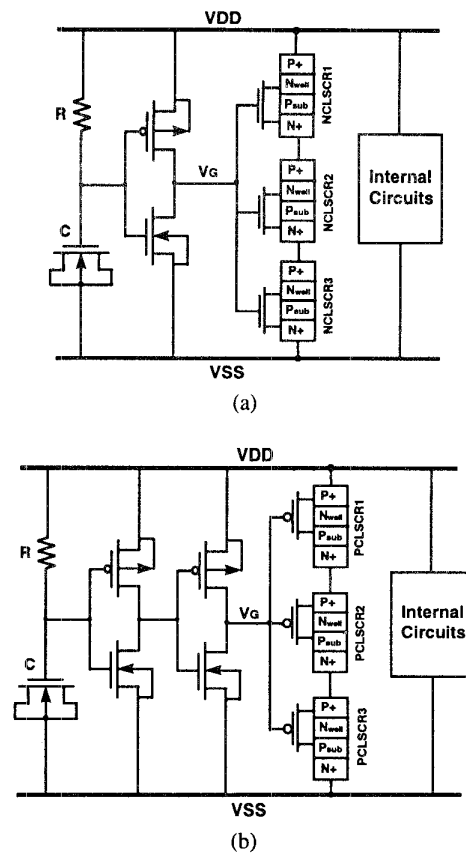


Fig.20 The VDD-to-VSS ESD clamp circuit using (a) the cascaded 3-NCLSCR's, and (b) the cascaded 3-PCLSCR's, with the RC-based control circuit.

## 7.2 Turn-on Verification :

To verify the turn-on behavior of the cascaded NCLSCR's in the VDD-to-VSS ESD clamp circuit, an ESD-like voltage pulse generated from a pulse generator (*hp8116A*) with a pulse width of 400ns and a rise time of 6ns is applied to the VDD of Fig.20(a) with the VSS grounded. The applied 0-to-8V voltage pulse is degraded by the cascaded 3-NCLSCR's, as shown in Fig.21(a). When the 0-to-8V voltage pulse is applied, the cascaded 3-NCLSCR's is triggered on and clamps the voltage pulse to the voltage level of 4.75V, which corresponds to the holding voltage of the cascaded 3-NCLSCR's. From the degraded waveform in Fig.21(a), it has also shown that the cascaded 3-NCLSCR's have a turn-on time of ~20ns to clamp the applied 0-to-8V voltage pulse on the VDD power line. If the ESD clamp circuit only has a single NCLSCR between the VDD and VSS power lines, the applied 0-to-8V voltage is clamped to only 1.5V in Fig.21(b). In Fig.21(b), the single NCLSCR also takes a time of ~ 20ns to turn itself on. After the

cascoded NCLSCR's are triggered on, the clamped voltage level is proportional to the holding voltage of the cascoded NCLSCR's. This has verified the turn-on efficiency of the cascoded NCLSCR's in the ESD-stress condition.

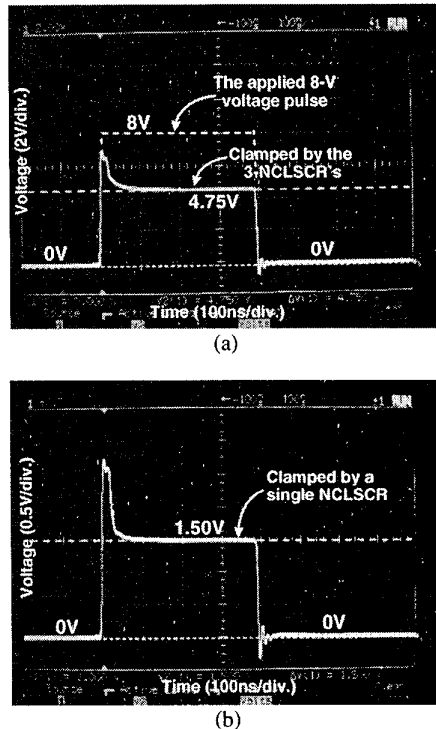


Fig.21 The degraded voltage waveforms of the 0-to-8V voltage pulse clamped by the ESD clamp circuit with (a) the cascoded 3-NCLSCR's, and (b) a single NCLSCR.

But, in the normal operating condition with 3-V VDD and 0-V VSS power supplies, the cascoded NCLSCR's in the ESD clamp circuit should not be triggered on by an overshooting voltage pulse on the VDD power line. To verify this issue, a 3-to-4V overshooting voltage pulse is applied to the VDD power line with the VDD-to-VSS ESD clamp circuit. The measured results at 25°C are shown in Fig.22(a) and 22(b) for the ESD clamp circuit with the cascoded 3-NCLSCR's and a single NCLSCR, respectively. In Fig.22(a), the 3-to-4V overshooting voltage pulse on the VDD power line is not degraded, because the cascoded 3-NCLSCR's are not triggered on by such an overshooting voltage pulse. But, in Fig.22(b), the 3-to-4V overshooting voltage pulse on the VDD power line is degraded and kept at 1.5V after the triggering of the 3-to-4V overshooting voltage pulse, because the VDD-to-VSS ESD clamp circuit with a single NCLSCR is triggered on by this

overshooting voltage pulse. The turned-on ESD clamp circuit with a single NCLSCR keeps the voltage level on the VDD power line to only 1.5V. This causes the so-called latchup problem in CMOS IC's. Thus, the VDD-to-VSS ESD clamp circuit or the input/output ESD protection circuits in CMOS IC's with a single LVTSCR are dangerous relative to the latchup problem in the noisy environments.

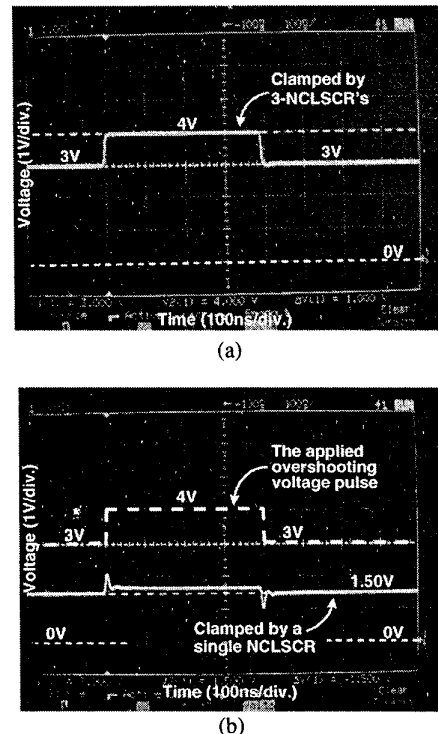


Fig.22 The voltage waveforms of the 3-to-4V overshooting voltage pulse clamped by the ESD clamp circuit with (a) the cascoded 3-NCLSCR's, and (b) a single NCLSCR.

To further verify the safe application of the cascoded LVTSCR's, a larger 3-to-8V overshooting voltage pulse is added to the VDD power line with the VDD-to-VSS ESD clamp circuit. The measured waveforms at 25°C are shown in Fig.23(a) and 23(b) for the ESD clamp circuit with the cascoded 3-NCLSCR's and the cascoded 2-PCLSCR's, respectively. In Fig.23(a), the 3-to-8V overshooting voltage pulse is degraded by the cascoded 3-NCLSCR's to the voltage level of 4.937V. But, after the triggering of the 3-to-8V overshooting voltage pulse, the VDD voltage level is restored to the original 3V. This means that the 3-NCLSCR's can effectively clamp the overshooting voltage pulse on the VDD power line but do not cause the VDD-to-VSS latchup problem in the ESD clamp circuit when the IC is in the normal operating condition.

In Fig.23(b), the 3-to-8V overshooting voltage pulse is degraded by the cascoded 2-PCLSCR's to the voltage level of 3.625V. But, after the triggering of the 3-to-8V overshooting voltage pulse, the VDD voltage level is also restored to the original 3V. Because the holding voltage of the cascoded 2-PCLSCR's at 25°C is around 3.22V, the cascoded 2-PCLSCR's can automatically turn off after the VDD voltage level is returned to 3V. As shown in Fig.16, the holding voltage of the cascoded 2-PCLSCR's is decreased to only 2.4V when the temperature is increased to 150°C. This implies that the cascoded 2-PCLSCR's are still dangerous to the latchup problem, if the CMOS IC's are operating in the high-temperature environments.

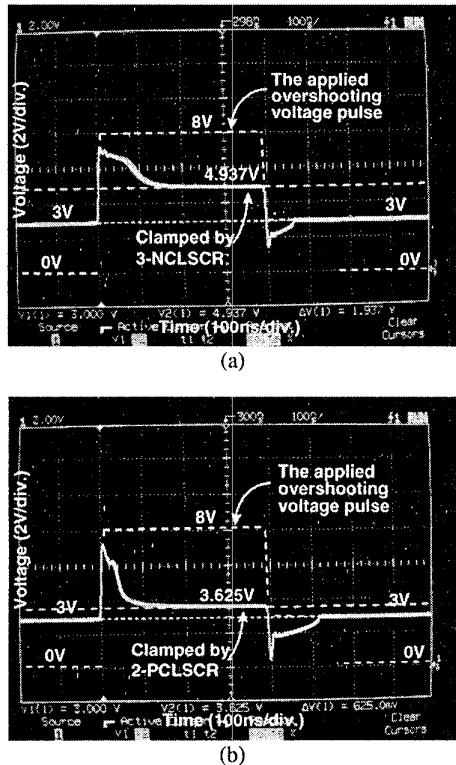


Fig.23 The degraded voltage waveforms of the 3-to-8V overshooting voltage pulse clamped by the ESD clamp circuit with (a) the cascoded 3-NCLSCR's, and (b) the cascoded 2-PCLSCR's.

### 7.3 ESD Robustness :

The VDD-to-VSS ESD clamp circuits designed in Fig.20 with different number of cascoded NCLSCR's or cascoded PCLSCR's are tested by the human-body-model (HBM) ESD stress. The failure criterion is defined as when the leakage current under the 5-V

bias from VDD to VSS is greater than 1μA. The HBM ESD robustness per device width ( $V_{ESD}/W$ ) of the cascoded NCLSCR's or the cascoded PCLSCR's is shown in Fig.24, where a gate-grounded NMOS (ggNMOS) with a device dimension (W/L) of 480/0.5 (μm/μm) in the same 0.35-μm bulk CMOS process is also tested for reference. All the cascoded NCLSCR's, PCLSCR's, and the ggNMOS are made using neither an ESD-implant process nor silicide-blocking process. The ESD robustness per device width ( $V_{ESD}/W$ ) of the cascoded 3-NCLSCR's (ggNMOS) is 50 V/μm (3.13 V/μm) in the 0.35-μm bulk CMOS process. The NMOS (PMOS) inserted in each NCLSCR (PCLSCR) device has a channel length of only 0.35 μm. The ggNMOS (W/L=480/0.5) occupies a layout area of 80×76 μm<sup>2</sup> can sustain an HBM ESD level of only 1.5KV. But the cascoded 3-NCLSCR's with a layout area of 60×60 μm<sup>2</sup> can sustain a 3-KV HBM ESD stress, where each NCLSCR has a device dimension (W/L) of only 60/20(μm/μm). So, the ESD robustness per layout area of the cascoded 3-NCLSCR's (ggNMOS) can be 0.83 V/μm<sup>2</sup> (0.25 V/μm<sup>2</sup>) in the 0.35-μm bulk CMOS process without using the extra silicide-blocking and ESD-implant process steps. Although the ESD performance of the cascoded LVTSCR's is degraded while the number of the LVTSCR's in the cascode configuration is increased, the ESD robustness and area efficiency of the cascoded LVTSCR's in 3-V application is still much greater than that of the ggNMOS.

With a total holding voltage greater than the VDD voltage level of CMOS IC's, the cascoded LVTSCR's can be safely applied for on-chip ESD protection without the accidental latchup danger.

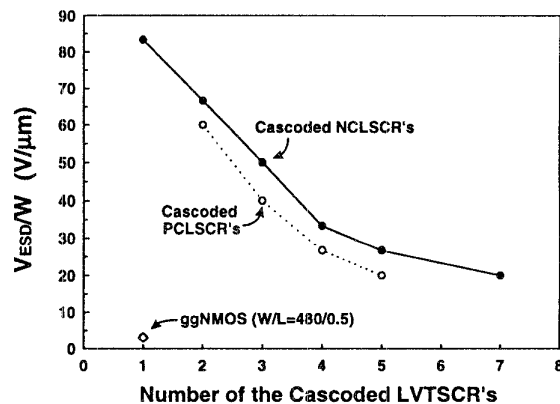


Fig.23 The HBM ESD robustness per device width ( $V_{ESD}/W$ ) of the cascoded LVTSCR's with different number of NCLSCR or PCLSCR devices.

## 8. Conclusions

The LVTSCR had been reported for on-chip ESD protection in CMOS IC's about 8-years ago, but such devices can be triggered on by the overshooting or undershooting of noise pulses which cause a latchup danger when the IC's are operated under normal conditions. In this work, a practical solution using cascoded LVTSCR's has been successfully designed in bulk CMOS processes to safely apply the LVTSCR for component-level ESD protection but without the fatal latchup trouble when the IC's are operating in system applications. The device characteristics of the cascoded LVTSCR's in a 0.35- $\mu\text{m}$  bulk CMOS process has been experimentally investigated. The holding voltage of the cascoded LVTSCR's can be linearly adjusted by changing the number of LVTSCR devices in the cascode configuration for different applications.

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