

Layout Design and Verification for Cell Library to Improve ESD/Latchup Reliability in Deep-Submicron CMOS Technology

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Abstract

A methodology to verify the ESD and latchup reliability of CMOS cell libraries has been proposed. The ESD- or latchup-sensitive layout in the cell library can be found by this proposed methodology with DRC (design rules check) and ERC (electrical rules check), before the chip is fabricated. By changing the layout in the suggested way of high immunity to ESD and latchup without increasing the layout area of the internal cores, the ESD and latchup reliability of CMOS IC's assembled by the verified cell library can be significantly improved without trial-and-error design modification and wafer fabrication.

Introduction

In deep-submicron CMOS technologies, the minimum spacing or clearance between the P+ and N+ diffusions has been much scaled down to reduce the layout area. With the scaled-down spacing, the p-n-p-n path in the internal cores of CMOS IC's is further sensitive to latchup if the deep-trench-isolation process or the epi-layer wafer are not used. Besides the latchup issue, the scaled-down CMOS IC's is also sensitive to ESD (electrostatic discharge) stresses [1]. Not only the input or output pins are easily damaged by the ESD, but the internal circuits are still sensitive to ESD damage. Some unexpected ESD damages had been found to locate at the internal cores beyond the input and output ESD protection circuits [2]-[7]. The ESD failure can locate along the parasitic p-n-p-n path or the parasitic lateral n-p-n bipolar path between the VDD and VSS. The ESD-induced failures located on the internal cores will become more often and serious in the scaled-down CMOS IC's.

Recently, due to the request of the "CE" mark from the European Community, an ESD gun with the ESD voltage of 8KV or even up to 15KV is used to test the electromagnetic compatibility (EMC) of the electronic products [8]-[10]. The system-level EMC/ESD test is illustrated in Fig.1. Such EMC/ESD test can cause a heavily-transient overshooting and undershooting voltage waveform of several-hundreds volts on the VDD pin of the IC's in the system board, as shown in Fig.2. Such a system-level electromagnetic-compatibility ESD test can not only cause the electronic system to "freeze" or "upset", but also easily cause the transient-induced latchup failure on the internal cores of the CMOS IC's [11]-[13]. Due to the peak-discharging effect of

ESD events, the p-n-p-n paths in the internal cores having the peak structure and narrower spacing in layout are more vulnerable to the system-level ESD-induced latchup failures.

In this paper, a verification method is proposed to find the ESD- or latchup-sensitive layout in the cell libraries. Before the chip is really fabricated, the ESD/latchup-sensitive layout in a chip can be found and replaced by the layout styles with high ESD/latchup reliability.

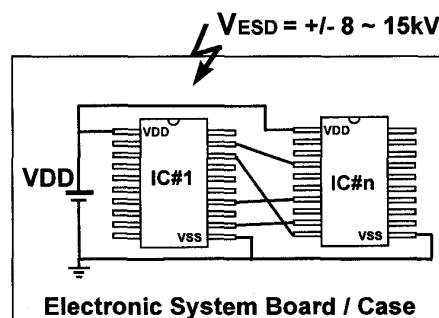


Fig.1 The schematic diagram to show the system-level electromagnetic compatibility (EMC) ESD test.

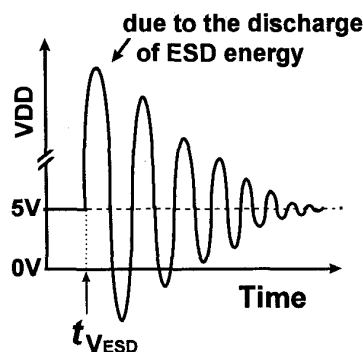


Fig.2 The transient overshooting/undershooting voltage waveform on the VDD pin of the IC's in the system board during the EMC/ESD testing.

ESD/Latchup Sensitive Layout

A. The parasitic p-n-p-n path

The ESD voltage due to component-level [1] or system-level [8] ESD stresses has been found to be across the VDD and VSS power lines of a CMOS IC, and to be diverted into the internal cores before the ESD voltage is bypassed

through the ESD clamp circuits. The fast transient ESD voltage across the VDD and VSS power lines easily leads to the occurrence of latchup in the internal cores. Although the guard rings are used to eliminate the triggering of CMOS latchup around the input or output pads, the guard rings are not used in the most layout of the internal cores in CMOS IC's, especially in the logic gates of the cell libraries.

The conventional layout style of the internal cores in a digital cell library realized in a p-substrate CMOS process is shown in Fig.3(a), where the substrate contact (N-well contact) is just placed under the VSS (VDD) power lines of the cell. But, the latchup-sensitive path is located from the VDD-connected source of PMOS to the VSS-connected source of NMOS, which is often drawn with a minimum spacing in the core cell. The cross-sectional view of such a latchup-sensitive path is illustrated in Fig.4. The typical I-V characteristics of such a p-n-p-n path in a 0.6- μm CMOS process with the spacing from the P+ diffusion to the N+ diffusion of 12 μm is shown in Fig.5, where its holding voltage is as low as 1.12V. With a holding voltage much below the VDD voltage level, it will cause serious latchup problem if such a p-n-p-n path is triggered on by the system-level ESD voltage. To block such a latchup-sensitive path, the guard rings may be placed between the p-n-p-n path. The cell layout with the guard rings to effectively block the latchup path is shown in Fig.3(b). The guard rings can block the p-n-p-n path to prevent latchup in the core cell, but the total layout area of the cell is significantly increased. Thus, the most cell libraries are still adopted the layout style of Fig.3(a) to realize the core cells for saving the chip size.

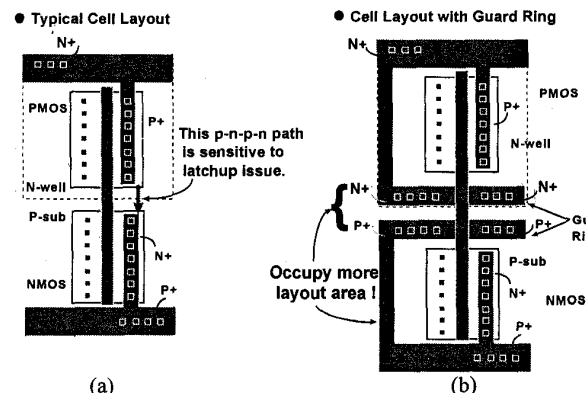


Fig.3 Schematic layout examples of the core cell with (a) the typical cell layout, and (b) the cell layout with additional latchup guard rings.

Table I

TSMC Process	X (μm)	Y (μm)	X+Y (μm)
0.8- μm	2.4	2.4	4.8
0.6- μm	1.8	1.8	3.6
0.5- μm	1.5	1.5	3.0
0.35- μm	1.2	1.2	2.4
0.25- μm	0.6	0.6	1.2

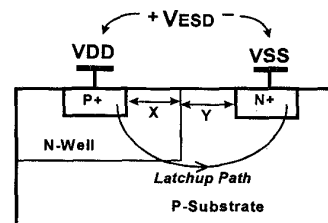


Fig.4 Cross-sectional view of the latchup-sensitive path in the core cell.

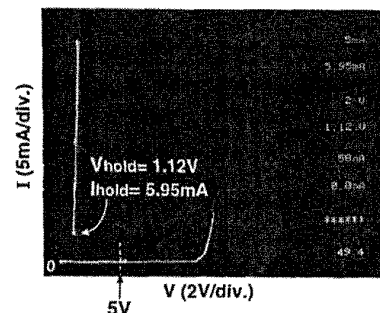


Fig.5 The I-V characteristics of a p-n-p-n path in the TSMC 0.6- μm CMOS process with the spacing from P+ to N+ of 12 μm .

But, the minimum spacing between the VDD-connected P+ diffusion in N-well and the VSS-connected N+ diffusion in the p-substrate (p-well) is much reduced in the deep-submicron CMOS technologies. The minimum spacings of the scaled-down p-n-p-n path in the TSMC CMOS technologies are listed in Table I. The minimum p-n-p-n spacing is reduced from 4.8 μm in the 0.8- μm CMOS process to only 1.2 μm in the 0.25- μm CMOS process. The reduced p-n-p-n spacing enhances the lateral bipolar action of the parasitic bipolar transistors in the latchup path. Therefore, the scaled-down p-n-p-n path is more sensitive to latchup, especially to the ESD-induced latchup.

B. The lateral n-p-n path

Another ESD-sensitive layout style in the internal cores is the parasitic lateral n-p-n bipolar path, which is formed by a VDD-connected N+ diffusion and a VSS-connected N+ diffusion with a narrow spacing. The schematic diagram of such a parasitic n-p-n bipolar device is shown in Fig.6(a). The I-V characteristics of the parasitic lateral n-p-n bipolar transistor is shown in Fig.6(b). The narrower spacing between the two N+ diffusions leads to the lower breakdown voltage (V_{bd}) and snapback voltage (V_{sb}). While the IC is under the ESD-stress conditions, the fast-transient ESD voltage will transfer to be across the VDD and VSS power lines of the IC. This transient ESD voltage can trigger on the parasitic n-p-n bipolar transistor into the snapback region to provide a short-circuit path between the VDD and VSS. Then, the ESD current is mainly discharged through the snapback n-p-n bipolar transistor. Because the n-p-n bipolar

transistor in the internal circuits are parasitically formed by two N+ diffusions which often have a small layout area and spacing in the internal cores. So, such a parasitic lateral n-p-n transistor is very easily damaged by the ESD energy.

A practical example of such ESD-induced failure located on the parasitic n-p-n path in the core cell is illustrated in Fig.7 [6], where an internal core cell of Schmitt trigger is not directly connected to the input pad. In the Schmitt trigger circuit, the drain of the NMOS M1 is connected to VDD. This VDD-connected N+ diffusion forms a parasitic lateral n-p-n bipolar transistor with the VSS-connected source of the NMOS M2. After the component-level ESD test [1] with a 1.5KV ESD voltage on the input pad, a leakage current of several mA is found between the VDD and VSS power lines of the ESD-stressed IC. Through detailed failure analysis, the ESD-induced failure does not locate on the ESD protection circuit of the input pad but locate on the parasitic n-p-n path of the Schmitt trigger circuit. The SEM picture in Fig.8 confirms that the ESD-induced failure is located along the parasitic n-p-n path between the VDD and VSS power lines.

The minimum spacing between two N+ diffusions in the TSMC CMOS processes is summarized in Table II. The spacing between two N+ diffusions is reduced from 1.6 μm in the 0.8- μm CMOS process to only 0.4 μm in the 0.25- μm CMOS process. With such a scaled-down spacing between two N+ diffusions in the deep-submicron CMOS processes, the parasitic lateral bipolar transistor is very easily triggered on and damaged by the ESD energy.

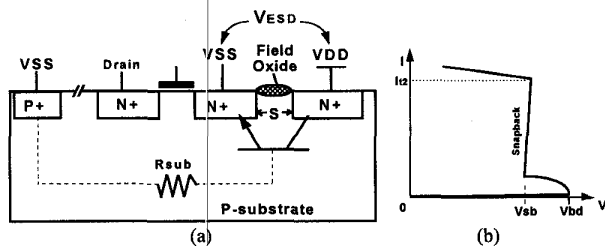


Fig.6 (a) The cross-sectional view, and (b) the I-V characteristics, of the parasitic lateral n-p-n bipolar transistor between the VDD and VSS power lines, which is sensitive to ESD stress.

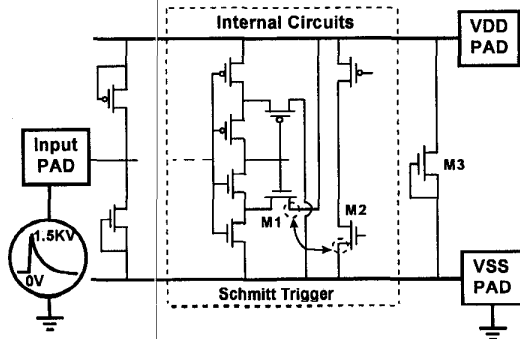


Fig.7 The schematic diagram to show the failure located on the parasitic lateral n-p-n path due to the component-level ESD testing.

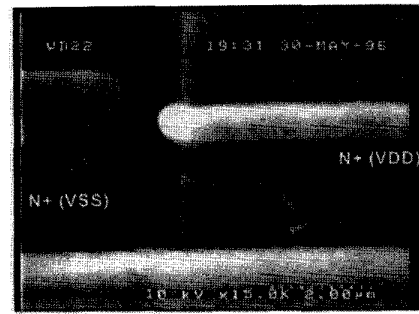


Fig.8 The SEM picture of ESD-induced failure located along the parasitic n-p-n path between the VDD and VSS in the Schmitt trigger circuit.

Table II

TSMC Process	S (μm)
0.8- μm	1.6
0.6- μm	1.2
0.5- μm	0.9
0.35- μm	0.6
0.25- μm	0.4

ESD/Latchup-Insensitive Layout Design

To reduce the latchup sensitivity of the p-n-p-n path in the core cells, a layout style with contact-reduced design is shown in Fig.9. In Fig.9(a), the core cell is drawn in the conventional style. The modified layout style with higher latchup immunity is shown in Fig.9(b), where the contacts for the VDD-connected source of PMOS and the VSS-connected source of NMOS are reduced to generate the series resistance R_p and R_n along the p-n-p-n path of the core cell. With such contact-reduced design, the drain-to-source currents of the PMOS and NMOS are not degraded or crowded on the source contacts, because there are still enough contacts to conduct the currents for PMOS and NMOS. For example, the current density for 10-years reliability of the contact in CMOS process is about 1mA/contact. For the core cell with a driving current often below 1mA, a contact is enough to sustain the normal operating current in the core cell. But, reducing the contact in the way along the p-n-p-n path as shown in Fig.9(b) can improve the latchup immunity of the core cell. The circuit diagram to explain the effect of such contact-reduced design on the latchup sensitivity is shown in Fig.9(c). The contact-reduced design uses the inherent sheet resistance R_n and R_p to limit the latchup current. The turn-on resistance of the p-n-p-n path in Fig.5 is about 3~5 Ω , but the R_p and R_n can have the resistance about 80~120 Ω through the contact-reduced layout. So, the turn-on sensitivity of latchup along the p-n-p-n path is much reduced by the additional R_p and R_n resistance.

To reduce the sensitivity of the parasitic lateral n-p-n transistor in the internal core cells, a layout example is shown in Fig.10. In the worst case of Fig.10, two NMOS's

are placed with a narrow spacing, but the VSS-connected N⁺ diffusion closes to the VDD-connected N⁺ diffusion. In such a way, the lateral n-p-n transistor in the worst-case layout is very easily triggered on and damaged by the ESD voltage. To overcome this issue, a good layout style is shown in the right-hand part of Fig.10, where the circuit has the same function and layout area but has no dangerous lateral n-p-n transistor in the layout. So, through a correct layout design, the logic gates in the cell libraries can have high immunity against the component-level and system-level ESD stresses.

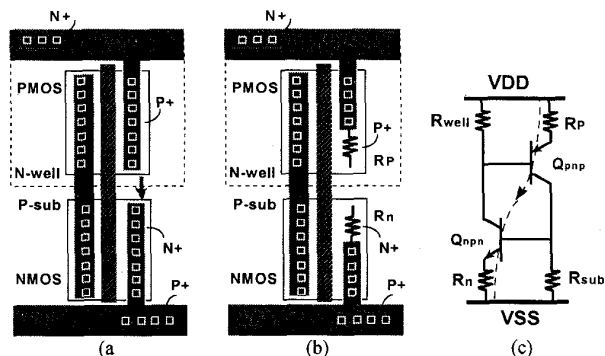


Fig.9 (a) The original layout style of the core cell, (b) the modified layout style with contact-reducing design for better latchup immunity, and (c) the schematic circuit to show the contact-reducing design to generate extra series resistance along the p-n-p path for latchup prevention.

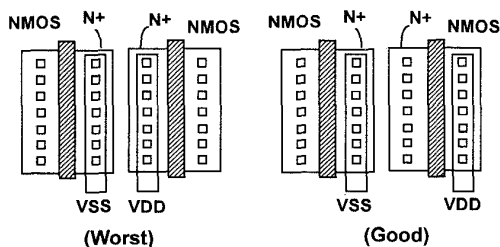


Fig.10 The different layout styles between two NMOS's with and without the parasitic lateral n-p-n bipolar transistor.

Layout Verification

As described in the above sections, the layouts of the core cells in the cell libraries often have some ESD/latchup sensitive paths. If we can find these sensitive paths during the development of a cell library, the sensitive paths can be modified in time to become insensitive by suitable layout design without increasing the cell layout area. The methodology to verify the layout having ESD/latchup sensitive paths is shown in Fig.11, where the DRACULA is used to check the spacing of the sensitive paths. By using the DRC and ERC functions of the DRACULA, the ESD/latchup sensitive paths can be found and replaced by the way of insensitive layout styles. Each cell layout in a cell library can be scanned by this method to find the ESD/ latchup sensitive layout during the development of a cell library. Through this

layout verification, the scaled-down CMOS IC's assembled by the verified cell libraries still have higher reliability to ESD and latchup issues.

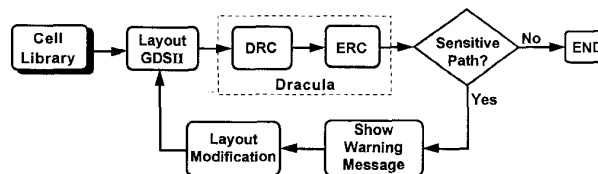


Fig.11 A flow chart to show the layout verification method during the development of the cell libraries in the scaled-down CMOS process.

Conclusion

A verification method and the ESD/latchup-insensitive layout design have been proposed to find and to fix the ESD/latchup-sensitive layouts in the scaled-down CMOS cell libraries. By using this layout verification method and layout design, the CMOS IC's can still have enough robustness against the ESD/latchup reliability issues in the further scaled-down CMOS technologies. The proposed layout design and verification method had been practically used to develop the CCL/ITRI's cell libraries in the 0.6- μ m, 0.5- μ m, and 0.35- μ m CMOS technologies.

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