NOVEL INPUT ESD PROTECTION CIRCUIT WITH SUBSTRATE-TRIGGERING TECHNIQUE IN A 0.25-μm SHALLOW-TRENCH-ISOLATION CMOS TECHNOLOGY

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Abstract

A substrate-triggering technique, to increase the ESD robustness and to reduce the trigger voltage of the ESD protection device, is proposed to improve the ESD-protection efficiency of the input ESD protection circuit in deep-submicron CMOS technology. Through suitable substrate-triggering design on the device structure, this proposed input ESD protection circuit can successfully protect the thinner gate oxide (50Å) of the input stage in a 0.25-μm CMOS technology and sustain an ESD level above 2000V without extra process modification.

Introduction

ESD (electrostatic discharge) damage has become the main reliability issue on the deep-submicron CMOS IC products. To overcome this ESD problem, the on-chip ESD protection circuits had been added around the input and output pads of the CMOC IC's against ESD damages. But, the efficiency of the ESD protection circuits is seriously degraded by the advanced CMOS fabrication technologies [1]. To protect the gate oxide of the input stage of CMOS IC's, a typical previous design of input ESD protection circuit is shown in Fig.1, where a field-oxide device (FOD) is cooperated with a short-channel NMOS device and a series resistor to protect the input stage against the ESD overstress.

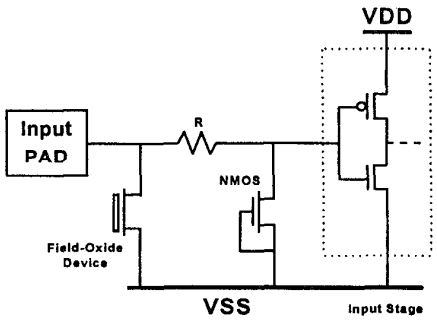

Fig.1 A traditional input ESD protection circuit with the field-oxide device.

Due to the scaling on the gate-oxide thickness in the deep-submicron CMOS technologies for high-speed and low-voltage applications, the breakdown voltage of the gate oxide in the input stage is much reduced. In order to protect the thinner gate oxide, the gate-grounded NMOS in Fig.1 is often designed with a minimum channel length to hold a lower breakdown voltage. But, the gate-grounded NMOS with a shorter channel length sustains a very low ESD level [1]. Therefore, a series resistor R is added in Fig.1 to limit the ESD current through the gate-grounded NMOS. To effectively limit the ESD current through the gate-grounded NMOS, the series resistor R is designed with a large resistance. But, the large series resistor R causes a long signal timing delay from the input pad to the input stage, which is not suitable for high-speed or high-frequency applications. In Fig.1, the FOD is used to mainly discharge the ESD current. The FOD without the LDD (lightly-doped drain) structure can sustain higher ESD current than the gate-grounded NMOS. But, the FOD with a longer channel length has a higher breakdown voltage than that of the gate-grounded NMOS. Therefore, the FOD has to be operated with the gate-grounded NMOS to provide the overall ESD protection function to protect the input stage.

Recently, the ESD characteristics of protection devices had been more studied, and it was found that the substrate bias can improve the ESD level of the protection devices [2]. The ESD performance of ESD-protection devices can be investigated by the It2 (second breakdown current). A FOD with a 0.8-V substrate bias can provide a four-times higher It2 than the NMOS device with 0-V substrate bias [3]. So, a FOD with a suitable substrate bias can provide higher ESD robustness within a much smaller layout area to protect the CMOS IC's.

In this paper, a novel substrate-triggering design is proposed to improve the efficiency of the input ESD protection circuit in a 0.25-μm CMOS technology. The trigger voltage of this substrate-triggering input ESD protection circuit can be lowered below the gate-oxide breakdown voltage, as well as the series resistance R between the input pad and the input stage can be even removed for high-speed or high-frequency application.

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Substrate-Triggering Input ESD Protection Circuit

To apply the substrate-triggering technique into the ESD protection circuit to improve the ESD-sustained level and to lower its trigger voltage, the proposed input ESD protection circuit is shown in Fig.2. The substrate-triggering input ESD protection circuit is formed by a short-channel NMOS (Mn1), a resistor (R), and a FOD, but with different connection to that of Fig.1. The drain of the short-channel NMOS (Mn1) is directly connected to the input pad, and the source of the Mn1 is connected to VSS through the resistor R. The source of the Mn1 is also connected to the substrate of the FOD to trigger on the parasitic lateral bipolar junction transistor (LBJT) in the FOD. The FOD in Fig.2 is turned on by the LBJT action with a forward-biased base-emitter junction in the FOD. The turn-on voltage of the FOD with a positive substrate bias is lower than its drain breakdown voltage. The Mn1 and resistor R are therefore designed to provide the substrate-triggering current to the FOD during the ESD stresses. This substrate-triggering FOD can sustain higher ESD stress with a lower turn-on voltage, so this substrate-triggering input ESD protection circuit can effectively protect the thinner gate oxide in the deep-submicron CMOS IC's.

While a positive ESD voltage happens to the input pin which is connected to the input pad through the bonding wire, the short-channel Mn1 is snapback broken down and generates a substrate current into the base of the LBJT in the FOD. The base voltage is increased when the breakdown current flowing through the resistors R to VSS. The LBJT of the FOD is quickly biased by the triggering current in its substrate. Therefore, the FOD can be early triggered on with a lower turn-on voltage to clamp the ESD voltage across the gate oxide of the input stage.

The substrate-triggering technique can be also applied to improve the ESD robustness of the thin-oxide NMOS device. An alternative design of the input ESD protection circuit by using the NMOS as the main ESD current discharging device is shown in Fig.3, where the Mn1 and R are similar to those in Fig.2. But, the Mn2 is designed with a longer channel length to sustain higher ESD current. The parasitic LBJT in the Mn2 is also designed to be triggered on by the substrate-triggering current which is generated from the Mn1 and R during the ESD stresses.

Substrate-Triggering Device Structures

A novel device structure to realize the substrate-triggering ESD protection circuit in a 0.25-μm shallow-trench-isolation CMOS technology [4] is shown in Fig.4, which includes the Mn1, R, and the FOD. In the center of Fig.4, an N-well is connected to the input pad, and this N-well is also connected to the drain of Mn1 to protect the Mn1. Because the Mn1 with a shorter channel length, LDD structure, and the silicided diffusion in the deep-submicron CMOS technologies is very weak to the ESD stress, the N-well is added to limit the ESD current through the Mn1 before the FOD is triggered on. Because the Mn1 is designed as a start-up device to initiate the turn-on of the FOD through the substrate, the added N-well structure does not affect the triggering function of the Mn1 in the ESD protection circuit. The resistor R is realized by the parasitic p-type substrate resistance as shown in Fig.4.

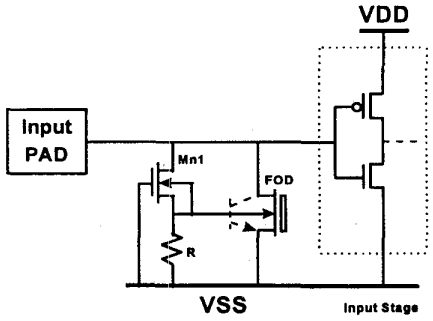

Fig.2 The proposed substrate-triggering input ESD protection circuit to protect the thinner gate oxide.

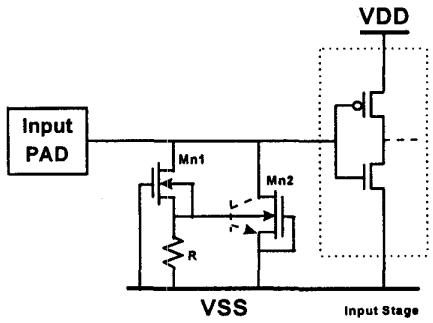

Fig.3 An alternative design of substrate-triggering input ESD protection circuit with a long-length NMOS as the ESD-current discharging device.

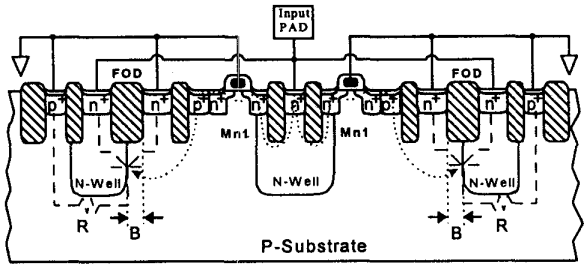

Fig.4 The device structure of the substrate-triggering input ESD protection circuit in Fig.2.

To improve the lateral BJT performance for ESD protection, another N-well is inserted into the source of the FOD as shown in Fig.4. This N-well also has an effect to increase the equivalent resistance of the resistor R in the ESD protection circuit. As the Mn1 is snapback broken down by the ESD voltage on the input pad, the breakdown

current of Mn1 is diverted into the p-substrate through the P+ diffusion as the substrate-triggering current. This substrate-triggering current is collected by the N-well of the FOD to bias the base-emitter junction of the LBJT in the FOD. Finally, the FOD is fully turned on to bypass ESD current from the input pad to VSS, so as to protect the input stage which is connected to this input pad. Through suitable design on the device structure, the ESD protection performance of the input ESD protection circuit can be significantly improved by this substrate-triggering technique.

Similarly, the realization of the ESD protection circuit in Fig.3 with an NMOS (Mn2) as the main ESD current discharging device is shown in Fig.5. The N-well in the center of Fig.5 is used to limit the ESD current discharged through the short-channel Mn1. Another N-well is also inserted into the source region of the Mn2 to improve the lateral BJT action in the Mn2 and to enhance the ESD robustness of the Mn2. Therefore, the ESD voltage on the input pad can be clamped to a much lower voltage level, so as to effectively protect the thinner gate oxide of the input stage in the deep-submicron CMOS technologies.

Experimental Results

The proposed substrate-triggering input ESD protection circuit has been designed and fabricated in a 0.25-μm shallow-trench-isolation CMOS process [4]. The I-V characteristics of the lateral BJT in the FOD is measured and shown in Fig.6. The snapback breakdown voltage of the FOD is as high as 11.9V, but the trigger voltage for the FOD entering into its snapback region is significantly reduced if there is a trigger current into its base. The I-V characteristics of the whole substrate-triggering input ESD protection circuit in Fig.2 is the combination of the I-V curves of the FOD, the Mn1, and the substrate resistance. The I-V characteristics of the substrate-triggering input ESD protection circuit is measured and shown in Fig.7, where the trigger voltage of the substrate-triggering input ESD protection circuit is lowered to only 6.4V. The trigger voltage of the FOD has been significantly reduced by the substrate-triggering current generated from the short-channel Mn1. The turn-on speed of the FOD is also enhanced by the substrate-triggering current. So, this proposed substrate-triggering input ESD protection circuit can provide effective and quick voltage-clamping function to protect the thinner gate oxide of 50Å in the 0.25-μm CMOS technology.

The secondary breakdown current (It2) of the substrate-triggering input ESD protection circuit is also measured by the TLPG (transmission line pulse generator) system. When the ESD-stress current on the input pad is greater than the It2 of the substrate-triggering input ESD protection circuit, the input ESD protection circuit is permanently damaged by the overstress current. Adjusting the device dimension of the LBJT in the FOD (or the Mn2), the It2 can be proportionally increased. Thus, the ESD robustness of the input ESD protection circuit can be adjusted. Two important device dimensions, which have strong effect on the ESD level of the substrate-triggering input ESD protection circuit, are the base spacing (B) and the channel width of the LBJT in the FOD (or the Mn2). The relations between the It2 and the base spacing (B) of the LBJT in the device structures of Fig.4 and Fig.5 are measured and shown in Fig.8. The relations between the It2 and the channel width of the FOD (or the Mn2) in Fig.4 and Fig.5 are measured and shown in Fig.9.

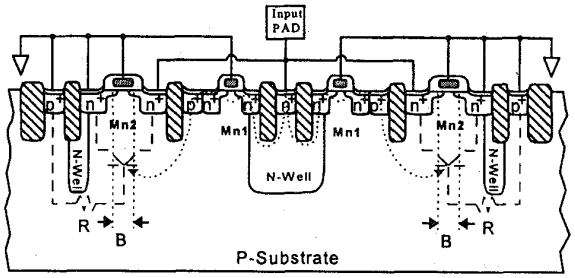

Fig.5 The device structure of the alternative substrate-triggering input ESD protection circuit in Fig.3.

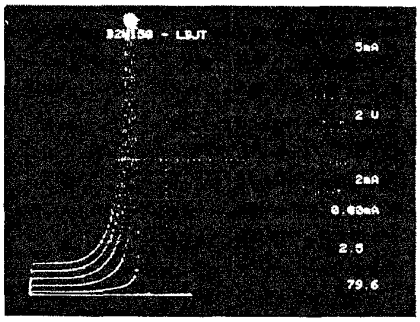

Fig.6 The measured I-V characteristics of a field-oxide device in the 0.25-μm CMOS technology.

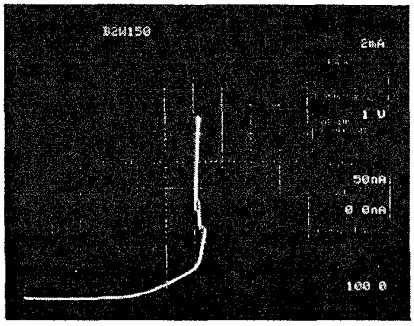

Fig.7 The measured I-V characteristics of the substrate-triggering input ESD protection circuit fabricated in the 0.25-μm CMOS technology.

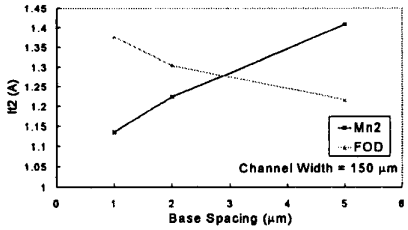

Fig.8 The relations between the It2 and the base spacing in the device structures of Fig.4 (FOD) and Fig.5 (Mn2).

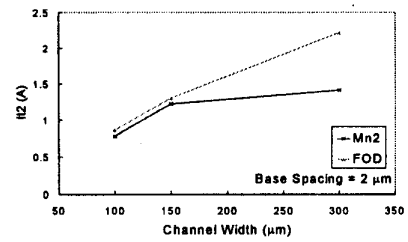

Fig.9 The relations between the It2 and the channel width of the device structures in Fig.4 (FOD) and Fig.5 (Mn2).

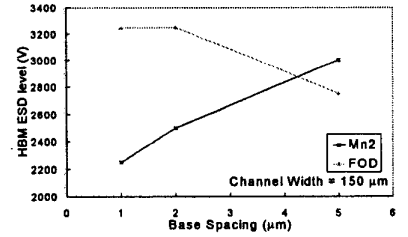

Fig.10 The relations between the HBM ESD level and the base spacing in the device structures of Fig.4 (FOD) and Fig.5 (Mn2).

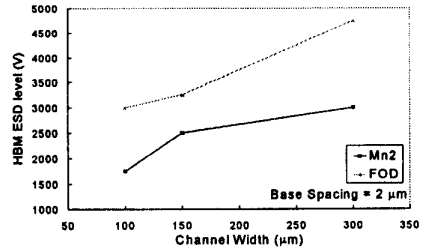

Fig.11 The relations between the HBM ESD level and the channel width in the device structures of Fig.4 (FOD) and Fig.5 (Mn2).

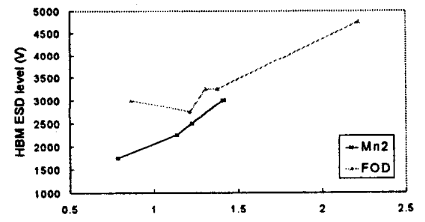

Fig.12 The dependence of ESD level on the It2 of the substrate-triggering input ESD protection circuits with the FOD or the long-channel NMOS (Mn2).

The fabricated substrate-triggering input ESD protection circuits are verified by the human-body-model (HBM) ESD test [5]. The results are shown in Figs.10 and 11. In Fig.10, the ESD-sustained level of the substrate-triggering input ESD protection circuit with the FOD is decreased as the base spacing in the FOD is increased. But, the ESD-sustained level of the substrate-triggering input ESD protection circuit with the Mn2 is increased as the base spacing in the Mn2 is increased. With a base spacing of 1μm in the LBJT, the substrate-triggering input ESD protection circuit with the FOD can sustain an ESD level of 3250V, but that with the Mn2 only sustains an ESD level of 2250V. In Fig.11, the ESD-sustained level of the substrate-triggering input ESD protection circuits with the FOD or the Mn2 are increased as the channel width of the FOD or the Mn2 are increased. This is consistent with the It2 in Fig.9. From Fig.11, the ESD level of the input ESD protection circuit with the FOD is increased 60% more than that with the Mn2, while the base spacing of the LBJT is kept at 2μm.

The dependence of ESD level on the It2 of the substrate-triggering input ESD protection circuits with the FOD or the long-channel NMOS (Mn2) is shown in Fig.12. The pulse width of the TLPG used to measure the It2 in this work is kept at 100ns. The slope of the substrate-triggering input ESD protection circuit with the FOD is about 1.7KΩ, but that with the Mn2 is about 1.9KΩ. These slopes are approximately consistent to the value of 1.5KΩ in the equivalent circuit of the HBM ESD events [5].

Conclusion

A novel input ESD protection circuit by using the substrate-triggering technique has been practically verified in a 0.25-μm shallow-trench-isolation CMOS process to provide an HBM ESD level greater than 2000V with a small device dimension. The trigger voltage of this input ESD protection circuit is lowered to only 6.4V to effectively protect the input thinner gate oxide (50Å) in the 0.25-μm CMOS technology.

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